



LC86E5420

8-Bit Single Chip Microcontroller

Preliminary

Overview

The LC86E5420 is a CMOS 8-bit single chip microcontroller with UVEPROM of the LC865500 / LC865400 series.

This microcontroller has the function and the pin description of the LC865500 / LC865400 series mask ROM version, and the 20K-byte EPROM. The program data is rewritable. It is suitable to develop the program.

Features

- (1) Option switching by EPROM data

The option function of the LC865400 series can be specified by the EPROM data.

The LC86E5420 can be checked the functions of the trial pieces using the mass production board.

- (2) Internal EPROM capacity : 20736 bytes
 (3) Internal RAM capacity : 512 bytes

Mask ROM version	PROM capacity	RAM capacity
LC865520	20480 bytes	512 bytes
LC865516	16384 bytes	512 bytes
LC865512	12288 bytes	512 bytes
LC865508	8192 bytes	512 bytes
LC865504	4096 bytes	512 bytes
LC865412	12288 bytes	224 bytes
LC865408	8192 bytes	224 bytes
LC865404	4096 bytes	224 bytes

- (4) Operating supply voltage : 4.5V to 6.0V
 (5) Instruction cycle time : 1.0 μ s to 366 μ s
 (6) Operating temperature : +10°C to +40°C
 (7) The pin compatible with the LC865400 series mask ROM devices
 (8) Applicable mask ROM version : LC865520 / LC865516 / LC865512 / LC865508 / LC865504
 LC865412 / LC865408 / LC865404
 (9) Factory shipment : DIC42S (with window)
 QIC48E (with window)

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Notice for use

The LC86E5420 is provided for the first release and small shipping of the LC865500 / LC865400 series.
At using, take notice of the followings.

(1) A point of difference the LC86E5420 and the LC865500 / LC865400 series

Item	LC86E5420	LC865520 / 16 / 12 / 08 / 04 / LC865412 / 08 / 04
Operation after reset releasing	The option is specified by degree until 3ms after going to a 'H' level to the reset terminal. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal.
Operating supply voltage range (VDD)	4.5V to 6.0V	2.5V to 6.0V
Operating temperature range (Topg)	+10 to +40°C	-30 to +70°C
Power dissipation	Refer to 'electrical characteristics' on the semiconductor news.	

The LC86E5420 functions same as the followings while resetting ; LC865520 / 16 / 12 / 08 / 04, LC865412 / 08 / 04.

The LC86E5420 uses 256 bytes that is addressed on 7F00H to 7FFFH in the program memory as the option configuration data area.

• A kind of the option corresponding of the LC86E5420

A kind of option	Pins, Circuits	Contents of the option
Input / output form of input / output ports	Port 0	1. N-channel open drain output
		2. CMOS output *1
	Port 1	1. Pull-up MOS Tr. provided
		2. Pull-up MOS Tr. not provided *2
Port 3	*1	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain
	*1	2. Input : Programmable pull-up MOS Tr. Output : CMOS

*1) Specified in bit

*2) Specified in nibble unit. Pull-up MOS Tr. is not provided in N-channel open drain output port.

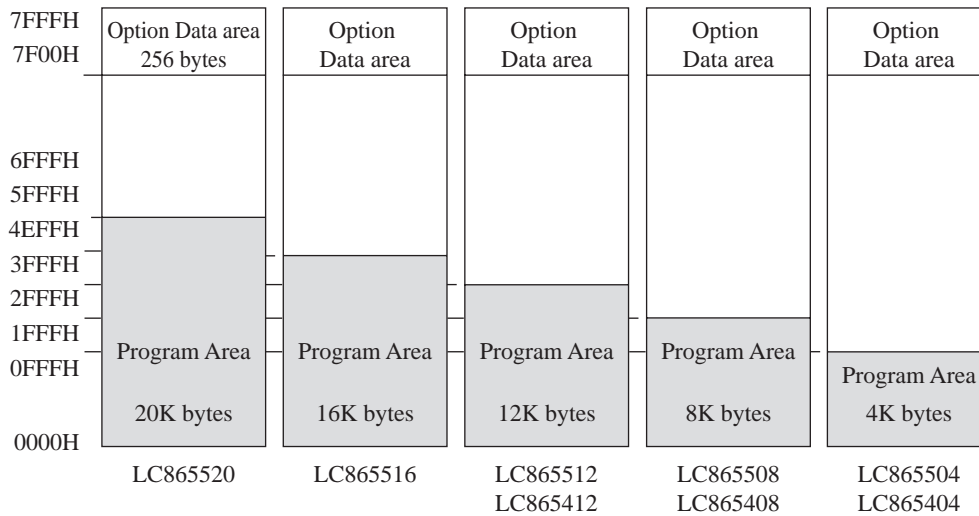
(2) Option

The option data is created by the option specified program "SU86K.EXE". The created option data is linked to the program area by the linkage loader "L86K.EXE".

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(3) ROM space

The LC86E5420 and LC865500 / LC865400 series use 256 bytes that is addressed on 7F00H to 7FFFH in the program memory as the option specified data area. These program memory capacity are 20480 bytes that is addressed on 0000H to 4FFFH.



How to use

(1) Create a programming data for LC86E5420

Programming data for EPROM of the LC86E5420 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86E5420.

(2) How to program for the EPROM

The LC86E5420 can be programmed by the EPROM programmer with attachment ; W86EP5420D, W86EP5420Q.

- Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

- "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set to "0000H to 7FFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function

"Data security" is the disabled function to read the data of the EPROM.

The following is the process in order to execute data security.

1. Set 'ON' the jumper of attachment.
2. Program again. Then the EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

- Data security is not executed when the data of all address have 'FFH' at the sequence 2 above.
- The programming by sequential operation "BLANK→PROGRAM→VERIFY" cannot be executed data security at the sequence 2 above.
- Set 'OFF' to the jumper after executing the data security.

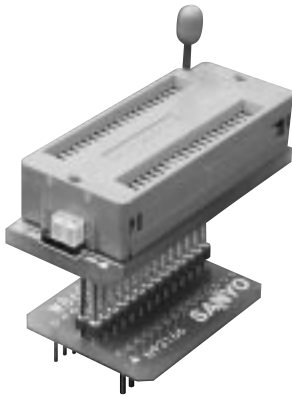
(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

(5) Shielding

The UVEPROM (ultraviolet erasable and programmable ROM) is in it. Put the seal on the window in use.

Data security

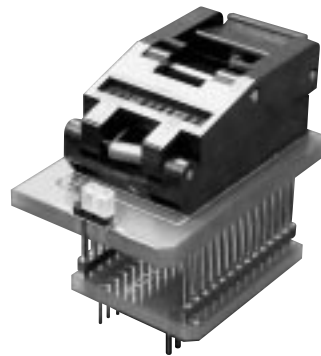


Not data security



W86EP5420D

Data security



Not data security

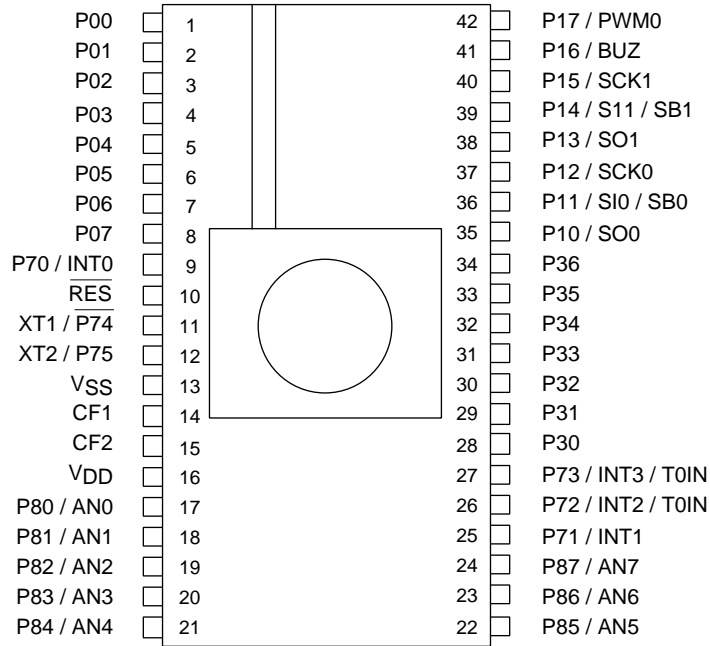


W86EP5420Q

LC86E5420

Pin Assignment

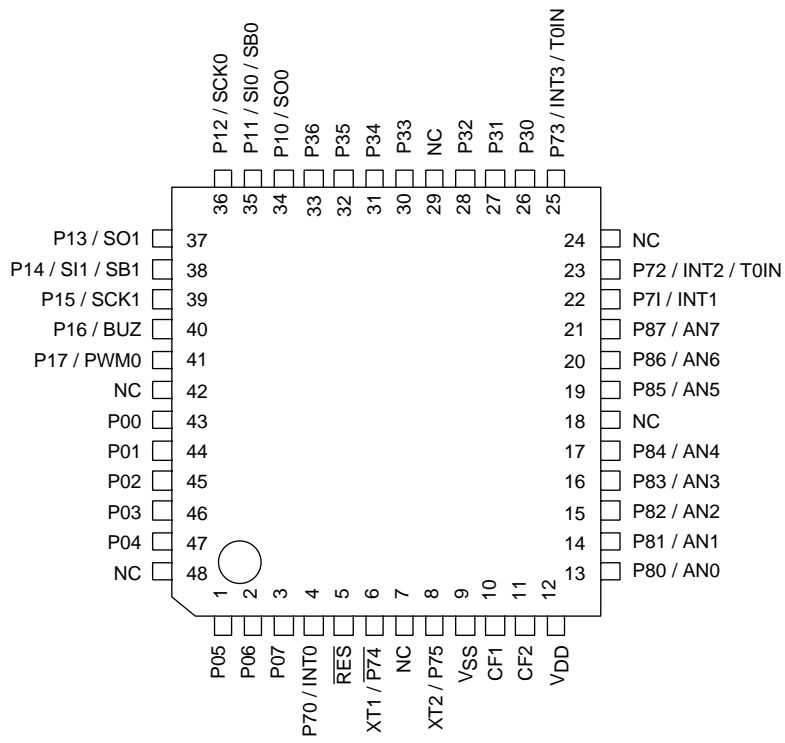
- DIC42S



ILC00015

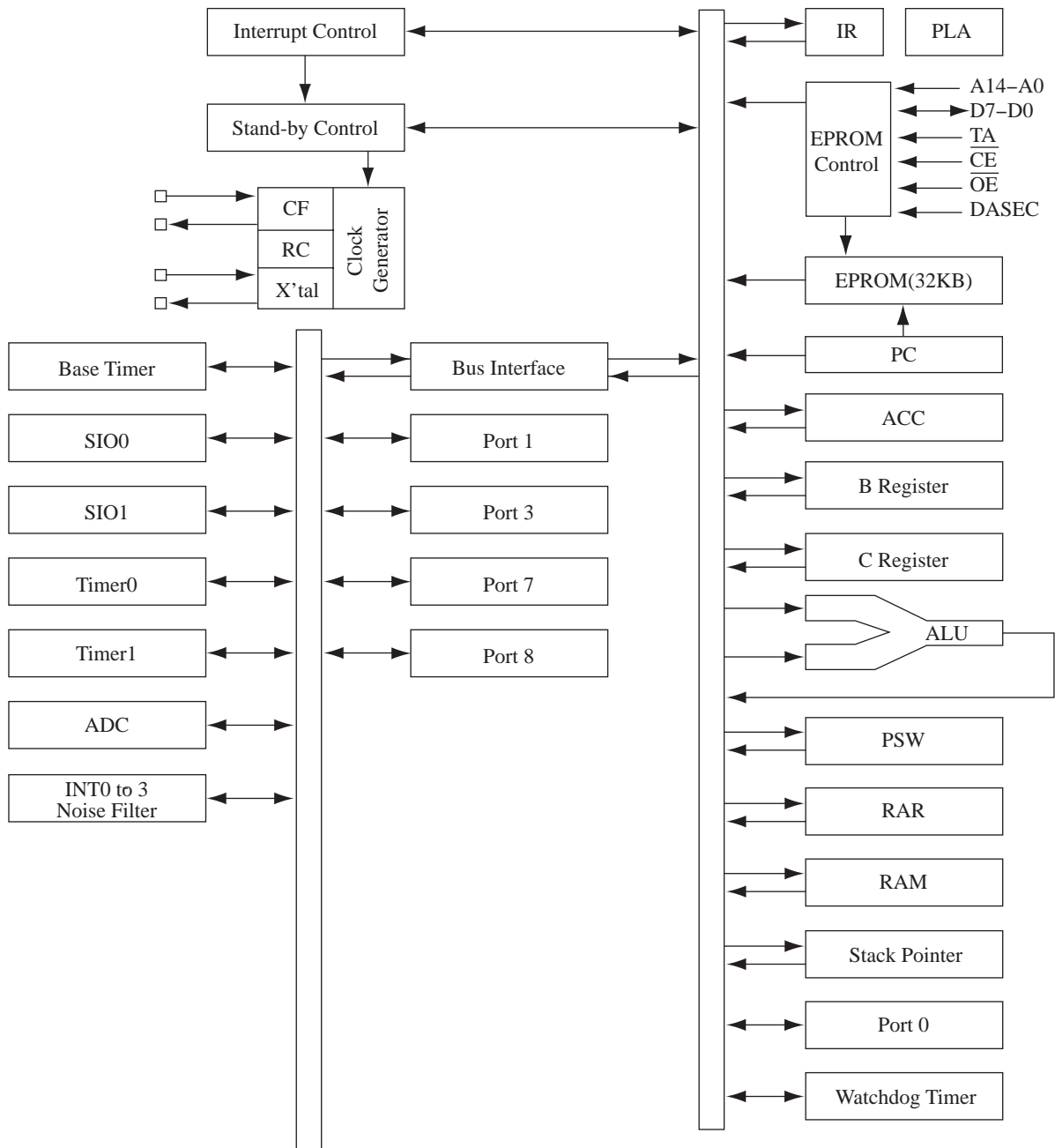
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• QIC48E



ILC00010

System Block Diagram



ILC00035

Pin Description

Pin name	I / O	Function description	Option	PROM mode																																			
VSS		Power pin (-)																																					
VDD		Power pin (+)																																					
PORT0 P00 to P07	I / O	<ul style="list-style-type: none"> •8-bit input / output port Input / output in nibble units •Input for port 0 interrupt •Input for HOLD release •15V withstand at N-channel open drain output 	<ul style="list-style-type: none"> •Pull-up resistor : Provided / Not provided (specify every 4-bit) •Output form : CMOS / N-channel open drain (specify in bit) 																																				
PORT1 P10 to P17	I / O	<ul style="list-style-type: none"> •8-bit input / output port Input / output can be specified in bit unit. •Other pin functions P10 SIO0 data output P11 SIO0 data input / bus input / output P12 SIO0 clock input / output P13 SIO1 data output P14 SIO1 data input / bus input / output P15 SIO1 clock input / output P16 Buzzer output P17 Timer1 (PWM0) output 	<ul style="list-style-type: none"> •Output form : CMOS / N-channel open drain. (specify in bit) 	Data line D0 to D7																																			
PORT3 P30 to P36	I / O	<ul style="list-style-type: none"> •7-bit input / output port Input / output in bit unit. •15V withstand at N-channel open drain output 	<ul style="list-style-type: none"> •Pull-up resistor : Provided / Not provided •Output form : CMOS / N-channel open drain 																																				
PORT7 P70 to P73 $\overline{P74}$, P75	I / O I	<ul style="list-style-type: none"> •4-bit input / output port Input / output in bit unit. •2-bit input port •Other pin functions. P70 : INT0 input / HOLD release input / N-channel Tr. output for watchdog timer P71 : INT1 input / HOLD release input P72 : INT2 input / timer 0 event input P73 : INT3 input with noise filter / timer 0 event input $\overline{P74}$: Input pin XT1 for 32.768kHz crystal oscillation P75 : Output pin XT2 for 32.768kHz crystal oscillation •Interrupt received form, vector address <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>High level</th> <th>Low level</th> <th>Vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table>		Rising	Falling	Rising & Falling	High level	Low level	Vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH		EPROM control signals <ul style="list-style-type: none"> •DASEC (*1) •\overline{OE} (*2) •\overline{CE} (*3)
	Rising	Falling	Rising & Falling	High level	Low level	Vector																																	
INT0	enable	enable	disable	enable	enable	03H																																	
INT1	enable	enable	disable	enable	enable	0BH																																	
INT2	enable	enable	enable	disable	disable	13H																																	
INT3	enable	enable	enable	disable	disable	1BH																																	

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Pin name	I / O	Function description	Option	PROM mode
PORT8 P80 to P83 P84 to P87	I I / O	<ul style="list-style-type: none"> •4-bit input port •4-bit input / output port Input / output can be specified in bit unit •Other function AD input port (AN7 to AN0) 		TA (*4)
RES	I	Reset pin.		
XT1 / $\overline{P74}$	I	<ul style="list-style-type: none"> •Input pin for the 32.768kHz crystal oscillation •Other function XT1 : Input port $\overline{P74}$ •In case of non use, connect to VDD 		
XT1 / P75	O	<ul style="list-style-type: none"> •Output pin for the 32.768kHz crystal oscillation •Other function XT2 : Input port P75 •In case of non use, connect to VDD at using as port or unconnect at using as oscillation. 		
CF1	I	Input pin for the ceramic resonator oscillation.		
CF2	O	Output pin for the ceramic resonator oscillation.		

© All of port options except the pull-down resistor option of Port 0 can be specified in a bit unit.

- *1 Memory select input for data security
- *2 Output enable input
- *3 Chip enable input
- *4 TA → EPROM control signal input

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1. Absolute Maximum Ratings at $V_{SS}=0V$ and $T_a=25^\circ C$

Parameter		Symbol	Pins	Conditions	Ratings			unit		
					VDD[v]	min.	typ.		max.	
Supply voltage		VDD MAX	VDD	VDD		-0.3		+7.0	V	
Input voltage		V _I (1)	<ul style="list-style-type: none"> •Ports 74, 75 •Ports 80, 81, 82, 83 •RES 			-0.3		VDD + 0.3		
Input/output voltage		V _{IO} (1)	<ul style="list-style-type: none"> •Port 1 •Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87 •Ports 0, 3 at CMOS output option 			-0.3		VDD + 0.3		
		V _{IO} (2)	Ports 0, 3 at N-ch open drain output option			-0.3		15		
High Level output current	Peak output current	IOPH	<ul style="list-style-type: none"> •Ports 0, 1, 3 •Ports 71, 72, 73 •Ports 84, 85, 86, 87 	CMOS output At each pins		-10			mA	
	Total output current	Σ IOAH(1)	Ports 0,1	The total all pins		-30				
		Σ IOAH(2)	Port 3	The total all pins		-15				
		Σ IOAH(3)	<ul style="list-style-type: none"> •Ports 71, 72, 73 •Ports 84, 85, 86, 87 	The total all pins		-10				
Low Level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	At each pins				20		
		IOPL(2)	<ul style="list-style-type: none"> •Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87 	At each pins				15		
	Total output current	Σ IOAL(1)	Ports 0, 1, 70	The total all pins					60	
		Σ IOAL(2)	Port 3	The total all pins					40	
		Σ IOAL(3)	<ul style="list-style-type: none"> •Ports 71, 72, 73 •Ports 84, 85, 86, 87 	The total all pins					20	
Power dissipation (max.)	Pdmax (1)	DIC42S		Ta=+10 to +40°C				630	mW	
	Pdmax (2)	QIC48E		Ta=+10 to +40°C				410		
Operating temperature range		Topr				+10		+40	°C	
Storage temperature range		Tstg				-65		150		

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2. Recommended Operating Range at $V_{SS}=0V$ and $T_a=+10^{\circ}C$ to $+40^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min.	typ.		max.
Operating supply voltage range	VDD	VDD	$0.98\mu s \leq t_{CYC}$ $t_{CYC} \leq 400\mu s$		4.5		6.0	V
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	V _{IH} (1)	Port 0 at CMOS output	Output disable	4.5 to 6.0	$0.33V_{DD} + 1.0$		V _{DD}	
	V _{IH} (2)	Port 0 at N-ch open drain output option.	Output disable	4.0 to 6.0	$0.75V_{DD}$		13.5	
	V _{IH} (3)	•Port 1 •Ports 72, 73 •Port 3 at CMOS output	Output disable	4.5 to 6.0	$0.75V_{DD}$		V _{DD}	
	V _{IH} (4)	Port 3 at N-ch open drain output option.	Output disable	4.5 to 6.0	$0.75V_{DD}$		13.5	
	V _{IH} (5)	•Port 70 Port input / interrupt •Port 71 • \overline{RES}	Output disable	4.5 to 6.0	$0.75V_{DD}$		V _{DD}	
	V _{IH} (6)	Port 70 Watchdog timer	Output disable	4.5 to 6.0	$0.9V_{DD}$		V _{DD}	
	V _{IH} (7)	•Port 8 •Ports $\overline{74}$, 75	Output disable Using as port	4.5 to 6.0	$0.75V_{DD}$		V _{DD}	
Input low voltage	V _{IL} (1)	Port 0 at CMOS output option	Output disable	4.5 to 6.0	V _{SS}		$0.2V_{DD}$	
	V _{IL} (2)	Port 0 at N-ch open drain output option.	Output disable	4.5 to 6.0	V _{SS}		$0.25V_{DD}$	
	V _{IL} (3)	•Ports 1, 3 •Ports 72, 73	Output disable	4.5 to 6.0	V _{SS}		$0.25V_{DD}$	
	V _{IL} (4)	•Port 70 Port input / interrupt •Port 71 • \overline{RES}	Output disable	4.5 to 6.0	V _{SS}		$0.25V_{DD}$	
	V _{IL} (5)	Port 70 Watchdog timer	Output disable	4.5 to 6.0	V _{SS}		$0.8V_{DD} - 1.0$	
	V _{IL} (6)	•Port 8 •Ports $\overline{74}$, 75	Output disable Using as port	4.5 to 6.0	V _{SS}		$0.25V_{DD}$	
Operation cycle time	t _{CYC}			4.5 to 6.0	0.98		400	μs

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Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min.	typ.		max.
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	5.88	6	6.12	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.05	0.50	ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.10	1.00	
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0		1.00	1.50	s

(Note 1) The oscillation constant is shown on table 1 and table 2.

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3. Electrical Characteristics at $V_{SS}=0V$ and $T_a=+10^{\circ}C$ to $+40^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min.	typ.		max.
Input high current	I _{IH} (1)	Ports 0, 3 of Open drain output	•Output disable •V _{IN} =13.5V (including off-leak current of the output Tr.)	4.5 to 6.0			5	μA
	I _{IH} (2)	•Ports 0 without pull-up MOS Tr. •Ports 1, 3 •Ports 70, 71, 72, 73 •Port 8	•Output disable •Pull-up MOS Tr. OFF. •V _{IN} =V _{DD} (including off-leak current of the output Tr.)	4.5 to 6.0			1	
	I _{IH} (3)	\overline{RES}	V _{IN} =V _{DD}	4.5 to 6.0			1	
	I _{IH} (4)	Ports $\overline{74}$, 75	V _{IN} =V _{DD} at using as port	4.5 to 6.0			1	
Input low current	I _{IL} (1)	•Ports 1, 3 •Port 0 without pull-up MOS Tr. •Ports 70, 71, 72, 73 •Port 8	•Output disable •Pull-up MOS Tr. OFF. •V _{IN} =V _{DD} (including off-leak current of the output Tr.)	4.5 to 6.0	-1			
	I _{IL} (2)	• \overline{RES}	V _{IN} =V _{SS}	4.5 to 6.0	-1			
	I _{IL} (3)	Ports $\overline{74}$, 75	V _{IN} =V _{SS} at using as port	4.5 to 6.0	-1			
Output high voltage	V _{OH} (1)	Ports 0, 1, 3 of CMOS output	I _{OH} = -1.0mA	4.5 to 6.0	V _{DD} -1			V
	V _{OH} (2)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	I _{OH} = -0.1mA	4.5 to 6.0	V _{DD} -0.5			
Output low voltage	V _{OL} (1)	Ports 0, 1, 3	I _{OL} =10mA	4.5 to 6.0			1.5	
	V _{OL} (2)		I _{OL} =1.6mA	4.5 to 6.0			0.4	
	V _{OL} (3)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	I _{OL} =1.6mA	4.5 to 6.0			0.4	
	V _{OL} (4)	Port 70	I _{OL} =1.0mA	4.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	R _{pu}	•Ports 0, 1, 3 •Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87	V _{OH} =0.9V _{DD}	4.5 to 6.0	15	40	70	kΩ
Hysteresis voltage	V _{HIS}	•Port 1 •Port 70, 71, 72, 73 • \overline{RES}	Output disable	4.5 to 6.0		0.1V _{DD}		V
Pin capacitance	CP	All pins	•f=1MHz Unmeasurement terminals for input are set to V _{SS} level. •T _a =25°C	4.5 to 6.0		10		pF

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4. Serial Input / Output Characteristics at $V_{SS}=0V$ and $T_a=+10^{\circ}C$ to $+40^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit		
				VDD [V]	min.	typ.		max.	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5	4.5 to 6.0	2		tCYC
		Low level pulse width	tCKL(1)			4.5 to 6.0	1		
		High level pulse width	tCKH(1)			4.5 to 6.0	1		
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	<ul style="list-style-type: none"> •Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5 	4.5 to 6.0	2		
		Low level pulse width	tCKL(2)			4.5 to 6.0		1 / 2tCKCY	
		High level pulse width	tCKH(2)			4.5 to 6.0		1 / 2tCKCY	
Serial input	Data set-up time	tICK	<ul style="list-style-type: none"> •SI0, SI1 •SB0, SB1 	<ul style="list-style-type: none"> •Data set-up to SCK0, 1 •Data hold from SCK0, 1 •Refer to figure 5 	4.5 to 6.0	0.1		μs	
	Data hold time	tCKI			4.5 to 6.0	0.1			
Serial output	Output delay time (Serial clock is external clock)	tCKO(1)	<ul style="list-style-type: none"> •SO0, SO1 •SB0,SB1 	<ul style="list-style-type: none"> •Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0, 1 •Refer to figure 5 	4.5 to 6.0			7 / 12tCYC +0.2	
	Output delay time (Serial clock is internal clock)	tCKO(2)			4.5 to 6.0			1 / 3tCYC +0.2	

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5. Pulse Input Conditions at $V_{SS}=0V$ and $T_a=+10^{\circ}C$ to $+40^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD [V]	min.	typ.	
High / low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2 / TOIN	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	1		tCYC
	tPIH(2) tPIL(2)	INT3 / TOIN (The noise rejection clock select to 1 / 1.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	2		
	tPIH(3) tPIL(3)	INT3 / TOIN (The noise rejection clock select to 1 / 16.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	32		
	tPIL(4) tPIL(4)	INT3 / TOIN (The noise rejection clock select to 1 / 64.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	128		
	tPIL(5)	RES	Reset acceptable	4.5 to 6.0	200		μs

6. A / D Converter Characteristics at $V_{SS}=0V$ and $T_a=+10^{\circ}C$ to $+40^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD [V]	min.	typ.	
Resolution	N			4.5 to 6.0		8	bit
Absolute precision (Note 2)	E _T			4.5 to 6.0			±1.5 LSB
Conversion time	tCAD		AD conversion time=16 X tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC=0.98μs)	65.28 (tCYC=4.08μs)	μs
			AD conversion time=32 X tCYC (ADCR2=1) (Note 3)		31.36 (tCYC=0.98μs)	130.56 (tCYC=4.08μs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	V _{SS}	V _{DD}	V
Analog port input current	I _{AINH}		VAIN=V _{DD}	4.5 to 6.0		1	μA
	I _{AINL}		VAIN=V _{SS}	4.5 to 6.0	-1		

(Note 2) Absolute precision excepts quantizing error ($\pm 1 / 2$ LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

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7. Current Dissipation Characteristics at $V_{SS}=0V$ and $T_a=+10^{\circ}C$ to $+40^{\circ}C$

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min.	typ.		max.
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	<ul style="list-style-type: none"> •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation. •System clock : CF oscillation •Internal RC oscillation stops. •1 / 1 divider 	4.5 to 6.0		14	26	mA
	IDDOP(2)		<ul style="list-style-type: none"> •FmCF=3MHz Ceramic resonator oscillation. •FsXtal=32.768kHz crystal oscillation. •System clock : CF oscillation •Internal RC oscillation stops. •1 / 2 divider 	4.5 to 6.0		6.5	14	
	IDDOP(3)		<ul style="list-style-type: none"> •FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation. •System clock : RC oscillation •1 / 2 divider 	4.5 to 6.0		4	12	
	IDDOP(4)		<ul style="list-style-type: none"> •FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops. •1 / 2 divider 	4.5 to 6.0		3.5	9	

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Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min.	typ.		max.
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD	<ul style="list-style-type: none"> •HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops. •1 / 1 divider 	4.5 to 6.0		4	9	mA
	IDDHALT(2)		<ul style="list-style-type: none"> •HALT mode FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops. •1 / 2 divider 	4.5 to 6.0		2.2	5	
	IDDHALT(3)		<ul style="list-style-type: none"> •HALT mode FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1 / 2 divider 	4.5 to 6.0		400	1600	μA
	IDDHALT(4)		<ul style="list-style-type: none"> •HALT mode FmCF=0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops. •1 / 2 divider 	4.5 to 6.0		25	100	
Current dissipation HOLD mode (Note 4)	IDDHOLD	VDD	HOLD mode	4.5 to 6.0		0.05	30	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

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Table 1. Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA 6.00MG	33pF	33pF
		CST 6.00MGW	on chip	
	Kyocera	KBR-6.0MSA	33pF	33pF
		PBRC 6.00A(chip type)	33pF	33pF
		KBR-6.0MKS	on chip	
	PBRC 6.00B(chip type)			
3MHz ceramic resonator oscillation	Murata	CSA 3.00MG	33pF	33pF
		CST 3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal oscillation	Kyocera			
	Dai SINKU	DT-38 (1TA252E00)	18pF	18pF

* Both C3 and C4 must use J rank ($\pm 5\%$) and CH characteristics.

(It is about the application which is not in need of high precision. Use K rank ($\pm 10\%$) and SL characteristics.)

- Notes
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
 - If you use other oscillators herein, we provide no guarantee for the characteristics.

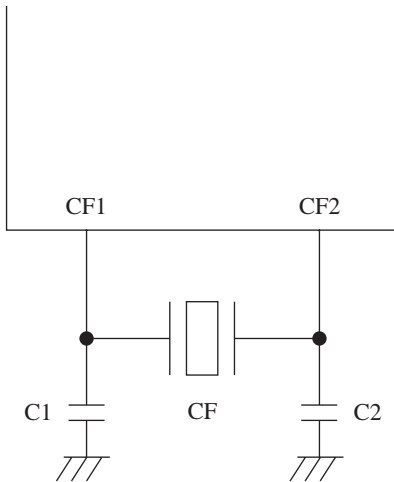


Figure1. Main-clock
Ceramic resonator oscillation

ILC00059

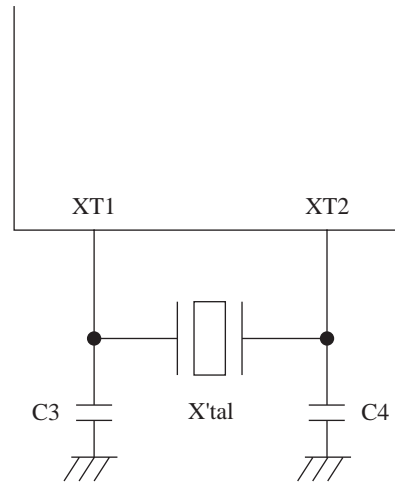


Figure2. Sub-clock
Crystal oscillation

ILC00065

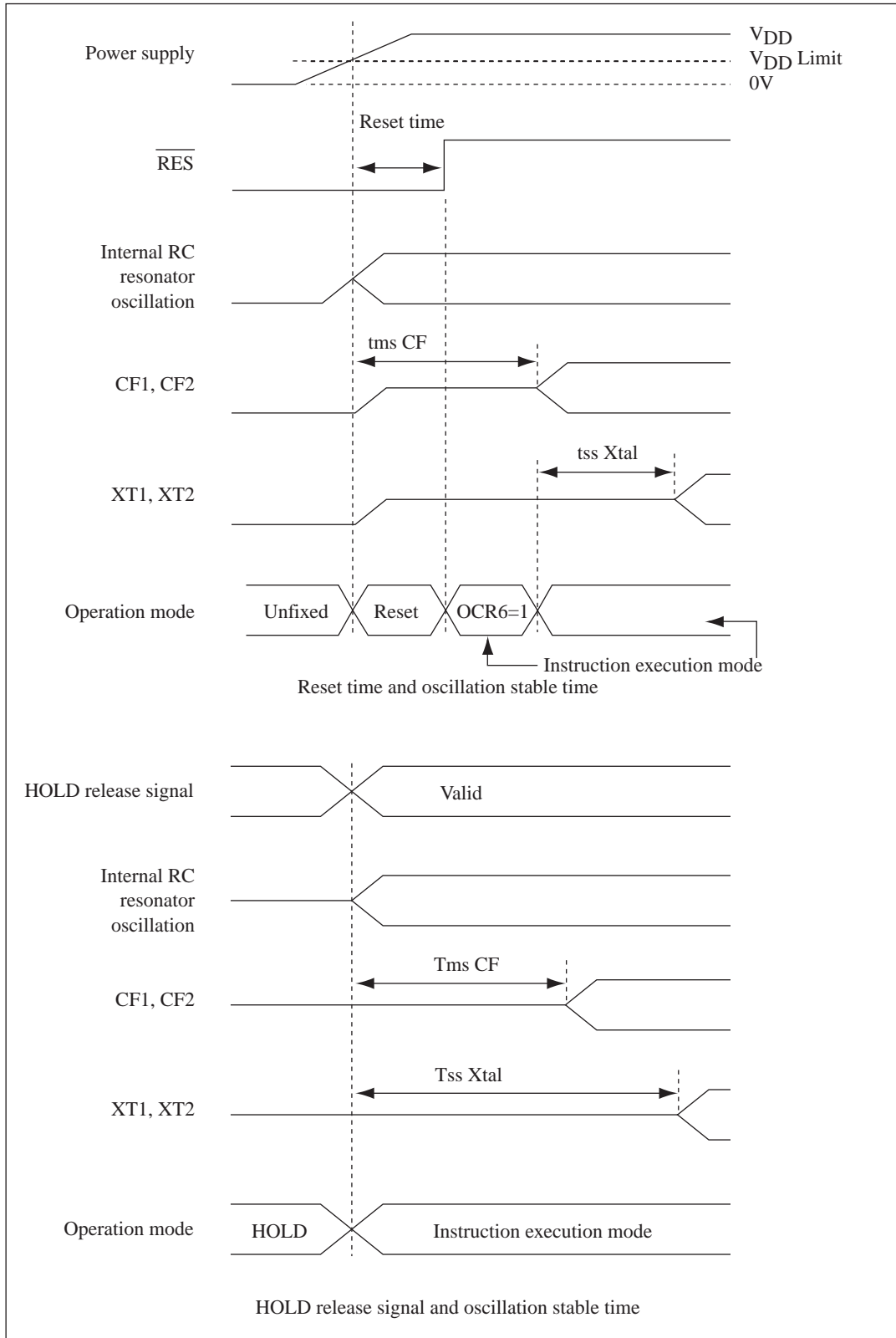
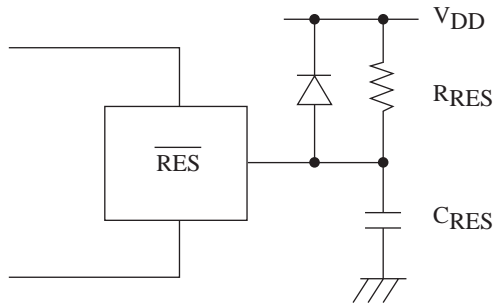


Figure3. Oscillation stable time

ILC00044



(Note) Fix the value of C_{RES} , R_{RES} that is sure to reset until $200\mu s$, after Power supply has been over inferior limit of supply voltage.

Figure4. Reset circuit

ILC00052

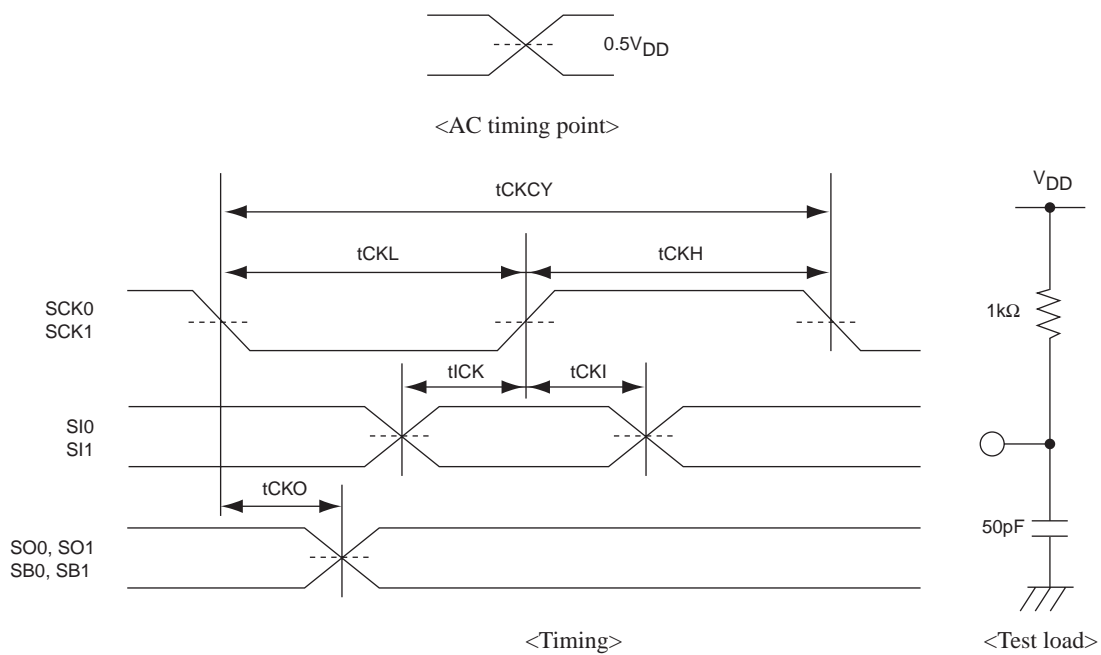


Figure5. Serial input / output test condition

ILC00073

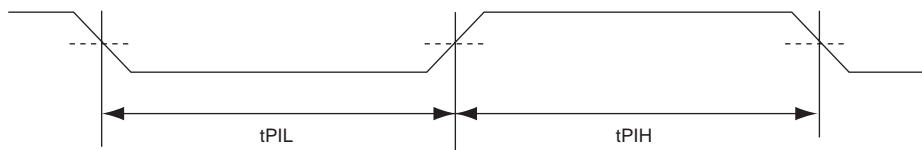


Figure6. Pulse input timing condition

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