



LC86E5632

8-Bit Single Chip Microcontroller with the One-Time Programmable UVEPROM

Preliminary

Overview

The LC86E5632 is a CMOS 8-bit single chip microcontroller with one-time UVEPROM for the LC865600 series. This microcontroller has the function and the pin description of the LC865600 series mask ROM version, and 32K-byte EPROM. The program data is rewritable. It is suitable to developing the program.

Features

- (1) Option switching by EPROM data
The option function of the LC865600 series can be specified by the EPROM data.
LC86E5632 can be checked the function of the trial pieces using the mass production board.
- (2) Internal one-time EPROM capacity : 32768 bytes
- (3) Internal RAM capacity : 512 bytes

Mask ROM version	PROM capacity	RAM capacity
LC865632	32512 bytes	512 bytes
LC865628	28672 bytes	512 bytes
LC865624	24576 bytes	512 bytes
LC865620	20480 bytes	384 bytes
LC865616	16384 bytes	384 bytes
LC865612	12288 bytes	384 bytes
LC865608	8192 bytes	384 bytes

Programming service

We offers various services at nominal charges. These include the ROM writing, the ROM reading, the package stamping and the screening. Contact our representative for further information.

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- (4) Operating supply voltage : 4.5V to 6.0V
- (5) Instruction cycle time : 0.98μs to 400μs
- (6) Operating temperature : +10°C to +40°C
- (7) The pin compatible with mask ROM version
- (8) Applicable mask ROM version : LC865632/ LC865628/ LC865624/LC865620/LC865616/
LC865612/ LC865608
- (9) Factory shipment : DIC64S, QFC64E

Notice for use

LC86E5632 is provided for the first release and small shipping of the LC865600 series.

At using, take notice of the followings.

- (1) A point of difference LC86E5632 and LC865600 series

Item	LC86E5632	LC865632/28/24/20/16/12/08
Port form at reset	Please refer "Port form at reset" on next page.	
Operation after reset releasing	The option is specified until 3ms after going to a 'H' level to the reset terminal by dgreees. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to reset terminal.
Operating supply voltage range (VDD)	4.5V to 6.0V	2.7V to 6.0V
Operating temperature range (Topg)	+10°C to +40°C	-30°C to +70°C
Total output current [ΣIOAH(1)] [ΣIOAH(2)]	Refer to 'electrical characteristics' on the semiconductor news.	
Power dissipation [IDDOP(1)] [IDDOP(2)] [IDDOP(3)] [IDDOP(4)]		

- A kind of the option corresponding of the LC86E5632

A kind of option	Pins, Circuits	Contents of the option
Input/output form of Input/output ports	Port 0 (Specified in a bit)	1. Input : No pull-up MOS Tr. Output : N-channel open drain 2. Input : Pull-up MOS Tr. Output : CMOS
	Port 1,2 (Specified in a bit)	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
	Port 3,4,5 (Specified in a bit)	1. Input : No Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
Pull-up MOS Tr. Of port7	port7 (Specified in a bit)	1. Pull-up MOS Tr. not provided 2. Pull-up MOS Tr. provided * P74 has on pull-up resistor option.

The port operation related the option is different at reset. Refer to the next table.

•Port form at reset

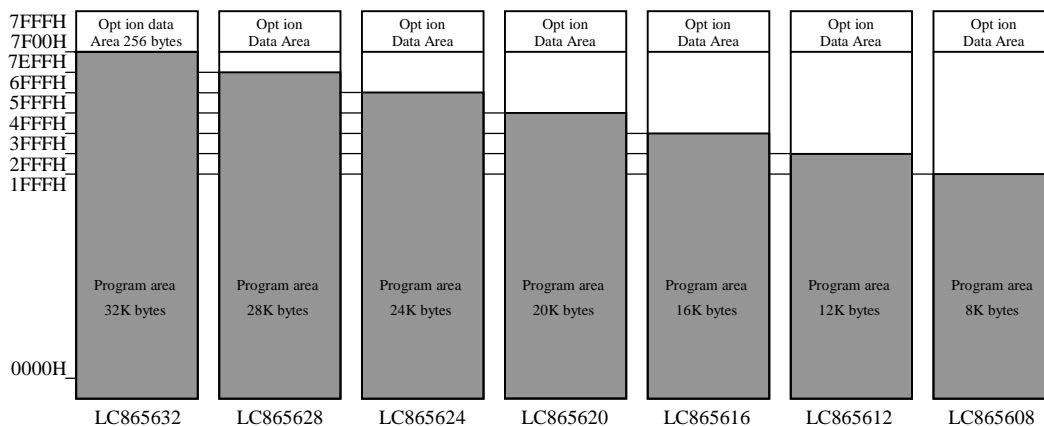
Pin	Contents of the option	LC86E5632	LC865632/28/24/20/16/12/08
P0	Input : Not pull-up MOS Tr. Output : N-channel open drain	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
	Input : Pull-up MOS Tr. Output : CMOS	Input mode •The pull-up MOS Tr. is not provided during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS Tr. is provided. (Output is OFF)	Input mode without pull-up MOS Tr. (Output is OFF)
P1, P2	Input : Programmable pull-up MOS Tr. Output : N-channel open drain	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
	Input : Programmable pull-up MOS Tr. Output : CMOS	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
P3, P4, P5	Input : Not Programmable pull-up MOS Tr. Output : N-channel open drain	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
	Input : Programmable pull-up MOS Tr. Output : CMOS	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
P7	Pull-up MOS Tr. not provided	(Same as the mask version)	Input mode without pull-up MOS Tr.
	Pull-up MOS Tr. provided	Input mode •The pull-up MOS Tr. is not provided during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS Tr. is provided.	Input mode without pull-up MOS Tr.

(2) Option

LC86E5632 uses 256 bytes which is addressed on 7F00H to 7FFFH in the program memory as option data area. This area does not affect the execution of program but the program memory capacity of LC865632 is 32512 bytes which is addressed on 0000H to 7EFFH.

The option data is created by the option specified program “SU865000.EXE”. The created option data is linked to the program area by linkage loader “L865000.EXE”.

(3) ROM space



How to use

(1) Specification of option

Programming data for EPROM of the LC86E5632 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86E5632.

(2) How to program for the EPROM

LC86E5632 can be programmed by the EPROM programmer with attachment ; W86EP5032D, W86EP5032Q.

- Recommended EPROM programmer

Product	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL 1890A

- “27512 (Vpp=12.5V) Intel high speed programming” mode available. The address must be set to “0000H to 7FFFH” and a jumper (DASEC) must be set to ‘OFF’ at programming.

(3) How to use the data security function

“Data security” is the disabled function to read the data of the EPROM.

The following is the process in order to execute the data security.

1. Set ‘ON’ the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

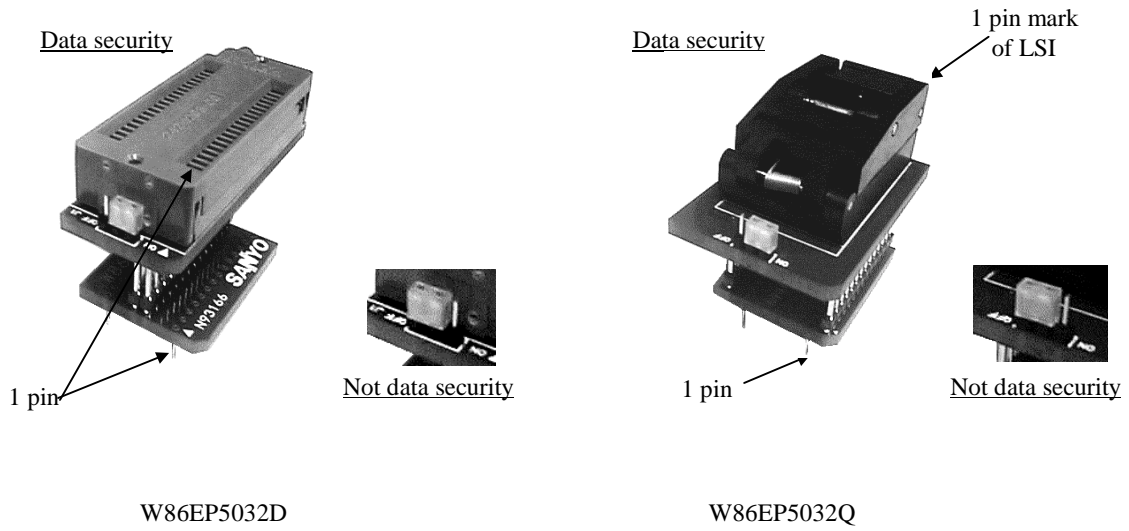
- Data security is not executed when the data of all address have ‘FF’ at the sequence 2 above.
- The programming by a sequential operation “BLANK⇒PROGRAM⇒VERIFY” cannot be executed data security at the sequence 2 above.
- Set to ‘OFF’ the jumper after executing the data security.

(4) How to eliminate

The programming data can be erased by using the EPROM eraser.

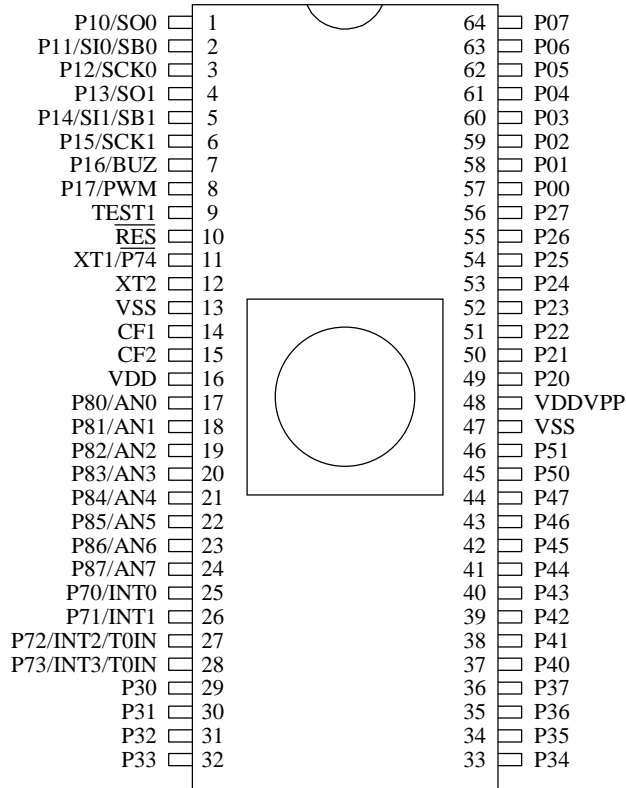
(5) Shielding

The UVEPROM (ultraviolet erasable programmable ROM) is in it. Put the seal on the window in use.

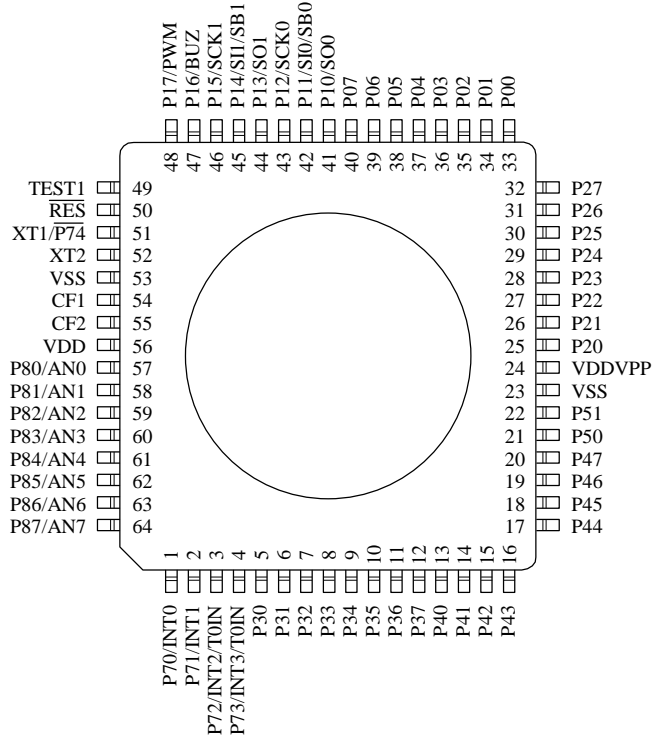


Pin Assignment

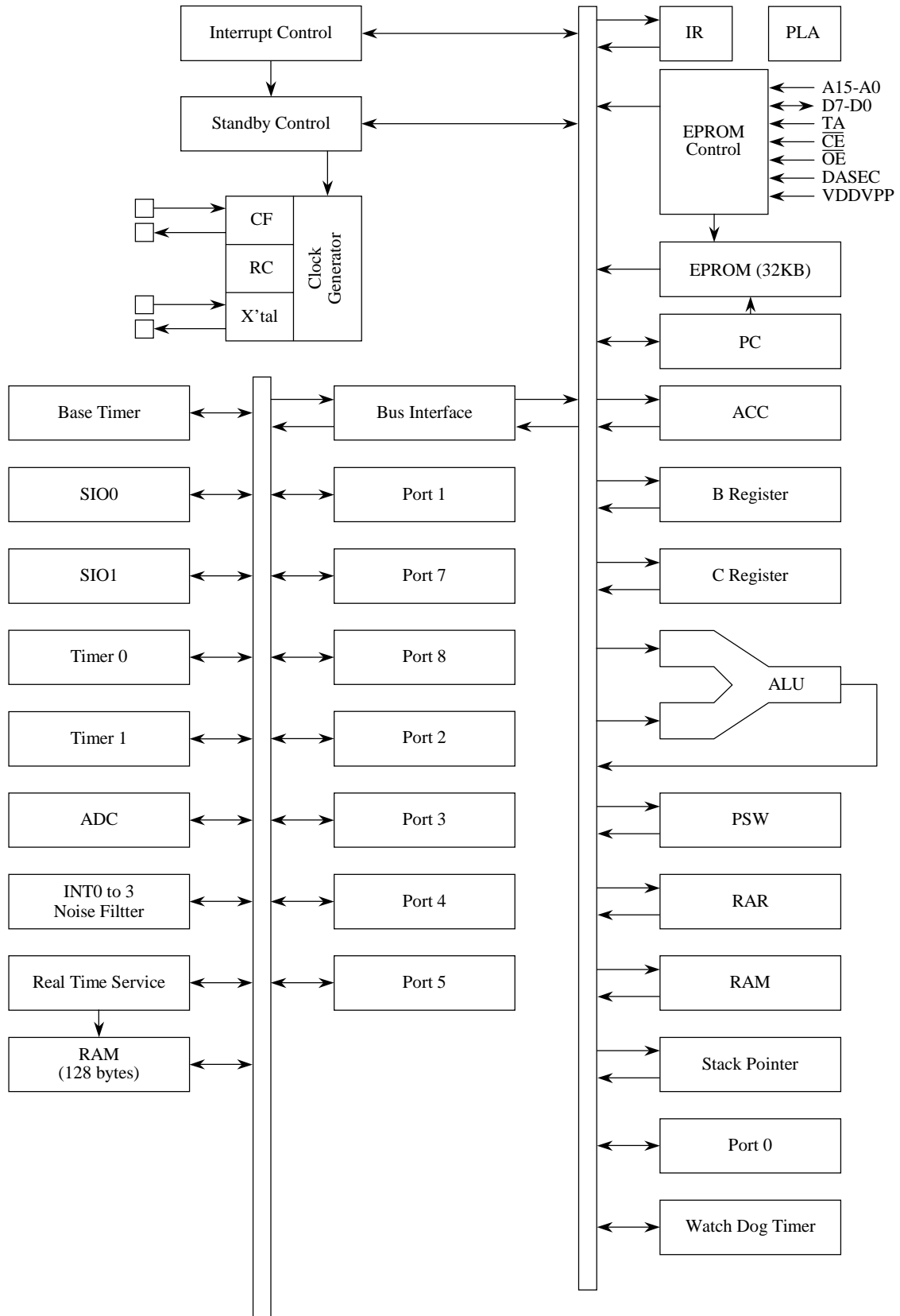
SANYO:DIC64S



SANYO:QFC64E



System Block Diagram



LC86E5632 Pin description

Pin name	I/O	Function description	Option	PROM mode																																			
VSS	-	Power pin (-)	-	-																																			
VDD	-	Power pin (+)	-	-																																			
VDDVPP	-	Power pin (+)	-	Power for programming																																			
PORT0 P00 to P07	I/O	<ul style="list-style-type: none"> •8-bit input/output port •Input for port 0 interrupt •Input/output in nibble units •Input for HOLD release 	<ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided •Output form : CMOS/N-channel open drain 	-																																			
PORT1 P10 to P17	I/O	<ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit unit •Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer 1 output (PWM0 output) 	Output form : CMOS/N-channel open drain	Data line D0 to D7																																			
PORT2 P20 to P27	I/O	<ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit unit 	Output form : CMOS/N-channel open drain																																				
PORT3 P30 to P37	I/O	<ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit unit •15V withstand at N-channel open drain output 	Output form : CMOS/N-channel open drain	Address input A7 to A0																																			
PORT4 P40 to P47	I/O	<ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit unit •15V withstand at N-channel open drain output 	Output form : CMOS/N-channel open drain	Address input A14 to A8 (*5) P47 : TA (*4)																																			
PORT5 P50 to P51	I/O	<ul style="list-style-type: none"> •2-bit input/output port •Input/output can be specified in a bit unit •15V withstand at N-channel open drain output 	Output form : CMOS/N-channel open drain																																				
PORT7 P70 P71 to $\overline{P74}$	I/O I	<ul style="list-style-type: none"> •5-bit input port •Other pin functions P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer P71 : INT1 input/HOLD release input P72 : INT2 input/timer 0 event input P73 : INT3 input with noise filter/timer 0 event input $\overline{P74}$: 32.768kHz crystal oscillation terminal XT1 •Interrupt received forms, the vector addresses <table border="1" data-bbox="365 1585 933 1774"> <thead> <tr> <th></th> <th>rising</th> <th>falling</th> <th>rising & falling</th> <th>high level</th> <th>low level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table>		rising	falling	rising & falling	high level	low level	vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	<ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided (P70,71,72,73) •$\overline{P74}$ has no pull-up resistor. 	Input of PROM control signals DASEC (*1) \overline{OE} (*2) \overline{CE} (*3)
	rising	falling	rising & falling	high level	low level	vector																																	
INT0	enable	enable	disable	enable	enable	03H																																	
INT1	enable	enable	disable	enable	enable	0BH																																	
INT2	enable	enable	enable	disable	disable	13H																																	
INT3	enable	enable	enable	disable	disable	1BH																																	

Continue.

Pin name	I/O	Function description	Option	PROM mode
PORT8 P80 to 87	I	•8-bit input port •Other function AD input port (AN7 to AN0)	-	-
RES	I	Reset pin	-	-
TEST1	O	Test pin Should be left unconnected.	-	-
XT1/ $\overline{P74}$	I	•Input pin for 32.768kHz crystal oscillation •Other function : Input port $\overline{P74}$ In case of non use, connect to VDD.	-	-
XT2	O	•Output pin for 32.768kHz crystal oscillation •Other function In case of non use, should be left unconnected.	-	-
CF1	I	Input pin for the ceramic resonator oscillation	-	-
CF2	O	Output pin for the ceramic resonator oscillation	-	-

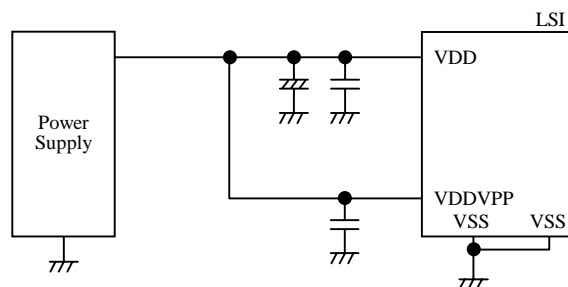
◆ All of port options can be specified in bit unit.

- *1 Memory select input for data security
- *2 Output enable input
- *3 Chip enable input
- *4 TA → PROM control signal input
- *5 A14 → Address input

* Connect like the following figure to reduce noise into a VDD terminal.

Short-circuit the VDD terminal to the VDDVPP terminal.

Short-circuit the VSS terminal to the VSS terminal.



1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Supply voltage	VDDMAX	VDD,VDDVPP	VDD=VDDVPP		-0.3		+7.0	V
Input voltage	VI(1)	•Ports 71,72,73, 74 •Port 8 •RES			-0.3		VDD+0.3	
Input/Output voltage	VIO(1)	•Ports 0,1,2 •Ports 3,4,5 at CMOS output			-0.3		VDD+0.3	
	VIO(2)	Ports 3,4,5 at N-ch open drain output option			-0.3		15	
High level output current	Peak output current	IOPH(1)	•Ports 0,1,2,3,4,5	•CMOS output •At each pins		-4		mA
	Total output current	ΣIOAH(1)	Ports 0,1,2	The total of all pins		-25		
		ΣIOAH(2)	Ports 3,4,5	The total of all pins			-20	
Low level output current	Peak output current	IOPL(1)	Ports 0,1,2,3,4,5	At each pins			20	
		IOPL(2)	Port 70	At each pins			15	
	Total output current	ΣIOAL(1)	Ports 0,1,70	The total of all pins				40
		ΣIOAL(2)	Port 2	The total of all pins				40
		ΣIOAL(3)	Ports 3,4,5	The total of all pins				80
Maximum power dissipation	Pdmax(1)	DIP64S	Ta=+10 to+40°C				720	mW
	Pdmax(2)	QFP64E	Ta=+10 to+40°C				420	
Operating Temperature range	Topr				10		40	°C
Storage Temperature range	Tstg				-65		150	

2. Recommended Operating Range at Ta=+10°C to +40°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Operating Supply voltage	VDD(1)	VDD	$0.98\mu\text{s} \leq t_{\text{CYC}}$ $t_{\text{CYC}} \leq 400\mu\text{s}$		4.5		6.0	V
Hold voltage	VHD	VDD	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	$0.4V_{\text{DD}}$ $+0.9$		VDD	
	VIH(2)	•Ports 1,2 •Ports 72,73 (Schmitt)	Output disable	4.5 to 6.0	$0.75V_{\text{DD}}$		VDD	
	VIH(3)	•Port 70 (Port input/interrupt) •Port 71 •RES (Schmitt)	Output N-channel Tr. OFF	4.5 to 6.0	$0.75V_{\text{DD}}$		VDD	
	VIH(4)	Port 70 (Watchdog timer)	Output N-channel Tr. OFF	4.5 to 6.0	$0.9V_{\text{DD}}$		VDD	
	VIH(5)	•Port 74 •Port 8	Output N-channel Tr. OFF	4.5 to 6.0	$0.75V_{\text{DD}}$		VDD	
	VIH(6)	Ports 3,4,5 of CMOS output (Schmitt)	Output disable	4.5 to 6.0	$0.75V_{\text{DD}}$		VDD	
	VIH(7)	Ports 3,4,5 of open drain output (Schmitt)	Output disable	4.5 to 6.0	$0.75V_{\text{DD}}$		13.5	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	VSS		$0.2V_{\text{DD}}$	
	VIL(2)	•Ports 1,2,3,4,5 •Ports 72,73 (Schmitt)	Output disable	4.5 to 6.0	VSS		$0.25V_{\text{DD}}$	
	VIL(3)	•Port 70 (Port input/interrupt) •Port 71 •RES (Schmitt)	N-channel Tr.OFF	4.5 to 6.0	VSS		$0.25V_{\text{DD}}$	
	VIL(4)	Port 70 (Watchdog timer)	N-channel Tr.OFF	4.5 to 6.0	VSS		$0.8V_{\text{DD}}$ -1.0	
	VIL(5)	•Port 74 •Port 8	N-channel Tr.OFF	4.5 to 6.0	VSS		$0.25V_{\text{DD}}$	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		6		MHz
	FmCF(2)	CF1, CF2	•1.5MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		1.5		
	FmRC		RC oscillation	4.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5 to 6.0		32.768		kHz

Continue.

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Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	<ul style="list-style-type: none"> •6MHz (ceramic resonator oscillation) •Refer to figure 3 	4.5 to 6.0				ms
	tmsCF(2)	CF1, CF2	<ul style="list-style-type: none"> •1.5MHz (ceramic resonator oscillation) •Refer to figure 3 	4.5 to 6.0				
	tssXtal	XT1, XT2	<ul style="list-style-type: none"> •32.768kHz (crystal oscillation) •Refer to figure 3 	4.5 to 6.0				s

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=+10°C to +40°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Input high current	I _{IH} (1)	Ports 3,4,5 at open drain output	•Output disable •VIN=13.5V (including off-leakage current of the output Tr.)	4.5 to 6.0			5	μA
	I _{IH} (2)	•Port 0 without pull-up MOS Tr. •Ports 1,2,3,4,5	•Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including off-leakage current of the output Tr.)	4.5 to 6.0			1	
	I _{IH} (3)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VDD	4.5 to 6.0			1	
	I _{IH} (4)	RES	VIN=VDD	4.5 to 6.0			1	
Input low current	I _{IL} (1)	•Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leakage current of the output Tr.)	4.5 to 6.0	-1			
	I _{IL} (2)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VSS	4.5 to 6.0	-1			
	I _{IL} (3)	RES	VIN=VSS	4.5 to 6.0	-1			
Output high voltage	V _{OH} (1)	Ports 0,1,2,3,4,5 at CMOS output	I _{OH} =-1.0mA	4.5 to 6.0	VDD-1			V
	V _{OH} (2)	CMOS output	I _{OH} =-0.1mA	4.5 to 6.0	VDD-0.5			
Output low voltage	V _{OL} (1)	Ports 0,1,2,3,4,5	I _{OL} =10mA	4.5 to 6.0			1.5	
	V _{OL} (2)		I _{OL} =1.6mA	4.5 to 6.0			0.4	
	V _{OL} (3)	Port 70	I _{OL} =1mA	4.5 to 6.0			0.4	
	V _{OL} (4)		I _{OL} =0.5mA	4.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	R _{pu}	•Ports 0,1,2,3,4,5 •Ports 70,71,72,73	V _{OH} =0.9VDD	4.5 to 6.0	15	40	70	kΩ
Hysteresis voltage	V _{HIS}	•Ports 0,1,2,3,4,5 •Ports 70,71,72,73 •RES	Output disable	4.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •VIN=VSS for all unmeasured terminals. •Ta=25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=+10°C to +40°C, VSS=0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings			unit	
						min.	typ.	max.		
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5	4.5 to 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) in the open drain output. •Refer to figure 5	4.5 to 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time	tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0	0.1			μs	
	Data hold time	tCKI				0.1				
Serial output	Output delay time (External clock using for serial transfer clock)	tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) in the open drain output. •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0			7/12	tCYC +0.2	
	Output delay time (Internal clock using for serial transfer clock)	tCKO(2)						1/3		tCYC +0.2

5. Pulse Input Conditions at Ta=+10°C to +40°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN •INT3	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	1		tCYC
	tPIH(2) tPIL(2)	INT3 (The noise rejection clock selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	2		
	tPIH(3) tPIL(3)	INT3 (The noise rejection clock selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	32		
	tPIL(4)	RES	Reset acceptable	4.5 to 6.0	200		μs

6. AD Converter Characteristics at Ta=+10°C to +40°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	
Resolution	N			4.5 to 6.0		8	bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1.5 LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)	65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)	130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS	VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0		1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1		

(Note 2) Absolute precision excepts the quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=+10°C to +40°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	<ul style="list-style-type: none"> •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops 	4.5 to 6.0		13	26	mA
	IDDOP(2)		<ul style="list-style-type: none"> •FmCF=1.5MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops 	4.5 to 6.0		7	14	
	IDDOP(3)		<ul style="list-style-type: none"> •FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation 	4.5 to 6.0		4	10	
	IDDOP(4)		<ul style="list-style-type: none"> •FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops 	4.5 to 6.0		4	8	

Continue.

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Current dissipation in HALT mode (Note 4)	IDDHALT(1)		<ul style="list-style-type: none"> •HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops 	4.5 to 6.0		5	10	mA
	IDDHALT(2)		<ul style="list-style-type: none"> •HALT mode •FmCF=1.5MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops 	4.5 to 6.0		2.2	4.6	
	IDDHALT(3)		<ul style="list-style-type: none"> •HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation 	4.5 to 6.0		550	1000	μA
	IDDHALT(4)		<ul style="list-style-type: none"> •HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops 	4.5 to 6.0		25	100	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2	Rf	Rd
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF	OPEN	560Ω
		CSA12.0MTZ	39pF	30pF	OPEN	0Ω
		CST12.0MTW	on chip		OPEN	560Ω
3MHz ceramic resonator oscillation	Murata	CSA3.00MG040	100pF	100pF	OPEN	1.5Ω
		CST3.00MGW040	on chip		OPEN	1.5Ω

* Both C1 and C2 must use K rank ($\pm 10\%$) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4
32.768kHz crystal oscillation	Kyocera	KF-38G-13P0200	18pF	18pF
	Seiko Epson	MC-306,C-002RX,32.768kHz	4pF	4pF

* Both C3 and C4 must use J rank ($\pm 5\%$) and CH characteristics.

(It is about the application which is not in need of high precision. Use K rank ($\pm 10\%$) and SL characteristics.)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

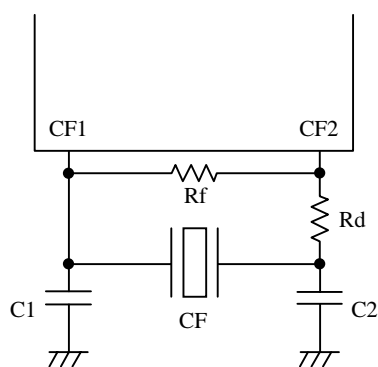


Figure 1 Main-clock circuit
Ceramic oscillation circuit

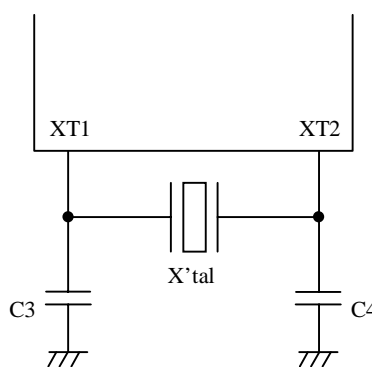


Figure 2 Sub-clock circuit
Crystal oscillation

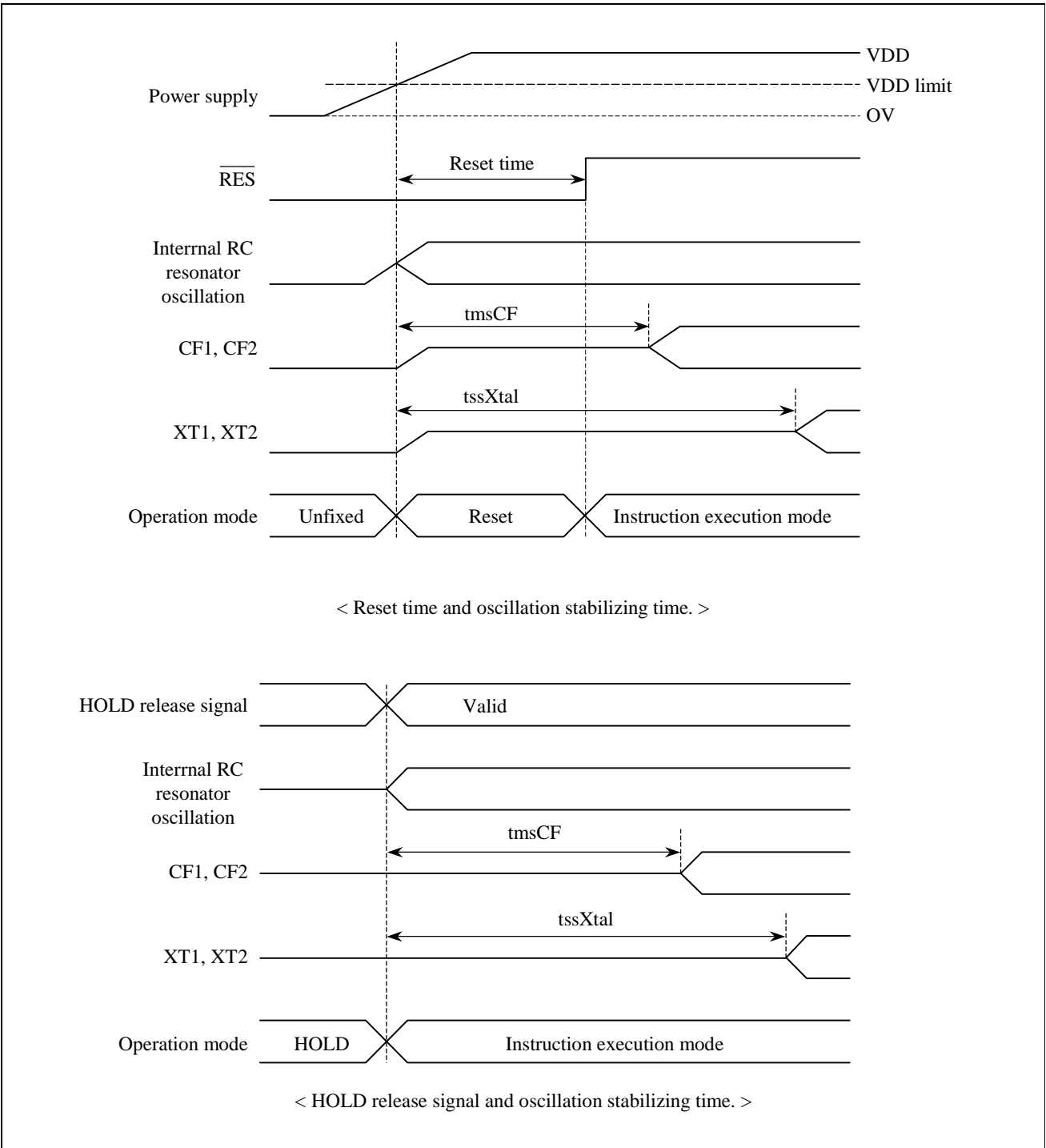
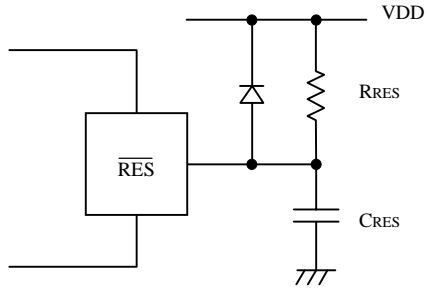


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200 μ s, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

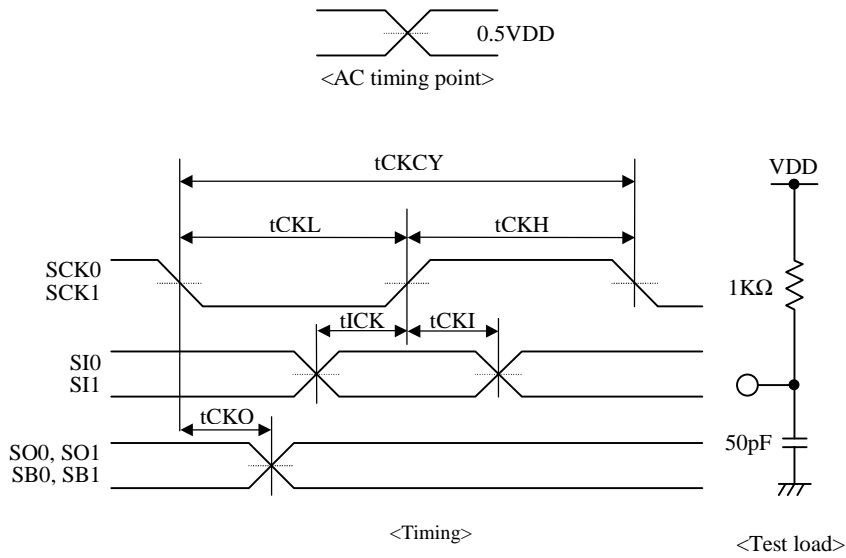


Figure 5 Serial input / output test condition

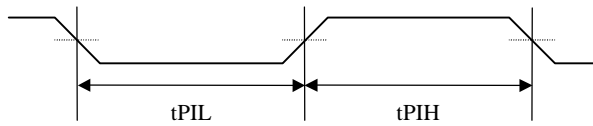


Figure 6 Pulse input timing condition

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