Ordering number : EN*8226

Preliminary

SANYO Semiconductors
DATA SHEET

CMOS IC

LC890561W — Digital Audio Interface Receiver with Built-in Data Buffer Memory

Overview

The LC890561W is an audio LSI that synchronizes with the input signal and demodulates the signal into the normal format signal during data transmission between digital audio devices via the IEC60958 and EIAJ CP-1201.
It supports sampling frequencies of up to 192kHz. It is replaceable with the existing LC89056W by devising the mounting board. The LC890561W has a build-in data buffer memory that allows a lip synchronization function.
It allows the audio data output to be delayed after demodulation.
The LC890561W is applicable to the reception of digital data transmission, such as AV amplifier, AV receiver and car audio.

1. Features

- Built-in PLL circuit to synchronize with transferred input bi-phase signal.
- Built-in PLL error lock prevention circuit for accurate locking.
- Equipped with three S/PDIF data input pins that support TTL input port of 5V interface.
- Receives sampling frequencies of 32kHz to 192kHz.
- Outputs the following clocks: 512fs, 384fs, 256fs, 64fs and fs.
- Outputs the fs information of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz 176.4kHz and 192kHz.
- Built-in oscillation amplifier: 24.57MHz or 12.28MHz
- Outputs transitional period signal where VCO clock and oscillation amplifier clock are switched.
- Outputs up to 24bits of data. Also supports 24bit I^2S data.
- Built-in SRAM of 24576word × 24bit to allow delay of output data.
- Two types of data output pins to set delay or not delay of output data.
- Contains the pin that outputs the delay setting state of output data.
- Contains the output pin for bit 1 (Non-PCM data detection bit) of channel status.
- Outputs channel status emphasis information.
- Outputs update flag for first 48bits of channel status.
- Outputs synchronization signal for burst preambles Pa, Pb, Pc and Pd.
- Outputs validity flag.
- Switching of the serial audio input data and recovery data is possible.
- The delay setting of output data for serial audio data input is possible.

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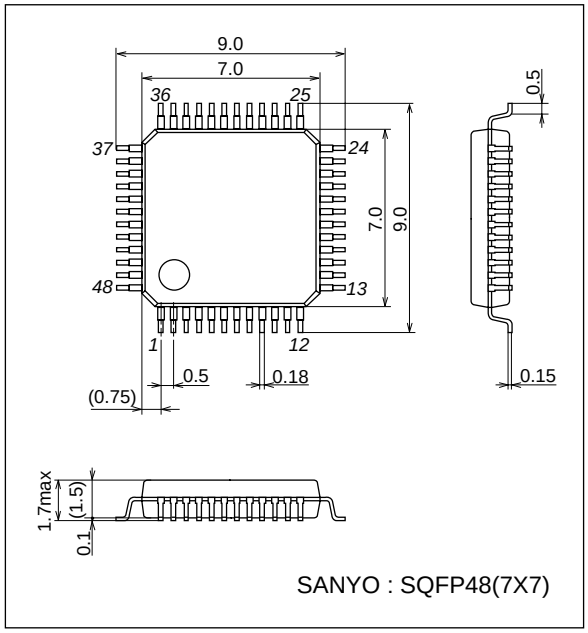
- Microcontroller interface enables various setting and outputs.
  - −Clock control.
  - −Digital/analog source signal switching.
  - −Selection of data input pin.
  - −Selection of data output format.
  - −Error flag selection.
  - −Lock range setting of input data.
  - −PLL error flag, input fs calculation result and first 48bits of channel status output.
  - −16bit Non-PCM burst preamble Pc data output.
- 3.3V single source power supply. (Built-in 1.8V output regulator, 5V TTL interface is possible.)
- Package: SQFP-48

2. Package Dimensions

unit : mm

3163B



3. Pin Assignment

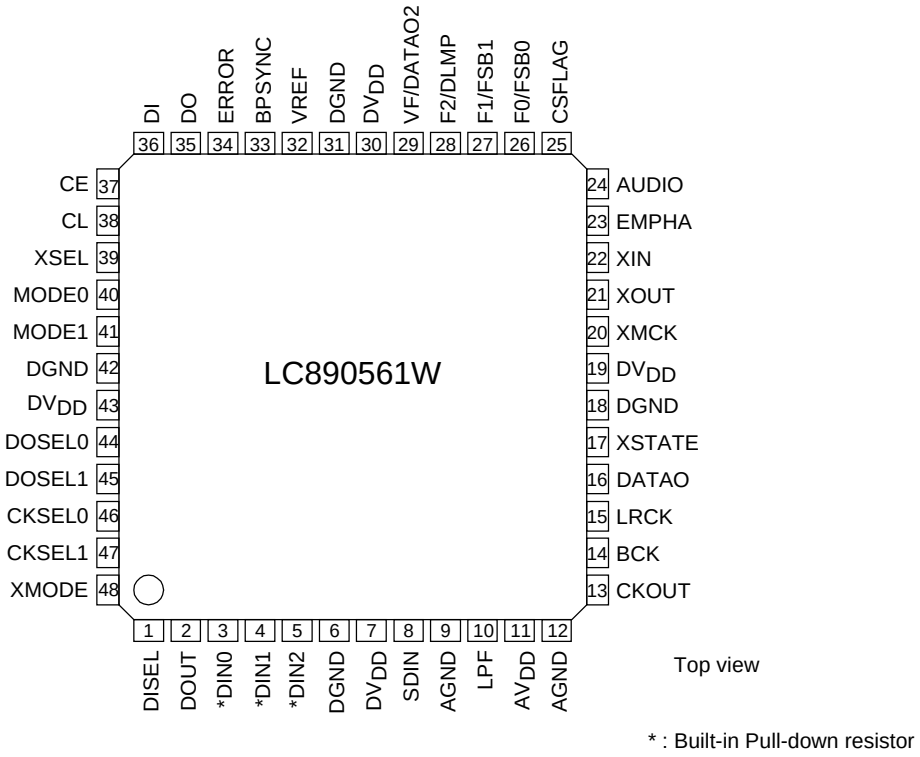


Figure 3.1 LC890561W Pin Assignment

4. Pin Functions

Table 4.1 Pin Functions

Pin No.	Pin Name	I/O	Function
1	DISEL	I_5	Selection input pin of data input pin (DIN0, DIN1)
2	DOUT	O	Input bi-phase data through output pin
3	DIN0	I_5	Input pin of TTL-compatible digital data (Pull-down resistor internal)
4	DIN1	I_5	Input pin of TTL-compatible digital data (Pull-down resistor internal)
5	DIN2	I_5	Input pin of TTL-compatible digital data (Pull-down resistor internal)
6	DGND	-	Digital GND
7	DV_{DD}	-	Digital power supply (3.3V)
8	SDIN	I_5	Input pin of TTL-compatible serial audio data
9	AGND	I	Analog GND for PLL
10	LPF	O	PLL loop filter setting pin
11	AV_{DD}	-	Analog power supply for PLL (3.3V)
12	AGND	-	Analog GND for PLL
13	CKOUT	O	Clock output pin (256fs, 384fs, 512fs, crystal oscillation, VCO free-running oscillation)
14	BCK	O	64fs clock output pin
15	LRCK	O	Fs clock output pin (L = R-ch, H = L-ch, inverted at I^2S)
16	DATAO	O	Post-demodulation audio data output pin (Delay function is possible)
17	XSTATE	O	Source clock switch monitor output pin
18	DGND	-	Digital GND
19	DV_{DD}	-	Digital power supply (3.3V)
20	XMCK	O	Crystal oscillation clock output pin (24.576MHz or 12.288MHz)
21	XOUT	O	Crystal oscillation connection output pin
22	XIN	I	Crystal oscillation input pin, external input supported (24.576MHz or 12.288MHz)
23	EMPHA	O	Channel status emphasis information output pin
24	AUDIO	O	Channel status bit 1 (non-PCM data detection bit) output pin
25	CSFLAG	O	Update flag output pin of first 48bits of channel status
26	F0/FSB0	O	Input fs calculation signal output pin || Input fs calculation signal arrange frequency bands output pin
27	F1/FSB1	O	Input fs calculation signal output pin || Input fs calculation signal arrange frequency bands output pin

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Pin No.	Name	I/O	Function
28	F2/DLMP	O	Input fs calculation signal output pin || Output data delay mute period monitor output pin
29	VF/DATAO2	O	Validity flag output pin/Data output pin (Delay is impossible)
30	DV_{DD}	-	Digital power supply (3.3V)
31	DGND	-	Digital GND
32	VREF	O	Regulator monitor output pin (1.8V)
33	BPSYNC	O	Non-PCM burst preamble Pa, Pb, Pc, Pd sync signal output pin
34	ERROR	O	PLL lock error or data error flag output pin
35	DO	O_5	Microcontroller I/F, read data output pin
36	DI	I_5	Microcontroller I/F, write data input pin
37	CE	I_5	Microcontroller I/F, chip enable input pin
38	CL	I_5	Microcontroller I/F, clock input pin
39	XSEL	I_5	[XIN] crystal oscillation selection input pin (24.576MHz or 12.288MHz)
40	MODE0	I_5	Mode setting input pin
41	MODE1	I_5	Mode setting input pin
42	DGND	-	Digital GND
43	DV_{DD}	-	Digital power supply (3.3V)
44	DOSEL0	I_5	Output data format selection input pin
45	DOSEL1	I_5	Output data format selection input pin
46	CKSEL0	I_5	Output clock selection input pin
47	CKSEL1	I_5	Output clock selection input pin
48	XMODE	I_5	System reset input pin

Note:

* Withstand voltage input/output: I or O = -0.3 to 3.6V, I_5 or O_5 = -0.3 to 5.5V
* To prevent logic circuit latch-up, digital power supply and analog power supply must be applied or removed simultaneously and with the same potential.

5. Block Diagram

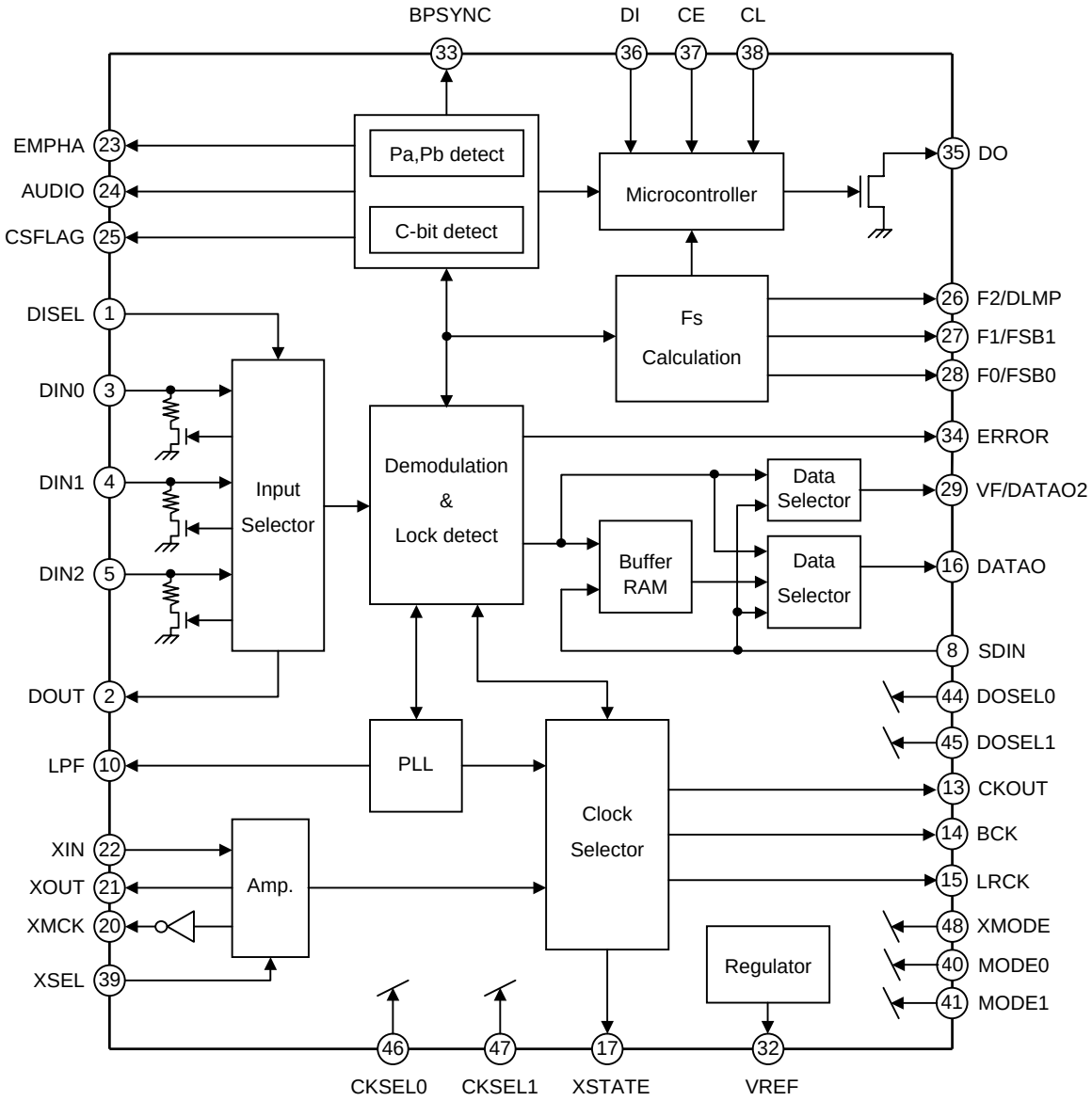


Figure 5.1 LC890561W Block Diagram

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	$V_{DD}33max$	6-1-1	-0.3 to 3.96	V
Input Voltage 1	V_I1	6-1-2	-0.3 to V_{DD}+0.3 (max.3.96)	V
Input Voltage 2	V_I2	6-1-3	-0.3 to 5.5	V
Output Voltage	V_O		-0.3 to V_{DD}+0.3 (max.3.96)	V
Storage Ambient Temperature	Tstg		-55 to 125	°C
Operating Ambient Temperature	Topr		-30 to 70	°C
Maximum Input/Output Current	I_{IN}, I_{OUT}	6-1-4	±20	mA

6-1-1: DV_{DD} and AV_{DD} pins
6-1-2: DISEL, XIN, XSEL, MODE0, MODE1, DOSEL0, DOSEL1, CKSEL0 and CKSEL1 input pins
6-1-3: DIN0, DIN1, DIN2, SDIN, DI, CE, CL and XMODE input pins
6-1-4: Per input/output pin

6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply Voltage	$V_{DD}33$	6-2-2	3.0	3.3	3.6	
Input Voltage Range 1	$V_{IN}1$	6-2-3	0		AV_{DD}, DV_{DD}	V
Input Voltage Range 2	$V_{IN}2$	6-2-4	0		5.5	V
Operating Temperature	Vopr		-30		70	°C

6-2-1: DV_{DD} and AV_{DD} pins
6-2-2: DISEL, XIN, XSEL, MODE0, MODE1, DOSEL0, DOSEL1, CKSEL0 and CKSEL1 input pins
6-2-3: DN0, DIN1, DIN2, SDIN, DI, CE, CL and XMODE input pins

6.3 DC Characteristics

Table 6.3 DC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input, High	V_{IH}	6-3-1	2.0			V
Input, Low	V_{IL}				$0.3DV_{DD}$	V
Input, High	V_{IH}	6-3-2	2.0			V
Input, Low	V_{IL}				0.8	V
Input, High	V_{IH}	6-3-3	2.0			V
Input, Low	V_{IL}				0.8	V
Output, High	V_{OH}	6-3-4	DV_{DD}-0.4			V
Output, Low	V_{OL}				0.4	V
Consumption Current	I_{DD}	6-3-5		20	40	mA
Pull-Down Resistor	DDN	6-3-6	45	90	180	kΩ

6-3-1: CMOS level: DISEL, XIN, XSEL, MODE0, MODE1, DOSEL0, DOSEL1, CKSEL0 and CKSEL1 input pins
6-3-2: TTL level: DIN0, DIN1, DIN2 and SDIN input pins
6-3-3: TTL Schmidt level: DI, CE, CL and XMODE input pins
6-3-4: I_{OH} = −12mA, I_{OL} = 12mA: CKOUT output pins
I_{OH} = −8mA, I_{OL} = 8mA: DOUT, XOUT and XMCK output pins
I_{OH} = −4mA, I_{OL} = 4mA: BCK, LRCK, DATAO, VF/DATAO2 and F2/DLMP output pins
I_{OH} = −2mA, I_{OL} = 2mA: output pins other than those listed above
6-3-5: Ta = 25°C, input data fs = 96kHz
6-3-6: DIN0, DIN1 and DIN2 input pins

6.4 AC Characteristics

Table 6.4 AC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DIN* Rising/Falling Edge Period	t_{Rd}, t_{FD}				15	ns
DIN* Data Pulse Width	t_{WDI}		20			ns
DIN* Duty	t_{DUTY}	6-4-1	40		60	%
XIN Crystal Resonator Frequency	$f_{XT}0$	6-4-2		24.576		MHz
XIN Crystal Resonator Frequency	$f_{XT}1$	6-4-3		12.288		MHz
XIN Crystal Resonator Frequency	$f_{XT}2$	6-4-4	12		25	MHz
XMCK Output Clock	f_{XO}		6		25	MHz
VCO Free-Running Frequency	f_{VCO}	6-4-5	1		100	MHz
CKOUT Output Clock Frequency	f_{MCK}		1		100	MHz
CKOUT Duty	t_{DUTY}			50		%
BCK Output Pulse Width	t_{WBO}	6-4-6		1/128fs		ns
Output Data Setup Time	t_{DSO}			1/256fs		ns
Output Data Hold Time	t_{DHO}			1/256fs		ns
Output Delay	t_{BD}		-10	0	10	ns

6-4-1: DIN* = 1 setting, at 1/2 DV_{DD}
6-4-2: XSEL = 0 (Except MODE0 = 1 and MODE1 = 1 setup)
6-4-3: XSEL = 1 (Except MODE0 = 1 and MODE1 = 1 setup)
6-4-4: XSEL = 1 (MODE0 = 1 and MODE1 = 1 setup)
6-4-5: Ta = 25°C, DV_{DD} = AV_{DD} = 3.3V (At the time of recommendation circuit setup)
6-4-6: fs = input sampling frequency

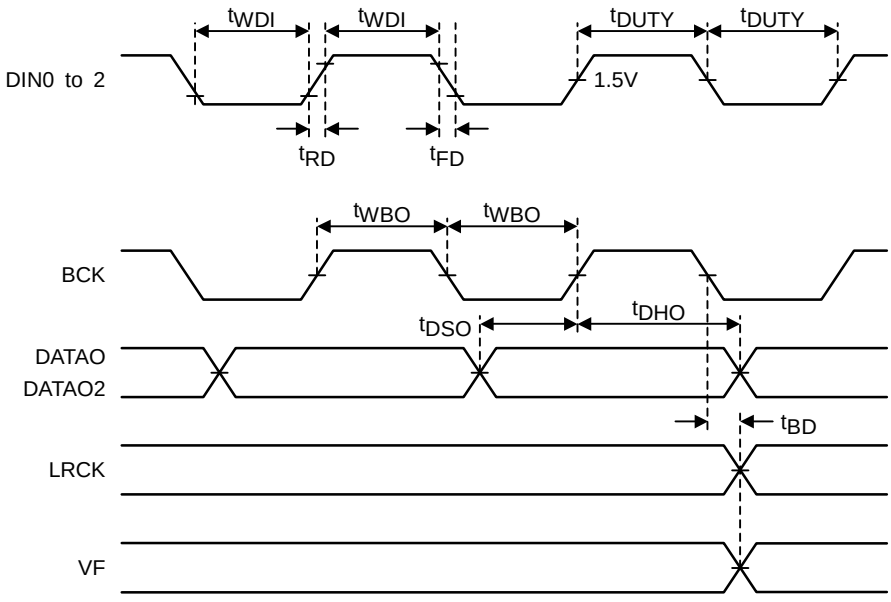


Figure 6.1 AC Characteristics

6.5 Microcontroller Interface AC Characteristics

Table 6.5 I/F AC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CSFLAG Pulse Width, High	$t_{CS}uw$	6-5-1	1			ms
BPSYNC Pulse Width, Low	$t_{BP}dw$	6-5-2		41.7		µs
CL Pulse Width, Low	$t_{CL}dw$		100			ns
CL Pulse Width, High	$t_{CL}uw$		100			ns
CL-CE Setup Time	$t_{CL}setup$		50			ns
CL-CE Hold Time	$t_{CE}hold$		50			ns
CL-DI Setup Time	$t_{DI}setup$		50			ns
CL-DE Hold Time	$t_{DI}hold$		50			ns
CL-CE Setup Time	$t_{CL}setup$		50			ns
CL-CE Hold Time	$t_{CL}hold$		50			ns
CL-DO Delay Time	t_{CL} to DO	6-5-3			*	ns
CE-DO Delay Time	t_{CE} to DO				*	ns
DI Delay Time	$t_{DI}dly$			0		s

6-5-1: fs = 32kHz to 192kHz

6-5-2: fs = 48kHz

6-5-3: With a capacitance of 10pF and a 10kΩ pull-up resistor connected, the delay time is up to 150ns max. for the rising edge and up to 50ns max. for the falling edge.

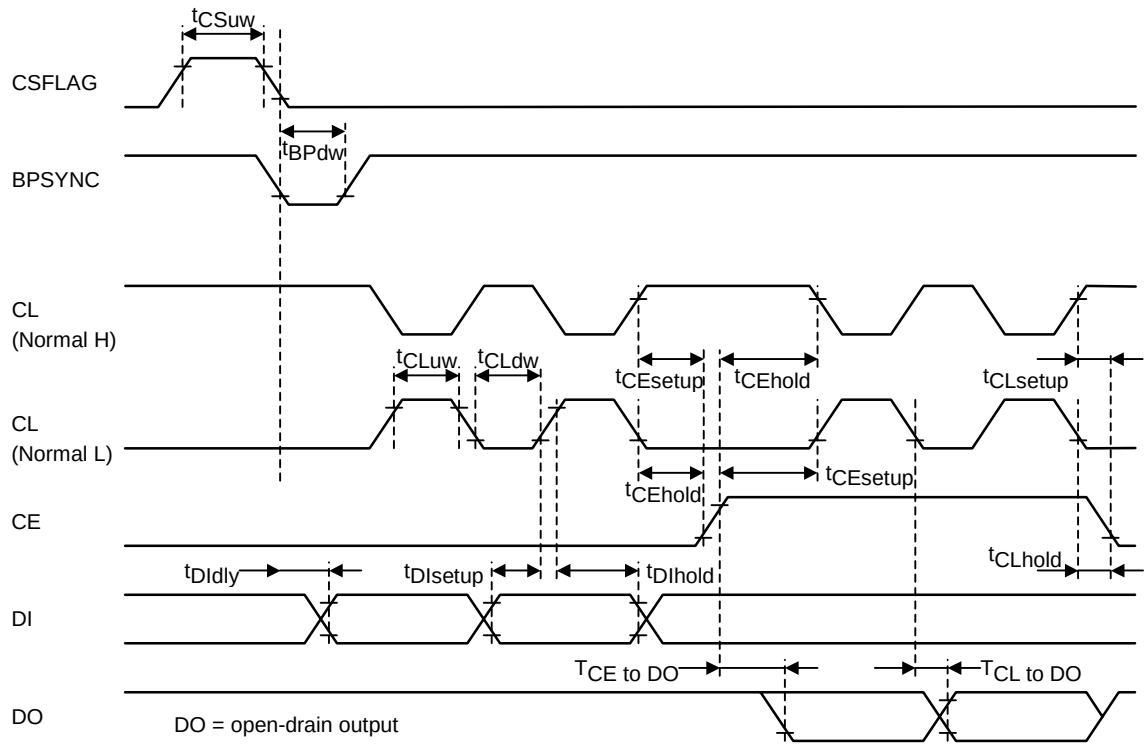


Figure 6.2 Microcontroller Interface AC Characteristics

7. System Reset (XMODE)

- The system operates normally when XMODE pin is set to high level after 3.0V or higher supply voltage is applied.
- After power-on, the system is reset by setting XMODE to low again.
- Make sure to reset the system after turning on the power.

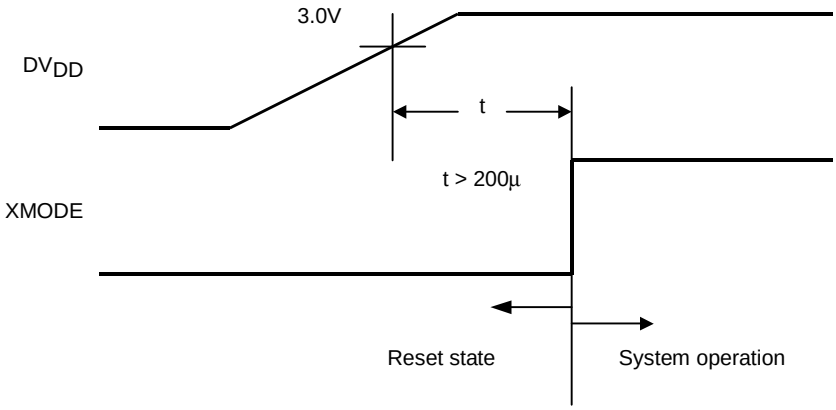
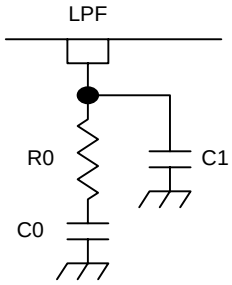


Figure 7.1 Reset Timing Chart

8. PLL (LPF)

- It has a build-in VCO (Voltage Controlled Oscillator) and synchronizes with sampling frequencies of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz.
- The lock judgment of PLL is performed by detection of preamble B, M and W.
- The lock frequency of PLL is selected by CKSEL0 and CKSEL1. However, only 256fs is selectable on the system which input sampling frequency is over 96kHz. The proper PLL function to input over 96kHz will not be ensured when other frequency value is selected.
- LPF is pin for loop filter of PLL and connects resistor and capacitor as shown below.

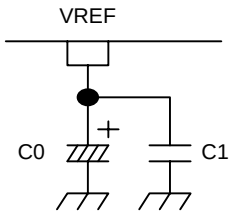


R0	C0	C1
220Ω	0.1µF	0.068µF

Figure 8.1 Configuration of a Loop filter

9. Built-in Regulator (VREF)

- It has built-in regulator that can step down 3.3V to 1.8V in order to supply voltage into logic part.
- VREF is pin for voltage smoothing which can output regulator and connects the capacity as shown below.



C0	C1
10μF	0.1μF

Figure 9.1 Composition of the regulator output

10. Analog Source Mode

- The analog source mode is entered under the following conditions.
  - –When the analog source mode is selected with the SMOD command.
  - –When the input pin selected for data demodulation is no signal.
- In the analog source mode, the oscillation amplifier clock or the externally supplied clock are used.
- Each signal in the analog source mode is described below.
  - –VCO holds the status of free-run oscillation when SMOD is set and also when no signal is input.
  - –ERROR pin outputs high and DATAO pin outputs SDIN input data.
  - –XSTATE pin outputs high after about 512*LRCK(fs) (LRCK=48kHz or 96kHz) counts after XSTATE pin outputs low.
  - –The clock set with XADC command is output from XMCK.
  - –The output of BCK and LRCK are as follows.

Table 10.1 BCK and LRCK Outputs with Analog Source

XIN pin	BCK pin	LRCK pin
12.288MHz	3.072MHz	48kHz
24.576MHz	6.144MHz	96kHz
12MHz to 25MHz	XIN/4	XIN/256

11. Setting of MODE0 and MODE1

- Selected operation mode with MODE0 and MODE1 terminals.

Table 11.1 Setting operating mode

Mode No.	MODE1 pin	MODE0 pin	Function
1	0	0	Normal mode
2	0	1	Fs free mode A
3	1	0	Test mode
4	1	1	Fs free mode B

(a) Mode1: Normal mode
- –Input data fs of 32kHz to 192kHz is received only when CKOUT=256fs.
- –The proper reception of data over 96kHz will not be ensured when other than 256fs is used for CKOUT output setting.

(b) Mode2: Input fs free mode A (Terminal setting priority)
- –Restriction of input fs is canceled.
- –12.288MHz or 24.576MHz clock is supplied to XIN.
- –The receiving range of input data is based on a setup of CKOUT output.
- –Fs calculation of input data is performed in the possible range. (fs ± 3 to 4%)

(c) Mode3: Test mode
- –Do not set this mode for the test.

(d) Mode4: Input fs free mode B (Terminal setting priority)
- –Restriction of input fs is canceled.
- –12MHz to 25MHz arbitrary clock is supplied to XIN.
- –The reception range of input data is based on a setup of the CKOUT output.
- –Input fs is not calculated. In this case, all F0, F1 and F2 output low.
- –Output data delay after recovery processing cannot be set. However, the delay setting of the SDIN input data is possible.

- In the normal mode, when fs of input data is out of the reception setting range or the fs calculation range (≠target fs frequency ± 3 to 4%), ERROR is output high even if PLL is locked.
- In the input fs free mode, the reception range is set up without any restriction and fs calculation result is set so that it is not reflected in ERROR output. ERROR output will be set to low if PLL is locked.

12. Function

12.1 Input Data (DIN0, DIN1, DIN2, DOUT, DISEL)

- DIN0, DIN1 and DIN2 are input pins that support TTL level inputs (5V tolerance).
- DIN0, DIN1 and DIN2 are grounded with the pull-down resistor when they are not selected.
- The input pin is selected with DISEL and the DIS[1:0] commands. (Command setting priority)
- With DISEL, it is selected from DIN0 or DIN1. With DIS[1:0], it is selected from DIN0, DIN1 or DIN2.
- DOUT performs through output the bi-phase data input to the selected data input pin. When, however, DOUT is not used, low fixed output setting is recommended in order to reduce the clock jitter.

Table 12.1 Data Input Pin Selection

DISEL pin	Input pin to be demodulated
0	DIN0
1	DIN1

12.2 Input Data Reception Range

- The input data reception range can be extended and restricted with FSL0 and FSL1 commands, and CKSEL0 and CKSEL1 terminals. Also, the restriction can be canceled with MODE0 and MODE1.
- In the initial status at power ON, although sampling frequency of input data can be received up to 192kHz, sampling frequency of input data to be received can be restricted up to 48kHz or 96kHz. In this case, input data over this range results in an error and output data is muted.
- For information about these settings, see section “14. Microcontroller Interface”.

12.3 VCO and Oscillation Amplifier Clock (XIN, XOUT, XMCK, XSEL, XSTATE)

- The oscillation amplifier circuit is configured with XIN and XOUT. XIN accepts the input of the external clock.
- The clock generated with XIN and XOUT is used for the following purposes.
  - –Clock for detection of data input
  - –Clock for A/D converter in analog source mode
  - –Clock for calculation of input sampling frequency
  - –Clock for PLL error lock countermeasure

- The frequency required for XIN and XOUT is selected with XSEL. Normally the crystal resonator clock set here or external clock must be input. Moreover, make sure to connect a transducer to XIN and XOUT or supply a clock to XIN. (Normal input)
- In the case of setting the input fs free mode B, 12MHz to 25MHz arbitrary clock must be supplied to between XIN and XOUT. This case, XSEL must select the closer frequency of transducer to be connected.

Table 12.2 XIN Supply Frequency Selection

XSEL pin	Frequency
0	24.576MHz
1	12.288MHz

- XIN and XOUT are valid when PLL is unlocked, and oscillation amplifier clock or the divided clock of external input clock is output from the clock output pins.
- When the PLL is locked the oscillation amplifier is stopped so that it does not influence the VCO clock. The clock supplied to XIN is blocked in I/O block and the inside operates only with VCO clock. However, XIN and XOUT can also always be operated with the XCNT command. In this case, the XIN and XOUT clock is at risk of influencing the VCO clock.
- XMCK outputs the clock generated with oscillation amplifier of XIN and XOUT as a clock for A/D converter. The XMCK clock frequency is selected with the XADC command.
- When oscillation amplifier is set up for continues operation, XMCK can be stopped only during PLL is locked. It is set by the XCKS command. XCKS is for reducing clock interference to input and output buffer during the continuous operation of oscillation amplifier.
- Table 12.3 shows the status of the XIN, XOUT and XMCK pins when PLL is locked and unlocked.

Table 12.3 Status of Oscillation Amplifier Circuit when PLL Locked or Unlocked (XCNT = 0)

Pin name	Specified time after locked *	Unlocked status
XIN	Input disabled	Input enabled
XOUT	H	XIN inverted clock output
XMCK	L	1/1 or 1/2 XIN clock output

* Note: The specified time is the time from when PLL is locked until 8 preamble B is counted to eight. During this time, the input sampling frequency is calculated.

- XSTATE outputs low from the time PLL is locked until the ERROR goes low (lock-in stage), or from the time PLL is unlocked until the output clock is stabilized (unlock stage).
- L pulse width of XSTATE in lock-in process is a period from the PLL lock to the cancel of the ERROR. It is decided from the count value of Preamble B and sampling frequency of input data. For the ERROR output waiting time, see explanation of EWT[1:0] commands.
- L pulse width of XSTATE in unlock process is 512 count periods of fs clock which uses oscillation amplifier as a source clock. For example, when an oscillation amplifier clock is 12.288MHz, fs clock output from LRCK is set to 48kHz. In other words, about 10ms that counted this fs 512 times is L pulse width period. In addition, the time until the start of oscillator is required when the crystal oscillator is connected to oscillation amplifier. In this case, L pulse width is added during start-up time.
- For the XMCK output timing, see Figure 12.1.
- XSTATE outputs the low pulse, when change arises on the clocks. (when XSTP=0 setup)
- Also, the output polarity of XSATAE can be changed by the XSTP command.
- All functions of a VCO oscillation clock and an oscillation amplifier can be stopped by the STOP command. At this time, all output clock terminals serve as DC output.

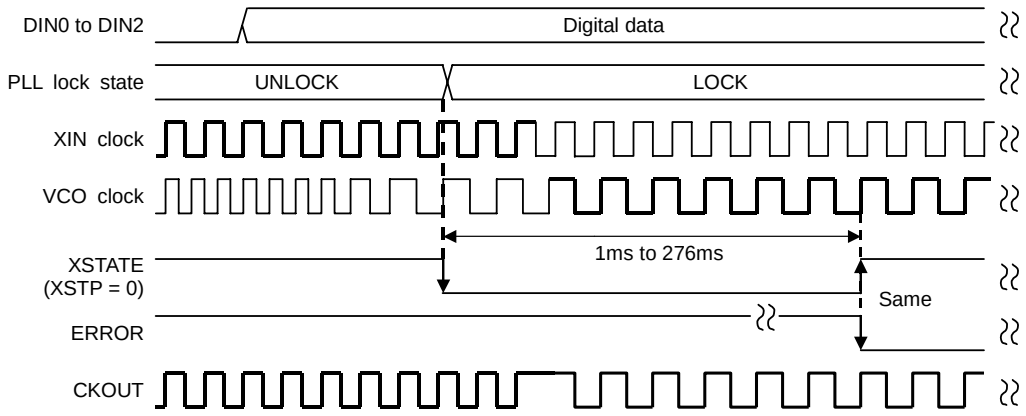
12.4 Output Clock (CKOUT, BCK, LRCK)

- The CKOUT output clock is selected by setting CKSEL0 and CKSEL1 terminals.

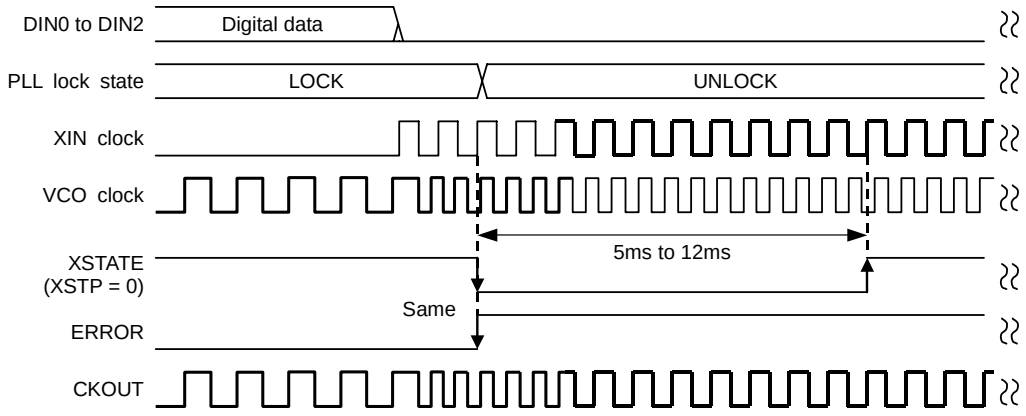
Table 12.4 CKOUT Output Clock Selection

CKSEL1 pin	CKSEL0 pin	CKOUT pin
0	0	256fs output
0	1	384fs output
1	0	512fs output
1	1	512fs/2 output

- 256fs must be chosen when receiving data over 96kHz as above table. There is no restriction of selection for data reception under 96kHz.
- 512fs/2 set PLL band as 512fs, and CKOUT clock outputs one half (256fs output).
- 64fs clock (64fs only) is outputted from BCK, and the fs clock is outputted from LRCK.
- When PLL is unlocked, the XIN and XOUT oscillation amplifier clock or the external input clock is output from CKOUT, and the divided clock of this clock is outputted from BCK and LRCK.
- Output of 1/2 CKOUT clock by CKDV command is possible.
- Reverse of the polarity of CKOUT clock by CKPO command is also possible.
- In the PLL lock and unlock phases, the CKOUT (BCK and LRCK likewise) clock switch timing is as follows.



(a): During lock-in phase



(b): During unlock phase

Figure 12.1 Output Clock Switch Timing

12.5 Serial Audio Data Input and Output

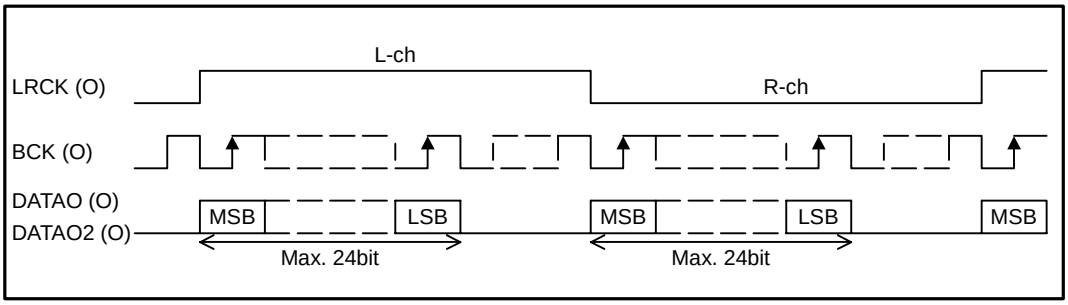
12.5.1 Output Data Format (DATAO, DATAO2, DOSEL0, DOSEL1)

- DATAO and DATO2 output the digital data after demodulation. DATAO2 should be switched by the VSEL command since DATAO2 is sharing pin with validity flag output.
- The output data format is set with DOSEL0 and DOSEL1 terminals, or the DOSW command. The output data is 24bit I^2S output when setup is DOSW=1. The setup of DOSW is given priority over DOSEL0 and DOSEL1.

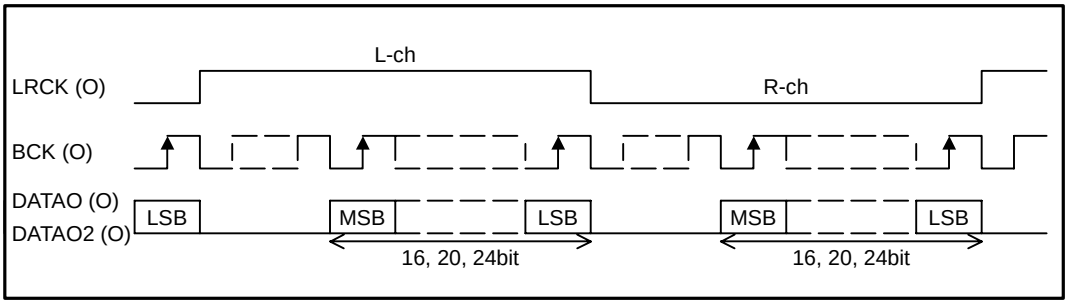
Table 12.5 Data output format Selection (DOSW = 0)

DOSEL1 pin	DOSEL0 pin	DATAO and DATAO2 pin
0	0	(0) 24bit MSB-first left justified
0	1	(1) 24bit MSB-first right justified
1	0	(2) 20bit MSB-first right justified
1	1	(3) 16bit MSB-first right justified

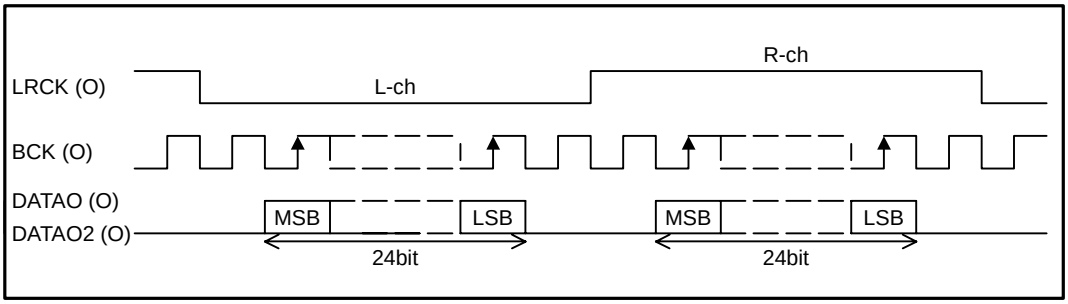
- Data is output in synchronization with the falling edge of BCK from the edge of LRCK immediately after the ERROR flag goes low. However, this is the case that the delay setup is disabled (initial setting). When the delay setup is effective, DATAO is output after the delay time set. The delay setting is not applicable to DATA02. For information about these settings, see section “13. Output Data Delay Function”.



(0): Setting with DOSEL0, DOSEL1



(1) (2) (3): Setting with DOSEL0, DOSEL1

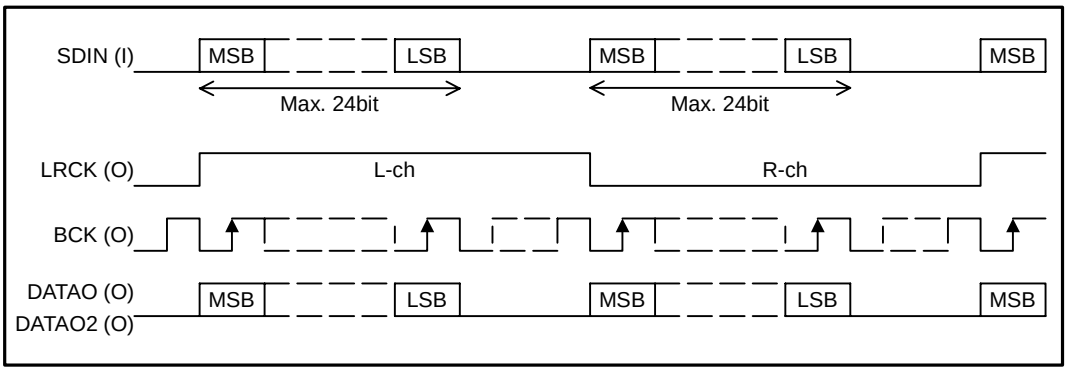


(4): Setting with the DOSW command

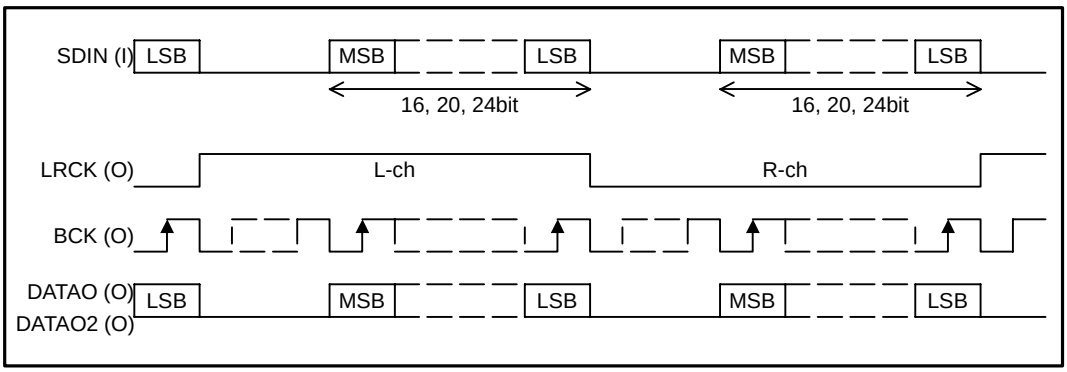
Figure 12.2 Data Output Timing Charts

12.5.2 Serial Audio Data Input Format (SDIN, DOSEL0, DOSEL1)

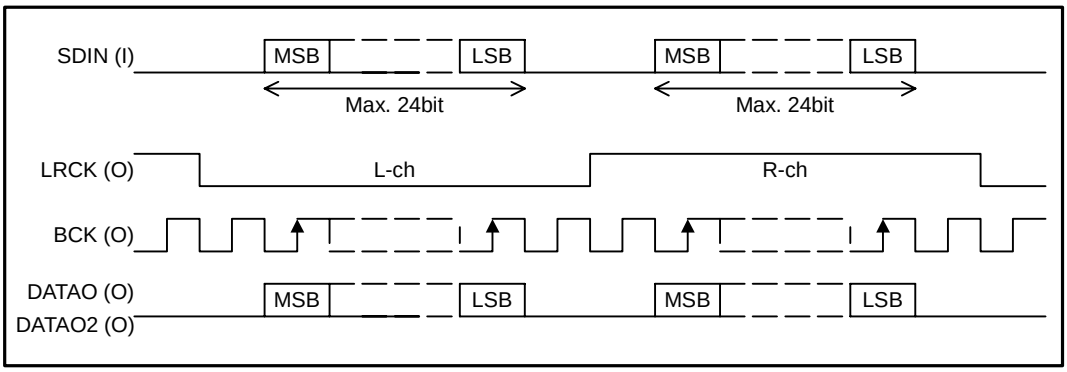
- The LC890561W has SDIN which is serial digital audio data input pin and makes input of 24bit data possible.
- The format of the serial audio data input into SDIN should be adjusted to the same format as the demodulated data output. Therefore, the input format of SDIN is the same as the setup of DOSEL0 and DOSEL1 terminals, and the DOSW command.
- The SDIN data to be input should be in synchronization with BCK and LRCK clock.
- SDIN input data is output to DATAO and DATAO2 behind two frames since it is latched to shift register.
- When not using the SDIN terminal, it is connected to GND.



(0): Setting with DOSEL0, DOSEL1



(1) (2) (3): Setting with DOSEL0, DOSEL1

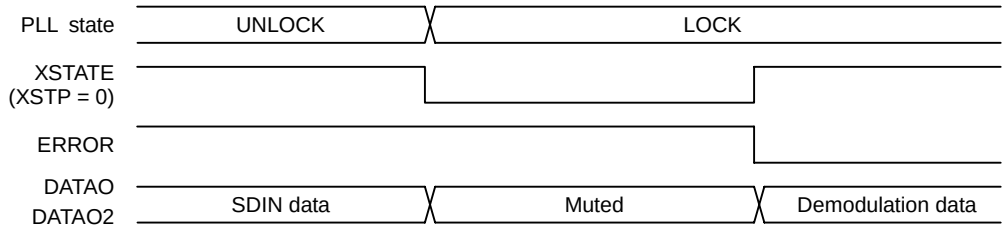


(4): Setting with the DOSW command

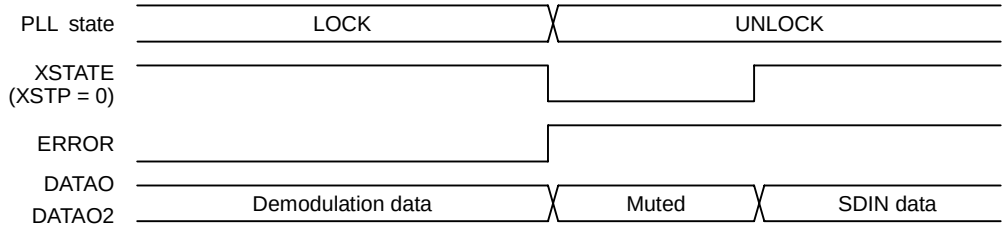
Figure 12.3 Data Input Timing Charts

12.5.3 Output Data Changing (DATAO, DATAO2, SDIN)

- DATAO and DATAO2 output demodulation data when PLL is locked, and output SDIN input data when PLL is unlocked. This switching is automatically performed according to the state of PLL lock or unlock.
- During the selection of SDIN input data, it must be switched to the clock source that is in synchronized with SDIN data.
- SDIIN input data is output to DATAO and DATAO2 with the SMOD command setting regardless of the lock / unlock state of PLL. In the case of switching PLL in the lock state, clock source is also switched to XIN. Furthermore, an ERROR flag also outputs high and a XSTATE signal also changes.
- DATAO and DATAO2 output can be muted forcibly with setting of the DOM[1:0] commands.



(a): Lock-in stage



(b): Unlock stage

Figure 12.4 DATAO and DATAO2 Outputs Data Chang Timing Charts

12.5.4 Data System Diagram (DIN0, DIN1, DIN2, SDIN, DOUT, DATAO, DATAO2)

- Data system diagram is shown below.
- The delay setup for DATAO is possible. However, the delay setup for DATAO2 is impossible because DATAO2 does not go through a memory.
- DIN0 to DIN2 and SDIN input data are output to DATAO and DATAO2 behind two frames. Delay setup of output data is processed with the DATAO output with 2-frame delay against the input data as delay for 0ms.
- Since DATAO2 shares the pin with the validity flag output, it should be changed by the VSEL command. The initial value of VSEL is the validity flag output.

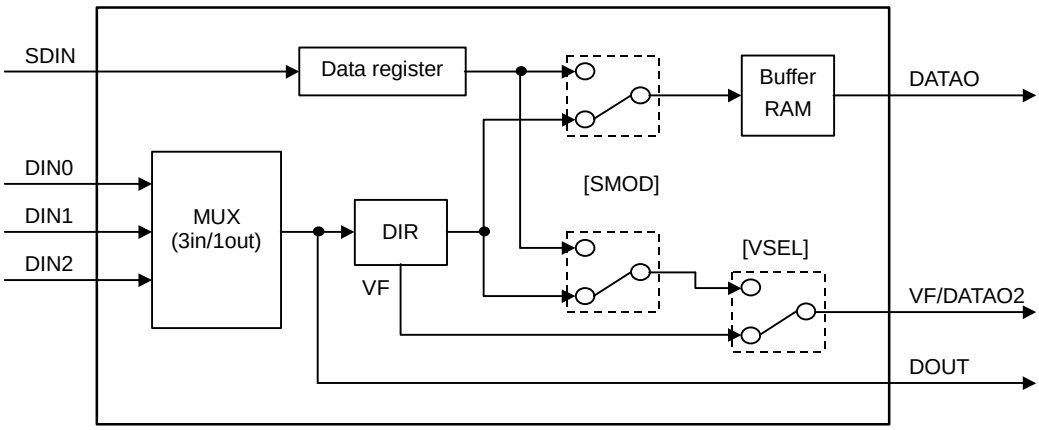


Figure 12.5 Data System Diagram

12.6 Lock Error and Data Error Signal (ERROR)

- ERROR outputs an error flag, when PLL lock error arises or when a data error arises.
- The output form of an error signal is chosen by the ERF[1:0] commands.

12.6.1 PLL Lock Error

- PLL is unlocked to the data that has lost the pattern of input bi-phase modulation or which preamble B, M and W cannot be detected.
- ERROR outputs high upon occurrence of PLL lock error and outputs low after holding high for 3msec to 300msec after data demodulation returns to normal. See Figure 12.8.
- After PLL is locked, the holding period for high output of ERROR is decided by counting preamble B. Also, this period is changeable with EWT [1:0] commands.

12.6.2 Input Data Parity Error

- Parity bit errors (odd number) of input data and input parity errors are detected.
- If nine or more input parity errors occur in succession, ERROR outputs high, and then low after detecting the PLL lock status and holding high for 3 to 300msecs.
- If eight or fewer input parity errors occur in succession, the output format of error flag can be selected with ERF[1:0] commands.

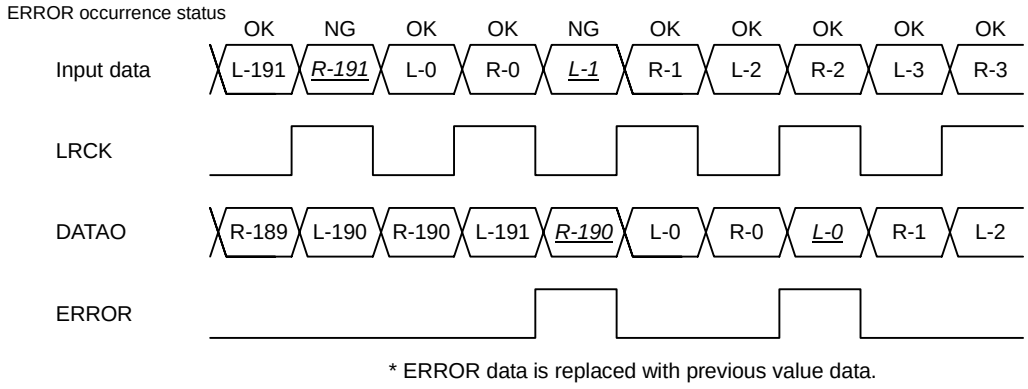


Figure 12.6 Parity Error Flag Output Timing Chart (ERF[1:0] = 01, non delay setting)

12.6.3 Others Error

- Even when ERROR goes low, channel status bits 24 to 27 (sampling frequency) are continuously sampled and the previous block of data and the current data are compared. If they are different, ERROR goes high immediately and the same processing as for the PLL lock error is performed. However, even if input data changes after ERROR goes low and the channel status information does not change, or if the input data changes within the PLL capture range, ERROR does not go high.

12.7 Output Data Error Processing

12.7.1 Upon Error Occurrence (Lock Error and Parity Error)

- The data processing upon error occurrence is described below. If input parity errors occur eight times or more in succession, transfer data is replaced by the data held in L-ch and R-ch of the previous frame in the case of PCM audio data. However, if the data is Non-PCM burst data, error data is output without change as the transfer data. Non-PCM burst data is detected based on data detected prior to occurrence of an input parity error when channel status bit 1 goes high or when burst preamble Pa and Pb are detected.
- For the channel status, the data of the previous block is held in bit when a parity error occurs, regardless of the data type.
- Output data is muted upon occurrence of a PLL lock error or nine continuous parity errors.

Table 12.6 Data Processing Upon Error Occurrence

Data	PLL lock error	Input parity error (a)	Input parity error (b)	Input parity error (c)
DATAO and DATAO2	L	L	Previous value data	Output
F0, F1, F2 outputs	L	Output	Output	Output
Channel status	L	Previous value data	Previous value data	Previous value data
Validity flag	L	Output	Output	Output

* Input parity error (a): If occurred 9 times or more in succession
* Input parity error (b): If occurred 8 times or fewer, in the case of PCM audio data
* Input parity error (c): If occurred 8 times or fewer, in the case of Non-PCM burst data

- Figure 12.7 shows an example of data processing upon occurrence of a parity error

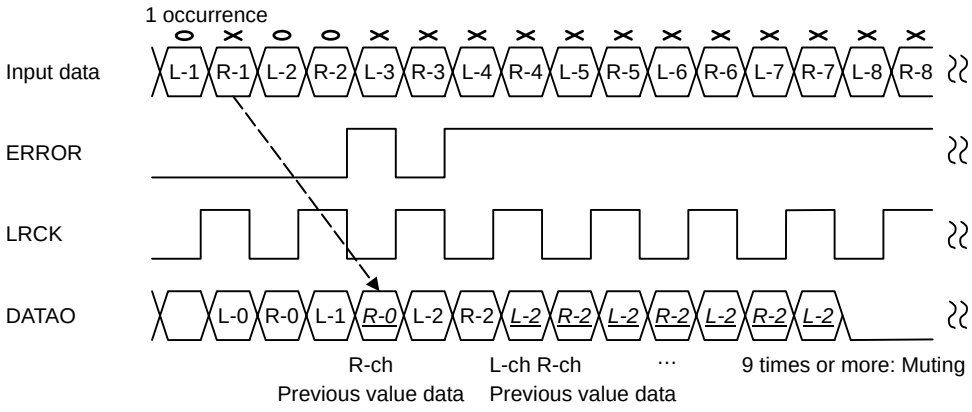


Figure 12.7 Example of Data Processing Upon Parity Error Occurrence (non delay setting)

12.7.2 Upon Error Recovery (Lock)

- When preamble B, M and W are detected, PLL is locked and data demodulation begins.
- DATAO and DATAO2 output data are output from the L/R clock edge after ERROR goes low.
- The start timing of the ERROR flag, and the DATAO and DATAO2 output data are shown in Figure 12.8.
- The above operation is in case the delay setup is not done. For information on operations with delay settings, see section “13. Output Data Delay Function”.

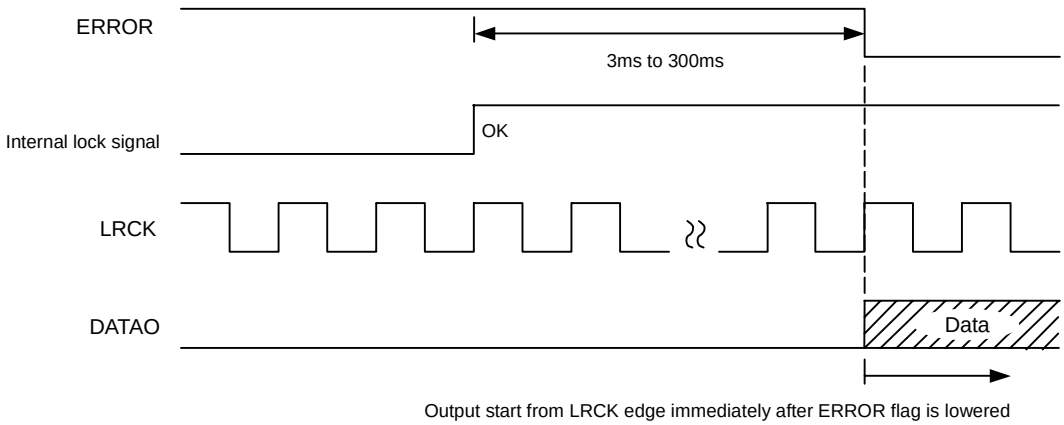


Figure 12.8 Data Processing at Data Demodulation Start (non delay setting)

12.8 Channel Status Emphasis Information Output (EMPHA)

- EMPHA outputs channel status information that indicates the presence or absence of 50/15μsec pre-emphasis.
- EMPHA is output immediately after the detection of ERROR even during high output.

Table 12.7 EMPHA Output

EMPHA pin	Output condition
L	No pre-emphasis
H	50/15μs pre-emphasis

12.9 Channel Status Bit 1 Output (AUDIO)

- AUDIO outputs bit 1 of the channel status that indicates whether transfer data has PCM audio data or data other than audio.
- AUDIO is output immediately after the detection of ERROR even during high output.

Table 12.8 AUDIO Output

AUDIO pin	Output condition
L	PCM audio data (CS bit 1 = L)
H	Data other than audio (CS bit 1 = H)

12.10 First 48 Channel Status Bits Update Flag Output (CSFLAG)

- CSFLAG compares the first 48 bits of channel status data of the previous block with those of the current block and outputs low in case they are the same, and high in case they are different, for 1 block of 192 frames. Therefore the channel status data output after the falling edge of the CSFLAG is the latest data.
- CSFLAG outputs high regardless of the comparison result until ERROR outputs low. After ERROR output becomes low, CSFLAG outputs low after the first 48bit data of the previous data and the current data have been confirmed to be identical.

Table 12.9 CSFLAG Output

CSFLAG pin	Output condition
L	Previous data current data are identical
H	Previous data differs from current data

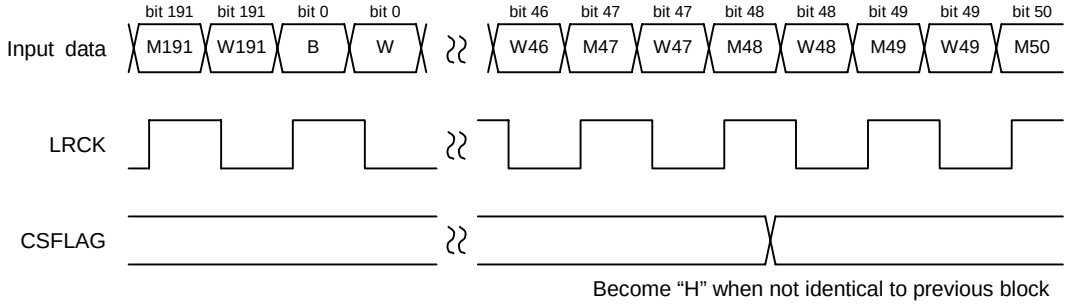


Figure 12.9 Timing Chart for Channel Status Update Flag Output

12.11 Non-PCM Burst Preamble Detection Signal Output (BPSYNC)

- BPSYNC outputs low while Non-PCM burst preamble Pa, Pb, Pc and Pd output, when Pa and Pb are detected following continuous all zero data of two frame. However, when output data delay is set up, low period of a BPSYNC signal and the output period of the Non-PCM burst preamble Pa, Pb, Pc, and Pd do not match. In this case, BPSYNC is output ahead of Pa, Pb, Pc, and Pd data.
- Pa, Pb, Pc and Pd are detected from the receive data even when an input parity error occurs.

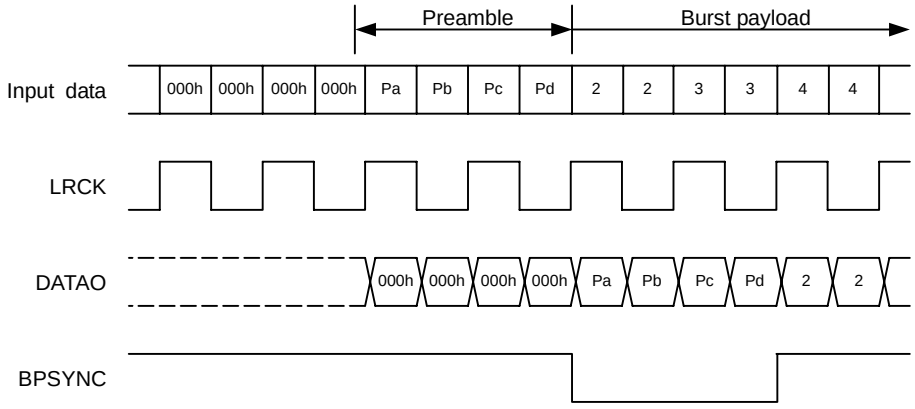


Figure 12.10 Timing Chart for Pa, Pb, Pc and Pd Detection Signal Output

12.12 Input Sampling Frequency Calculation Signal Output (F0, F1, F2)

- By inputting 12.288MHz or 24.576MHz oscillation amplifier clock or external input clock, input sampling frequencies of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz are calculated and the result is output from F0, F1 and F2.
- This processing is completed until preamble B is counted to eight after PLL is locked. Therefore, it is fixed by the time the ERROR flag is lowered, and it will not change until PLL is unlocked.
- If the frequency other than 12.288MHz or 24.576MHz is set, the F0, F1 and F2 outputs are not guaranteed.
- This information can also be read with the microcontroller interface.
- The fs of input data except input fs free mode is within the calculation range.

Table 12.10 Fs Calculation Results when 12.288MHz or 24.576MHz is Set (Ta = 25°C, V_{DD} = 3.3V)

F2 pin	F1 pin	F0 pin	Target fs frequency	Calculation range
L	L	L	Out of Range	-
L	L	H	32kHz	30.8kHz to 33.3kHz
L	H	L	44.1kHz	42.4kHz to 45.8kHz
L	H	H	48kHz	46.2kHz to 49.9kHz
H	L	L	88.2kHz	85.4kHz to 91.7kHz
H	L	H	96kHz	93.1kHz to 99.0kHz
H	H	L	176.4kHz	170.7kHz to 180.7kHz
H	H	H	192kHz	186.2kHz to 198.1kHz

Note: *Output when PLL is unlocked or when a sampling frequency cannot be calculated.

12.13 Validity Flag Output (VF)

- VF/DATAO2 outputs the validity flag.
- VF/DATAO2 shares the pin with the demodulated audio data output pin (delay setup is impossible). Setting as VSEL=0 (default) makes output validity flag possible.

Table 12.11 VF Output

VF pin	Output condition
L	No (no burst data)
H	Error (possibility of burst data)

13. Output Data Delay Function (DATAO, FSB0, FSB1, DLMP)

- It has built-in RAM that is utilized for the lip synchronization function that delays the sound data to the movie.
- Output data can be delayed for 256ms (fs = 48kHz) at the maximum.
- Delay processing of output data supports 24bit width data.
- The delayed data is outputted from DATAO terminal, not from DATAO2 terminal.
- Delay processing of output data is possible for demodulated data during PLL lock and serial audio data entered from the SDIN terminal.
- V, U and C bits transferred with S/PDIF input data are not delayed.
- The signal that can be used for delay setting control of output data is outputted from FSB0, FSB1 and DLMP terminals.

13.1 How to Set

13.1.1 Output Data Delay Setup after Recovery Processing (DTMA[4:0], DTMB[3:0], DTMC[2:0])

- Output data delay after demodulation is set up by DTMA[4:0], DTMB[3:0] and DTMC[2:0] commands.
- It is possible to set different delay time for every input sampling frequency band by 10ms step unit.
- The delay time of 32kHz, 44.1kHz and 48kHz input data are set up with DTMA[4:0] commands.
- The delay time of 88.2kHz and 96kHz input data are set up with DTMB[3:0] commands.
- The delay time of 176.4kHz and 192kHz input data are set up with DTMC[2:0] commands.

Table 13.1 Delay Time Setup of Output Data for the Data after Recovery Processing

Delay time (sec)	Data fs after recovery processing (Hz) and setting commands		
	32k, 44.1k, 48k (DTMA[4:0])	88.2k, 96k (DTMB[3:0])	176.4k, 192k (DTMC[2:0])
0	○	○	○
10m	○	○	○
20m	○	○	○
30m	○	○	○
40m	○	○	○
50m	○	○	○
60m	○	○	○
70m	○	○	◆
80m	○	○	
90m	○	○	
100m	○	○	
110m	○	○	
120m	○	○	
130m	○	◆	
140m	○	See section “14.5.2 Details of Write Commands”	
150m	○		
160m	○		
170m	○		
180m	○		
190m	○		
200m	○		
210m	○		
220m	○		
230m	○		
240m	○		
250m	○		
Max.	◆		

(“○” can be set, “◆” maximum delay time is set)

- DTMA[4:0], DTMB[3:0] and DTMC[2:0] commands have the same address. Therefore, they can be set up together.
- Each command setting value is assigned to output data according to the sampling frequency of input data.
- Delay time is set up with the number of frames which is obtained by multiplying the sampling frequency calculation value of input data by the setting value of DTMA[4:0], DTMB[3:0] and DTMC[2:0] commands.
- Delay time can be freely switched within the range where the setup is possible.
- This setup is continued until it is canceled (delayed 0ms, non delay).
- This function is not performed when mode 4, “Input fs free mode B”, by MODE0 and MODE1 is set. Even the above setting is set, it will be invalid.

13.1.2 Output Data Delay Setup of SDIN Input Data (DTMX[4:0], DTMY[3:0])

- Output data delay of SDIN input data is set up by DTMX[4:0] and DTMY[3:0] commands.
- SDIN input data needs to synchronize with BCK and LRCK output clocks. Therefore, the sampling frequency of SDIN data is decided by setup of XSEL (XIN input clock frequency). In other word, input data is either 48kHz or 96kHz, and uses a setup of either DTMX[4:0] or DTMY[3:0] commands.
- Delay time can be freely switched within the range where the setup is possible.
- This setup is continued until it is canceled (delayed 0ms, non delay).
- The following delay time is performed when mode 4, “Input fs free mode B”, by MODE0 and MODE1 is set.

  Delay time = {(256fs × delay time of DTMX [4:0] or DTMY [3:0]) / XIN input clock}

Table 13.2 Delay Time Setup of Output Data for the SDIN Input Data

Delay time (sec)	SDIN input data fs (Hz) and setting commands	
	48k (DTMX[4:0])	96k (DTMY[3:0])
0	○	○
10m	○	○
20m	○	○
30m	○	○
40m	○	○
50m	○	○
60m	○	○
70m	○	○
80m	○	○
90m	○	○
100m	○	○
110m	○	○
120m	○	○
130m	○	◆
140m	○	See section “14.5.2 Details of Write Commands”
150m	○	
160m	○	
170m	○	
180m	○	
190m	○	
200m	○	
210m	○	
220m	○	
230m	○	
240m	○	
250m	○	
Max.	◆	

(“○” can be set, “◆” maximum delay time is set)

13.2 DATAO Output Data Processing

- When any of the DTMA [4:0], DTMB [3:0], DTMC [2:0], DTMX [4:0], DTMY [3:0] is set up (setup of those other than an initial state), delay processing of output data is performed.
- Delay processing of the target data and mute processing of output data are explained below.

13.2.1 Output Data Delay Setup after Recovery Processing (Setting at the state of ERROR = H)

- When the DTMA[4:0], DTMB[3:0] and DTMC[2:0] commands are set up or changed during high output of ERROR flag, data is written into memory in synchronization with the rising edge of XSTATE after PLL is locked.
- Readout of the data written in the memory is started after the set delay time (frame).
- The data read out is constantly output form DATAO with the delay of the setup time.
- DATAO will be muted until the set delay time is over, because sufficient data is not written into memory immediately after the low output of ERROR flag.

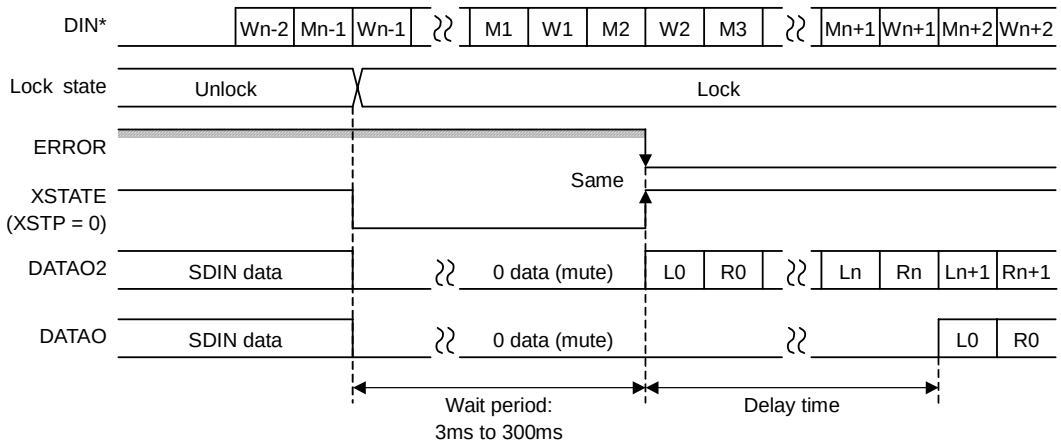


Figure 13.1 Timing Chart for Output Data after Setup or Change of the Delay Time During PLL Lock-in

- When the DTMA[4:0], DTMB[3:0] and DTMC[2:0] commands are canceled during high output of ERROR flag, data is output from DATAO synchronizing with the rising edge of XSTATE after PLL is locked. This is normal operation which does not perform a delay processing setup.

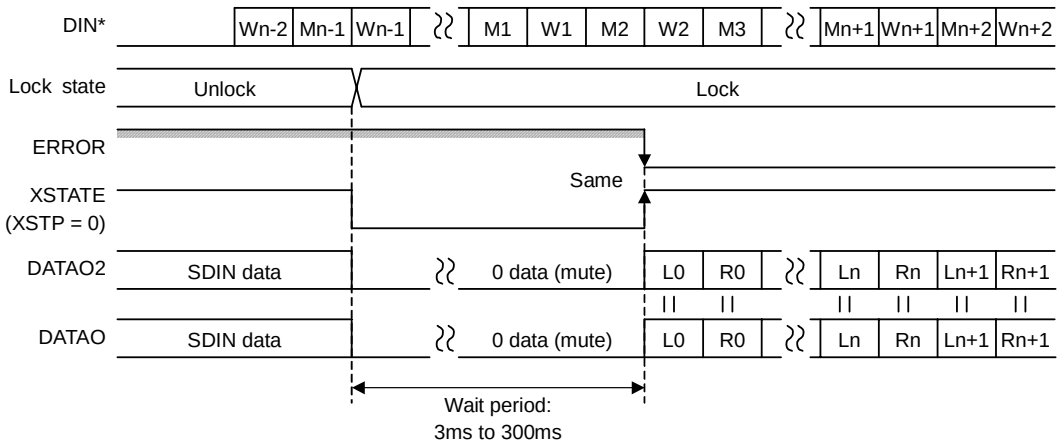


Figure 13.2 Timing Chart for Output Data after Cancel of the Delay Time Setting During PLL Lock-in

13.2.2 Output Data Delay Setup after Recovery Processing (Setting at the state of ERROR = L)

- When the DTMA[4:0], DTMB[3:0] and DTMC[2:0] commands are set up or changed during L output of ERROR flag, delay processing is performed according to the setup of those commands.
- After power up, when the command is set up for the first time, a memory domain is assigned according to the set delay, and data is written in a memory.
- A memory domain is reset when the delay time is changed in the state where the command is already set up. And a memory domain is assigned according to the newly set-up delay time, and the data writing to a memory is started.
- Readout of the data written in the memory is started after the set delay time (frame).
- DATAO output is muted immediately after the command setup until the end of the set delay time.

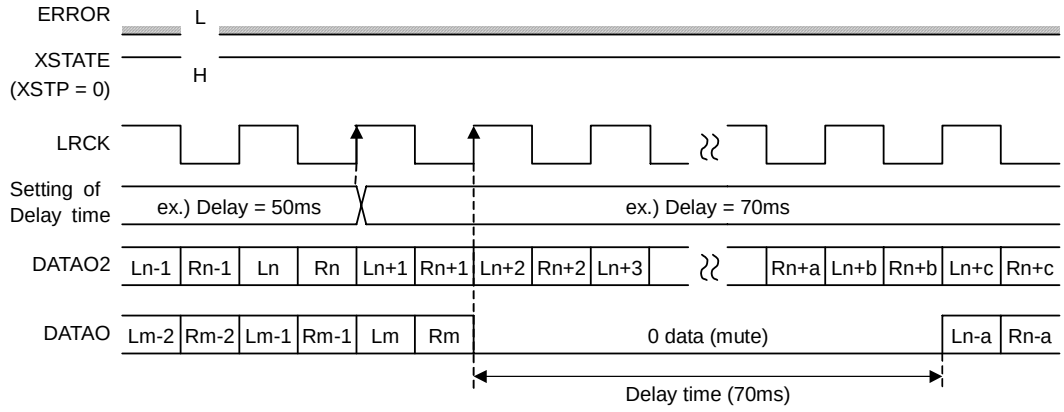


Figure 13.3 Timing Chart for Output Data after Setup or Change of the Delay Time During PLL Lock

- When delay time is canceled in the state where the command is already set up, the writing to the memory is stopped. However, DATAO is output after muting the input data for 512-frame period. DATAO is not output immediately after cancel of command setting. The 512-frame period is dependent on the sampling frequency of input data.

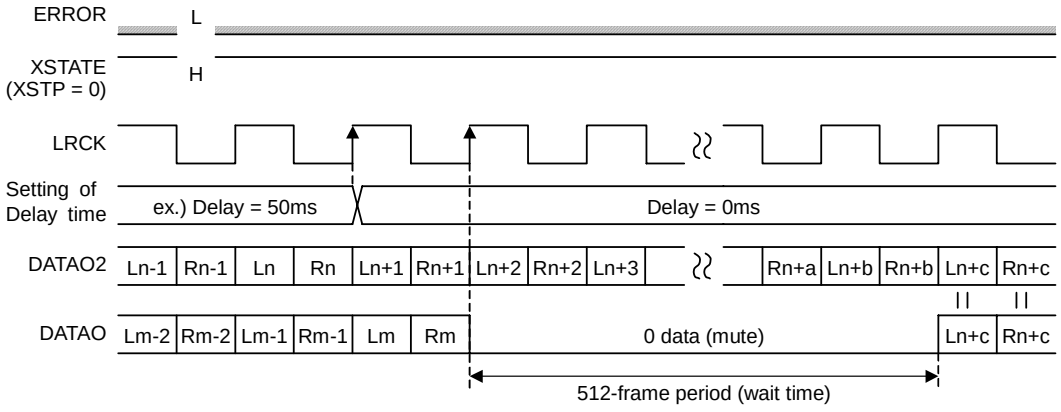


Figure 13.4 Timing Chart for Output Data after Cancel of the Delay Time Setting During PLL Locked

- When the command is changed before the completion of command setting, the delay process is initialized every command setting. For DATAO output, mute output is continued until the setting is fixed.

13.2.3 Output Data Delay Setup of SDIN Input Data (Setting at the state of ERROR = L)

- When the DTMX[4:0] or DTMY[3:0] commands are set up during low output of ERROR flag, data is written to a memory in synchronization with the rising edge of XSTATE after PLL unlock.
- Readout of the data written in the memory is started after the set delay time (frame).
- The data read out is constantly output form DATAO with the delay of the setup time.
- DATAO will be muted until the set delay time is over, because sufficient data is not written into memory immediately after the low output of ERROR flag.

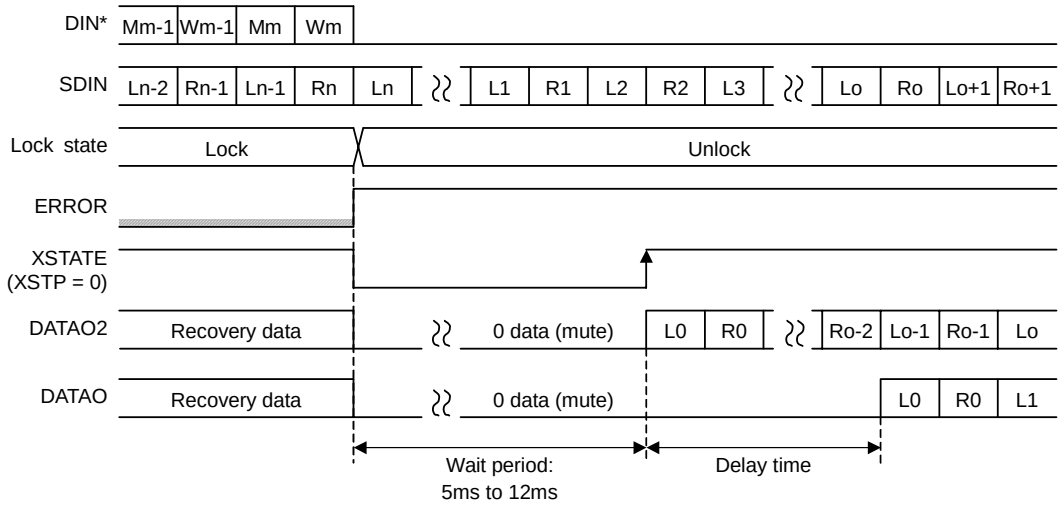


Figure 13.5 Timing Chart for Output Data after Setup or Change of the Delay Time During PLL Unlock

- When the DTMX[4:0] or DTMY[3:0] commands are canceled during low output of ERROR flag, data is output from DATAO synchronizing with the rising edge of XSTATE after PLL unlock. This is normal operation which does not perform a delay processing setup.

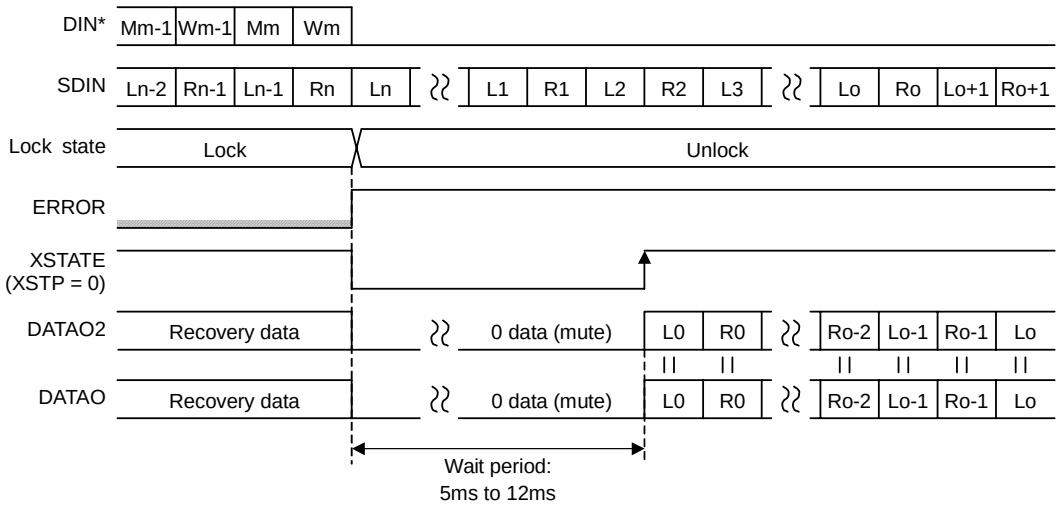


Figure 13.6 Timing Chart for Output Data after Cancel of the Delay Time Setting During PLL Unlock

13.2.4 Output Data Delay Setup of SDIN Input Data (Setting at the state of ERROR = H)

- When the DTMX[4:0] or DTMY[3:0] commands are set up or changed during high output of ERROR flag, delay processing is performed according to the setup of those commands.
- After power up, when the command is set up for the first time, a memory domain is assigned according to the set delay, and data is written in a memory.
- A memory domain is reset when the delay time is changed in the state where the command is already set up. And a memory domain is assigned according to the newly set delay time, and the data writing to a memory is started.
- Readout of the data written in the memory is started after the set delay time (frame).
- DATAO output is muted immediately after the command setup until the end of the set delay time.

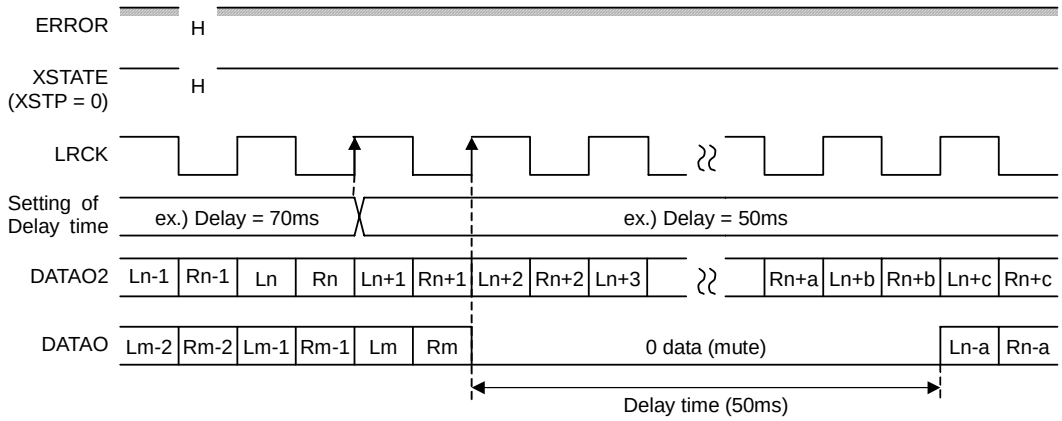


Figure 13.7 Timing Chart for Output Data after Setup or Change of the Delay Time During PLL Unlock

- When delay time is canceled in the state where the command is already set up, the writing to the memory is stopped. However, DATAO is output after muting the input data for 512-frame period. DATAO is not output immediately after cancel of command setting. The 512-frame period is dependent on the sampling frequency of input data.

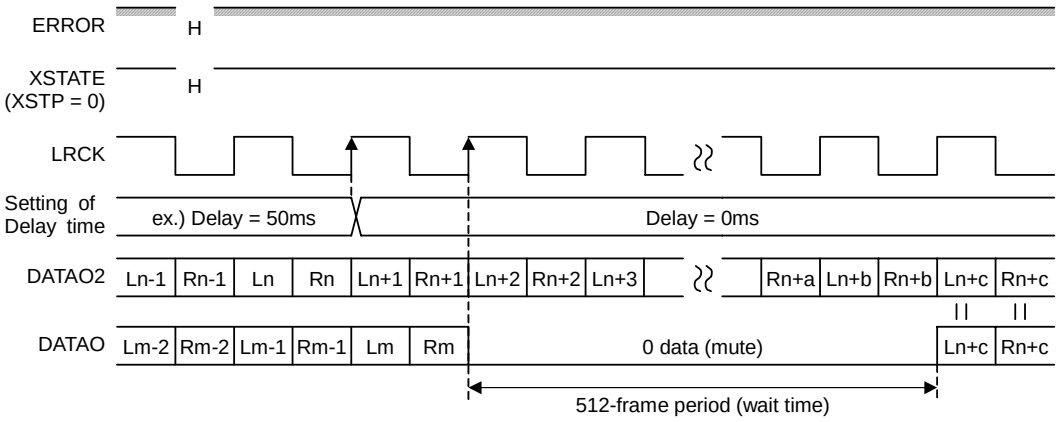


Figure 13.8 Timing Chart for Output Data after Cancel of the Delay Time Setting During PLL Unlock

- When the command is changed before the completion of command setting, the delay process is initialized every command setting. For DATAO output, mute output is continued until the setting is fixed.

13.3 Time Lag of the Command Setup (DTMA[4:0], DTMB[3:0], DTMC[2:0], DTMX[4:0], DTMY[3:0])

- DTMA [4:0], DTMB [3:0], DTMC [2:0], DTMX [4:0] and DTMY [3:0] commands are performed synchronizing with the rising edge (the falling edge is used for the I^2S data format setup) of LRCK clock. Therefore, the time lag of 1 LRCK cycle at the maximum arises after setting up the command until it is executed.
- Moreover, the minimum interval of a command setup becomes 1 LRCK period.
- Furthermore, data processing by command setup is performed after 1 LRCK period progress.
- Setup, change and cancel of the delay time are processed per command.
- Setup, change and cancel of the command in the same address are performed for the data of the target input sampling frequency.
- Cancel of the command is the case where the delay time is set as 0.

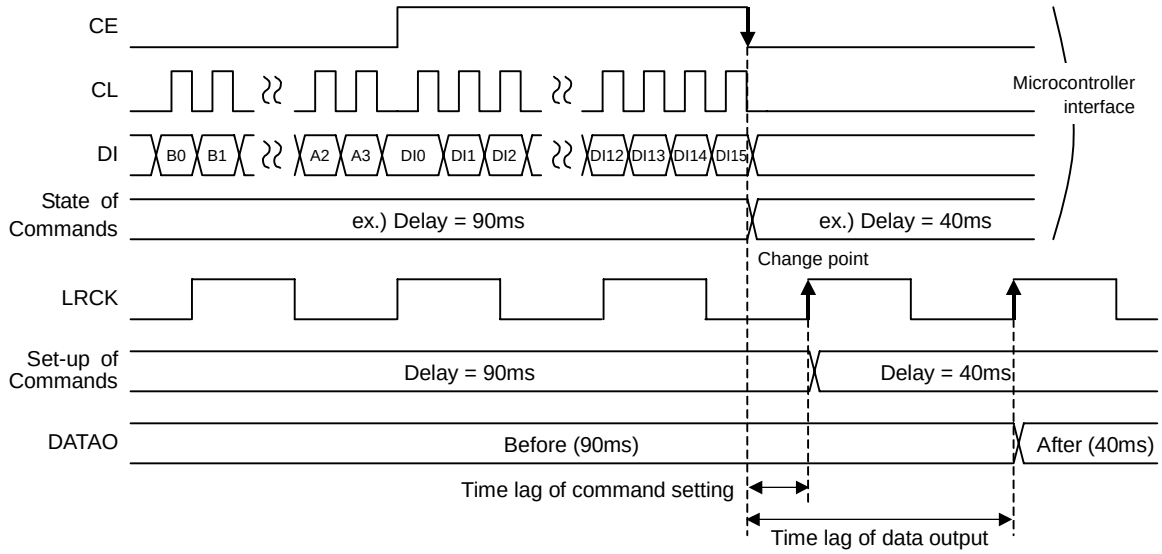


Figure 13.9 Timing Chart from a Command Setup to Execution

13.4 Monitor Setup for Output Data Delay Setting (FSEL)

- Information available for delay setting of output data can be monitored by FSB0, FSB1 and DLMP pins by switching the FSEL command. This setup is switched by FSEL command.
- FSB0 and FSB1 terminal classifies the calculation result of the sampling frequency of input data into standard frequency, standard ×2, and standard ×4 and outputs.
- However, when S/PDIF data is not received, PLL is not locked, or when the mode 4 is set up with MODE0 and MODE1 terminal, FSB0 and FSB1 terminals output low.
- DLMP terminal outputs a pulse signal during the waiting time period at the time of ERROR flag switching, or during the mute period at the time of a delay setup. This pulse can change polarity by DLPO command.

Table 13.3. FSB0 and FSB1 output state (FSEL = 1)

FSB1 pin	FSB0 pin	Output state
L	L	S/PDIF data is not received, or PLL is unlocked, when the mode 4 is set up with MODE0 and MODE1 terminal.
L	H	S/PDIF data is either of the 32kHz or 44.1kHz or 48kHz. (Standard frequency)
H	L	S/PDIF data is either of the 88.2kHz or 96kHz. (Standard ×2 frequency)
H	H	S/PDIF data is either of the 176.4kHz or 192kHz. (Standard ×4 frequency)

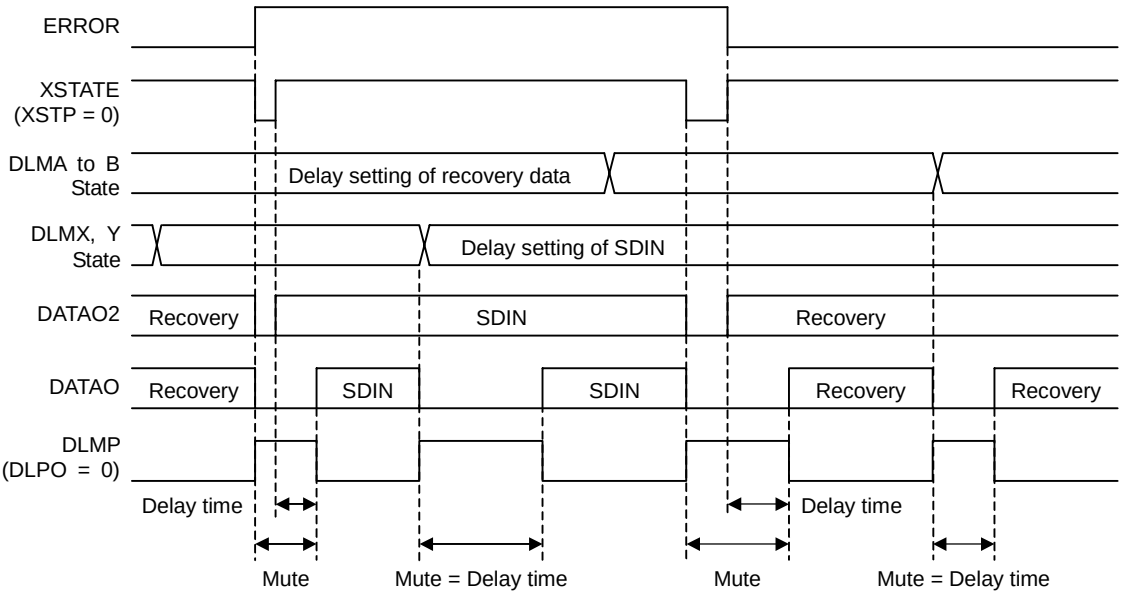


Figure 13.10 Timing Chart for DLMP Output Mute Period (command cancel is not included)

14. Microcontroller Interface (CL, CE, DI, DO)

14.1 Chip Address Settings

- The microcontroller interface uses Sanyo's original serial bus format (CCB). Data input/output is performed after data input/output address has been assigned. DO pin is an open drain output system.

Table 14.1 Addresses Settings

Data input/output	CCB address	B0	B1	B2	B3	A0	A1	A2	A3
Data input 1	0xE8	0	0	0	1	0	1	1	1
C bit output	0xE9	1	0	0	1	0	1	1	1
Pc data output	0xEA	0	1	0	1	0	1	1	1
Data input 2	0xEB	1	1	0	1	0	1	1	1
Data input 3	0xEC	0	0	1	1	0	1	1	1
Data input 4	0xED	1	0	1	1	0	1	1	1

14.2 Input/Output Timing

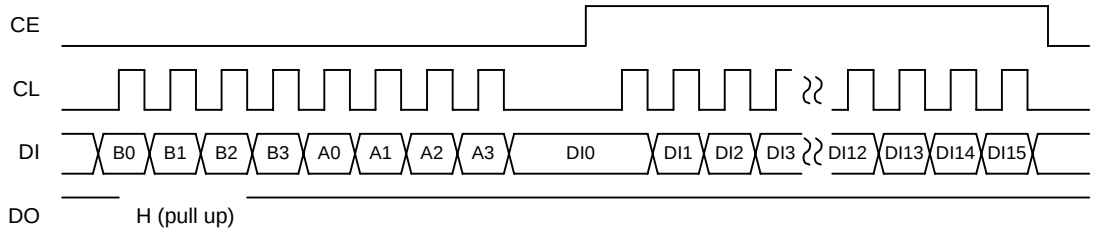


Figure 14.1 Input Timing Chart (Normal L Clock)

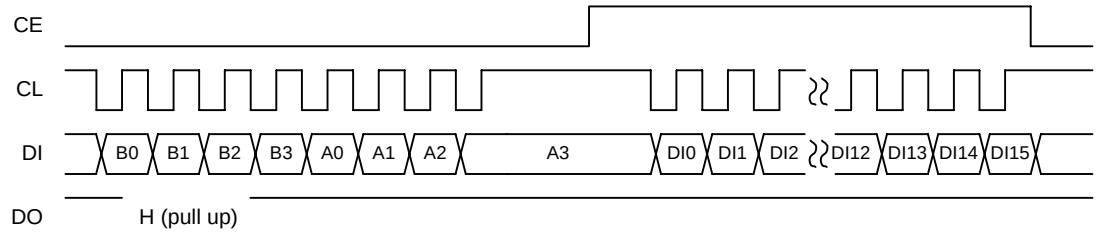


Figure 14.2 Input Timing Chart (Normal H Clock)

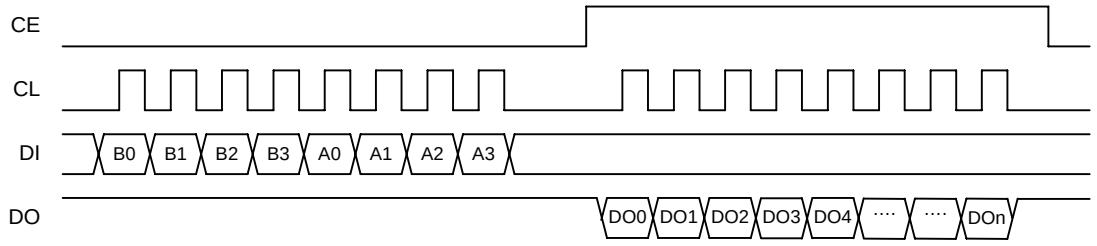


Figure 14.3 Output Timing Chart (Normal L Clock, DO includes a pull-up resister)

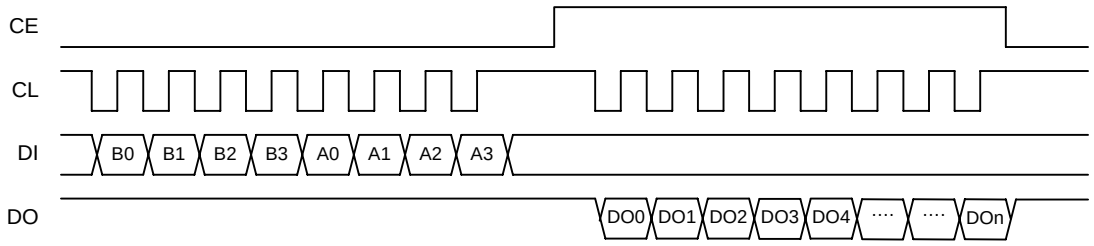


Figure 14.4 Output Timing Chart (Normal H Clock, DO includes a pull-up resister)
*Valid only when IMOD=1
**Output data can not be read when IMOD=0

14.3 0xE9 Data Output Timing

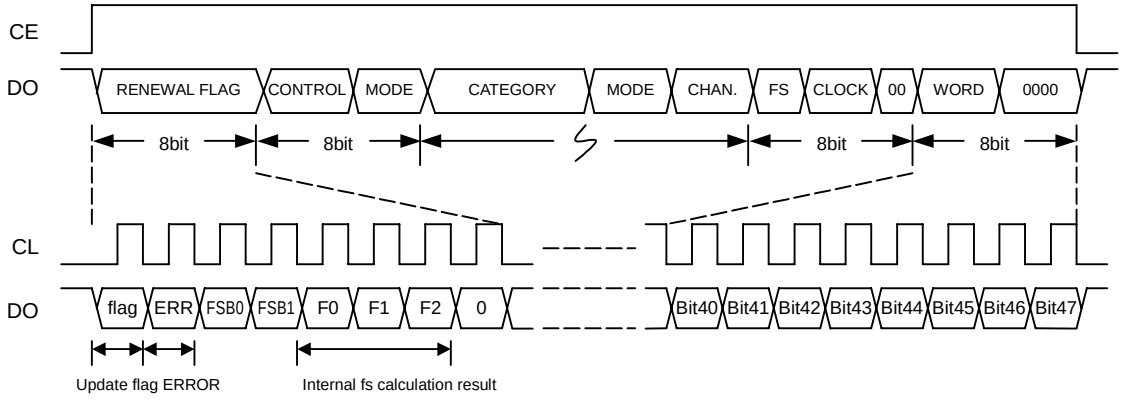


Figure 14.5 Output Timing of Flag + Channel Status Data

14.4 0xEA Data Output Timing

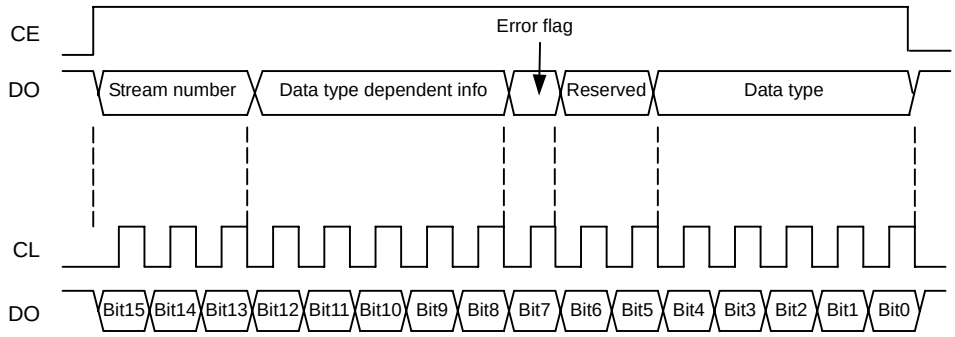


Figure 14.6 Output Timing of Preamble Pc Data

14.5 Write Data

14.5.1 List of Write Commands

• A list of the write commands is shown below.

Table 14.2 Input Register Map

Register	Address: 0xE8	Address: 0xEB	Address: 0xEC	Address: 0xED
DI0	0	IMOD	DTMA0	DTMX0
DI1	0	0	DTMA1	DTMX1
DI2	0	FSEL	DTMA2	DTMX2
DI3	DOSW	VSEL	DTMA3	DTMX3
DI4	STOP	CKPO	DTMA4	DTMX4
DI5	SMOD	0	0	0
DI6	XCNT	XSTP	0	0
DI7	XADC	XCKS	0	0
DI8	DIS0	DLPO	DTMB0	DTMY0
DI9	DIS1	0	DTMB1	DTMY1
DI10	FSL0	DOM0	DTMB2	DTMY2
DI11	FSL1	DOM1	DTMB3	DTMY3
DI12	ERF0	0	0	0
DI13	ERF1	0	DTMC0	0
DI14	BMOD	EWT0	DTMC1	0
DI15	CKDV	EWT1	DTMC2	0

Note: * “0” is a reserved bit. It is write-protected.

14.5.2 Details of Write Commands

CCB address: 0xE8

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
XADC	XCNT	SMOD	STOP	DOSW	0	0	0
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
CKDV	BMOD	ERF1	ERF0	FSL1	FSL0	DIS1	DIS0

DOSW Output data format setting
- 0 : Follow setting of DOSEL0 and DOSEL1 (default)
- 1 : 24bit I^2S data output

STOP System stop setting
- 0 : Don't stop system (default)
- 1 : Stop system

SMOD Source setting
- 0 : Digital mode, digital data reception enabled (default)
- 1 : Analog mode, digital data reception disabled

XCNT XIN, XOUT oscillation amplifier operation setting
- 0 : PLL is stopped when locked (default)
- 1 : PLL always operates, regardless of locked/unlocked

XADC XMCK output clock setting
- 0 : Output XIN clock (default)
- 1 : Output 1/2 of XIN clock

DIS[1:0] S/PDIF Input data pin setting

- 00 : Follow DISEL setting (default)
- 01 : Select DIN0
- 10 : Select DIN1
- 11 : Select DIN2

FSL[1:0] S/PDIF Input data reception range setting

- 00 : Normal mode (Same as the mode 1 of MODE0 and MODE1) (default)
- 01 : 32kHz to 48kHz
- 10 : Fs free mode A (Same as the mode 2 of MODE0 and MODE1)
- 11 : 32kHz to 96kHz

If set reception range is exceeded, ERROR is output as high even if PLL is locked.

ERF[1:0] Parity error flag output setting if 8 or fewer input parity errors occur in succession

- 00 : Error flag is not output (default)
- 01 : Only output during sub-frame with error
- 10 : Reserved
- 11 : Only output upon Non-PCM burst data recognition

In case ERF[1:0]=00, although no error flag is output, the process for error is executed for output data.
In case ERF[1:0]=01, no error flag is output when the delay setting of output data is performed.
In case ERF[1:0]=11, Non-PCM burst data recognition is performed when channel status bit1 is high.

BMOD DOUT output state setting

- 0 : Outputs a selected input data (default)
- 1 : L fixed

CKDV CKOUT output state setting when PLL is locked

- 0 : Output CKSEL0 and CKSEL1 setting clock (default)
- 1 : Output 1/2 of CKSEL0 and CKSEL1 setting clock

CCB address: 0xEB

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
XCKS	XSTP	0	CKPO	VSEL	FSEL	0	IMOD
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
EWT1	EWT0	0	0	DOM1	DOM0	0	DLPO

IMOD — CL pin setting
- 0 : Data readout is performed with normal L clock (default)
- 1 : Data readout is performed with normal H clock

FSEL — F0/FSB0, F1/FSB1, F2/DLMP pin setting
- 0 : F0, F1, F2; Input sampling frequency calculated signal output (default)
- 1 : FSB0, FSB1, DLMP; The monitor signal output for a delay setting

VSEL — VF/DATAO2 pin setting
- 0 : VF; Validity flag output (default)
- 1 : DATAO2; Data output after demodulation

CKPO — CKOUT output polarity setting
- 0 : Normal output (default)
- 1 : Inverted-phase output

XSTP — XSTATE output polarity setting
- 0 : Normal H output (default)
- 1 : Normal L output

XCKS — XMCK output setting while PLL is locked (Enable, when XCNT= 1)
- 0 : Output according to the operation of oscillation amplifier (default)
- 1 : Stop output only when PLL is locked during the continuous operation of oscillation amplifier

DLPO　　DLMP output polarity setting (Enable, when FSEL = 1)

0 : Normal L output (default)

1 : Normal H output

DOM[1:0]　　DATAO, DATAO2 mute setting

00 : The data chosen by SMOD is outputted (default)

01 : Only DATAO is muted

10 : Only DATAO2 is muted

11 : DATAO and DATAO2 are muted

EWT[1:0]　　An ERROR output waiting time setup after a PLL lock

00 : Cancel error after preamble B is counted to 48 (default)

01 : Cancel error after preamble B is counted to 12

10 : Cancel error after preamble B is counted to 6

11 : Cancel error after preamble B is counted to 3

The pulse width of XSTATE output after a PLL lock by input data is as follows.

XSTATE pulse width = {192/fs × (“EWT[1:0] count value” - 2)}

Table 14.3. Pulse Width of XSTATE output

Input fs	EWT[1:0]			
	“00”	“01”	“10”	“11”
32kHz	276.0ms	60.0ms	24.0ms	6.0ms
44.1kHz	200.2ms	43.5ms	17.4ms	4.3ms
48kHz	184.0ms	40.0ms	16.0ms	4.0ms
88.2kHz	100.1ms	21.7ms	8.7ms	2.1ms
96kHz	92.0ms	20.0ms	8.0ms	2.0ms
176.4kHz	50.0ms	10.8ms	4.3ms	1.0ms
192kHz	46.0ms	10.0ms	4.0ms	1.0ms

CCB address: 0xEC

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	DTMA4	DTMA3	DTMA2	DTMA1	DTMA0
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
DTMC2	DTMC1	DTMC0	0	DTMB3	DTMB2	DTMB1	DTMB0

DTMA[4:0] Delay time setting for DATAO output data
Setup for 32kHz, 44.1 kHz and 48kHz S/PDIF input data

00000 : Non delay (default)
00001 : Delayed 10ms
00010 : Delayed 20ms
00011 : Delayed 30ms
00100 : Delayed 40ms
00101 : Delayed 50ms
00110 : Delayed 60ms
00111 : Delayed 70ms
01000 : Delayed 80ms
01001 : Delayed 90ms
01010 : Delayed 100ms
01011 : Delayed 110ms
01100 : Delayed 120ms
01101 : Delayed 130ms
01110 : Delayed 140ms
01111 : Delayed 150ms
10000 Delayed 160ms
10001 Delayed 170ms
10010 Delayed 180ms
10011 Delayed 190ms
10100 Delayed 200ms
10101 Delayed 210ms
10110 Delayed 220ms
10111 Delayed 230ms
11000 Delayed 240ms
11001 Delayed 250ms
11010 Delayed to the maximum
11011 Non delay
11100 Non delay
11101 Non delay
11110 Non delay
11111 Non delay

The delay value at the time of 11010 setup is as follows.
When fs=32kHz, delayed 384ms
When fs=44.1kHz, delayed 278ms
When fs=48kHz, delayed 256ms

DTMB[3:0] Delay time setting for DATAO output data
Setup for 88.2kHz and 96kHz S/PDIF input data

0000	:	Non delay (default)
0001	:	Delayed 10ms
0010	:	Delayed 20ms
0011	:	Delayed 30ms
0100	:	Delayed 40ms
0101	:	Delayed 50ms
0110	:	Delayed 60ms
0111	:	Delayed 70ms
1000	:	Delayed 80ms
1001	:	Delayed 90ms
1010	:	Delayed 100ms
1011	:	Delayed 110ms
1100	:	Delayed 120ms
1101	:	Delayed to the maximum
1110	:	Non delay
1111	:	Non delay

The delay value at the time of 1101 setup is as follows.
When fs=88.2kHz, delayed 139ms
When fs=96kHz, delayed 128ms

DTMC[2:0] Delay time setting for DATAO output data
Setup for 176.4kHz and 192kHz S/PDIF input data

000	:	Non delay (default)
001	:	Delayed 10ms
010	:	Delayed 20ms
011	:	Delayed 30ms
100	:	Delayed 40ms
101	:	Delayed 50ms
110	:	Delayed 60ms
111	:	Delayed to the maximum

The delay value at the time of 111 setup is as follows.
When fs=176.4kHz, delayed 69ms
When fs=192kHz, delayed 64ms

CCB address: 0xED

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	DTMX4	DTMX3	DTMX2	DTMX1	DTMX0
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	0	0	0	DTMY3	DTMY2	DTMY1	DTMY0

DTMX[4:0] Delay time setting for DATAO output data
Setup for 48kHz SDIN input data

00000 : Non delay (default)
00001 : Delayed 10ms
00010 : Delayed 20ms
00011 : Delayed 30ms
00100 : Delayed 40ms
00101 : Delayed 50ms
00110 : Delayed 60ms
00111 : Delayed 70ms
01000 : Delayed 80ms
01001 : Delayed 90ms
01010 : Delayed 100ms
01011 : Delayed 110ms
01100 : Delayed 120ms
01101 : Delayed 130ms
01110 : Delayed 140ms
01111 : Delayed 150ms
10000 Delayed 160ms
10001 Delayed 170ms
10010 Delayed 180ms
10011 Delayed 190ms
10100 Delayed 200ms
10101 Delayed 210ms
10110 Delayed 220ms
10111 Delayed 230ms
11000 Delayed 240ms
11001 Delayed 250ms
11010 Delayed to the maximum
11011 Non delay
11100 Non delay
11101 Non delay
11110 Non delay
11111 Non delay

The delay value at the time of 11010 setup is as follows.
When fs=48kHz, delayed 256ms

DTMY[3:0] Delay time setting for DATAO output data
Setup for 96kHz SDIN input data

0000	:	Non delay (default)
0001	:	Delayed 10ms
0010	:	Delayed 20ms
0011	:	Delayed 30ms
0100	:	Delayed 40ms
0101	:	Delayed 50ms
0110	:	Delayed 60ms
0111	:	Delayed 70ms
1000	:	Delayed 80ms
1001	:	Delayed 90ms
1010	:	Delayed 100ms
1011	:	Delayed 110ms
1100	:	Delayed 120ms
1101	:	Delayed to the maximum
1110	:	Non delay
1111	:	Non delay

The delay value at the time of 1101 setup is as follows.
When fs=96kHz, delayed 128ms

14.6 Read Data

14.6.1 List of Read Commands

- The following data are read with output code.
  * Update flag for the first 48bits of channel status. (Address: E9, Register: DO0)
  * ERROR pin status. (Address: E9, Register: DO1)
  * Delay time setting status for DATAO output data. (Address: E9, Register: DO2, 3)
  * Input sampling frequency calculation result. (Address: E9, Register: DO4 to 7)
  * The first 48bits of channel status data. (Address: E9, Register: DO8 to 55)
  * 16bit non-PCM burst preamble Pc data. (Address: EA, Register: DO0 to 15)

Table 14.3 Read Data

Register	Address	
	E9	EA
DO0	CSFLAG	Pc-bit15
DO1	ERROR	Pc-bit14
DO2	FSB0	Pc-bit13
DO3	FSB1	Pc-bit12
DO4	F0	Pc-bit11
DO5	F1	Pc-bit10
DO6	F2	Pc-bit9
DO7	0	Pc-bit8
DO8	C-bit0	Pc-bit7
DO9	C-bit1	Pc-bit6
DO10	C-bit2	Pc-bit5
DO11	C-bit3	Pc-bit4
DO12	C-bit4	Pc-bit3
DO13	C-bit5	Pc-bit2
DO14	C-bit6	Pc-bit1
DO15	C-bit7	Pc-bit0
DO16	C-bit8	0
DO17	C-bit9	0
DO18	C-bit10	0
DO19	C-bit11	0
DO20	C-bit12	0
DO21	C-bit13	0
DO22	C-bit14	0
DO23	C-bit15	0
DO24	C-bit16	0
DO25	C-bit17	0
DO26	C-bit18	0
DO27	C-bit19	0

Register	Address	
	E9	EA
DO28	C-bit20	0
DO29	C-bit21	0
DO30	C-bit22	0
DO31	C-bit23	0
DO32	C-bit24	0
DO33	C-bit25	0
DO34	C-bit26	0
DO35	C-bit27	0
DO36	C-bit28	0
DO37	C-bit29	0
DO38	C-bit30	0
DO39	C-bit31	0
DO40	C-bit32	0
DO41	C-bit33	0
DO42	C-bit34	0
DO43	C-bit35	0
DO44	C-bit36	0
DO45	C-bit37	0
DO46	C-bit38	0
DO47	C-bit39	0
DO48	C-bit40	0
DO49	C-bit41	0
DO50	C-bit42	0
DO51	C-bit43	0
DO52	C-bit44	0
DO53	C-bit45	0
DO54	C-bit46	0
DO55	C-bit47	0

14.6.2 Read Out Register 0xE9 (First 48bit channel status data)

- For reading the register, set the CCB address as 0xE9.
- CSFLAG (DO0), ERROR (DO1), FSB0 (DO2), FSB1 (DO3), F0 (DO4), F1 (DO5) and F2 (DO6) output the status of pin 25 (CSFLAG), pin34 (ERROR), pin26 (F0/FSB0), pin27 (F1/FSB1) and pin28 (F2) at the time of read.
- The channel status bits 0 to 47 are output with LSB first.
- The channel status data after a CCB address setup is not updated.
- The latest data can be transferred by reading the falling edge of CSFLAG as the load enable signal.
- The relation between the read register and channel status data is shown below.

Table 14.4 Read register for the first 48bits of channel status data

Register	Bit No.	Contents	Register	Bit No.	Contents
DO8	Bit 0	Application	DO32	Bit 24	Sampling frequency
DO9	Bit 1	Control	DO33	Bit 25	
DO10	Bit 2		DO34	Bit 26	
DO11	Bit 3		DO35	Bit 27	
DO12	Bit 4		DO36	Bit 28	Clock accuracy
DO13	Bit 5		DO37	Bit 29	
DO14	Bit 6	Not defined	DO38	Bit 30	Not defined
DO15	Bit 7		DO39	Bit 31	
DO16	Bit 8	Category code	DO40	Bit 32	Word length
DO17	Bit 9		DO41	Bit 33	
DO18	Bit 10		DO42	Bit 34	
DO19	Bit 11		DO43	Bit 35	
DO20	Bit 12		DO44	Bit 36	Not defined
DO21	Bit 13		DO45	Bit 37	
DO22	Bit 14		DO46	Bit 38	
DO23	Bit 15		DO47	Bit 39	
DO24	Bit 16	Source number	DO48	Bit 40	
DO25	Bit 17		DO49	Bit 41	
DO26	Bit 18		DO50	Bit 42	
DO27	Bit 19		DO51	Bit 43	
DO28	Bit 20	Channel number	DO52	Bit 44	
DO29	Bit 21		DO53	Bit 45	
DO30	Bit 22		DO54	Bit 46	
DO31	Bit 23		DO55	Bit 47	

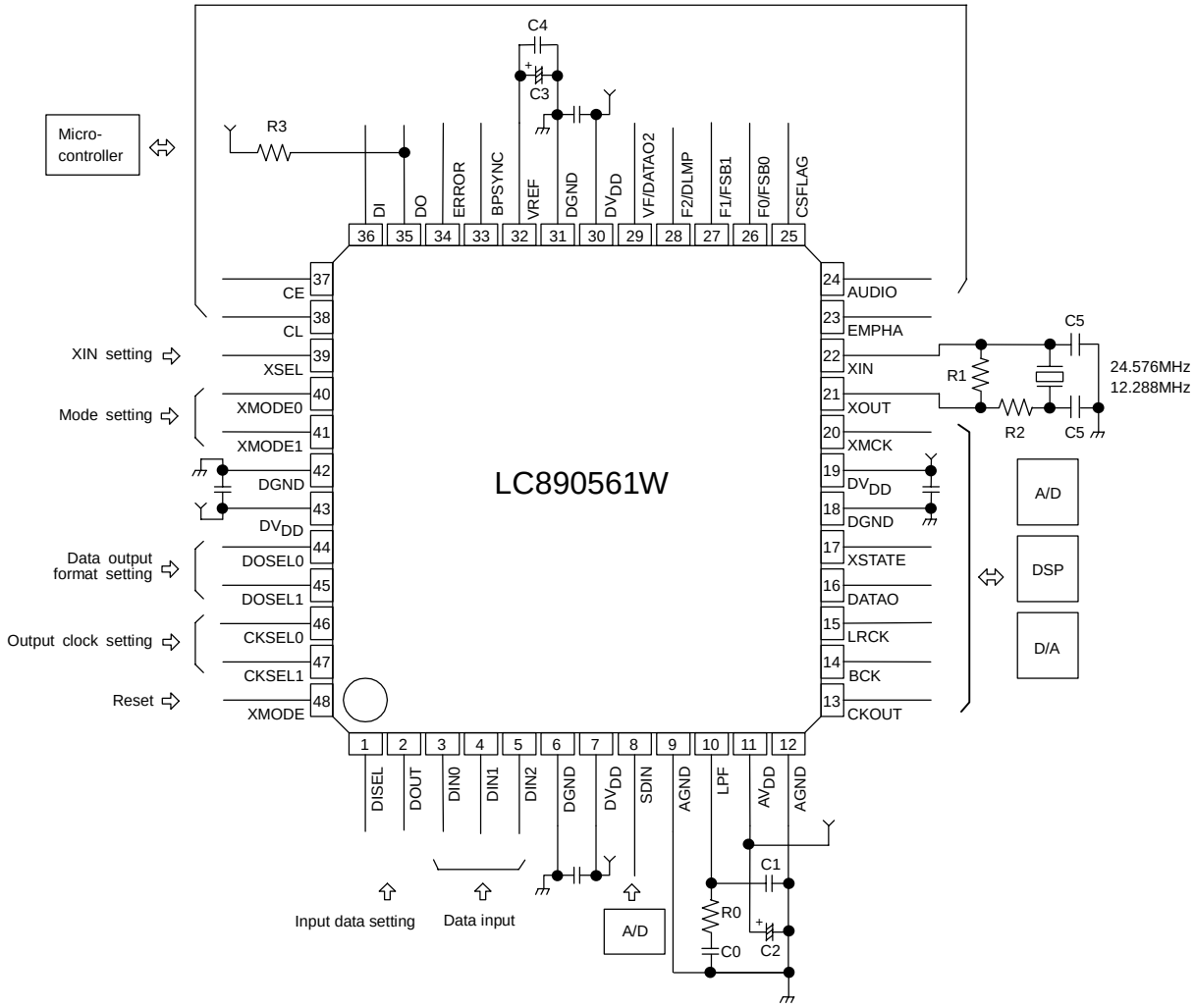
14.6.3 Read Out Register 0xEA (Burst Preamble Pc Data)

- For reading the register, set the CCB address as 0xEA.
- 16-bit data of burst preamble Pc is output with MSB first
- The latest data can be transferred by reading the falling edge of BPSYNC as the load enable signal.
- The relation between the read register and burst preamble Pc data is shown below.

Table 14.5 Burst Preamble Pc data

Register	Bit No.	Contents
DO0	Bit 15	Bit stream number
DO1	Bit 14	
DO2	Bit 13	
DO3	Bit 12	Data type dependent information
DO4	Bit 11	
DO5	Bit 10	
DO6	Bit 9	
DO7	Bit 8	
DO8	Bit 7	Error
DO9	Bit 6	Reserved
DO10	Bit 5	
DO11	Bit 4	Data type
DO12	Bit 3	
DO13	Bit 2	
DO14	Bit 1	
DO15	Bit 0	

15. Application Circuit Example



C0: 0.1µF
C1: 0.01µF
C2: 47µF
C3: 10µF
C4: 0.1µF
C5: 1p to 33pF**

R0: 100Ω
R1: 1MΩ**
R2: 220Ω**
R3: 5k to 10kΩ

**Since the values of C5, R1, and R2 differ with an oscillator, please examine them enough.