CMOS LSI

LC89066, 89066M

6-Bit Video A/D Converters

Overview

The LC89066 and LC89066M are high-speed analog-to-digital converters. They are of flash type, operate from single 5V supply, and feature a 15 Mega-samples per second conversion rate and low power dissipation.
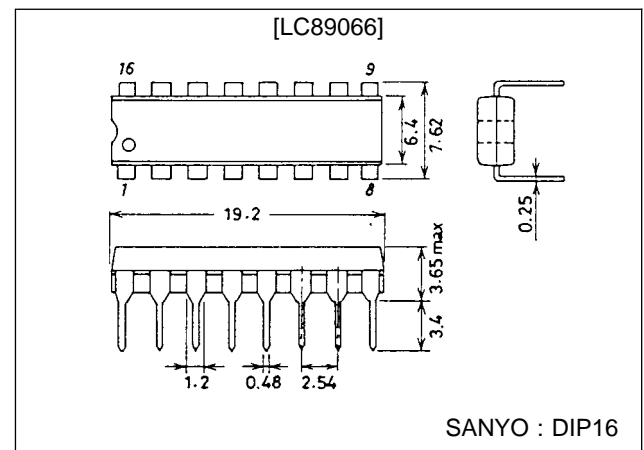
Features

- Conversion rate: 15 MSPS
- Low power dissipation: 120 mW
- Linearity error within ±0.8 LSB (max)
- TTL-compatible inputs
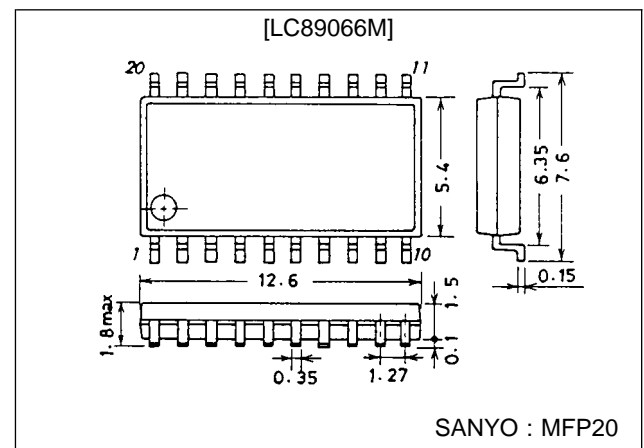- LC89066: DIP-16
  LC89066M: MFP-20

Package Dimensions

unit : mm

3006B-DIP16

SANYO : DIP16

unit : mm

3036B-MFP20

SANYO : MFP20

Specifications

Absolute Maximum Ratings at Ta = 25 °C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD} +0.3	V
Operating temperature	Topr	LC89066	−30 to +75	°C
		LC89066M	−30 to +65	°C
Storage temperature	Tstg		−40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Reference voltage (high)	V_{RH}				V_{DD}	V
Reference voltage (low)	V_{RL}		0			V
Input high-level voltage	V_{IH}		2.2		V_{DD} +0.3	V
Input low-level voltage	V_{IL}		−0.3		+0.8	V
Analog input voltage	V_{ANI}		V_{RL}		V_{RH}	V
Clock high period	T_{WH}		30			ns
Clock low period	T_{WL}		30			ns

Electrical Characteristics at Ta = 25 °C, V_{DD} = 5.0 V, V_{RH} = 5.0 V, V_{RL} = 3.0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Resolution	RES				6	bit
Maximum sampling frequency	Fs max		15			MSPS
Power dissipation	Pd	Fs = 15 MSPS		120	200	mW
Linearity error	I.L.	DC accuracy			±0.8	LSB
Differential linearity error	D.L.	DC accuracy			±0.5	LSB
String resistance	Rst		400	600	800	Ω
Analog input capacitance	C_{AIN}			50		pF
Analog input resistance	R_{AIN}		10			MΩ
Output delay time	TdL			20	45	ns

Equivalent Circuit Block Diagram
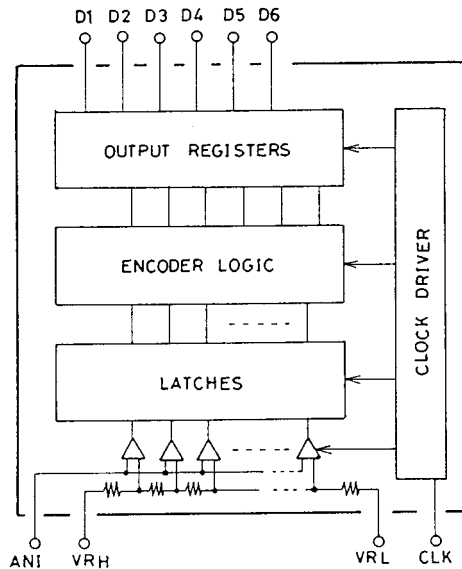
Timing Chart
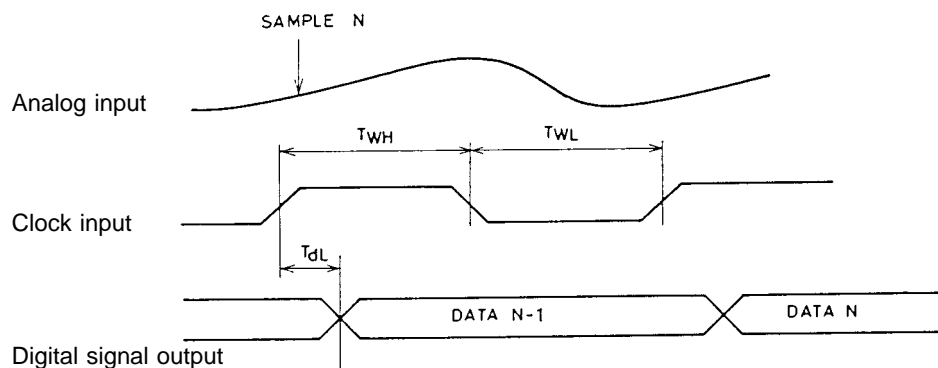
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Pin Functions

• LC89066

Pin No.	Symbol	Description
1	D6	Digital output data (least significant bit)
2	D5	Digital output data
3	D4	
4	D3	
5	D2	
6	D1	Digital output data (most significant bit)
7	CLK	Clock input
8	GND	Ground (analog)
9	V_{DD}	Power supply (analog)
10	V_{DD}	
11	V_{RH}	Reference voltage input (high)
12	ANI	Analog voltage input
13	V_{RL}	Reference voltage input (low)
14	V_{DD}	Power supply (digital)
15	V_{DD}	
16	GND	Ground (digital)

• LC89066M

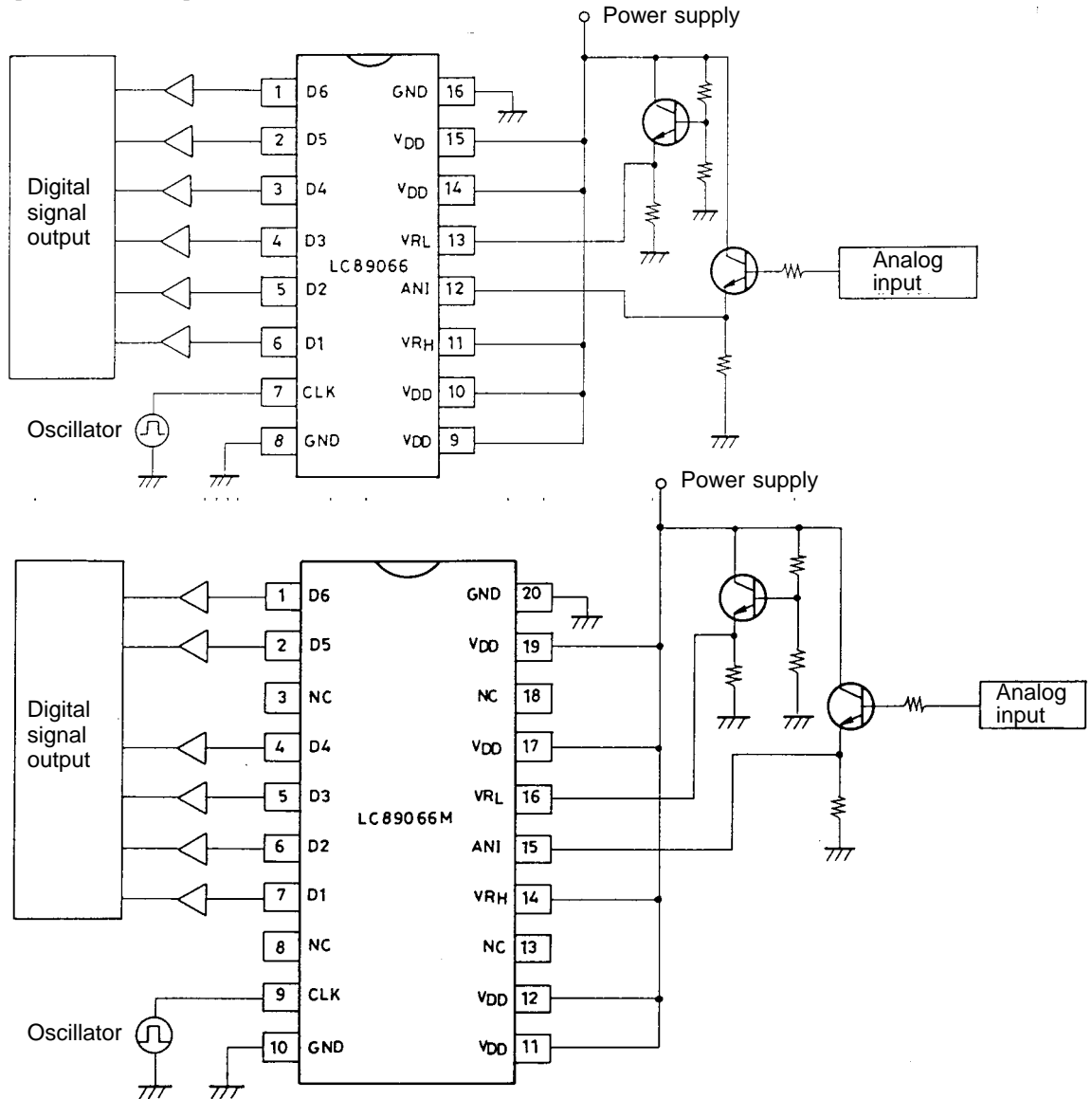| Pin No.	Symbol	Description
1	D6	Digital output data (least significant bit)
2	D5	Digital output data
3	N.C.	No connection
4	D4	Digital output data
5	D3	
6	D2	
7	D1	Digital output data (most significant bit)
8	N.C.	No connection
9	CLK	Clock input
10	GND	Ground (analog)
11	V_{DD}	Power supply (analog)
12	V_{DD}	
13	N.C.	No connection
14	V_{RH}	Reference voltage input (high)
15	ANI	Analog voltage input
16	V_{RL}	Reference voltage input (low)
17	V_{DD}	Power supply (digital)
18	N.C.	No connection
19	V_{DD}	Power supply (digital)
20	GND	Ground (digital)

Functional Description

Signal on the analog signal input pin ANI is input into the comparators on the rising edge of the CLK input signal. This signal is compared with the voltage divided by resistors and digitized. This digitized signal is coded by the encoder logic and output on the next rising edge of the CLK input signal. The conversion range depends on the converter high and low reference voltage V_{RH} and V_{RL}. When zero transient voltage is set to 3.000 V by V_{RL} voltage and full scale transient voltage to 4.984 V by V_{RH} voltage, the output data is linearly related to the input voltage as shown in the table below.

	Input voltage (V)	Output data
0	to 3.000	000000
1	3.000 to 3.032	000001
2	3.032 to 3.064	000010
3	3.064 to 3.096.	000011
⋮	⋮	⋮
61	4.920 to 4.952	111101
62	4.952 to 4.984	111110
63	4.984 to	111111

Sample Application Circuits

The following diagrams show typical application circuits for the LC89066 and LC89066M. The high reference voltage is connected to the positive supply line, and the low reference voltage generated by a voltage divider and emitter follower. The analog signal is input with a low impedance.

This catalog provides information as of January, 1997. Specifications and information herein are subject to change without notice.