Ordering number : EN*5072A

CMOS LSI

LC99052-V64A

Image Sensor Control LSI

Preliminary

Overview

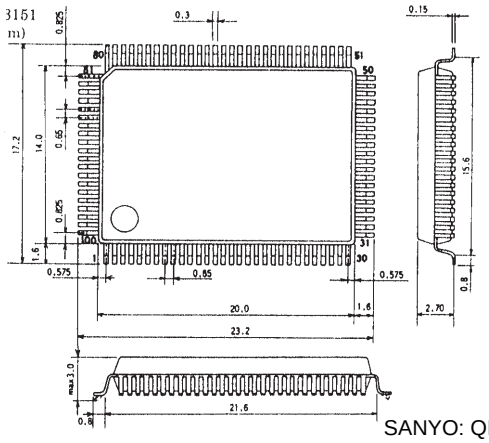
The LC99052-V64A is a digital image sensor system LSI that includes A/D converter and timing circuits for analog signal processing. The LC99052-V64A is implemented in a single chip using standard cells.

Package Dimensions

unit: mm

3151-QFP100E

[LC99052-V64A]



SANYO: QIP100E

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
I/O voltages	V_I, V_O		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 60°C	950	mW
Operating temperature	Topr		–15 to +60	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering conditions		Hand soldering: 3 seconds	350	°C
		Reflow: 10 seconds	235	°C
I/O currents	I_I, I_O	Per individual I/O reference cell	±20	mA

Allowable Operating Ranges at Ta = –15 to +60°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage range	V_{IN}		0		V_{DD}	V

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Electrical Characteristics at Ta = –15 to +60°C, V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH}	TTL compatible Schmitt: applicable pin (3)	2.5			V
Input low level voltage	V_{IL}	TTL compatible Schmitt: applicable pin (3)			0.6	V
Input high level voltage	V_{IH}	CMOS compatible: applicable pins (1), (2) and (4)	0.7 V_{DD}			V
Input low level voltage	V_{IL}	CMOS compatible: applicable pins (1), (2) and (4)			0.3 V_{DD}	V
Output high level voltage	V_{OH}	I_{OH} = –3 mA: applicable pins (9), (10) and (11)	V_{DD} – 2.1			V
Output low level voltage	V_{OL}	I_{OL} = 3 mA: applicable pins (9), (10) and (11)			0.4	V
Output high level voltage	V_{OH}	I_{OH} = –6 mA: applicable pins (5) and (7)	V_{DD} – 2.1			V
Output low level voltage	V_{OL}	I_{OL} = 6 mA: applicable pins (5) and (7)			0.4	V
Output high level voltage	V_{OH}	I_{OH} = –30 mA: applicable pin (8)	V_{DD} – 2.1			V
Output low level voltage	V_{OL}	I_{OL} = 10 mA: applicable pin (8)			0.4	V
Output high level voltage	V_{OH}	I_{OH} = –12 mA: applicable pin (6)	V_{DD} – 1.5			V
Output low level voltage	V_{OL}	I_{OL} = 4 mA: applicable pin (6)			0.4	V
Input leakage current	I_{IL}	V_I = V_{SS}, V_{DD}: applicable pins (1), (2), (3) and (4)	–10		+10	µA
Output leakage current	I_{OZ}	In high-impedance output mode: applicable pin (10)	–10		+10	µA

Note: The applicable pin sets are defined as follows:

Input

(1) .....MCKI
(2) .....OEB, RESB
(3) .....CLKS, DATAS, FTTRG, HR, REGRESB, STTRG, VR
(4) .....DACLKIN, DIN0 to DIN7, EXT1 to EXT4, ICONIN, IREF1, IREF2, MIRROR, TESTB, TV

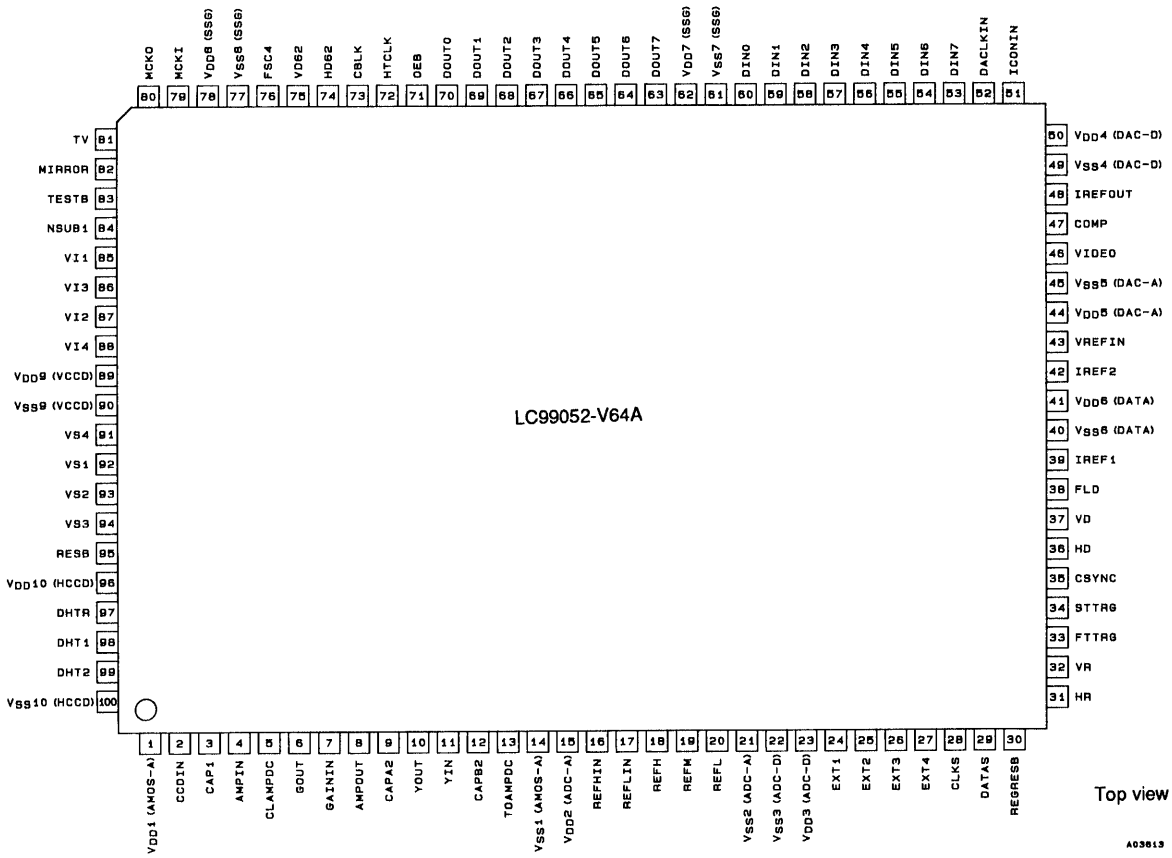
Output

(5) FSC4
(6) .....MCKO
(7) .....DHTR
(8) DHT1, DHT2
(9) .....CBLK, CSYNC, HD62, HTCLK, NSUB1
(10) ....DOUT0 to DOUT7
(11) ....FLD, HD, VD62, VI1 to VI4, VS1 to VS4
* .....IREFOUT

AMPOUT, COMP, GOUT, REFH, REFHIN, REFL, REFLIN, REFM, VIDEO, VREFIN, YOUT

The pins listed above are not included in the DC characteristics.

Pin Assignment



Pin Functions

I/O → I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

Pin No.	Symbol	I/O	Function
1	$V_{DD}1$ (AMOS-A)		
2	CCDIN	I	CCD input pin
3	CAP1	I	AMOS-CDS bias pin
4	AMPIN	I	6 dB amplifier input pin
5	CLAMPDC	O	6 dB amplifier clamp circuit bias output pin
6	GOUT	O	Gain control output
7	GAININ	I	Gain control input
8	AMPOUT	O	6 dB amplifier output pin
9	CAPA2	I	AMOS-AGC bias pin
10	YOUT	O	AGC output
11	YIN	I	Clamp, A/D converter input
12	CAPB2	I	AMOS-clamp bias pin
13	TOAMPDC	O	6 dB amplifier bias output pin
14	$V_{SS}1$ (AMOS-A)		
15	$V_{DD}2$ (ADC-A)		
16	REFHIN	I	A/D converter high level reference input
17	REFLIN	I	A/D converter low level reference input
18	REFH	O	A/D converter high level reference output
19	REFM	O	A/D converter middle level reference output
20	REFL	O	A/D converter low level reference output
21	$V_{SS}2$ (ADC-A)		
22	$V_{SS}3$ (ADC-D)		
23	$V_{DD}3$ (ADC-D)		
24	EXT1	I	EXT1, 2 = 00: Direct H and V reset, 10: Direct C.sync reset 01: Mode 3, an external clamp pulse can be input from pin 32 (VR), ENDFLG is output from pin 36 (CSYNC). 11: NON
25	EXT2	I	
26	EXT3	I	EXT3, 4 = 00: Auto iris, 10: Normal, 01: External shutter, 11: External FT, ST
27	EXT4	I	
28	CLKS	I	Serial clock input
29	DATAS	I	Serial data input
30	REGRESB	I	Register reset; 0: Reset
31	HR	I	Hsync, CSYNC reset pulse input
32	VR	I	Vsync reset pulse input
33	FTTRG	I	External frame_sift trigger input Auto iris mode = selmet1
34	STTRG	I	External shutter trigger input Auto iris mode = selmet2
35	CSYNC	O	In mode 3 (H reset mode), this pin outputs ENDFLG. This pin is affected by the SSG_DELAY (register).
36	HD	O	This pin is affected by the SSG_DELAY (register).
37	VD	O	This pin is affected by the SSG_DELAY (register).
38	FLD	O	This pin is affected by the SSG_DELAY (register). Outputs a video output frame index pulse in long exposure mode.
39	IREF1	I	Automatic iris and AGC hold; 1: Hold, 0: Active
40	$V_{SS}6$ (DATA)		
41	$V_{DD}6$ (DATA)		
42	IREF2	I	Automatic iris fine adjustment; 1: Bright, 0: Normal
43	VREFIN	I	D/A converter reference voltage input
44	$V_{DD}5$ (DAC-A)		
45	$V_{SS}5$ (DAC-A)		
46	VIDEO	O	D/A converter output (video output)
47	COMP	O	D/A converter bias pin
48	IREFOUT	O	D/A converter reference voltage output
49	$V_{SS}4$ (DAC-D)		
50	$V_{DD}4$ (DAC-D)		

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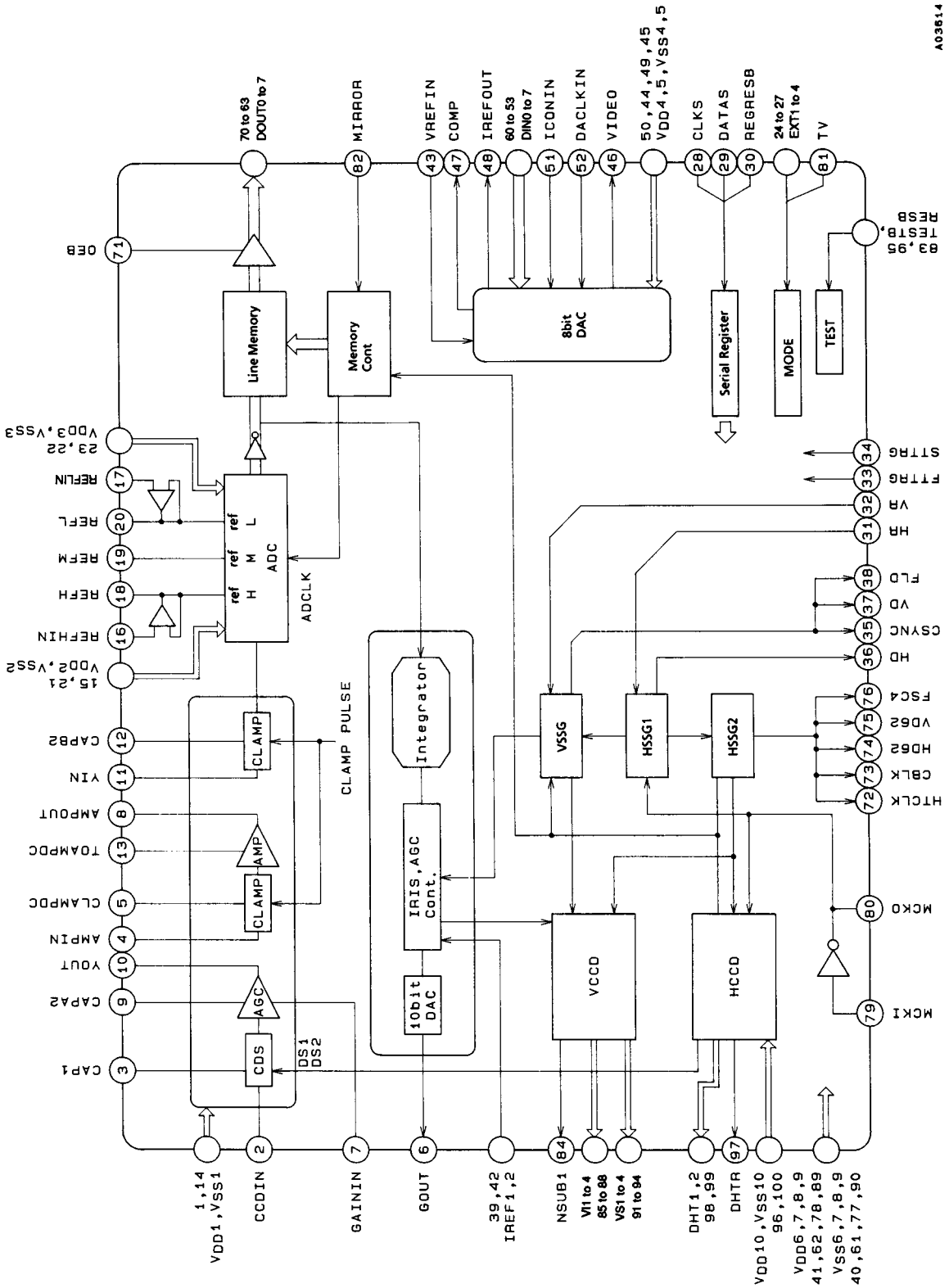
I/O → I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

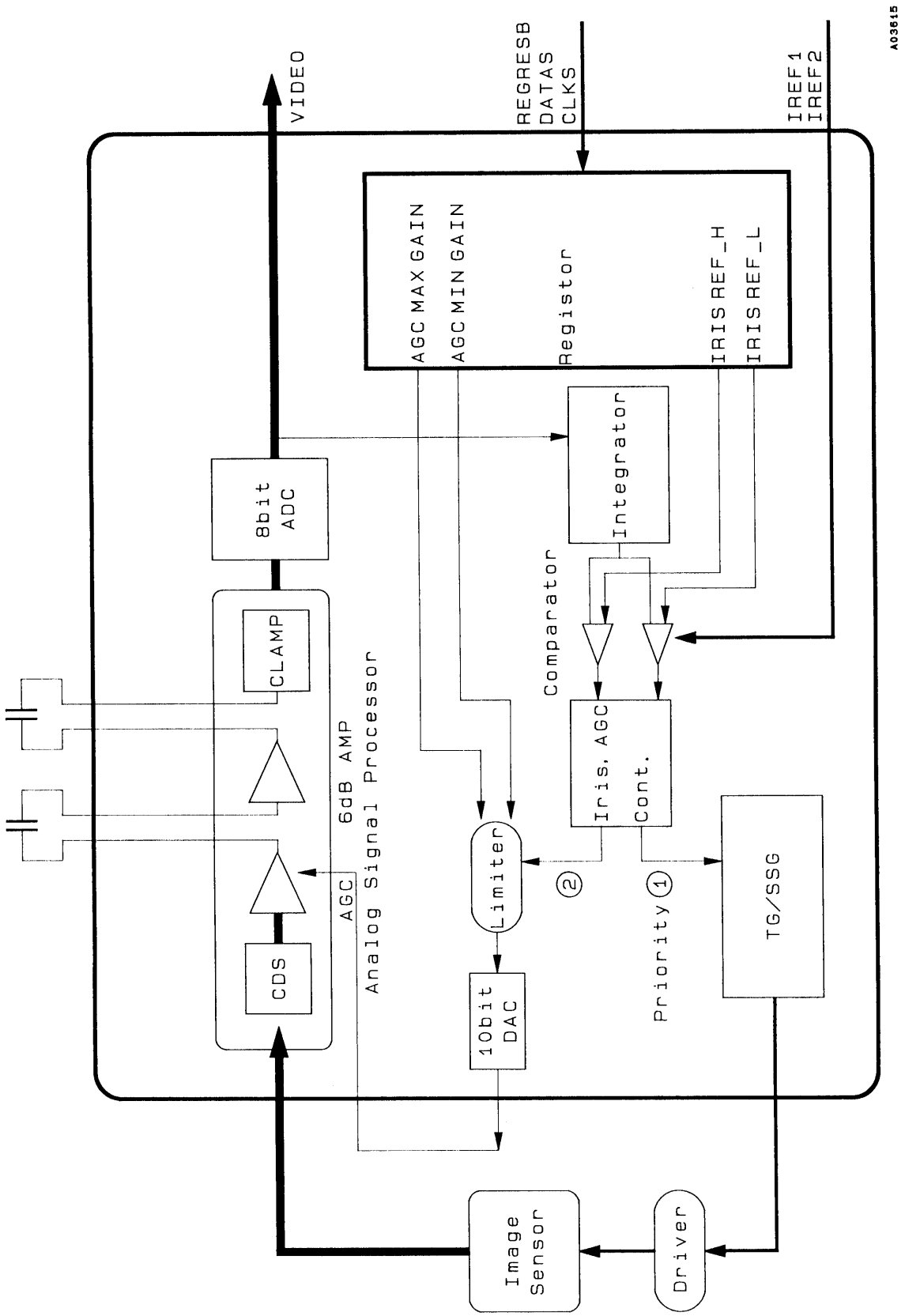
Pin No.	Symbol	I/O	Function
51	ICONIN	I	D/A converter current offset control pulse
52	DACLKIN	I	D/A converter clock
53	DIN7	I	D/A converter digital input (MSB) (positive polarity)
54	DIN6	I	D/A converter digital input
55	DIN5	I	D/A converter digital input
56	DIN4	I	D/A converter digital input
57	DIN3	I	D/A converter digital input
58	DIN2	I	D/A converter digital input
59	DIN1	I	D/A converter digital input
60	DIN0	I	D/A converter digital input
61	$V_{SS}7$ (SSG)		
62	$V_{DD}7$ (SSG)		
63	DOUT7	O	A/D converter digital output (MSB) (positive polarity). Affected by the MIRROR pin.
64	DOUT6	O	D/A converter digital output
65	DOUT5	O	D/A converter digital output
66	DOUT4	O	D/A converter digital output
67	DOUT3	O	D/A converter digital output
68	DOUT2	O	D/A converter digital output
69	DOUT1	O	D/A converter digital output
70	DOUT0	O	D/A converter digital output
71	OEB	I	Output enable pin for DOUT0 to DOUT7; 0: Active, 1: High impedance
72	HTCLK	O	Latch clock for DOUT0 to DOUT7
73	CBLK	O	Composite blanking pulse
74	HD62	O	For use with an LC99062 (Not affected by the SSG_Delay register.)
75	VD62	O	For use with an LC99062 (Not affected by the SSG_Delay register.)
76	FSC4	O	MCK/2 clock out
77	$V_{SS}8$ (SSG)		
78	$V_{DD}8$ (SSG)		
79	MCKI	I	Master clock input
80	MCKO	O	
81	TV	I	0: NTSC, 1: PAL
82	MIRROR	I	0: Normal, 1: Mirror
83	TESTB	I	Test pin; 0: Test, 1: Real
84	NSUB1	O	CCD NSUB drive pulse
85	VI1	O	CCD image area drive pulse
86	VI3	O	CCD image area drive pulse
87	VI2	O	CCD image area drive pulse
88	VI4	O	CCD image area drive pulse
89	$V_{DD}9$ (VCCD)		
90	$V_{SS}9$ (VCCD)		
91	VS4	O	CCD storage area drive pulse
92	VS1	O	CCD storage area drive pulse
93	VS2	O	CCD storage area drive pulse
94	VS3	O	CCD storage area drive pulse
95	RESB	I	Test reset pin; 0: Test, 1: Real
96	$V_{DD}10$ (HCCD)		
97	DHTR	O	Reset gate pulse for output buffer (FDA)
98	DHT1	O	CCD horizontal register drive pulse
99	DHT2	O	CCD horizontal register drive pulse
100	$V_{SS}10$ (HCCD)		

Note: All V_{DD} and V_{SS} pins must be connected to power or ground; do not leave any of these pins unconnected.

Block Diagram



Iris, AGC Block



Main Functions Provided by the LC99052-V64A

1. SSG
   - Handles both the NTSC and PAL formats.
   - The NTSC reference clock is 8Fsc = 28.63636 MHz.
   - The PAL reference clock is 28.375 MHz.
     However, the LC99052-V64A does not generate a 4Fsc clock. 4Fsc is not required when an LC99062-W50 is used.
   - The SSG delay with respect to the TG phase can be set to an arbitrary value to compensate for the delay in the digital signal processing connected to the last stage.
   - Handles external synchronization. Includes a sync separator circuit that separates HSYNC and VSYNC from C.SYNC.

2. TG
   - Generates all pulses required to drive Sanyo CCD products (LC9947G/48G/97G/98G).
   - Supports interlaced and non-interlaced drive.
   - Handles long exposure drive (1 V to 16 V).
   - External exposure time control can be implemented easily.

3. Electronic Iris
   - Incorporates, as digital circuits, all circuits required for electronic iris (exposure control using an electronic shutter function), including video signal integration, detector, and exposure control circuits. Allows stabilized control.
   - Response speed and rate are settable.
   - Five light metering patterns are supported.
     — Full-screen light metering, center area light metering, lower-side light metering
     — Center-weighted metering with three areas measured
     — Lower-side-weighted metering with three areas measured
   - Handles long exposure times.

4. CDS (coefficient dual-sampling circuit)
   - Hold capacitor built in
   - Adjustment-free

5. AGC Amplifier Circuit
   - Adjustment-free
   - The AGC control signals are generated by a digital control system linked to the electronic iris and a built-in 10-bit D/A converter. The gain can be set with digital codes.
   - The gain variability is 10 dB. The maximum gain is about 20 dB when the built-in 6 dB amplifier is not used.

6. A/D Converter
   - After CDS, AGC, and OPB clamp processing has been applied to the CCD imaged signal, the A/D converter converts that signal to an 8-bit digital signal.
   - Built-in OPB clamp circuit in the front end.
   - Built-in operational amplifier for reference voltage generation. The reference voltage can be resistor divided to provide any required voltage. Note that black level adjustment is not required since the same voltage is used as the reference voltage and as the front end clamp circuit bias voltage.

7. Line Memory
   - Mirror processing (left-to-right reversal) is supported by setting a single external pin.
   - The digital image output can be freely delayed with respect to the CCD drive. This function allows the 8-bit D/A converter output timing to be set to the same phase as the CCD drive to prevent pulse interference in the video period without affecting the external digital signal processing delay time.

8. D/A Converter
   - The D/A converter processes 8-bit video signals, either from the A/D converter or from external digital signal processing systems.
   - Can provide a 2 Vp-p output.
   - Can add synchronization even for full 8-bit (0 to 255) video signals that do not include a synchronization signal by accepting a CSYNC pulse input.

9. Other Functions
   - Two-pin serial interface for setting register values
   - Stand-alone operation is possible. All adjustments and settings can be performed from external inputs, even in stand-alone mode.