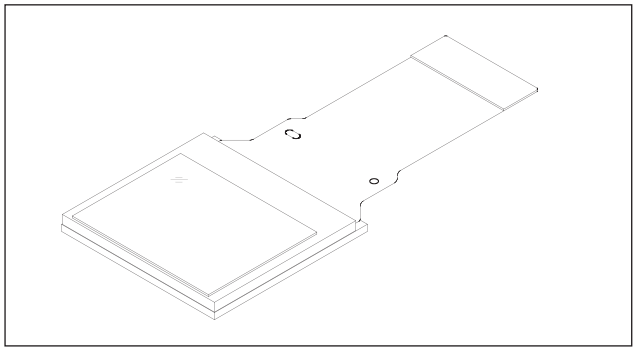
SONY

LCX020BK

1.8cm (0.7-inch) Color LCD Panel



Description

The LCX020BK is a 1.8cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel provides full-color representation. RGB dots are arranged in a striped pattern optimum for data applications and capable of displaying fine text and vertical lines.

The adoption of an advanced on-chip black matrix realizes a high luminance screen, and high picture quality is possible with built-in cross talk free and ghost free circuits.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. In addition, the built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains a display area varying circuit which supports Macintosh16*1/SVGA/VGA/PC98*2 data signals by changing the display area according to the type of input signal. In addition, double-speed processed NTSC/PAL/WIDE can also be supported.

*1 "Macintosh" is a trademark of Apple Company Inc.
*2 "PC98" is a trademark of NEC.

Features

- Number of active dots: 1,557,000, 1.8cm (0.7-inch) in diagonal
- Supports Macintosh16 (832 × 624), SVGA (800 × 600), VGA (640 × 480) and PC98 (640 × 400) display
- Supports NTSC (640 × 480), PAL (762 × 572) and WIDE (832 × 480) display by processing the video signal at double speed
- High optical transmittance: 1% (typ.)
- Built-in cross talk free circuit
- High contrast ratio with normally white mode: 70 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function

Element Structure

- Dots: 2496 (H) × 624 (V) = 1,557,504
- Built-in peripheral driving circuit using polycrystalline silicon super thin film transistors

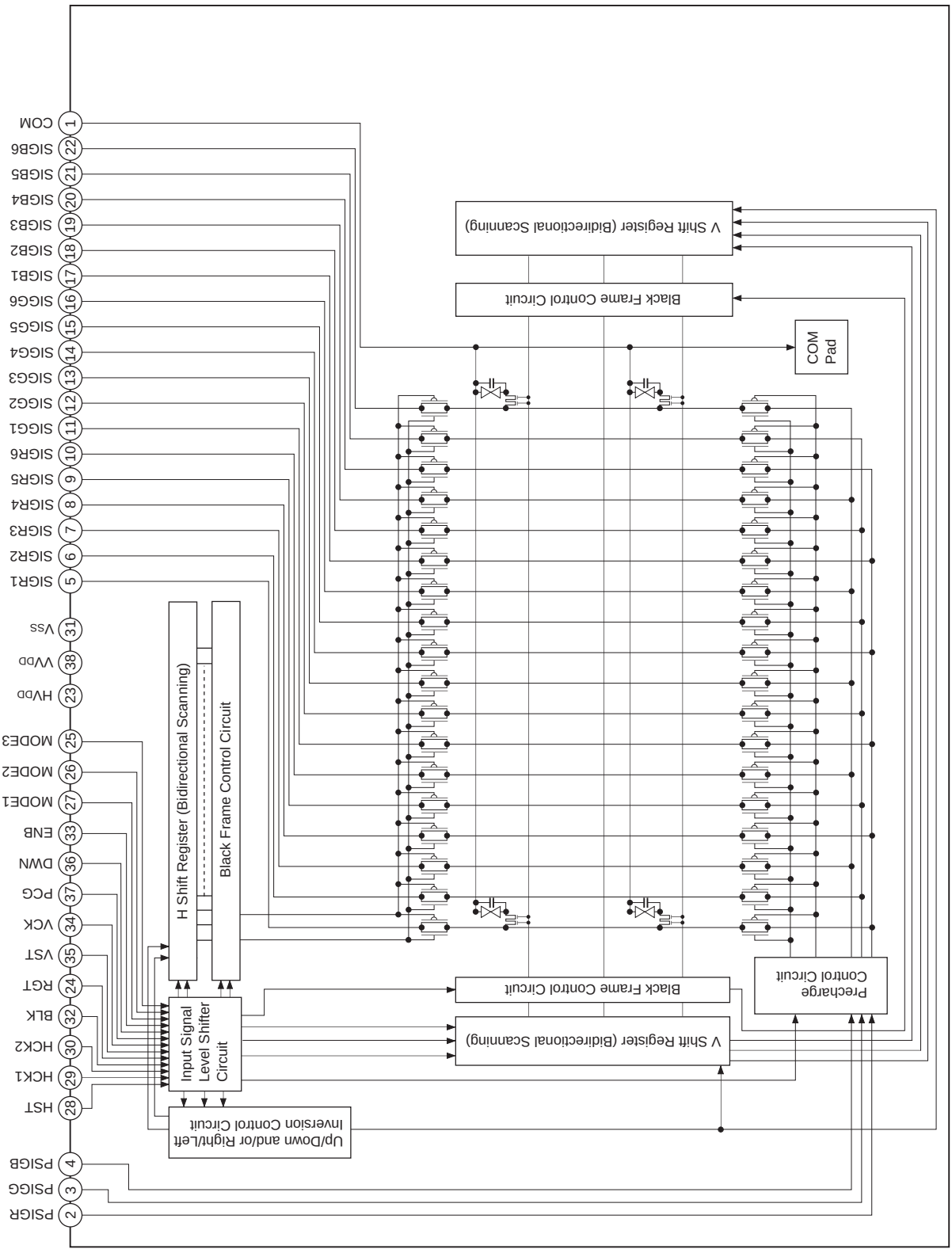
Applications

- Liquid crystal EVFs for personal PCs/DVDs
- Small monitors, etc.

E99210-PS

Block Diagram

The Block Diagram of the panel is shown below.



Absolute Maximum Ratings (Vss = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Common pad voltage	COM	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG, BLK, ENB, DWN MODE1, MODE2, MODE3	–1.0 to +17	V
• Video signal input pin voltage	SIGR1 to SIGR6, SIGG1 to SIGG6, SIGB1 to SIGB6, PSIGR, PSIGG, PSIGB	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (Vss = 0V)

• Supply voltage

HV_{DD} 15.5 ± 0.3V

VV_{DD} 15.5 ± 0.3V

• Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

Vin 5.0 ± 0.5V

Pin Description

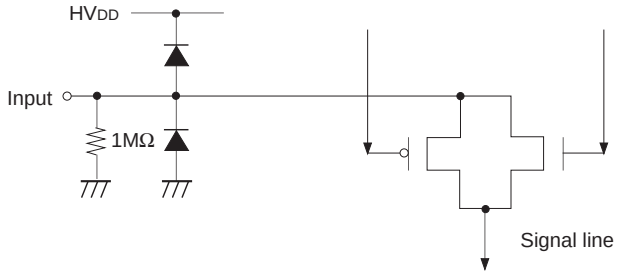
Pin No.	Symbol	Description
1	COM	Common voltage of panel
2	PSIGR	Uniformity improvement signal input (R)
3	PSIGG	Uniformity improvement signal input (G)
4	PSIGB	Uniformity improvement signal input (B)
5	SIGR1	Video signal input to panel (R-1)
6	SIGR2	Video signal input to panel (R-2)
7	SIGR3	Video signal input to panel (R-3)
8	SIGR4	Video signal input to panel (R-4)
9	SIGR5	Video signal input to panel (R-5)
10	SIGR6	Video signal input to panel (R-6)
11	SIGG1	Video signal input to panel (G-1)
12	SIGG2	Video signal input to panel (G-2)
13	SIGG3	Video signal input to panel (G-3)
14	SIGG4	Video signal input to panel (G-4)

Pin No.	Symbol	Description
15	SIGG5	Video signal input to panel (G-5)
16	SIGG6	Video signal input to panel (G-6)
17	SIGB1	Video signal input to panel (B-1)
18	SIGB2	Video signal input to panel (B-2)
19	SIGB3	Video signal input to panel (B-3)
20	SIGB4	Video signal input to panel (B-4)
21	SIGB5	Video signal input to panel (B-5)
22	SIGB6	Video signal input to panel (B-6)
23	HV_{DD}	Power supply input for H driver
24	RGT	Drive direction input for H shift register (H: normal, L: reverse)
25	MODE3	Display area switching 3 input
26	MODE2	Display area switching 2 input
27	MODE1	Display area switching 1 input
28	HST	Start pulse input for H shift register drive
29	HCK1	Clock pulse input for H shift register drive
30	HCK2	Clock pulse input for H shift register drive
31	V_{SS}	GND (H, V drivers)
32	BLK	Black frame display pulse input
33	ENB	Gate selection pulse enable input
34	VCK	Clock pulse input for V shift register drive
35	VST	Start pulse input for V shift register drive
36	DWN	Drive direction input for V shift register (H: normal, L: reverse)
37	PCG	Uniformity improvement pulse input
38	VV_{DD}	Power supply input for V driver
39	SOUT	H and V shift register drive checking (Test pin; no connection.)

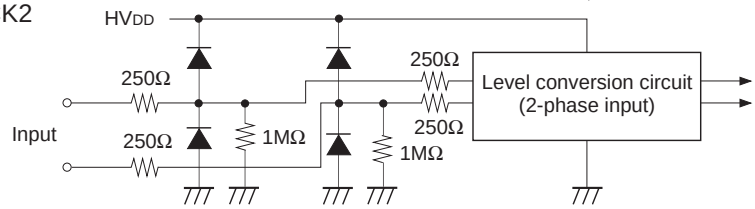
Input Equivalent Circuits

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except video signal inputs. All pins are connected to Vss with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistor value: typ.)

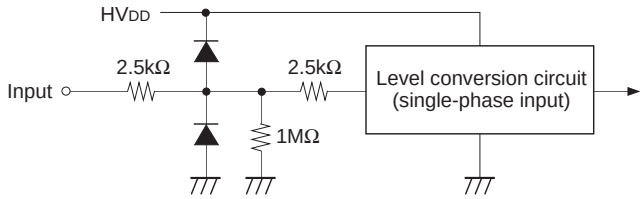
(1) SIGR1 to SIGR6, SIGG1 to SIGG6, SIGB1 to SIGB6, PSIGR, PSIGG, PSIGB



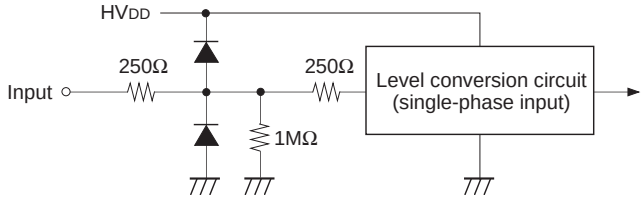
(2) HCK1, HCK2



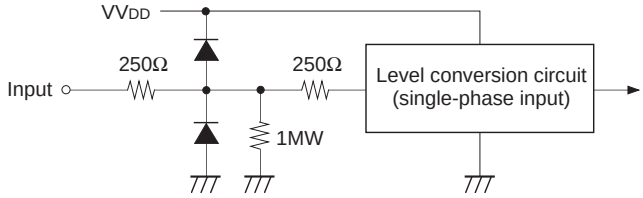
(3) RGT, MODE1, MODE2, MODE3



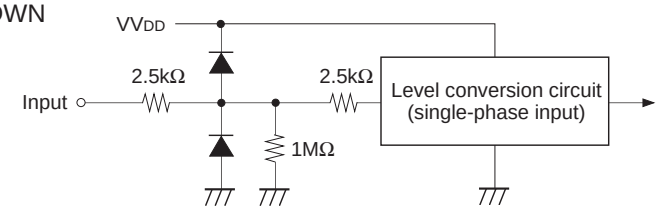
(4) HST



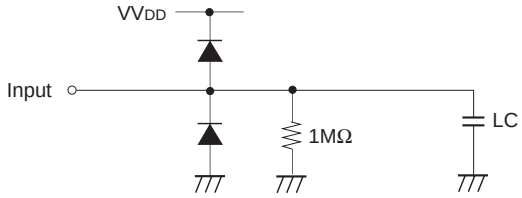
(5) PCG, VCK



(6) VST, BLK, ENB, DWN



(7) COM



Input Signals

1. Input signal voltage conditions (Vss = 0V)

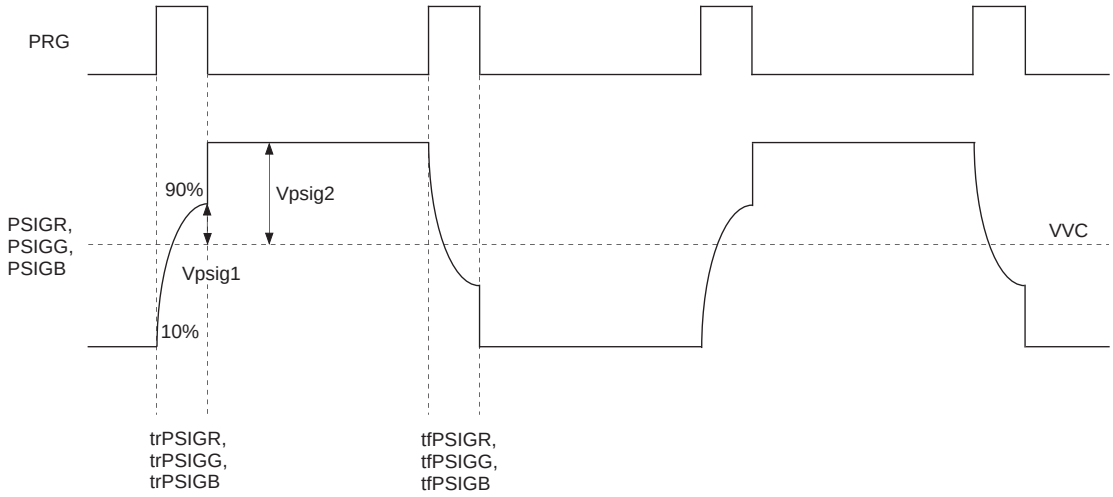
Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK1, HCK2, RGT	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage MODE1, MODE2, MODE3, BLK, VST, VCK, PCG, ENB, DWN	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	6.9	7.0	7.1	V
Video signal input range*1		Vsig	VVC – 4.5	7.0	VVC + 4.5	V
Common pad voltage of panel*2		Vcom	VVC – 0.5	VVC – 0.4	VVC – 0.3	V
Uniformity improvement signal input voltage (PSIGR, PSIGG, PSIGB)*3		Vpsig1	VVC ± 2.0	VVC ± 3.0	VVC ± 4.0	V
		Vpsig2	VVC ± 4.0	VVC ± 4.5	VVC ± 4.6	V

*1 Video input signal shall be symmetrical to VVC.

*2 The optimum typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value. When the typical value is lowered, the maximum and minimum values may lower.

*3 Input a uniformity improvement signals PSIGR, PSIGG and PSIGB in the same polarity with video signals SIGR1 to 6, SIGG1 to 6 and SIGB1 to 6 and which is symmetrical to VVC. PSIGR, PSIGG and PSIGB have two steps as shown by the waveform in the figure below, and in the table above, the upper value indicates the signal level of the first step, and the lower value, the signal level of the second step.
Here, the rising and falling of PSIGR, PSIGG and PSIGB are synchronized with the rising of PCG pulse, and the rise and fall times trPSIGR, trPSIGG, trPSIGB, tfPSIGR, tfPSIGG and tfPSIGB are suppressed within 800ns.

Input waveform of uniformity improvement signal PSIG



LCX020BK level conversion circuit

The LCX020BK has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The Vcc of external ICs are applicable to 5 ± 0.5V.

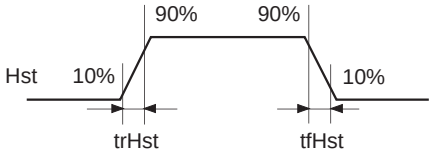
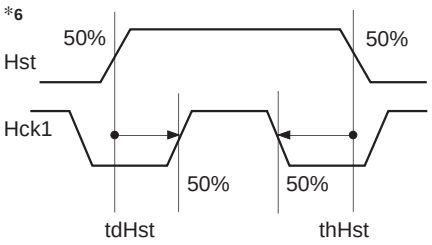
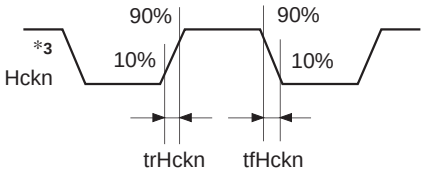
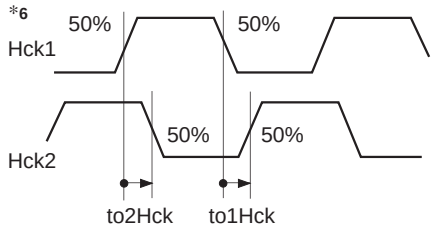
2. Clock timing conditions (Ta = 25°C) (Macintosh16 mode: fHckn = 4.8MHz, fVck = 24.9kHz)

	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data setup time	tdHst	70	80	90	
	Hst data hold time	thHst	15	25	35	
HCK	Hckn rise time*4	trHckn	—	—	30	
	Hckn fall time*4	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data setup time	tdVst	5	10	15	µs
	Vst data hold time	thVst	5	10	15	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Vck rise/fall to Enb rise time	toEnb	400	500	—	
	Horizontal video period end to Enb fall time	tdEnb	900	1000	—	
	Enb fall to Pcg rise time	toPcg	900	1000	—	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Pcg rise to Prg rise time	toPrgr	0	—	—	
	Pcg fall to Prg fall time	toPrgf	200	250	—	
	Pcg rise to Vck rise/fall time	toVck	0	1000	1100	
	Pcg pulse width	twPcg	1100	1200	1300	
BLK*5	Blk rise time	trBlk	—	—	100	
	Blk fall time	tfBlk	—	—	100	
	Blk fall to Vst rise time	toVst	1	—	2	line
	Blk pulse width	twBlk	1	—	—	

*4 Hckn means Hck1 and Hck2.

*5 Blk is the timing during SVGA mode (fHckn = 4.0MHz, fVck = 24.0kHz).
This pulse is positive polarity other than in Macintosh16 mode. Set to L level in Macintosh16 mode.

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data setup time	tdHst		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn rise time*3	trHckn		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hckn fall time*3	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		

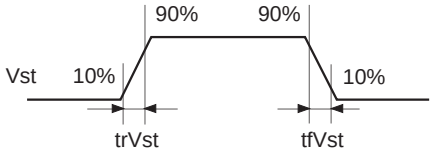
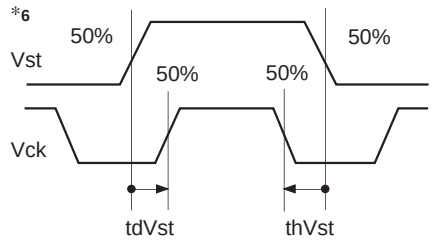
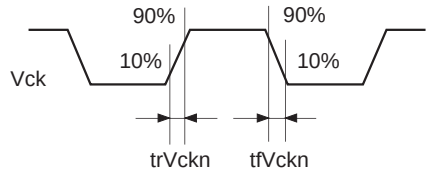
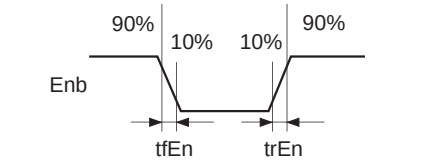
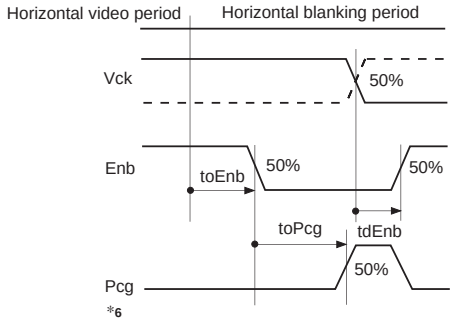
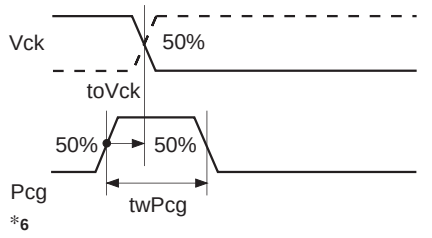
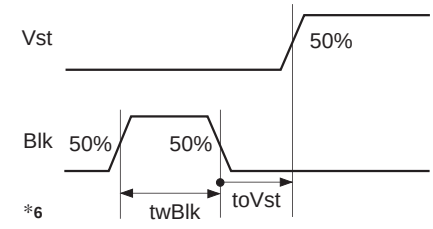
*6 Definitions:

The right-pointing arrow (•→) means +.

The left-pointing arrow (←•) means –.

The black dot at an arrow (•) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data setup time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Vck rise/fall to Enb rise time	toEnb		
	Horizontal video period end to Enb fall time	tdEnb		
	Enb fall to Pcg rise time	toPcg		
PCG*7	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg rise to Vck rise/fall time	toVck		
	Pcg pulse width	trPcg		
BLK	Blk rise time	twBlk		
	Blk fall time	tfBlk		
	Blk fall to Vst rise time	toVst		
	Blk pulse width	twBlk		

*7 Input the pulse obtained by taking the OR of the above pulses and BLK to the PCG input pin.

Electrical Characteristics (Ta = 25°C, HV_{DD} = 15.5V, VV_{DD} = 15.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	HCKn	CHckn	—	8	13	pF	
	HST	CHst	—	8	13	pF	
Input pin current	HCK1		–500	–110	—	µA	HCK1 = GND
	HCK2		–1000	–350	—	µA	HCK2 = GND
	HST		–500	–180	—	µA	HST = GND
	RGT		–150	–30	—	µA	RGT = GND
Video signal input pin capacitance		Csig	—	150	270	pF	
Current consumption		IH	—	16.0	30.0	mA	HCKn: HCK1, HCK2 (4.8MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	VCK	CVck	—	8	13	pF	
	VST	CVst	—	8	13	pF	
Input pin current	VCK		–1000	–160	—	µA	VCK = GND
PCG, VST, ENB, DWN, BLK, MODE1, MODE2, MODE3			–150	–30	—	µA	PCG, VST, ENB, DWN, BLK, MODE1, MODE2, MODE3 = GND
Current consumption		IV	—	3.0	5.0	mA	VCK: (24.9kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (MAC16)	PWR	—	300	600	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – Vss input resistance	Rpin	0.4	1	—	MΩ

5. Uniformity improvement signal input capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Uniformity improvement signal input capacitance	CPSIGon	—	7	16	nF

Electro-optical Characteristics (Ta = 25°C, NTSC mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR_{25}	1	40	70	—	—
		60°C	CR_{60}		40	70	—	
Optical transmittance			T	2	0.85	1.0	—	%
Chromaticity	R	X	Rx	3	0.560	0.600	0.670	CIE standards
		Y	Ry		0.300	0.360	0.410	
	G	X	Gx		0.260	0.300	0.350	
		Y	Gy		0.541	0.595	0.650	
	B	X	Bx		0.120	0.148	0.187	
		Y	By		0.040	0.148	0.187	
V-T characteristics	V_{90}	25°C	$V_{90\text{-}25}$	4	0.9	1.4	2.0	V
		60°C	$V_{90\text{-}60}$		1.0	1.6	2.2	
	V_{50}	25°C	$V_{50\text{-}25}$		1.2	1.8	2.4	
		60°C	$V_{50\text{-}60}$		1.3	1.9	2.5	
	V_{10}	25°C	$V_{10\text{-}25}$		1.9	2.4	3.0	
		60°C	$V_{10\text{-}60}$		1.8	2.3	3.0	
Half tone color reproduction range		R-G	V_{50RG}	5	—	–0.10	0.25	V
		B-G	V_{50BG}		—	0.05	0.45	
Response time	ON time	0°C	ton0	6	—	20	100	ms
		25°C	ton25		—	14	40	
	OFF time	0°C	toff0		—	45	150	
		25°C	toff25		—	35	70	
Flicker		60°C	F	7	—	—	–40	dB
Image retention time		60 min.	YT60	8	—	—	20	s

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

HV_{DD} = 15.5V, VV_{DD} = 15.5V

VVC = 7.0V, Vcom = 6.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

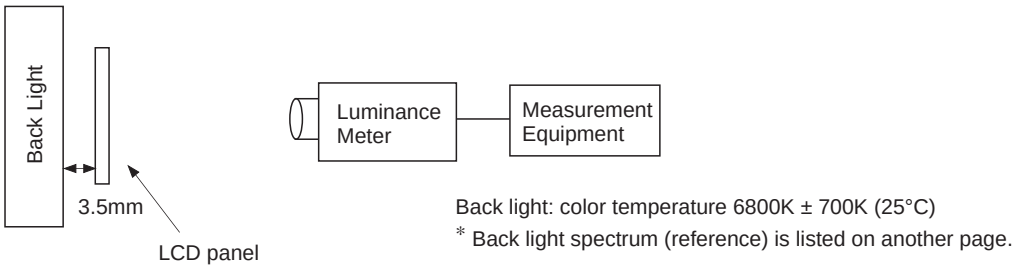
(4) Measurement systems

Two types of measurement system are used as shown below.

(5) Video input signal voltage (Vsig)

Vsig = 7.0 ± V_{AC} [V] (V_{AC} = signal amplitude)

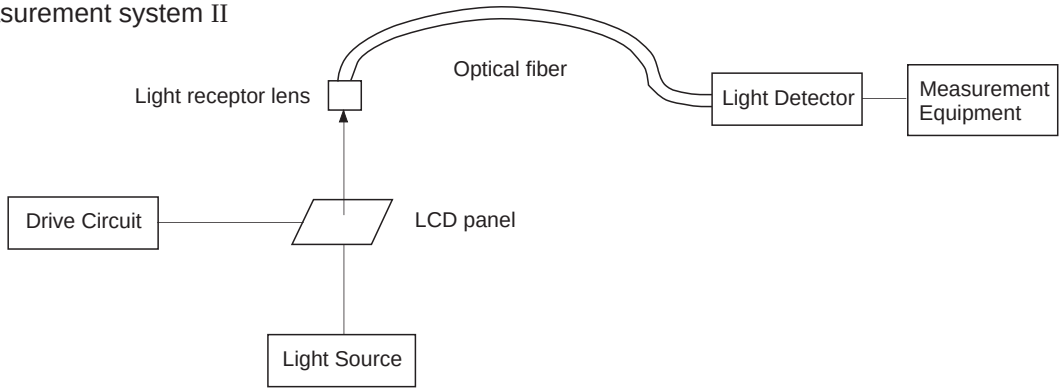
* Measurement system I



Back light: color temperature 6800K ± 700K (25°C)

* Back light spectrum (reference) is listed on another page.

* Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \quad ... (1)$$

L (White): Surface luminance of the TFT-LCD panel at the input signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the panel at V_{AC} = 4.5V.

Both luminosities are measured by System I.

2. Optical Transmittance

Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{L\ (White)}{Luminance\ of\ Back\ Light} \times 100\ [\%] \ldots (2)$$

L (White) is the same expression as defined in the "Contrast Ratio" section.
Optical transmittance is measured by System I.

3. Chromaticity

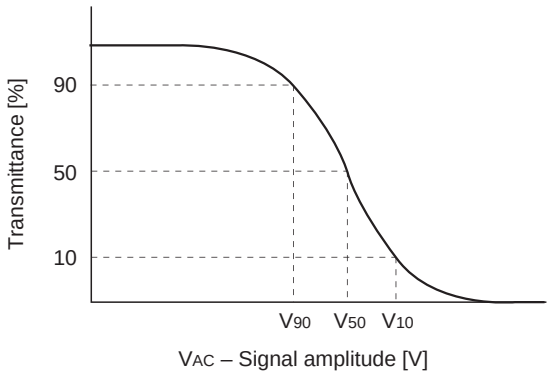
Chromaticity of the panel is measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses x and y of the CIE standards as the chromaticity here.

		Signal amplitudes (V_{AC}) supplied to each input		
		R input	G input	B input
Raster	R	0.5	4.5	4.5
	G	4.5	0.5	4.5
	B	4.5	4.5	0.5

(Unit: V)

4. V-T Characteristics

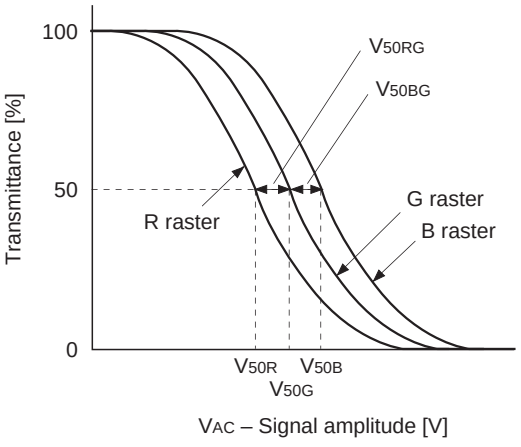
V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to each voltage which defines 90%, 50%, and 10% of transmittance respectively.



5. Half Tone Color Reproduction Range

The half tone color reproduction range of the LCD panel is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II. System II defines signal voltages of each R, G and B raster mode which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B} respectively. V_{50RG} and V_{50BG} represent the differences between V_{50R} and V_{50G} and between V_{50B} and V_{50G}, and are given by the following formulas (3) and (4) respectively.

$V_{50RG} = V_{50R} - V_{50G} \ldots (3)$
$V_{50BG} = V_{50B} - V_{50G} \ldots (4)$



6. Response Time

Response time ton and toff are defined by formulas (5) and (6) respectively.

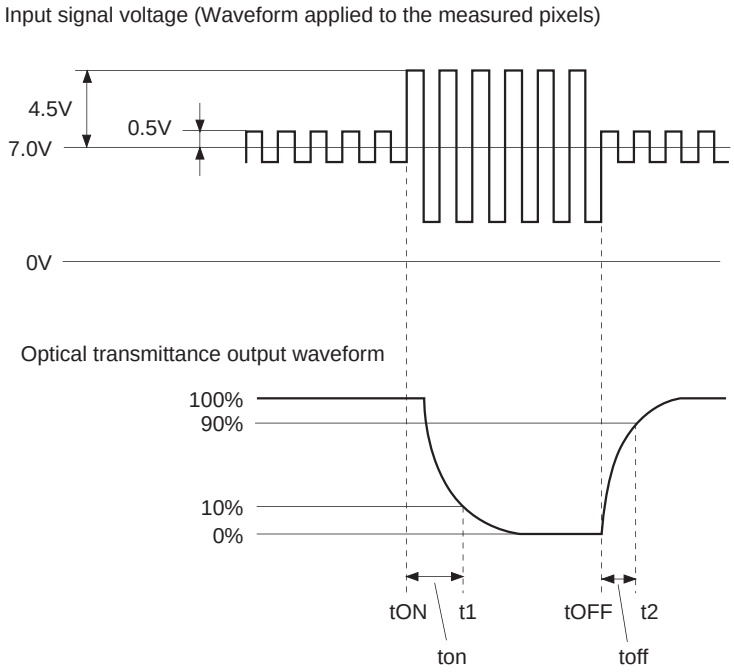
ton = t1 – tON ... (5)

toff = t2 – tOFF ... (6)

t1: time which gives 10% transmittance of the panel.

t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



7. Flicker

Flicker (F) is given by the formula (7). DC and AC (MAC16/SVGA/VGA/PC98/NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

$$F\ [dB] = 20\log \{ \frac{\text{AC component}}{\text{DC component}} \} \quad ... (7)$$

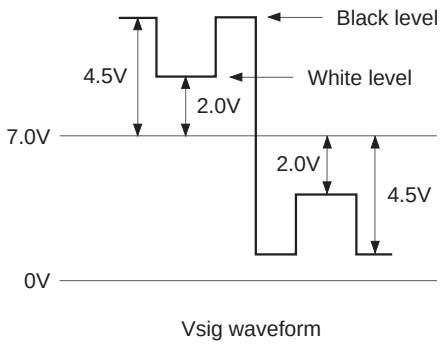
* R, G, B input signal voltage for gray raster mode is given by
Vsig = 7.0 ± V_{50} [V]
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T curve.

8. Image Retention Time

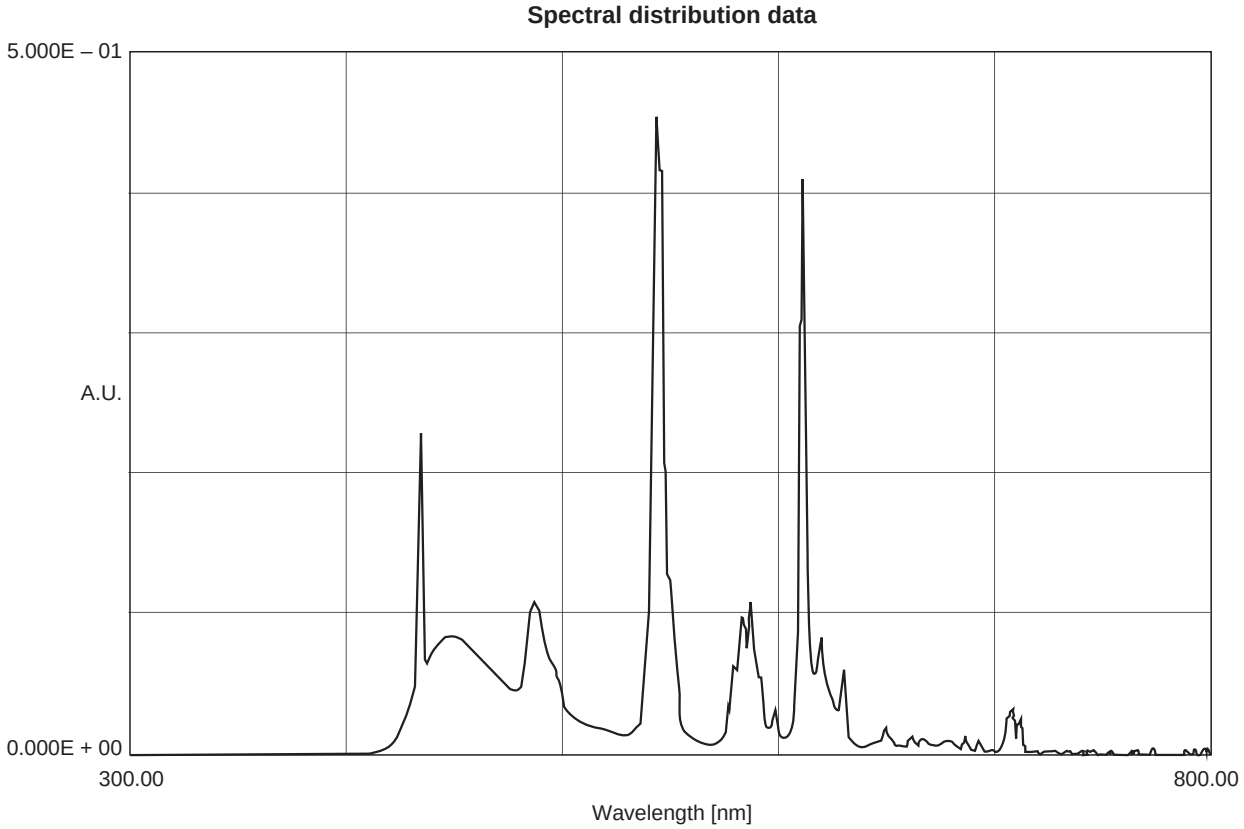
Image retention time is given by the following procedures.

Apply a monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 7.0 ± V_{AC} [V] (V_{AC}: 3 to 4V) so as to give the maximum image retention. Hold input signal V_{AC}. The time for the residual image to disappear gives the image retention time.

* Monoscope signal conditions
Vsig = 7.0 ± 4.5 or 7.0 ± 2.0 [V]
(shown in the right figure)
Vcom = 6.6V

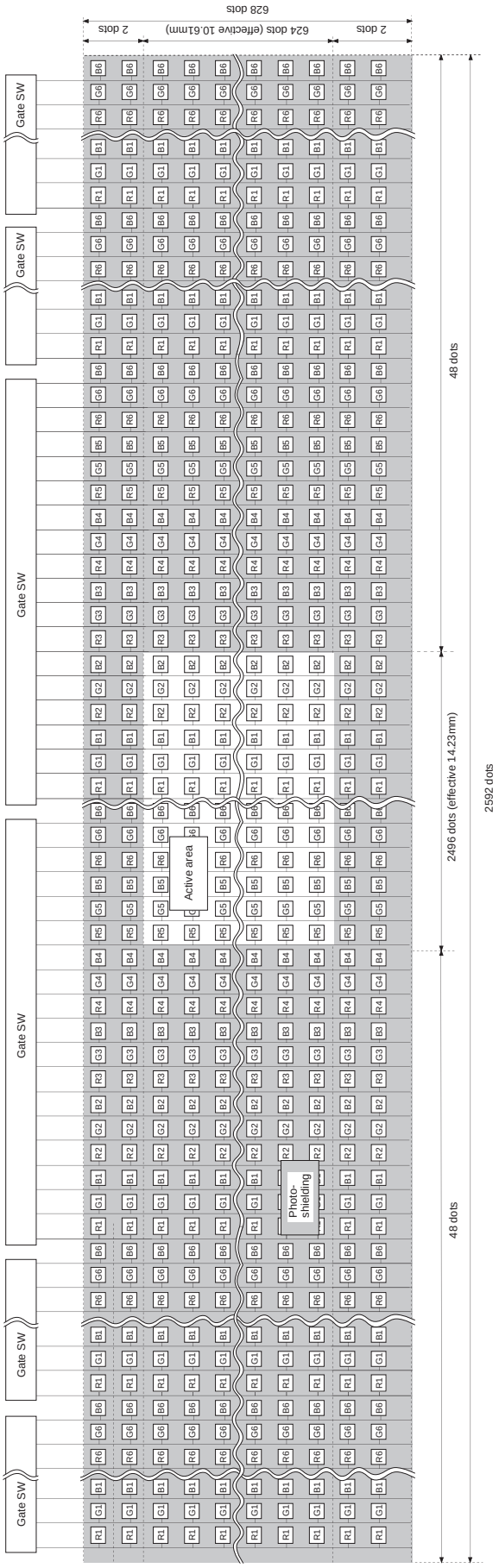


Example of Back Light Spectrum (Reference)



1. Dot Arrangement

RGB dots are arranged in a stripe pattern. The shaded area is used for the dark border around the display.



2. LCD Panel Operations

[Description of basic operations]

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 624 gate lines sequentially in every single horizontal scanning period. (in Macintosh16 mode)

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 2496 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs for one dot) turn on to apply a video signal to the dot. The same procedures lead to the entire 2496 × 832 dots to display a picture in a single vertical scanning period.

- The data and video signals shall be input with polarity-inverted system in every horizontal cycle.

[Description of operating mode]

The LCD panel can change the angle of view by displaying a black frame to support various signal systems. The angle of view is switched by MODE1, 2 and 3. However, the picture center does not change. The angle of view mode settings are shown below.

MODE1	MODE2	MODE3	Display mode
L	L	L	Macintosh16: 832 × 624
L	L	H	SVGA: 800 × 600
L	H	L	PAL: 762 × 572
L	H	H	VGA/NTSC: 640 × 480
H	L	L	PC98: 640 × 400
H	L	H	WIDE: 832 × 480

The LCD panel has the following functions to easily apply to various uses, as well as various signal systems.
- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and up/down mode settings are shown in the tables below.

RGT	Mode
H	Right scan
L	Left scan

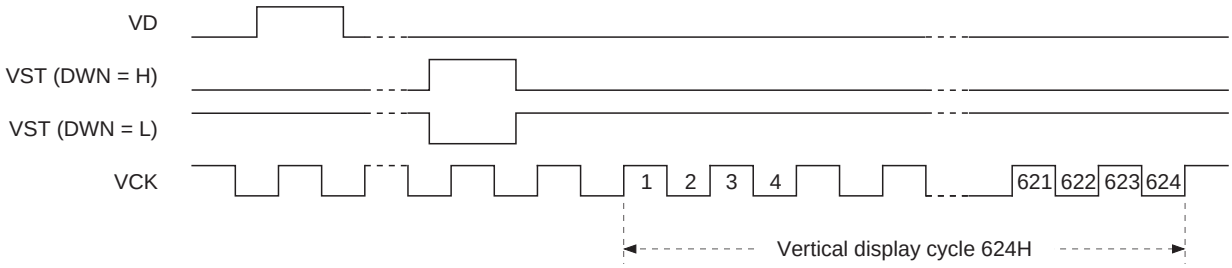
DWN	Mode
H	Down scan
L	Up scan

Right/left and up/down mean the direction when the Pin 1 marking is located at the right side with the pin block facing upward.

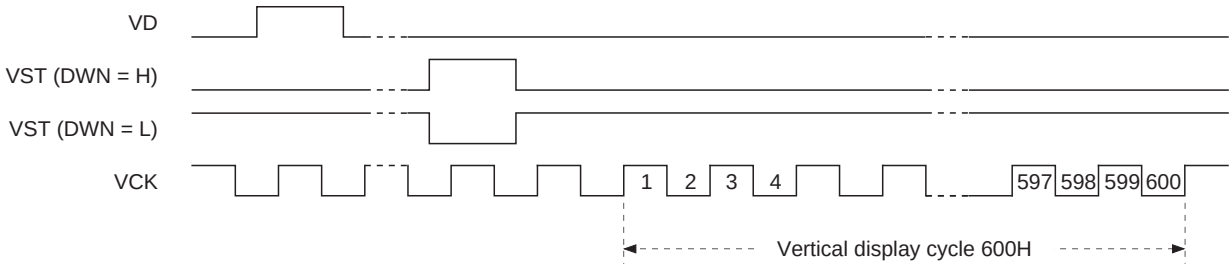
Since the display area is located in the center of the panel in each mode, the start pulse, clock phase and polarity for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown on the following pages.

(1) Vertical direction display cycle

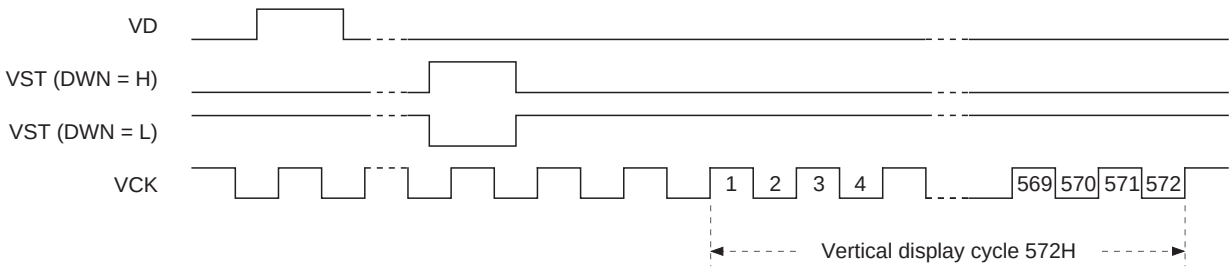
(1.1) Macintosh 16



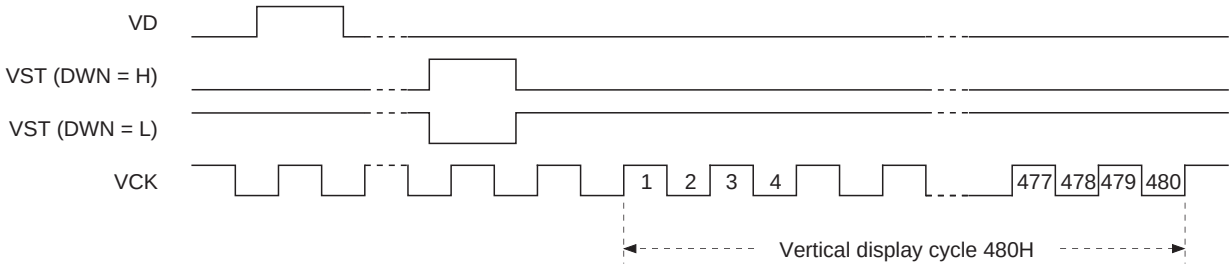
(1.2) SVGA



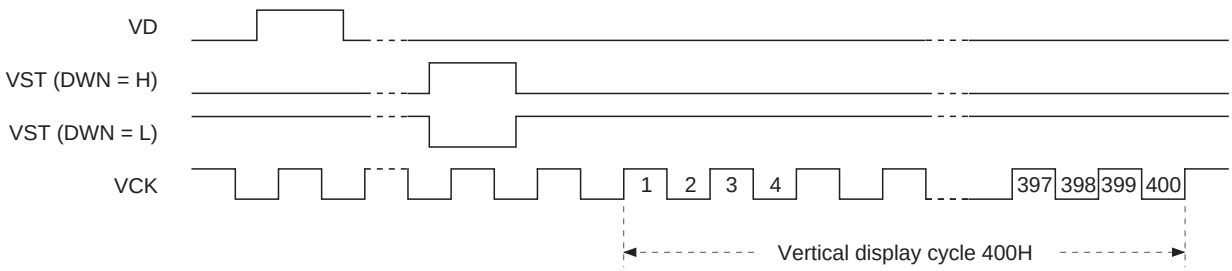
(1.3) PAL



(1.4) VGA/NTSC, WIDE

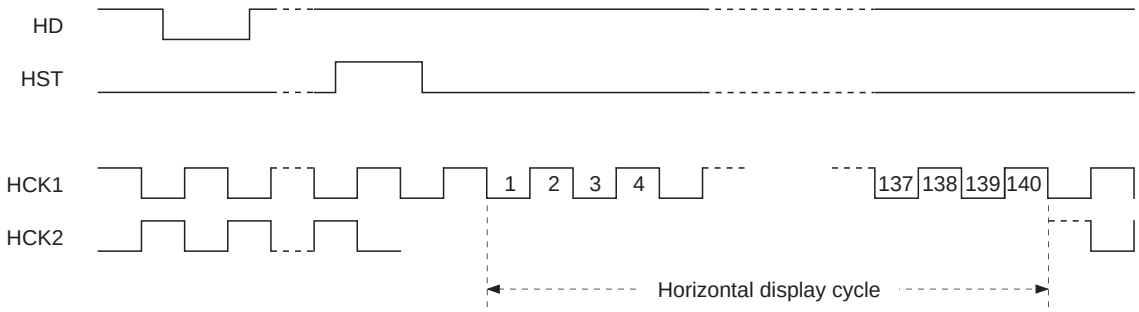


(1.5) PC98

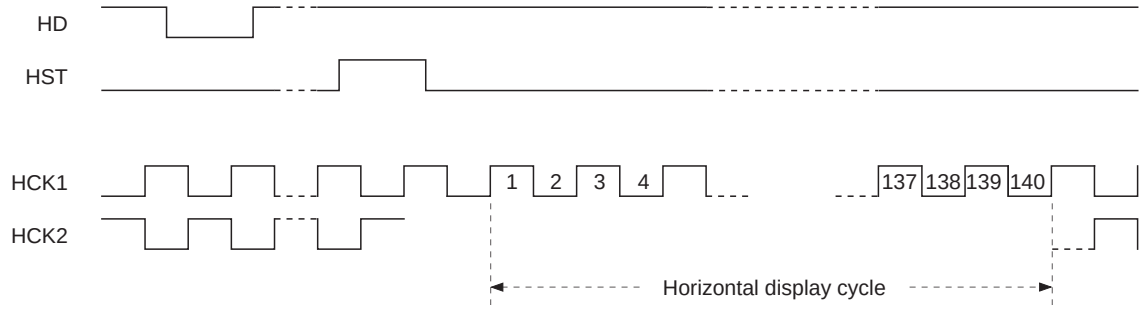


(2) Horizontal direction display cycle

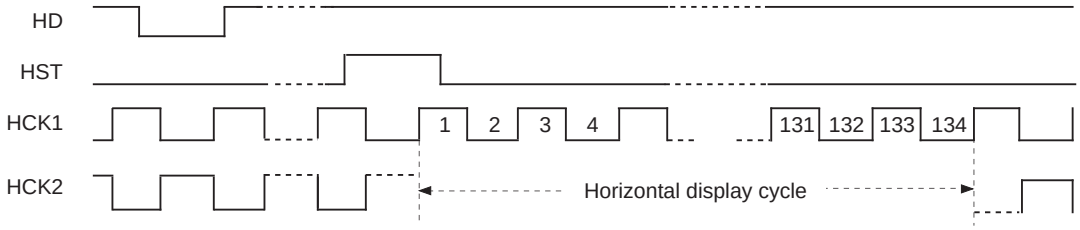
(2.1.1) Macintosh 16, WIDE, RGT = H



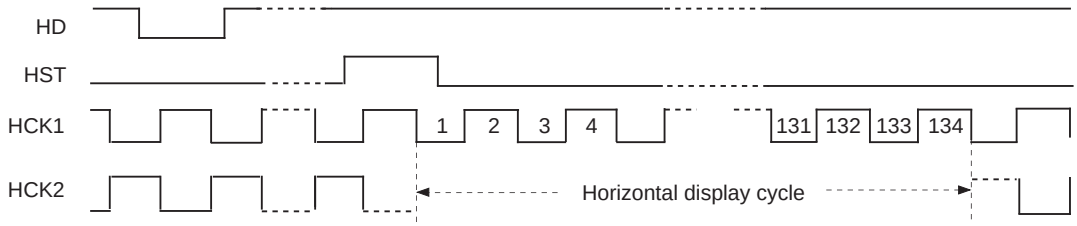
(2.1.2) Macintosh 16, WIDE, RGT = L



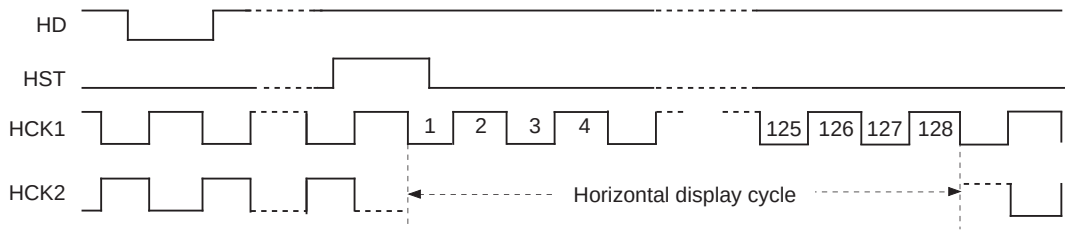
(2.2.1) SVGA, RGT = H



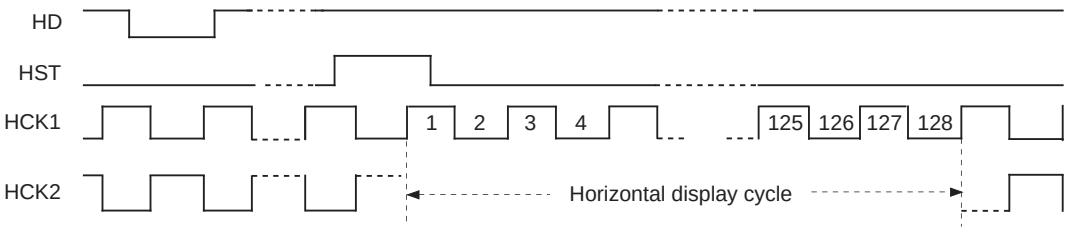
(2.2.2) SVGA, RGT = L



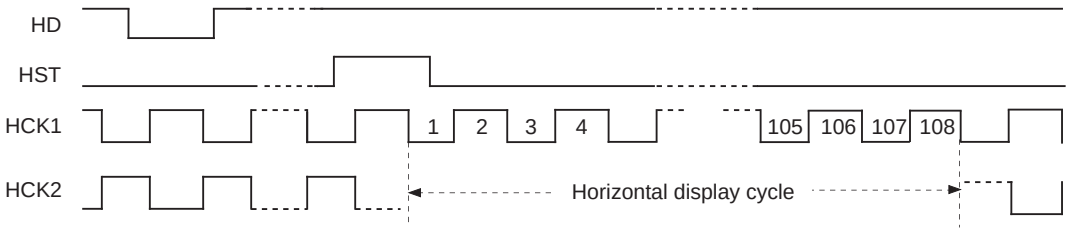
(2.3.1) PAL, RGT = H



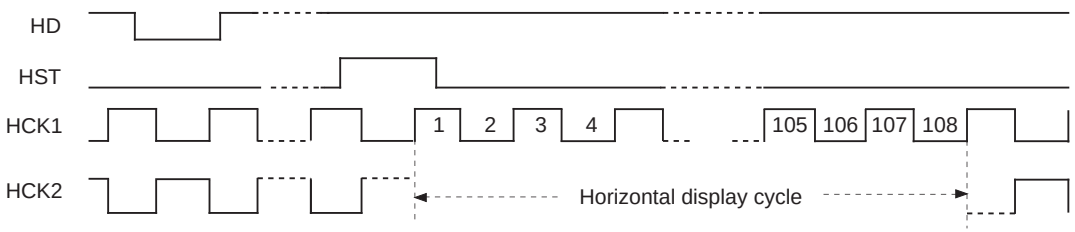
(2.3.2) PAL, RGT = L



(2.4.1) VGA/NTSC/PC98, RGT = H



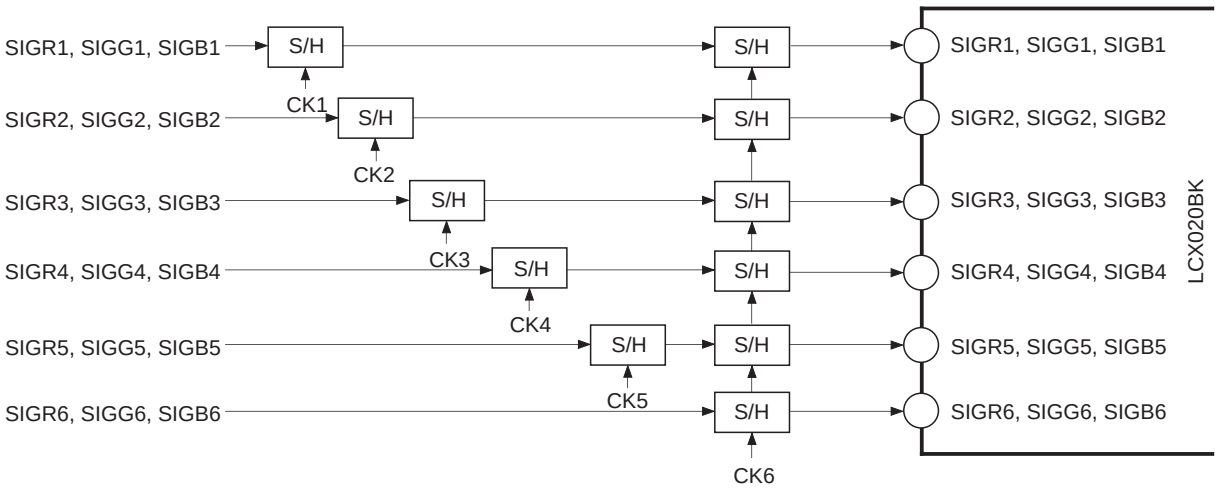
(2.4.2) VGA/NTSC/PC98, RGT = L



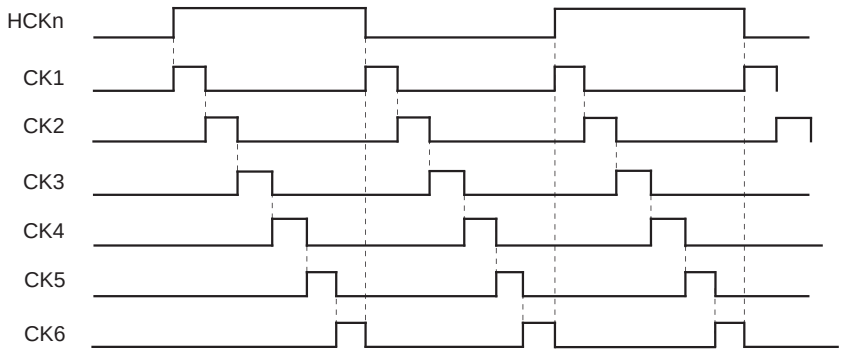
3. 18-dot Simultaneous Sampling

The horizontal shift register performs SIGR1 to SIGR6, SIGG1 to SIGG6 and SIGB1 to SIGB6 signal sampling simultaneously, which requires phase matching between each signal to prevent the horizontal resolution from deteriorating. Phase matching by an external signal delaying circuit is needed before applying video signals to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right-direction scanning (RGT = High level). For left-direction scanning (RGT = Low level), the phase settings should be inverted for the SIGR1 to SIGR6, SIGG1 to SIGG6 and SIGB1 to SIGB6 signals.

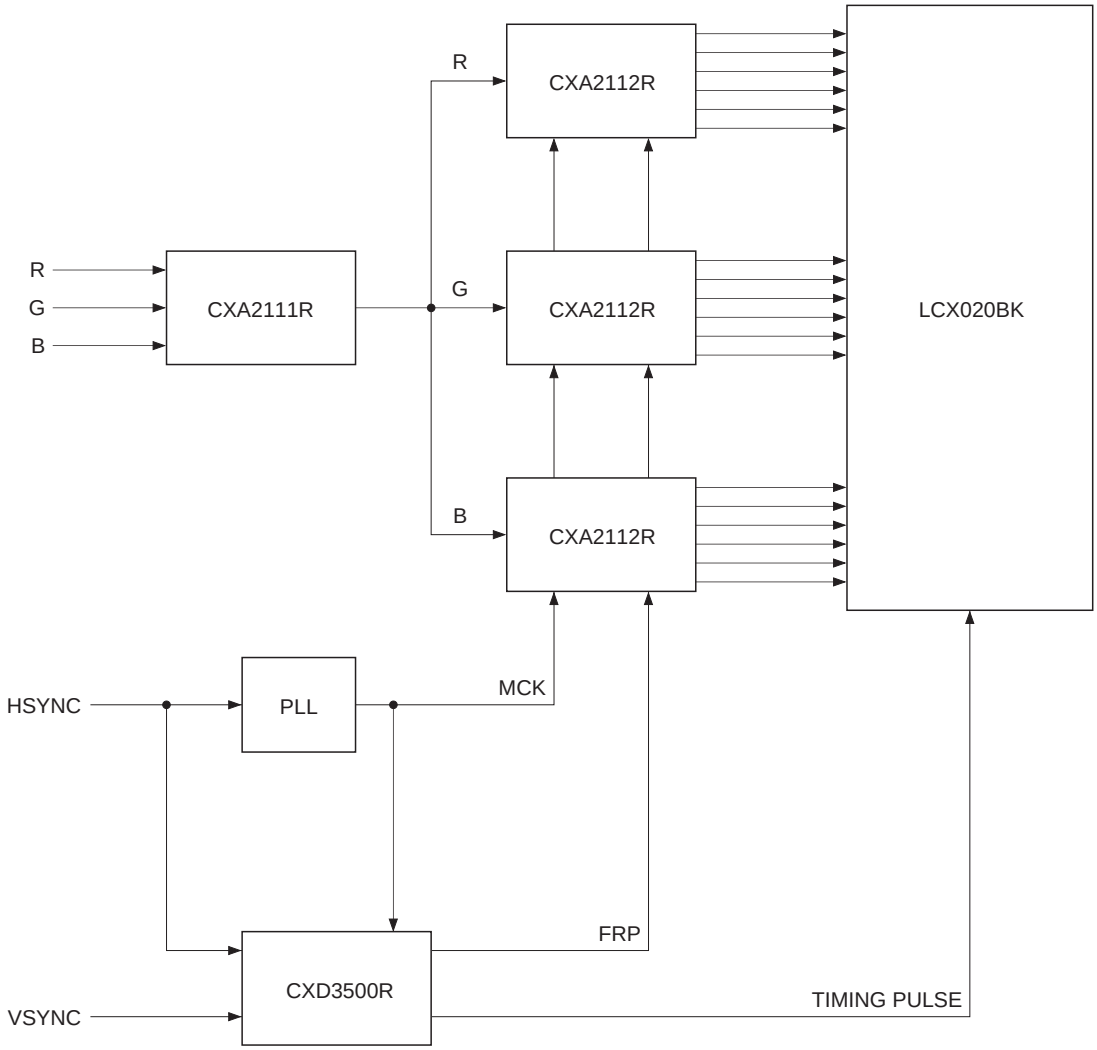


<Phase relationship of delaying sample-and-hold pulses> (right-direction scanning)



Display System Block Diagram

An example display system configuration is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

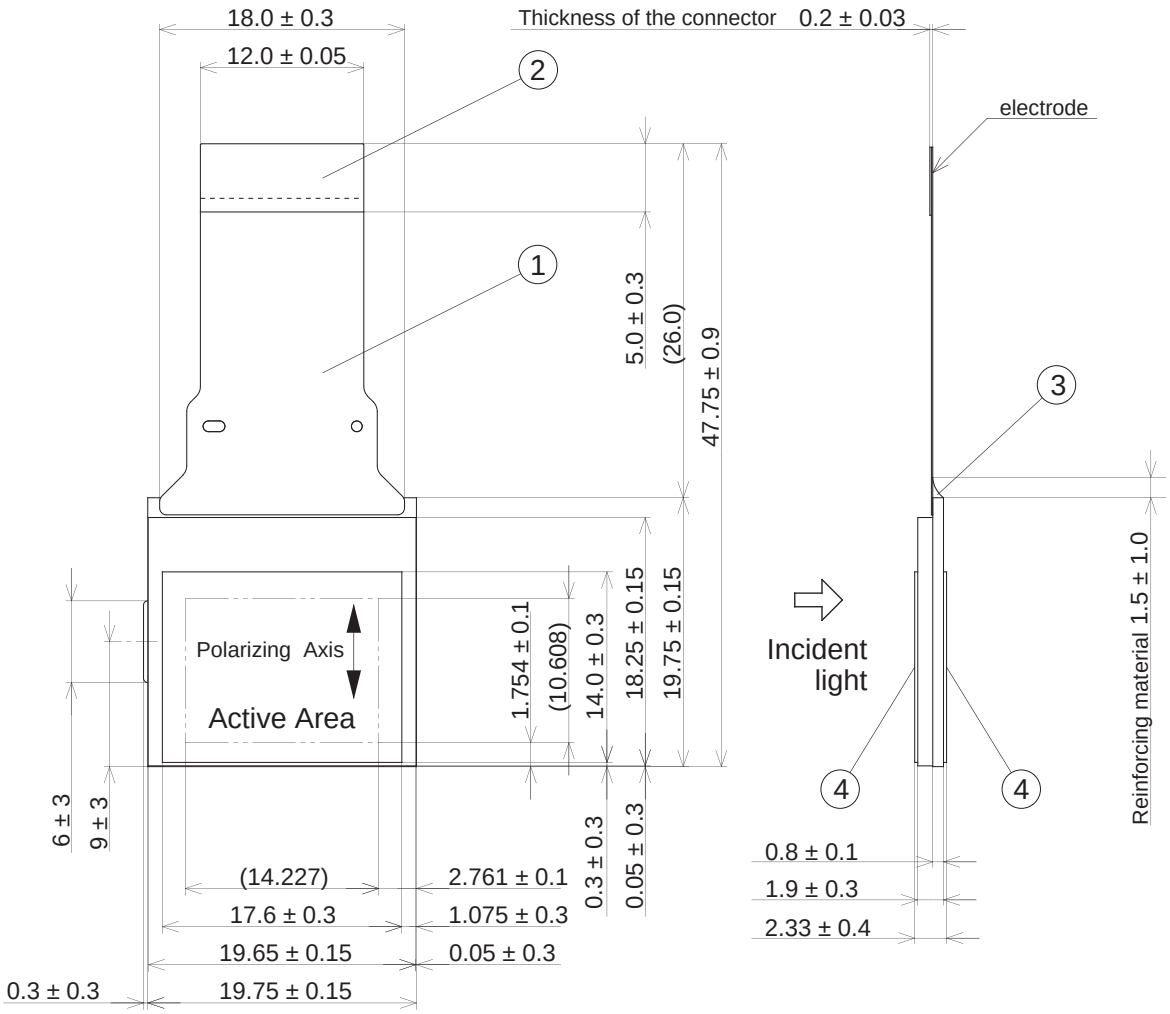
(2) Protection from dust and dust

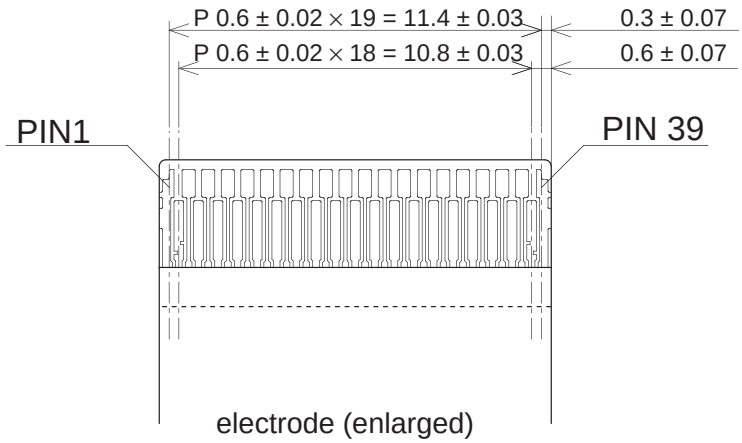
a) Operate in a clean environment.
b) When delivered, panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
c) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
d) Use ionized air to blow dust off the polarizer.

(3) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel.
c) Do not twist or bend the panel or panel frame.
d) Keep the panel away from heat sources.
e) Do not dampen the panel with water or other solvents.
f) Avoid storing or using the panel at a high temperature or high humidity, which may result in panel damages.

Package Outline Unit: mm





No	Description
1	F P C
2	Reinforcing board
3	Reinforcing material
4	Polarizing film

weight 2g