

## 2.3cm (0.9-inch) Black-and-White LCD Panel

### Description

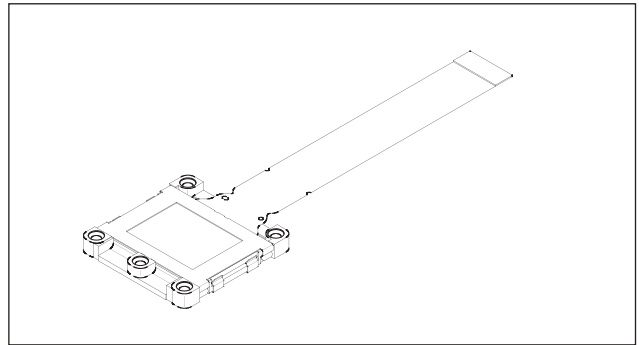
The LCX026ALF is a 2.3cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX026ALF panels provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of an advanced on-chip black matrix realizes a high luminance screen. And cross talk free circuit and ghost free circuit contribute to high picture quality.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains an active area variable circuit which supports SVGA/VGA/PC98\*1 data signals by changing the active area according to the type of input signal. In addition, double-speed processed NTSC/PAL can also be supported.

\*1 "PC98" is a trademark of NEC Corporation.



### Features

- Number of active dots: 485,000 (0.9-inch, 2.3cm in diagonal)
- Accepts the computer requirements of SVGA (804 × 604), VGA (644 × 484) and PC98 (644 × 404) platforms
- Supports NTSC (644 × 484) and PAL (762 × 572) by processing the video signal at double speed
- High optical transmittance: 17% (typ.)
- Built-in cross talk free circuit and ghost free circuit
- High contrast ratio with normally white mode: 350 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function
- High durable polarizer used
- Built-in  $\lambda/2$  retardation film for red light (V)

### Element Structure

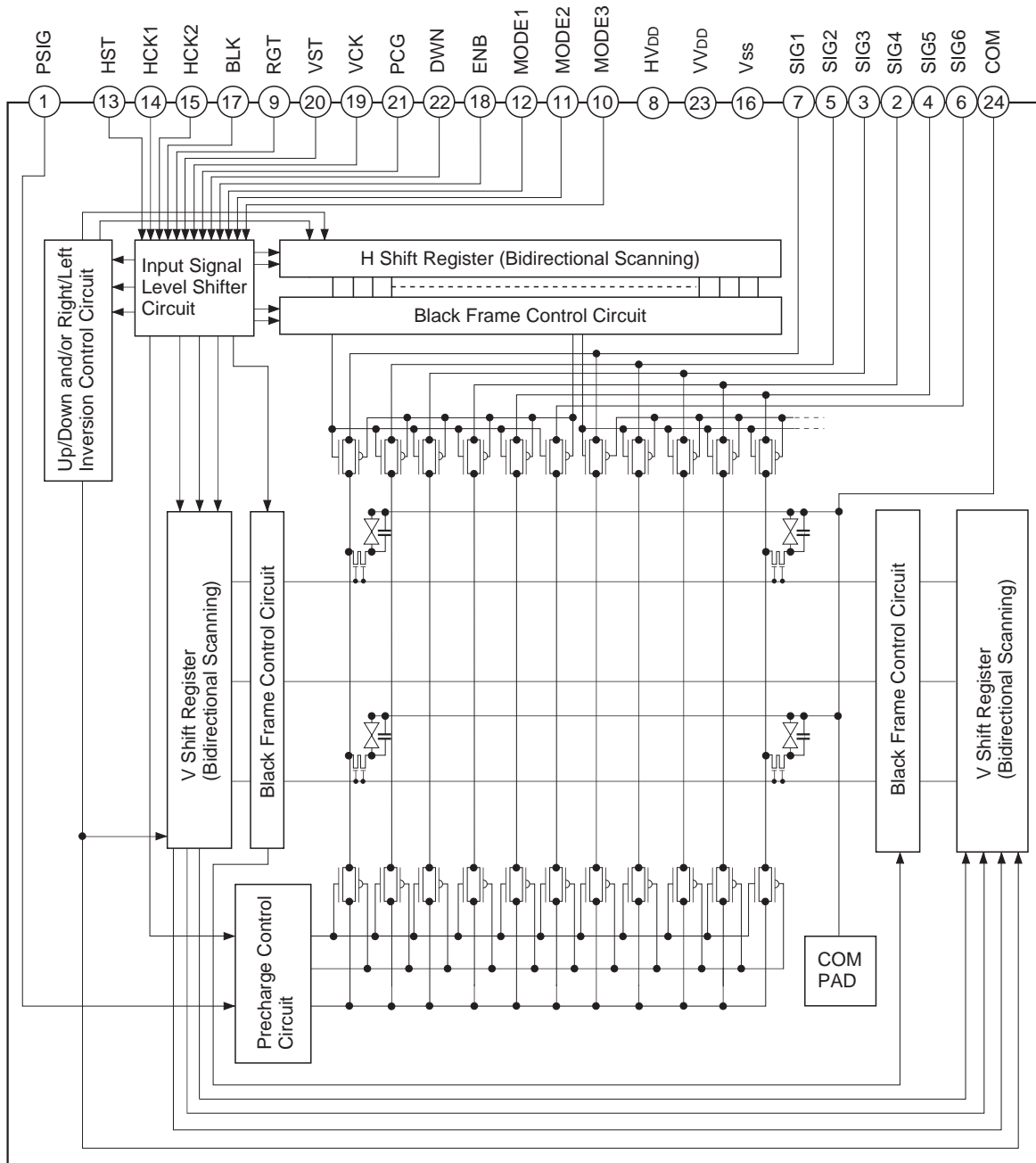
- Dots: 804 (H) × 604 (V) = 485,616
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

### Applications

- Liquid crystal data projectors
- Liquid crystal projectors, etc.

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Block Diagram



**Absolute Maximum Ratings** ( $V_{SS} = 0V$ )

|                                      |  |             |    |
|--------------------------------------|--|-------------|----|
| • H driver supply voltage            | HV <sub>DD</sub>                                       | -1.0 to +20 | V  |
| • V driver supply voltage            | VV <sub>DD</sub>                                       | -1.0 to +20 | V  |
| • Common pad voltage                 | COM  | -1.0 to +17 | V  |
| • H shift register input pin voltage | HST, HCK1, HCK2,<br>RGT                                | -1.0 to +17 | V  |
| • V shift register input pin voltage | VST, VCK, PCG,<br>BLK, ENB, DWN<br>MODE1, MODE2, MODE3 | -1.0 to +17 | V  |
| • Video signal input pin voltage     | SIG1, SIG2, SIG3, SIG4,<br>SIG5, SIG6, PSIG            | -1.0 to +15 | V  |
| • Operating temperature              | Topr   | -10 to +70  | °C |
| • Storage temperature                | Tstg   | -30 to +85  | °C |

**Operating Conditions** ( $V_{SS} = 0V$ )

|   |                  |             |
|---|------------------|-------------|
| • Supply voltage  |                  |             |
|   | HV <sub>DD</sub> | 15.5 ± 0.5V |
|   | VV <sub>DD</sub> | 15.5 ± 0.5V |
| • Input pulse voltage (V <sub>p-p</sub> of all input pins except video signal and uniformity improvement signal input pins) | V <sub>in</sub>  | 5.0 ± 0.5V  |

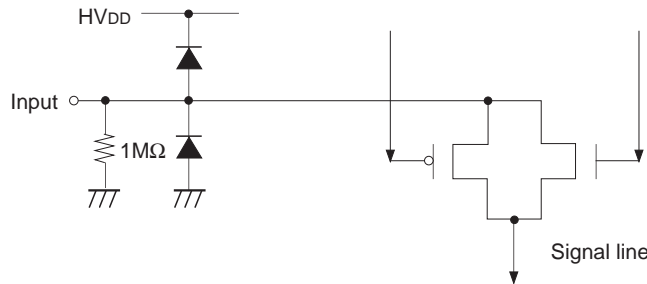
**Pin Description**

| Pin No. | Symbol           | Description  | Pin No. | Symbol           | Description  |
|---------|------------------|--|---------|------------------|--|
| 1       | PSIG             | Uniformity improvement signal                                      | 13      | HST              | Start pulse for H shift register drive                             |
| 2       | SIG4             | Video signal 4 to panel  | 14      | HCK1             | Clock pulse for H shift register drive                             |
| 3       | SIG3             | Video signal 3 to panel  | 15      | HCK2             | Clock pulse for H shift register drive                             |
| 4       | SIG5             | Video signal 5 to panel  | 16      | Vss              | GND (H, V drivers)   |
| 5       | SIG2             | Video signal 2 to panel  | 17      | BLK              | Black Frame display pulse  |
| 6       | SIG6             | Video signal 6 to panel  | 18      | ENB              | Enable pulse for gate selection                                    |
| 7       | SIG1             | Video signal 1 to panel  | 19      | VCK              | Clock pulse for V shift register drive                             |
| 8       | HV <sub>DD</sub> | Power supply for H driver  | 20      | VST              | Start pulse for V shift register drive                             |
| 9       | RGT              | Drive direction pulse for H shift register (H: normal, L: reverse) | 21      | PCG              | Improvement pulse for uniformity                                   |
| 10      | MODE3            | Display area switching 3   | 22      | DWN              | Drive direction pulse for V shift register (H: normal, L: reverse) |
| 11      | MODE2            | Display area switching 2   | 23      | VV <sub>DD</sub> | Power supply for V driver  |
| 12      | MODE1            | Display area switching 1   | 24      | COM              | Common voltage of panel  |

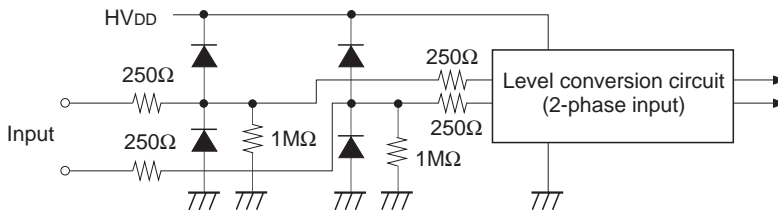
**Input Equivalent Circuit**

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

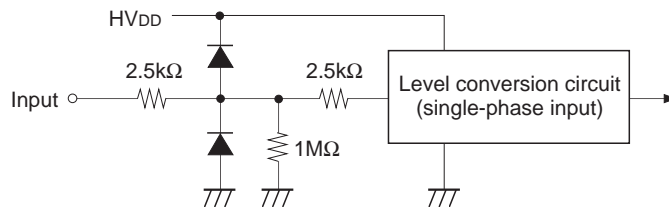
- (1) SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG



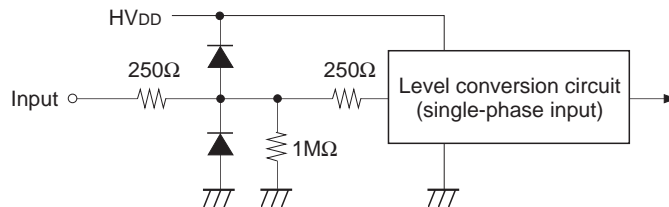
- (2) HCK1, HCK2



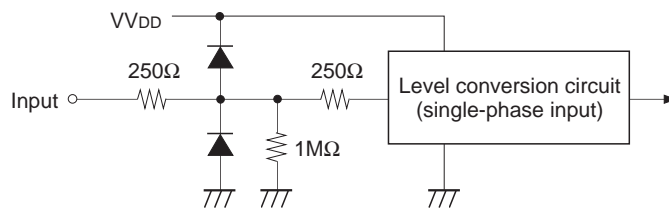
- (3) RGT



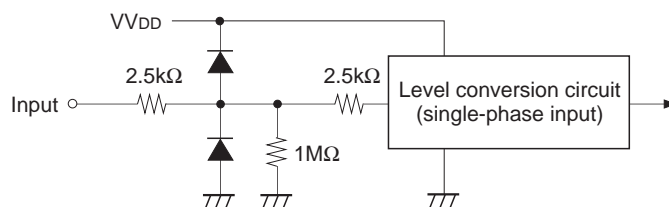
- (4) HST



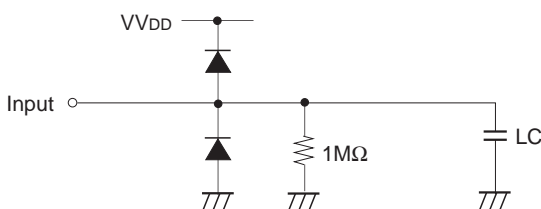
- (5) PCG, VCK



- (6) VST, BLK, ENB, DWN, MODE1, MODE2, MODE3



- (7) COM



**Input Signals**

**1. Input signal voltage conditions** ( $V_{SS} = 0V$ )

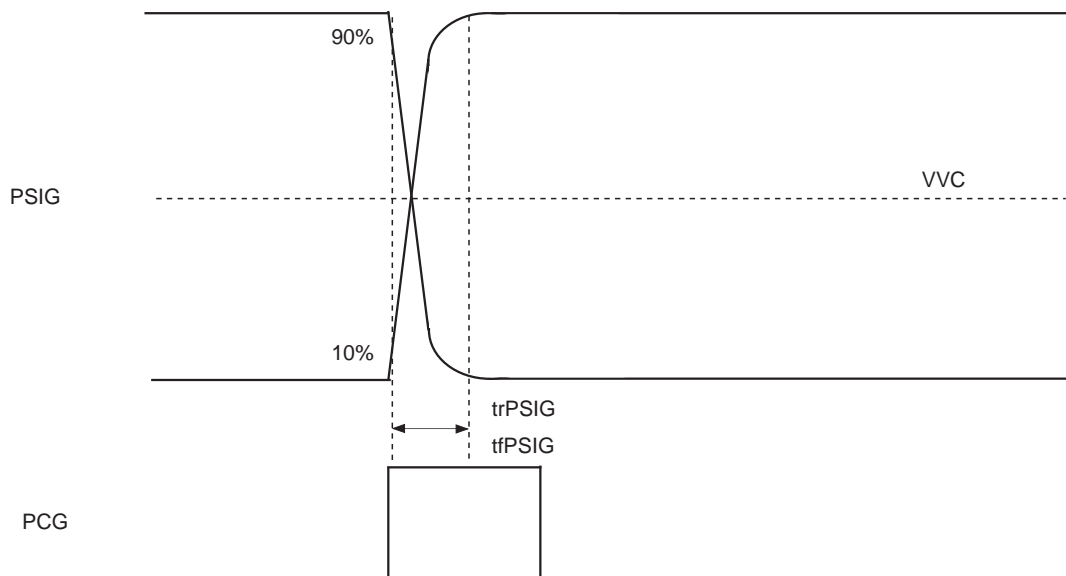
| Item  | Symbol | Min.          | Typ.          | Max.          | Unit |   |
|---|--------|---------------|---------------|---------------|------|---|
| H shift register input voltage<br>HST, HCK1, HCK2, RGT                                    | (Low)  | VHIL          | -0.5          | 0.0           | 0.4  | V |
|   | (High) | VHIH          | 4.5           | 5.0           | 5.5  | V |
| V shift register input voltage<br>MODE1, MODE2, MODE3,<br>BLK, VST, VCK, PCG,<br>ENB, DWN | (Low)  | VVIL          | -0.5          | 0.0           | 0.4  | V |
|   | (High) | VVIH          | 4.5           | 5.0           | 5.5  | V |
| Video signal center voltage   | VVC    | 6.8           | 7.0           | 7.2           | V    |   |
| Video signal input range*1  | Vsig   | $VVC - 4.5$   | 7.0           | $VVC + 4.5$   | V    |   |
| Common voltage of panel*2   | Vcom   | $VVC - 0.5$   | $VVC - 0.4$   | $VVC - 0.3$   | V    |   |
| Uniformity improvement signal<br>input voltage (PSIG)*3                                   | Vpsig  | $VVC \pm 4.3$ | $VVC \pm 4.5$ | $VVC \pm 4.7$ | V    |   |

\*1 Input video signal shall be symmetrical to VVC.

\*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction to use. In this case, use the voltage of which has maximum contrast as typical value. When the typical value is lowered, the maximum and minimum values may lower.

\*3 Input a uniformity improvement signal PSIG in the same polarity with video signals SIG1 to 6 and which is symmetrical to VVC. Also, the rising and falling of PSIG are synchronized with the rising of PCG pulse, and the rise time  $tr_{PSIG}$  and fall time  $tf_{PSIG}$  are suppressed within 800ns (as shown in a diagram below). The optimum input voltage of PSIG may be changed according as drive conditions of the drive side.

**Input waveform of uniformity improvement signal PSIG**



**Level Conversion Circuit**

The LCX026ALF has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to  $HV_{DD}$  or  $VV_{DD}$ . The  $V_{CC}$  of external ICs are applicable to  $5 \pm 0.5V$ .

## 2. Clock timing conditions (Ta = 25°C)

(SVGA mode: fHCKn = 4.0MHz, fVCK = 24.0kHz)

|       | Item                           | Symbol | Min. | Typ. | Max. | Unit |
|-------|--------------------------------|--------|------|------|------|------|
| HST   | Hst rise time                  | trHst  | —    | —    | 30   | ns   |
|       | Hst fall time                  | tfHst  | —    | —    | 30   |      |
|       | Hst data set-up time           | tdHst  | 50   | 60   | 70   |      |
|       | Hst data hold time             | thHst  | 50   | 60   | 70   |      |
| HCK   | Hckn rise time*4               | trHckn | —    | —    | 30   | ns   |
|       | Hckn fall time*4               | tfHckn | —    | —    | 30   |      |
|       | Hck1 fall to Hck2 rise time    | to1Hck | -15  | 0    | 15   |      |
|       | Hck1 rise to Hck2 fall time    | to2Hck | -15  | 0    | 15   |      |
| VST   | Vst rise time                  | trVst  | —    | —    | 100  | μs   |
|       | Vst fall time                  | tfVst  | —    | —    | 100  |      |
|       | Vst data set-up time           | tdVst  | 5    | 10   | 15   |      |
|       | Vst data hold time             | thVst  | 5    | 10   | 15   |      |
| VCK   | Vck rise time                  | trVck  | —    | —    | 100  | ns   |
|       | Vck fall time                  | tfVck  | —    | —    | 100  |      |
| ENB   | Enb rise time                  | trEnb  | —    | —    | 100  | ns   |
|       | Enb fall time                  | tfEnb  | —    | —    | 100  |      |
|       | Vck rise/fall to Enb rise time | tdEnb  | 400  | 500  | 600  |      |
|       | Enb pulse width                | twEnb  | 2400 | 2500 | 2600 |      |
| PCG   | Pcg rise time                  | trPcg  | —    | —    | 30   | ns   |
|       | Pcg fall time                  | tfPcg  | —    | —    | 30   |      |
|       | Pcg rise to Vck rise/fall time | toVck  | 900  | 1000 | 1100 |      |
|       | Pcg pulse width                | twPcg  | 1100 | 1200 | 1300 |      |
| BLK*5 | Blk rise time                  | trBlk  | —    | —    | 100  | μs   |
|       | Blk fall time                  | tfBlk  | —    | —    | 100  |      |
|       | Blk fall to Vst rise time      | toVst  | 32   | 33   | 34   |      |
|       | Blk pulse width                | twBlk  | 20   | 21   | 22   |      |

\*4 Hckn means Hck1 and Hck2.

\*5 Blk is the timing during SVGA mode (fHckn = 4.0MHz, fVck = 24.0kHz).

<Horizontal Shift Register Driving Waveform>

| Item |                             | Symbol | Waveform | Conditions   |
|------|-----------------------------|--------|----------|--|
| HST  | Hst rise time               | trHst  |          | <ul style="list-style-type: none"> <li>• Hckn*3</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul> |
|      | Hst fall time               | tfHst  |          |  |
|      | Hst data set-up time        | tdHst  |          | <ul style="list-style-type: none"> <li>• Hckn*3</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul> |
|      | Hst data hold time          | thHst  |          |  |
| HCK  | Hckn rise time*3            | trHckn |          | <ul style="list-style-type: none"> <li>• Hckn*3</li> <li>duty cycle 50%</li> <li>to1Hck = 0ns</li> <li>to2Hck = 0ns</li> </ul> |
|      | Hckn fall time*3            | tfHckn |          |  |
|      | Hck1 fall to Hck2 rise time | to1Hck |          |  |
|      | Hck1 rise to Hck2 fall time | to2Hck |          |  |

\*6 Definitions: The right-pointing arrow (  $\bullet \rightarrow$  ) means +.

The left-pointing arrow (  $\leftarrow \bullet$  ) means -.

The black dot at an arrow (  $\bullet$  ) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

| Item  |                                | Symbol | Waveform | Conditions |
|-------|--------------------------------|--------|----------|------------|
| VST   | Vst rise time                  | trVst  |          |            |
|       | Vst fall time                  | tfVst  |          |            |
|       | Vst data set-up time           | tdVst  |          |            |
|       | Vst data hold time             | thVst  |          |            |
| VCK   | Vck rise time                  | trVck  |          |            |
|       | Vck fall time                  | tfVck  |          |            |
| ENB   | Enb rise time                  | trEnb  |          |            |
|       | Enb fall time                  | tfEnb  |          |            |
|       | Vck rise/fall to Enb rise time | tdEnb  |          |            |
|       | Enb pulse width                | twEnb  |          |            |
| PCG*7 | Pcg rise time                  | trPcg  |          |            |
|       | Pcg fall time                  | tfPcg  |          |            |
|       | Pcg rise to Vck rise/fall time | toVck  |          |            |
|       | Pcg pulse width                | trPcg  |          |            |
| BLK   | Blk rise time                  | twBlk  |          |            |
|       | Blk fall time                  | tfBlk  |          |            |
|       | Blk fall to Vst rise time      | toVst  |          |            |
|       | Blk pulse width                | twBlk  |          |            |

\*7 Input the pulse obtained by taking the OR of the above pulse (PCG) and BLK to the PCG input pin.



**Electrical Characteristics** ( $T_a = 25^\circ\text{C}$ ,  $HV_{DD} = 15.5\text{V}$ ,  $VV_{DD} = 15.5\text{V}$ )**1. Horizontal drivers**

| Item                               | Symbol | Min.  | Typ.  | Max. | Unit | Condition                 |            |
|------------------------------------|--------|-------|-------|------|------|---------------------------|------------|
| Input pin capacitance              | HCKn   | CHckn | —     | 7    | 12   | pF                        |            |
|                                    | HST    | CHst  | —     | 7    | 12   | pF                        |            |
| Input pin current                  | HCK1   |       | -500  | -250 | —    | $\mu\text{A}$             | HCK1 = GND |
|                                    | HCK2   |       | -1000 | -300 | —    | $\mu\text{A}$             | HCK2 = GND |
|                                    | HST    |       | -500  | -150 | —    | $\mu\text{A}$             | HST = GND  |
|                                    | RGT    |       | -150  | -30  | —    | $\mu\text{A}$             | RGT = GND  |
| Video signal input pin capacitance | Csig   | —     | 130   | 200  | pF   |                           |            |
| Current consumption                | IH     | —     | 10.0  | 15.0 | mA   | HCKn: HCK1, HCK2 (4.0MHz) |            |

**2. Vertical drivers**

| Item   | Symbol | Min. | Typ.  | Max. | Unit | Condition      |  |
|--|--------|------|-------|------|------|----------------|--|
| Input pin capacitance                        | VCK    | CVck | —     | 7    | 12   | pF             |  |
|  | VST    | CVst | —     | 7    | 12   | pF             |  |
| Input pin current                            | VCK    |      | -1000 | -150 | —    | $\mu\text{A}$  | VCK = GND  |
| PCG, VST, ENB, DWN, BLK, MODE1, MODE2, MODE3 |        |      | -150  | -30  | —    | $\mu\text{A}$  | PCG, VST, ENB, DWN, BLK, MODE1, MODE2, MODE3 = GND |
| Current consumption                          | IV     | —    | 3.0   | 6.0  | mA   | VCK: (24.0kHz) |  |

**3. Total power consumption of the panel**

| Item                                 | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------------------|--------|------|------|------|------|
| Total power consumption of the panel | PWR    | —    | 200  | 300  | mW   |

**4. Pin input resistance**

| Item                       | Symbol | Min. | Typ. | Max. | Unit             |
|----------------------------|--------|------|------|------|------------------|
| Pin – Vss input resistance | Rpin   | 0.4  | 1    | —    | $\text{M}\Omega$ |

**5. Uniformity improvement signal**

| Item  | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|------|------|------|------|
| Input pin capacitance for uniformity improvement signal | CPSIGo | —    | 8    | 12   | nF   |

Electro-optical Characteristics

(SVGA mode)

| Item                  |                 | Symbol | Measurement method  | Min. | Typ. | Max. | Unit |    |
|-----------------------|-----------------|--------|---------------------|------|------|------|------|----|
| Contrast ratio        |                 | 25°C   | CR                  | 1    | 150  | 350  | —    |    |
| Optical transmittance |                 | 25°C   | T                   | 2    | 15   | 17   | —    |    |
| V-T characteristics   | V <sub>90</sub> | 25°C   | RV <sub>90-25</sub> | 3    | 1.0  | 1.3  | 1.7  | V  |
|                       |                 |        | GV <sub>90-25</sub> |      | 1.1  | 1.5  | 1.9  |    |
|                       |                 |        | BV <sub>90-25</sub> |      | 1.2  | 1.6  | 2.0  |    |
|                       |                 | 60°C   | RV <sub>90-60</sub> |      | 1.0  | 1.3  | 1.6  |    |
|                       |                 |        | GV <sub>90-60</sub> |      | 1.0  | 1.4  | 1.7  |    |
|                       |                 |        | BV <sub>90-60</sub> |      | 1.1  | 1.5  | 1.9  |    |
|                       | V <sub>50</sub> | 25°C   | RV <sub>50-25</sub> |      | 1.4  | 1.7  | 2.0  |    |
|                       |                 |        | GV <sub>50-25</sub> |      | 1.5  | 1.8  | 2.1  |    |
|                       |                 |        | BV <sub>50-25</sub> |      | 1.6  | 1.9  | 2.2  |    |
|                       |                 | 60°C   | RV <sub>50-60</sub> |      | 1.4  | 1.6  | 1.9  |    |
|                       |                 |        | GV <sub>50-60</sub> |      | 1.4  | 1.7  | 2.0  |    |
|                       |                 |        | BV <sub>50-60</sub> |      | 1.5  | 1.8  | 2.1  |    |
|                       | V <sub>10</sub> | 25°C   | RV <sub>10-25</sub> |      | 1.9  | 2.2  | 2.5  |    |
|                       |                 |        | GV <sub>10-25</sub> |      | 2.0  | 2.3  | 2.6  |    |
|                       |                 |        | BV <sub>10-25</sub> |      | 2.1  | 2.4  | 2.7  |    |
|                       |                 | 60°C   | RV <sub>10-60</sub> |      | 1.9  | 2.1  | 2.4  |    |
|                       |                 |        | GV <sub>10-60</sub> |      | 1.9  | 2.2  | 2.5  |    |
|                       |                 |        | BV <sub>10-60</sub> |      | 1.9  | 2.3  | 2.6  |    |
| Response time         | ON time         | 0°C    | ton0                | 4    | —    | 30   | 80   | ms |
|                       |                 | 25°C   | ton25               |      | —    | 12   | 40   |    |
|                       | OFF time        | 0°C    | toff0               |      | —    | 100  | 200  |    |
|                       |                 | 25°C   | toff25              |      | —    | 30   | 70   |    |
| Flicker               |                 | 60°C   | F                   | 5    | —    | -65  | -40  | dB |
| Image retention time  |                 | 25°C   | YT60                | 6    | —    | —    | 0    | s  |
| Cross talk            |                 | 25°C   | CTK                 | 7    | —    | —    | 5    | %  |

Reflection Preventive Processing

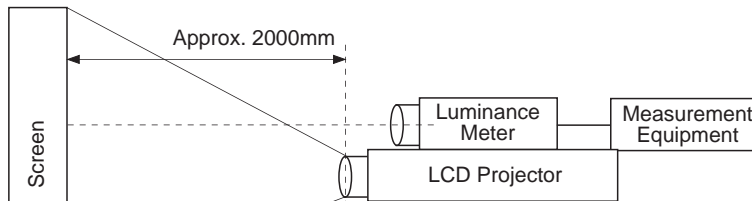
When a retardation film which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a retardation film with reflection preventive processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

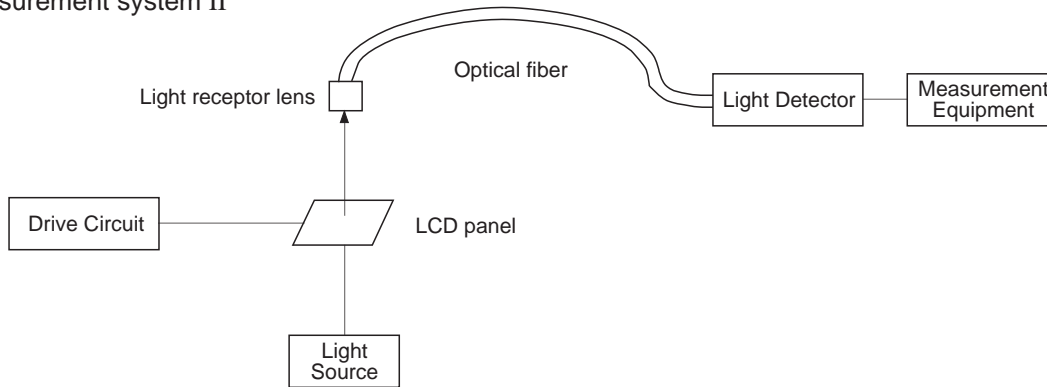
- (1) Driving voltage  
 $HV_{DD} = 15.5V, VV_{DD} = 15.5V$   
 $VVC = 7.0V, V_{com} = 6.6V$
- (2) Measurement temperature  
 25°C unless otherwise specified.
- (3) Measurement point  
 One point in the center of the screen unless otherwise specified.
- (4) Measurement systems  
 Two types of measurement systems are used as shown below.
- (5) Video input signal voltage ( $V_{sig}$ )  
 $V_{sig} = 7.0 \pm V_{AC} [V]$  ( $V_{AC} = \text{signal amplitude}$ )

• Measurement system I



Screen: Made by Sony (VPS-120FH: Gain 2.8, Glass Beaded Type) or equivalent  
 Projection lens: Focal distance 80mm, F1.9  
 Light source: 155W metal Haloid arc lamp (Color temperature 7500K ± 500)  
 (× 24, Sensor area: 7mmφ)  
 Polarizer: Nitto Denko's EG-1224DU or Polatechno's SKN-1824ZT or equivalent

• Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L(\text{White})}{L(\text{Black})} \dots (1)$$

L (White): Surface luminance of the center of the screen at the input signal amplitude  $V_{AC} = 0.5V$ .

L (Black): Surface luminance of the center of the screen at  $V_{AC} = 4.5V$ .

Both luminosities are measured by System I.

**2. Optical Transmittance**

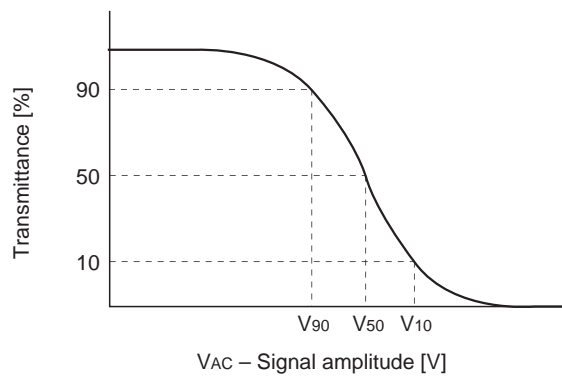
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100 [\%] \dots (2)$$

"White luminance" means the maximum luminance on the screen at the input signal amplitude  $V_{AC} = 0.5V$  on Measurement System I.

**3. V-T Characteristics**

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panels, are measured by System II by inputting the same signal amplitude  $V_{AC}$  to each input pin.  $V_{90}$ ,  $V_{50}$ , and  $V_{10}$  correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



**4. Response Time**

Response time  $t_{on}$  and  $t_{off}$  are defined by formulas (5) and (6) respectively.

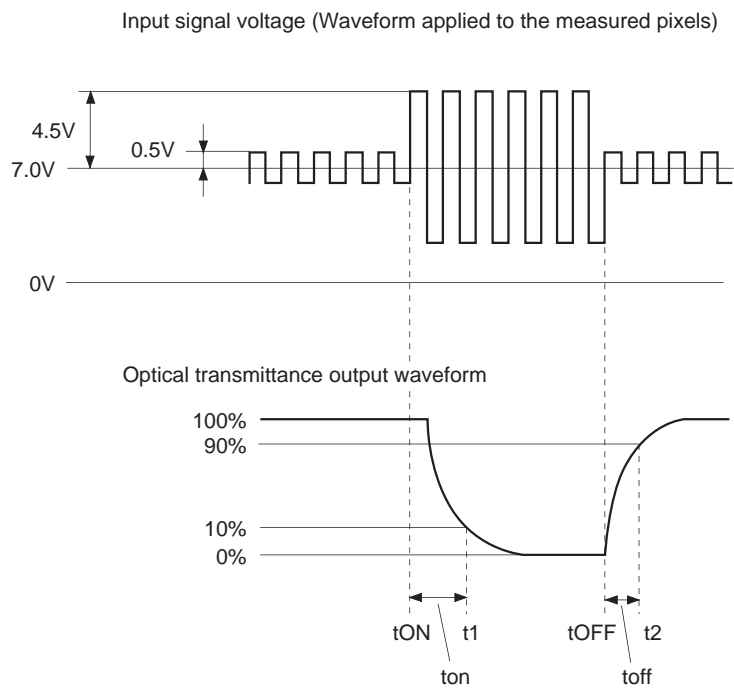
$$t_{on} = t_1 - t_{ON} \dots (5)$$

$$t_{off} = t_2 - t_{OFF} \dots (6)$$

$t_1$ : time which gives 10% transmittance of the panel.

$t_2$ : time which gives 90% transmittance of the panel.

The relationships between  $t_1$ ,  $t_2$ ,  $t_{ON}$  and  $t_{OFF}$  are shown in the right figure.



**5. Flicker**

Flicker (F) is given by formula (7). DC and AC (SVGA/VGA/PC98/NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster\* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

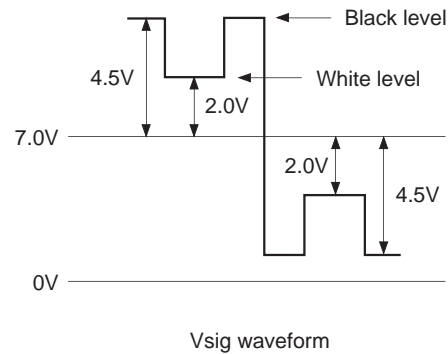
$$F [dB] = 20 \log \left\{ \frac{\text{AC component}}{\text{DC component}} \right\} \dots(7)$$

\* Each input signal voltage for gray raster mode is given by  $V_{sig} = 7.0 \pm V_{50}$  [V] where:  $V_{50}$  is the signal amplitude which gives 50% of transmittance in V-T characteristics.

**6. Image Retention Time**

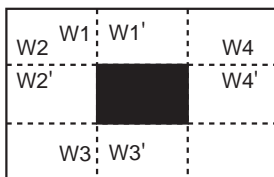
Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of  $V_{sig} = 7.0 \pm V_{AC}$  ( $V_{AC}$ : 3 to 4V). Judging by sight at the  $V_{AC}$  that holds the maximum image retention, measure the time till the residual image becomes indistinct.

\* Monoscope signal conditions:  
 $V_{sig} = 7.0 \pm 4.5$  or  $\pm 2.0$  [V]  
 (shown in the right figure)  
 $V_{com} = 6.6V$



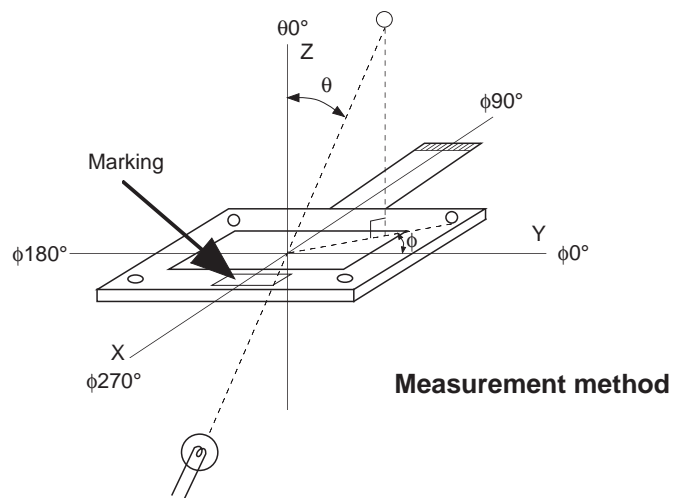
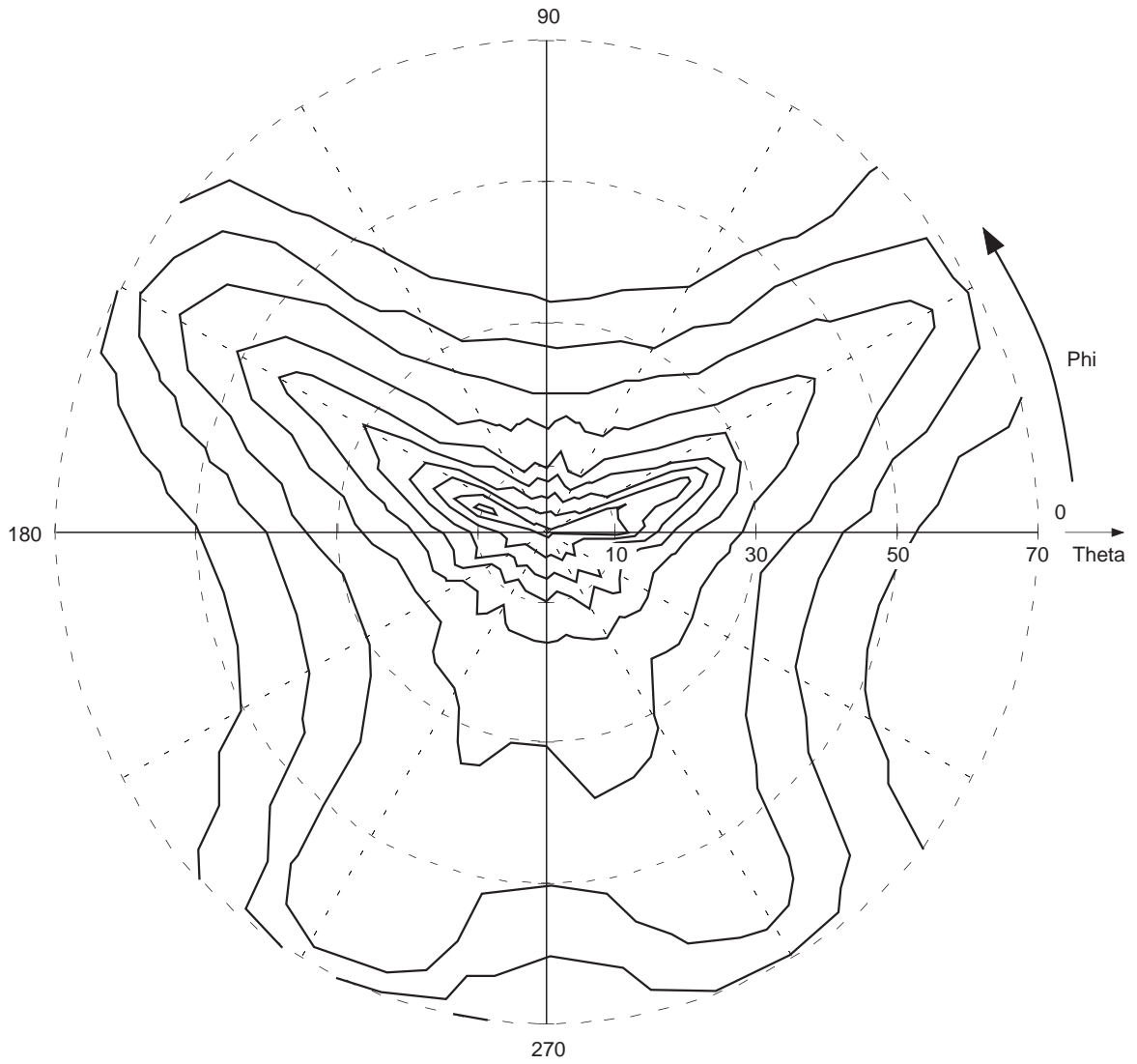
**7. Cross Talk**

Cross talk is determined by the luminance differences between adjacent areas represented by  $W_i'$  and  $W_i$  ( $i = 1$  to 4) around a black window ( $V_{sig} = 4.5 V/1V$ ).

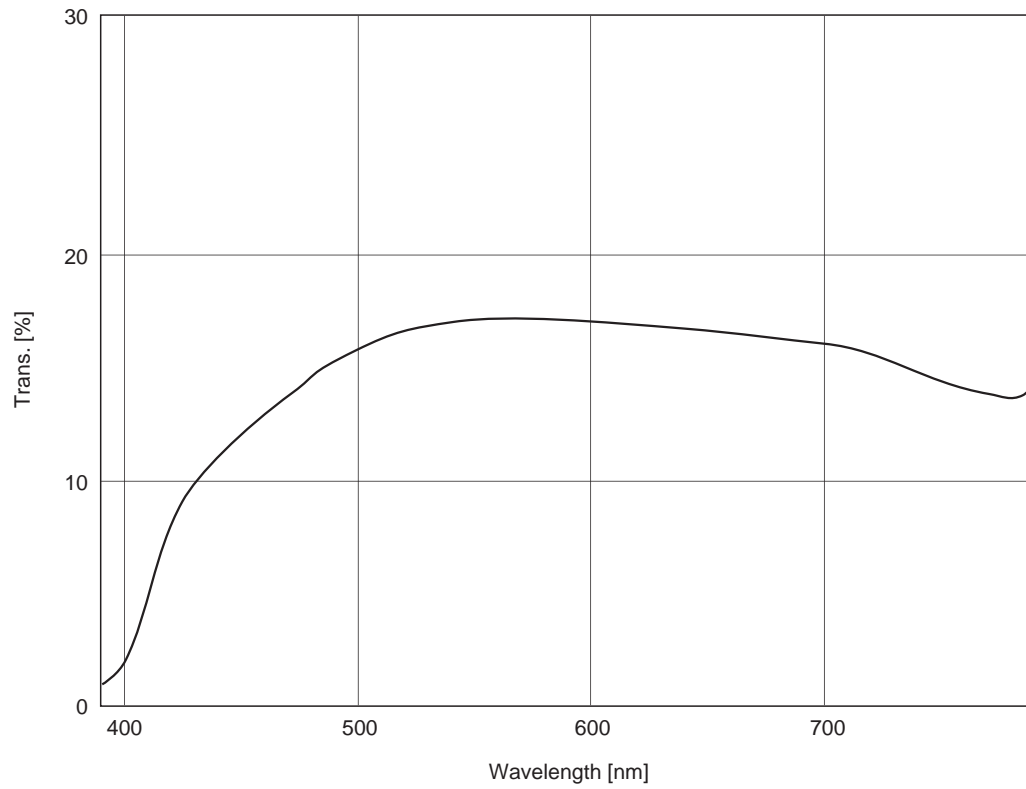


$$\text{Cross talk value CTK} = \left| \frac{W_i' - W_i}{W_i} \right| \times 100 [\%]$$

Viewing angle characteristics (Typical Value)



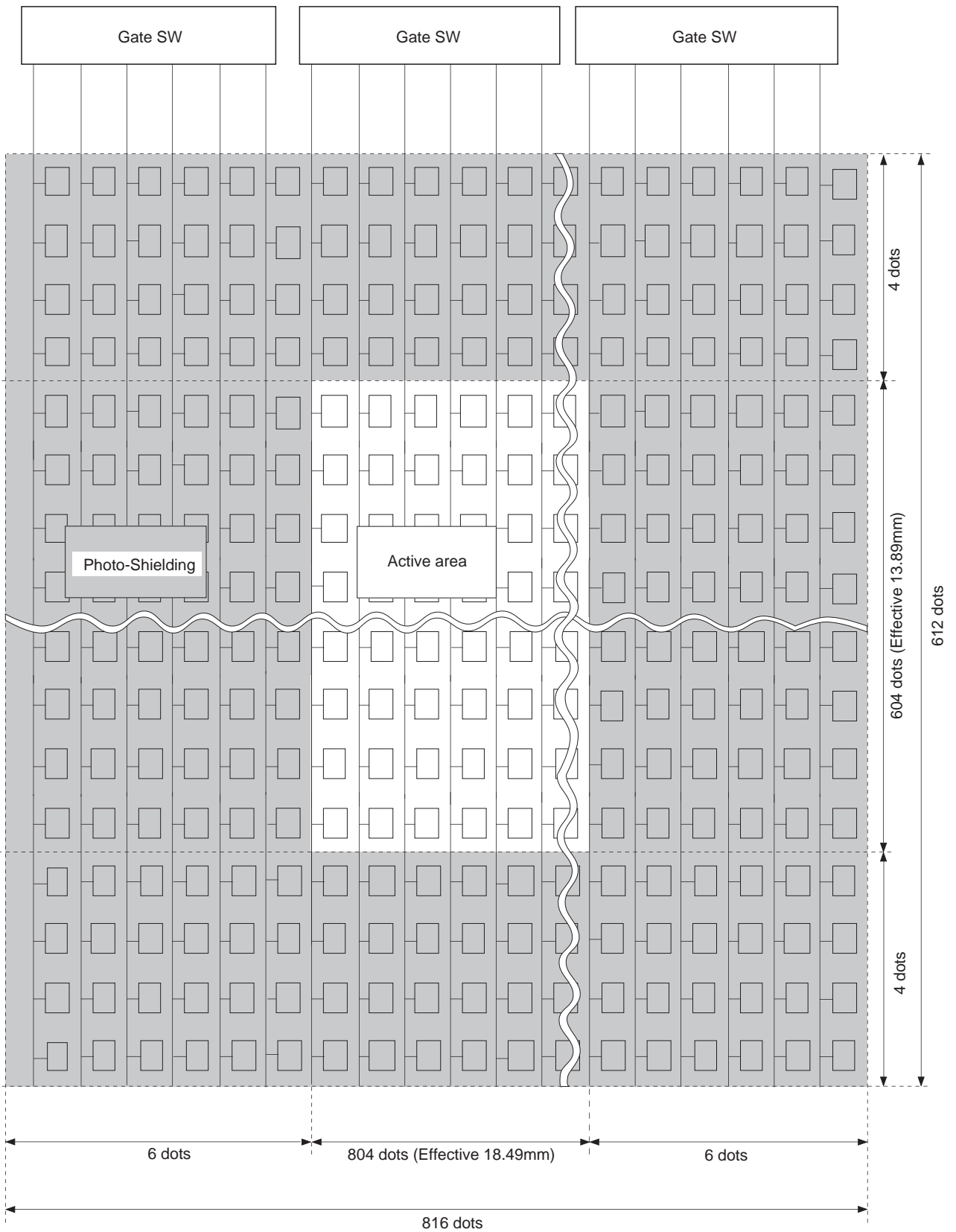
Optical transmittance of LCD panel (Typical Value)



Measurement method: Measurement system II

1. Dot Arrangement

The dots are arranged in a stripe. The shaded area is used for the dark border around the display.





## 2. LCD Panel Operations

### [Description of basic operations]

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 604 gate lines sequentially in a single horizontal scanning period. (in SVGA mode)
- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 804 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.
- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs) turn on to apply a video signal to the dot. The same procedures lead to the entire 604 × 804 dots to display a picture in a single vertical scanning period.
- The data and video signals shall be input with the 1H-inverted system.

### [Description of operating mode]

This LCD panel can change the active area by displaying a black frame to support various computer or video signals. The active area is switched by MODE1, 2 and 3. However, the center of the screen is not changed. The active area setting modes are shown below.

| MODE1 | MODE2 | MODE3 | Display mode          |
|-------|-------|-------|-----------------------|
| L     | L     | H     | SVGA<br>804 × 604     |
| L     | H     | L     | PAL<br>762 × 572      |
| L     | H     | H     | VGA/NTSC<br>644 × 484 |
| H     | L     | L     | PC98<br>644 × 404     |

This LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and/or up/down setting modes are shown below.

| RGT | Mode       |
|-----|------------|
| H   | Right scan |
| L   | Left scan  |

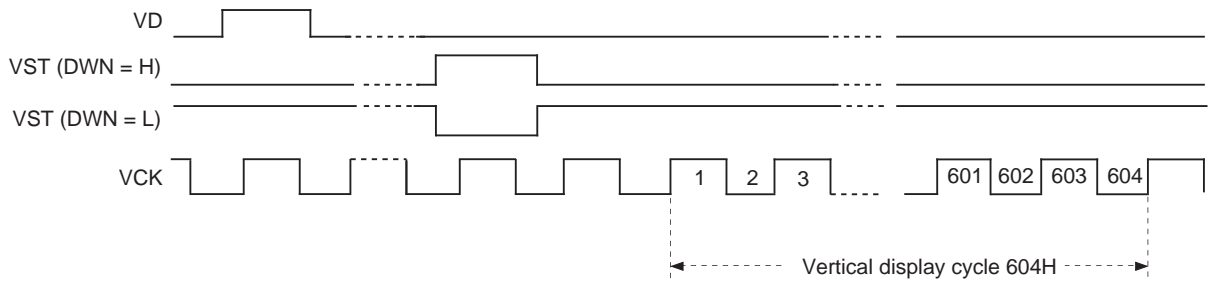
| DWN | Mode      |
|-----|-----------|
| H   | Down scan |
| L   | Up scan   |

Right/left and/or up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

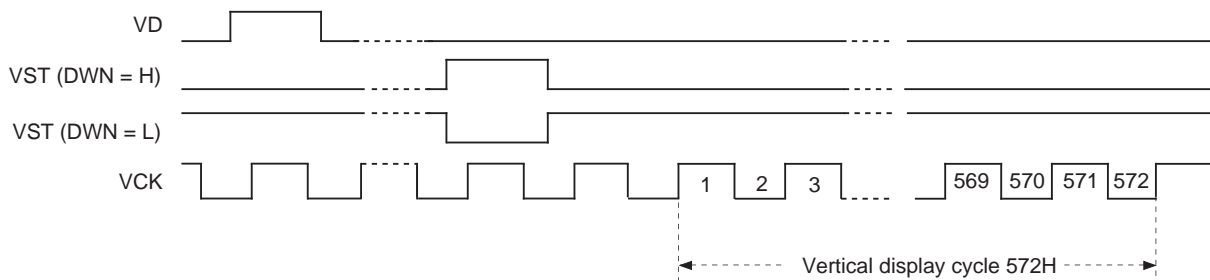
To locate the active area in the center of the panel in each mode, polarity of the start pulse and clock phase for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown on the following pages.

(1) Vertical direction display cycle

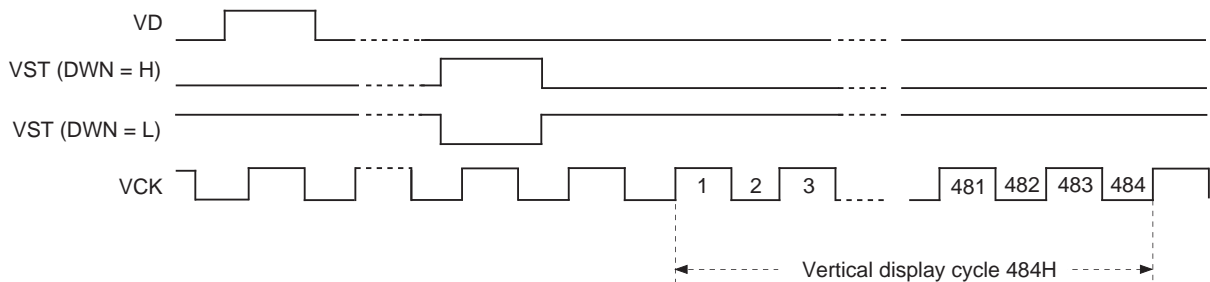
(1.1) SVGA



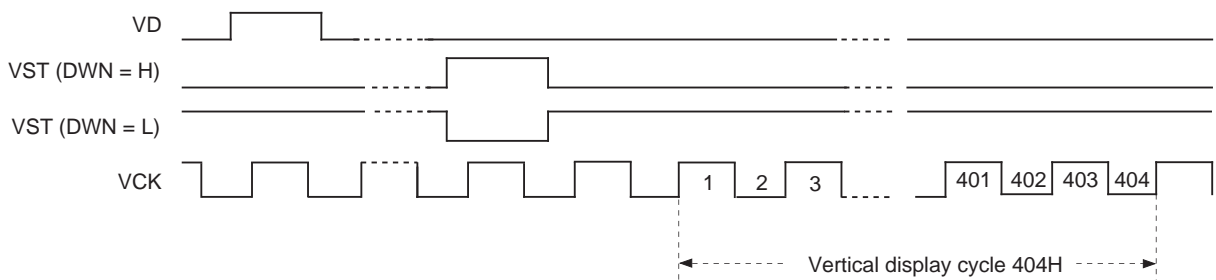
(1.2) PAL



(1.3) VGA/NTSC

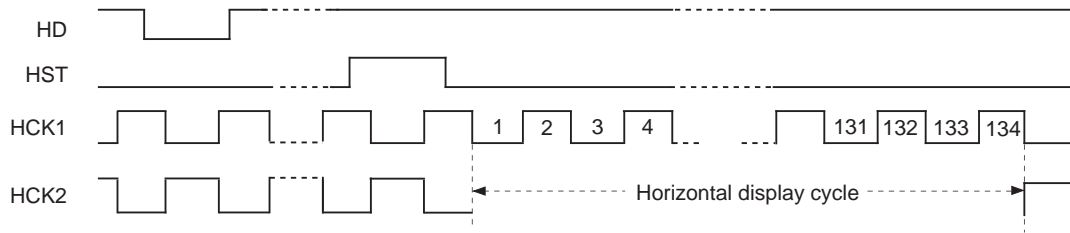


(1.4) PC98

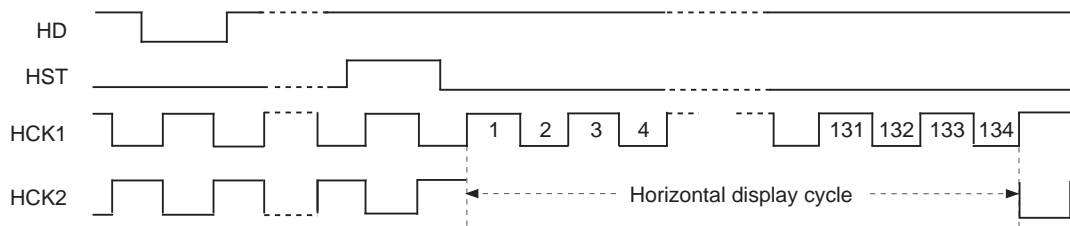


**(2) Horizontal direction display cycle**

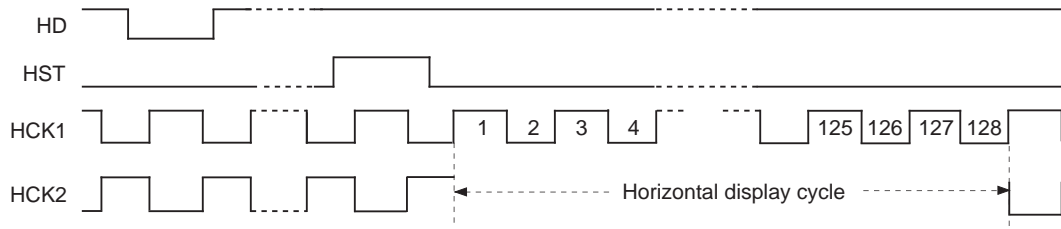
**(2.1.1) SVGA, RGT = H**



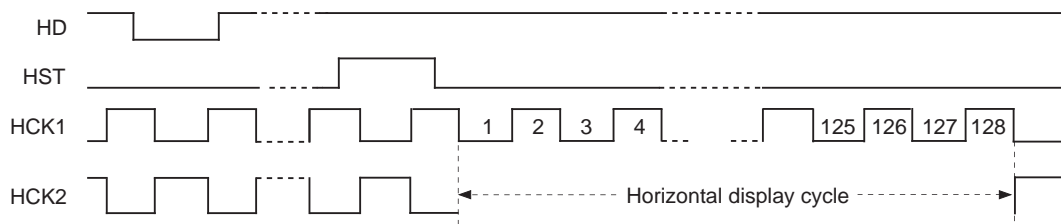
**(2.1.2) SVGA, RGT = L**



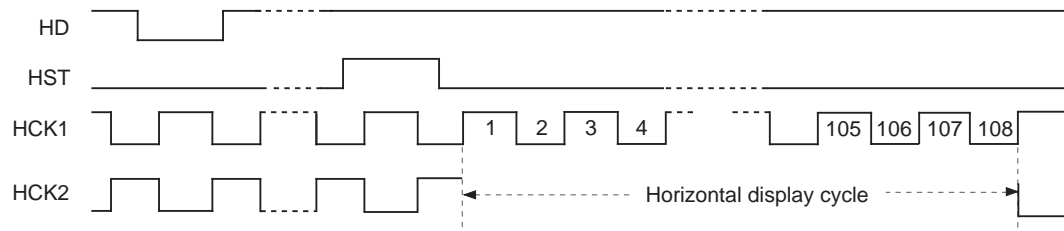
**(2.2.1) PAL, RGT = H**



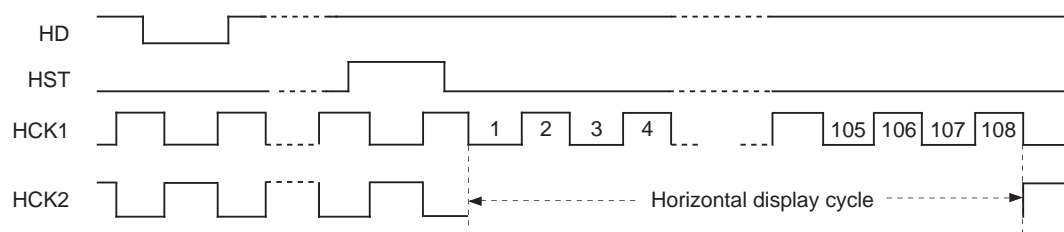
**(2.2.2) PAL, RGT = L**



(2.3.1) VGA/NTSC/PC98, RGT = H



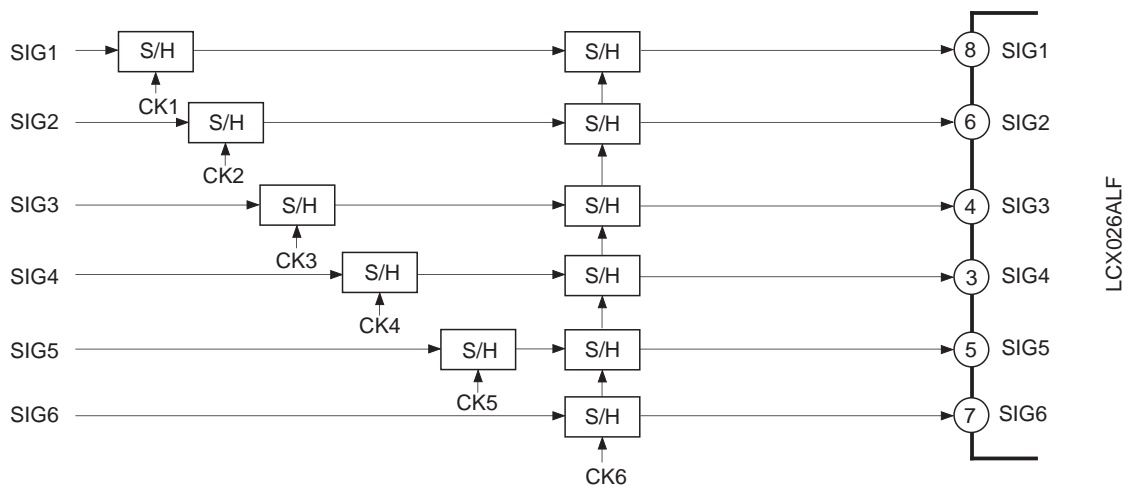
(2.3.2) VGA/NTSC/PC98, RGT = L



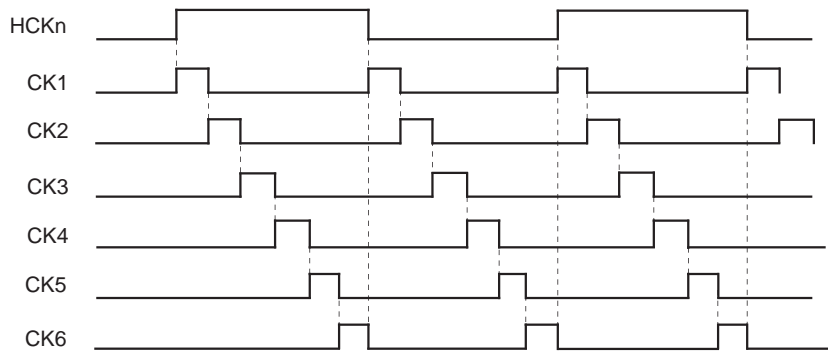
**3. 6-dot Simultaneous Sampling**

The horizontal shift register samples signals SIG1 to SIG6 simultaneously. This requires phase matching between signals SIG1 to SIG6 to prevent the horizontal resolution from deteriorating. Thus, phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High level). For left scan (RGT = Low level), the phase settings for signals SIG1 to SIG6 are exactly reversed.

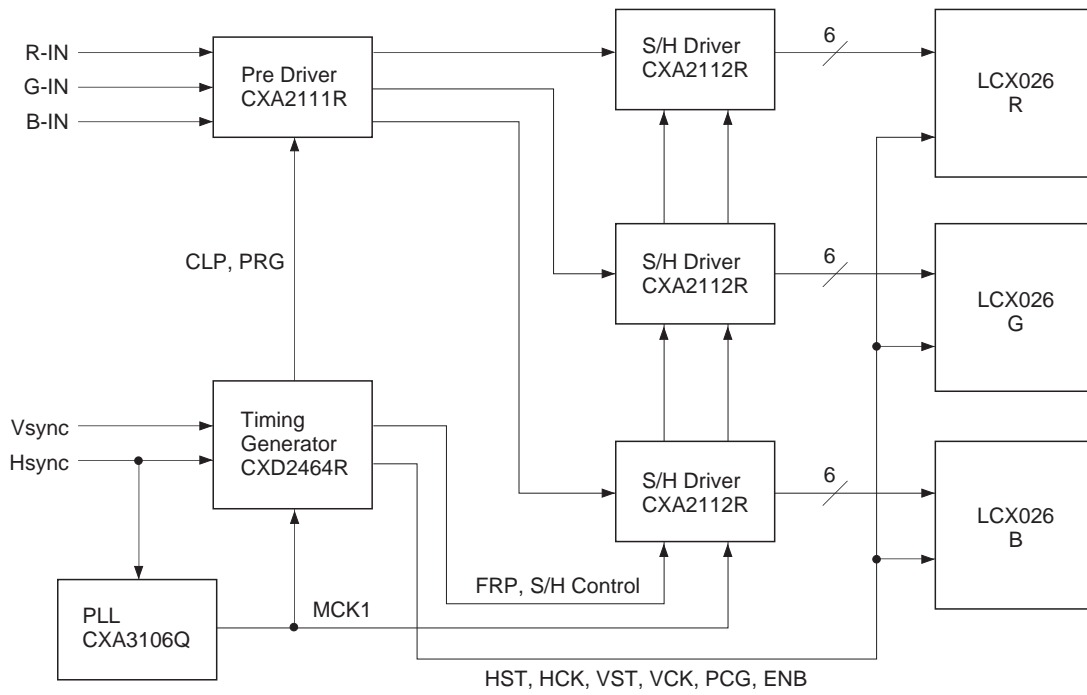


**<Phase relationship of delaying sample-and-hold pulses> (right scan)**



**Display System Block Diagram**

An example of display system is shown below.



**Notes on Handling****(1) Static charge prevention**

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

- a) Use non-chargeable gloves, or simply use bare hands.
- b) Use an earth-band when handling.
- c) Do not touch any electrodes of a panel.
- d) Wear non-chargeable clothes and conductive shoes.
- e) Install conductive mats on the working floor and working table.
- f) Keep panels away from any charged materials.
- g) Use ionized air to discharge the panels.

**(2) Protection from dust and dirt**

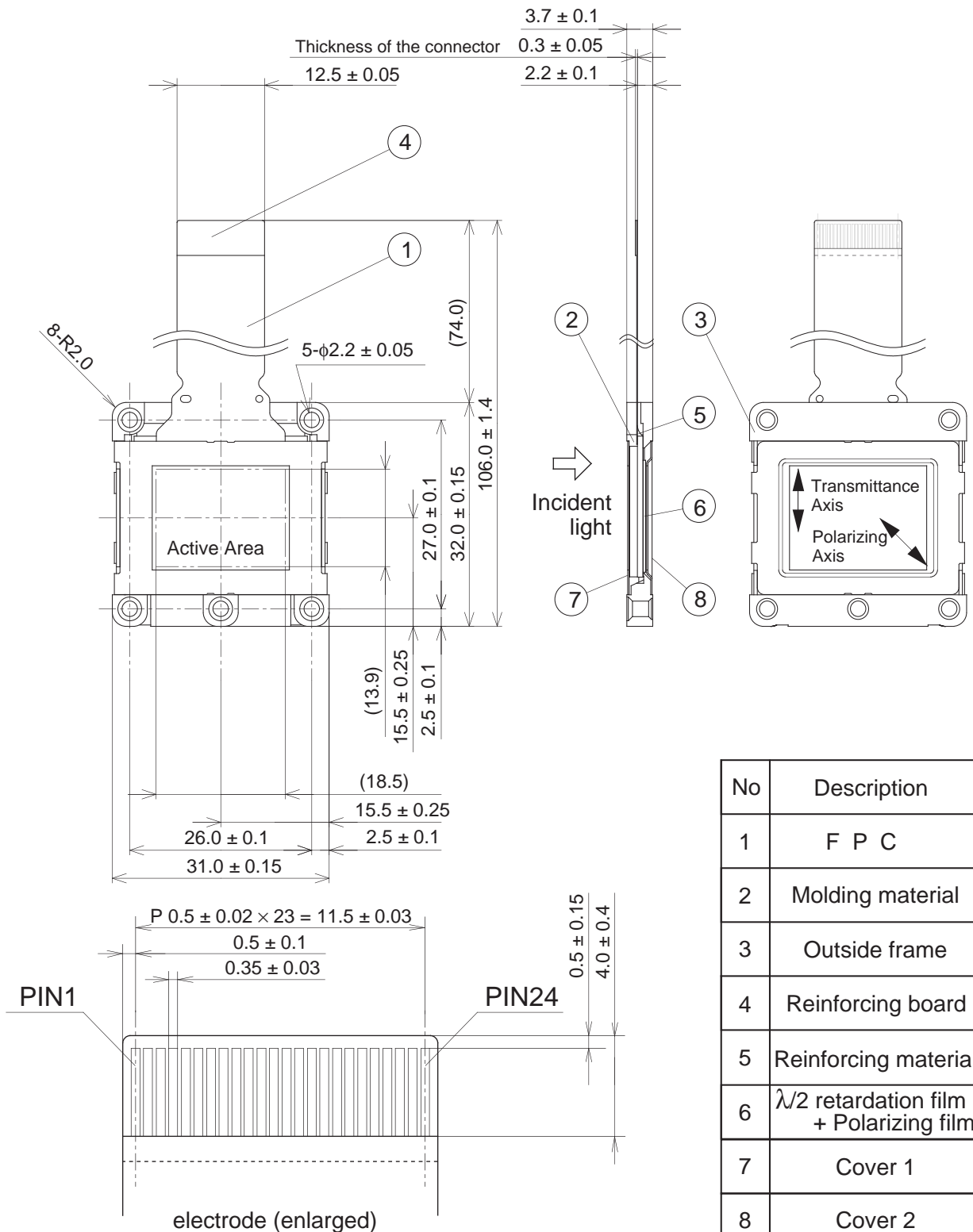
- a) Operate in a clean environment.
- b) When delivered, the panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
- c) Do not touch the panel surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
- d) Use ionized air to blow dust off the panel.

**(3) Other handling precautions**

- a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
- b) Do not drop the panel.
- c) Do not twist or bend the panel or panel frame.
- d) Keep the panel away from heat sources.
- e) Do not dampen the panel with water or other solvents.
- f) Avoid storing or using the panel at a high temperature or high humidity, which may result in panel damages.
- g) Minimum radius of bending curvature for a flexible substrate must be 1mm.
- h) Torque required to tighten screws on a panel must be 3kg · cm or less.

Package Outline

Unit: mm



The rotation angle of the active area relative to H and V is  $\pm 1^\circ$ .

weight 5.3g