# Boost Controller for LED Backlight

***REV: 00***

## General Description

The LD5857 is a wide-input asynchronous current mode boost controller, capable to operate in the range between 9V and 28V and to generate 12V of voltage to the GATE pin of MOSFET to reduce thermal loss. The current mode control architecture enhances transient response and simplifies the loop compensation. The DIM input enables the brightness control for LED Backlight or LED lighting.

The device also features internal slope compensation, input voltage under-voltage lockout, output voltage short circuit protection, cycle-by-cycle current limit and thermal shutdown protection.

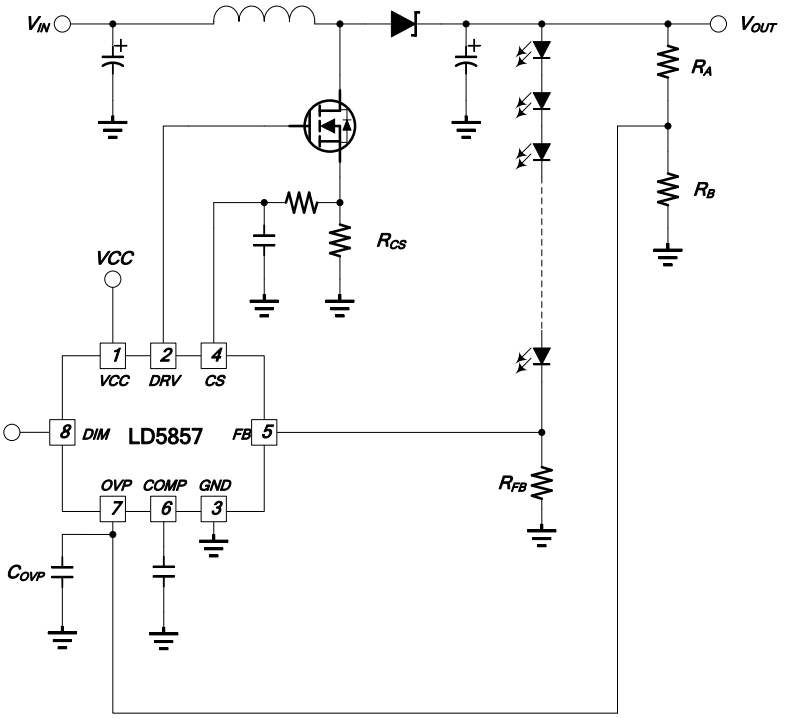
## Features

- Wide Input Range: 9V to 28V
- Current Mode Control
- 0.3V LED Feedback Current Sensing Reference
- Fixed Switching Frequency
- Cycle-by-Cycle Current Limit
- Over Temperature Protection
- High performance of Dimming Linearity.
- Programmable PWM Dimming Input and Analog Dimming Output with Software Control

## Applications

- LED TV Backlight
- LED Monitor Backlight
- LED lighting

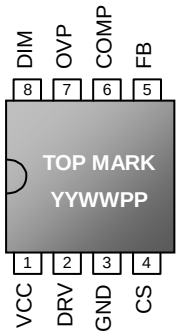
## Typical Application




**Application circuit**

## Pin Configuration

SOP-8 (TOP VIEW)




YY: Year code
WW: Week code
PP: Production code

## Ordering Information

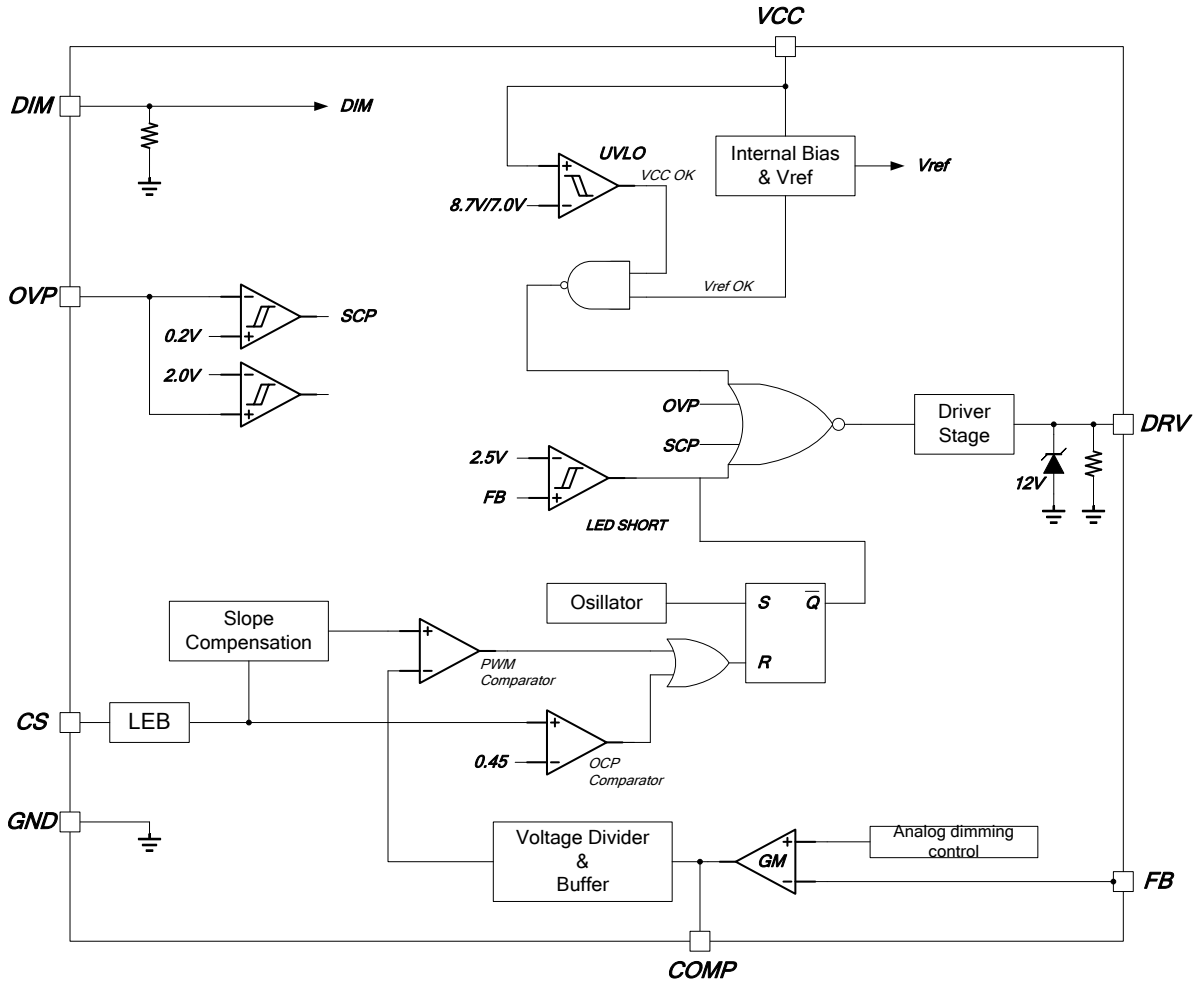
| Part number | Package | TOP MARK | Shipping |
|---|---|---|---|
| LD5857 GS | SOP-8 | LD5857 GS | 2500 /tape & reel |

Note: The LD5857 is ROHS compliant/ Green Packaged.

## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | VCC | Power source VCC pin. |
| 2 | DRV | Gate drive output to drive the external MOSFET. |
| 3 | GND | Ground. |
| 4 | CS | Current Sense pin. Connect with an external current sensing resistor to GND. CS pin voltage is used to provide current feedback in the control loop and detect an overcurrent condition. |
| 5 | FB | LED output current feedback through a current sense resistor. |
| 6 | COMP | It's a compensation of the error amplifier |
| 7 | OVP | Over-voltage protection. |
| 8 | DIM | FB Dimming Input. (Input PWM signal.) |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| VCC, DRV, CS, FB, OVP | 30V |
| All Other Pins | -0.3V ~ 5.5V |
| Power Dissipation, $P_D$@85°C, SOP-8 | 250mW |
| Package Thermal Resistance, SOP-8, $\theta_{JA}$ | 160°C/W |
| Maximum Junction Temperature | 150°C |
| Operating Junction Temperature | -40°C~ 125°C |
| Operating Ambient Temperature | -40°C ~ 85°C |
| Storage Temperature Range | -55°C~ 125°C |
| Lead Temperature (Soldering, 10sec) | 260°C |
| ESD Level (Human Body Model) | 2.0KV |
| ESD Level (Machine Model) | 200V |

**Recommended Operating Conditions**

| | |
|---|---|
| Input Supply Voltage | 10.8V ~ 26.4V |
| DIM Frequency | 200Hz ~ 30KHz |
| Dimming duty cycle | 5% ~ 100% |
| DIM PIN voltage | 0V ~ 5V |

**Caution:**

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

## Electrical Characteristics

($V_{CC}$=12V, $T_A$=25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | Symbol | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| **Input Power (VCC)** | | | | | | |
| Turn On Level | UVLO(on) | UVLO_ON | | | 8.7 | V |
| Turn Off Level | UVLO(off) | UVLO_OFF | 7 | | | V |
| Shutdown Current | DIM=Low, over 30ms | IOFFVIN | | 40 | | μA |
| Operating Current | DIM=High, Switching at no load | IQVIN | | 5 | | mA |
| **Boost Converter** | | | | | | |
| Switching Frequency | | FSW | 180 | 200 | 220 | KHz |
| Boost Maximum Duty Cycle | Switching frequency=200KHz | DMAX | 85 | 90 | 95 | % |
| DRV Gate Drive | Source current, $V_{IN}$=12V | CR_DRV | | 1.2 | | A |
| | Sink current, $V_{IN}$=12V | CF_DRV | | 1.3 | | A |
| DRV Output High Clamp Level | $V_{CC}$=24V | DRV_H | | 12 | | V |
| DRV pin Rising Time | DRV pin load=1nF | TR_DRV | | 75 | | ns |
| DRV pin Falling Time | DRV pin load=1nF | TF_DRV | | 75 | | ns |
| COMP clamp voltage | | VCOMP | | 3.8 | | V |
| **Feedback (FB)** | | | | | | |
| Reference Voltage | | VFB | 0.291 | 0.3 | 0.309 | V |
| Tolerance of Reference Voltage | | | -3.0 | | 3.0 | % |
| **PWM Dimming (DIM)** | | | | | | |
| DIM Voltage threshold | Enable | VDIM_H | 2.5 | | | V |
| | Disable | VDIM_L | | | 1 | V |
| Resistance from DIM pin to GND | | R_DIM | | 150 | | KΩ |
| PWM dimming Frequency | | | 200 | | 30K | Hz |
| Dimming Duty-Cycle | | | 5 | | 100 | % |
| Shutdown Recover Delay Time ($T_{DOWN}$) | | TRSD | | 21 | | ms |
| **Current Sensing (CS)** | | | | | | |
| Current Sense Input Threshold Voltage | | VCS | 0.4 | 0.45 | 0.5 | V |
| LEB time | | T_LEB | | 275 | | nS |

| PARAMETER | CONDITIONS | SYM | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| **Over Voltage Protection** | | | | | | |
| Over Voltage Threshold | OVP | VOVP | 1.86 | 2 | 2.14 | V |
| **Output Short Circuit Protection** | | | | | | |
| Output Short Voltage Threshold | OSP | VOSP | | 0.17 | | V |
| **Over Temperature Protection** | | | | | | |
| OTP Trip Point | | | | 150 | | °C |
| De-Bounce Point | | | | 30 | | °C |

## Typical Performance Characteristics

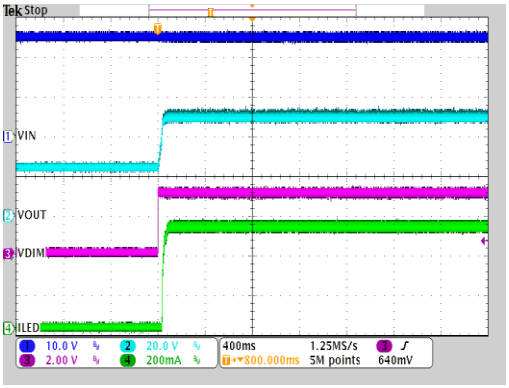



Fig. 1 $V_{IN}$=24V, "DIM Turn On, Duty=100%"

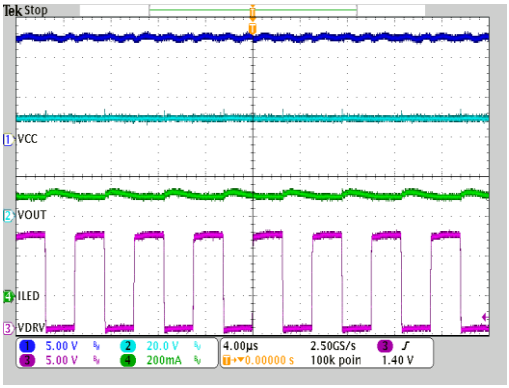



Fig. 2 $V_{CC}$=24V, "Steady State, Duty=100%"

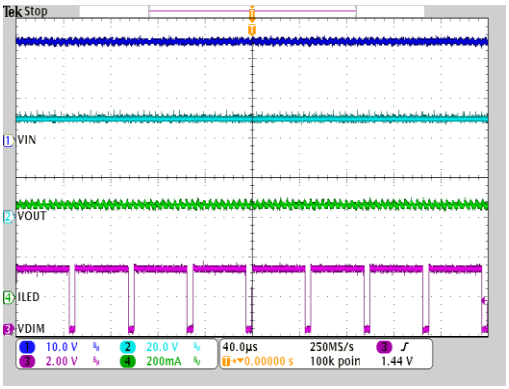



Fig. 3 $V_{IN}$=24V, "$f_{DIM}$=20kHz ,Dim Duty=90%"

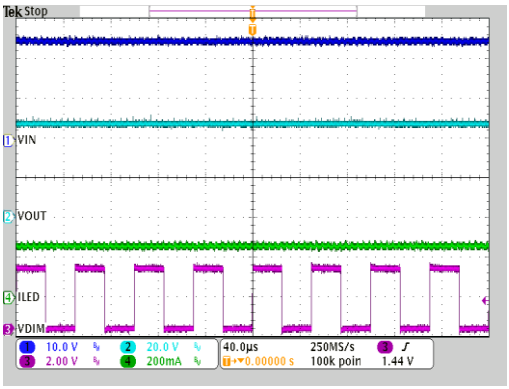



Fig. 4 $V_{IN}$=24V, " $f_{DIM}$=20kHz, Duty=50%

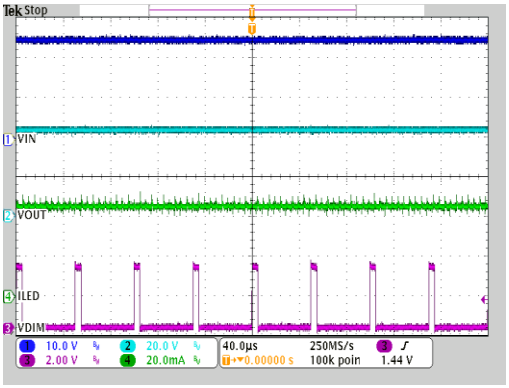



Fig. 5 $V_{IN}$=24V, "$f_{DIM}$=20kHz, Dim Duty=10%"

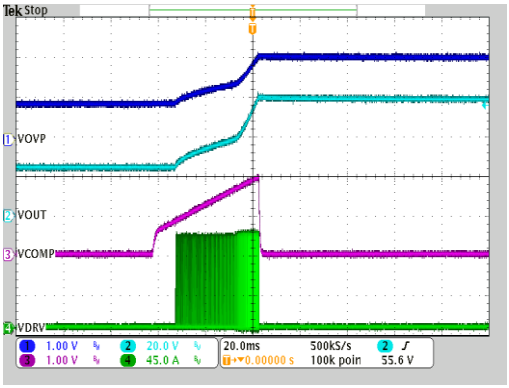



Fig. 6 $V_{IN}$=24V, "LED Open Protection , Duty=100%

# Application Information

## Operation Overview

The LD5857 is designed for current-mode control power converters. It features current-mode control, including cycle-by cycle current limit and the simplified loop compensation.

## Output Drive Stage

An output stage of a CMOS buffer, with typical driving capability of 1.2A/-1.3A, is incorporated to drive the power MOSFET directly. The output voltage is clamped at 12V to protect the MOSFET gate even when the VCC voltage rises over 12V.

## Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across the VCC pin. It would turn on the LD5857 as it detects there's enough supply voltage to drive the power MOSFET. As shown in Fig. 7, a hysteresis is built in to prevent shutdown from the voltage dip during start up. The turn-on and turn-off threshold level are set at 10.0V and 8V, respectively.

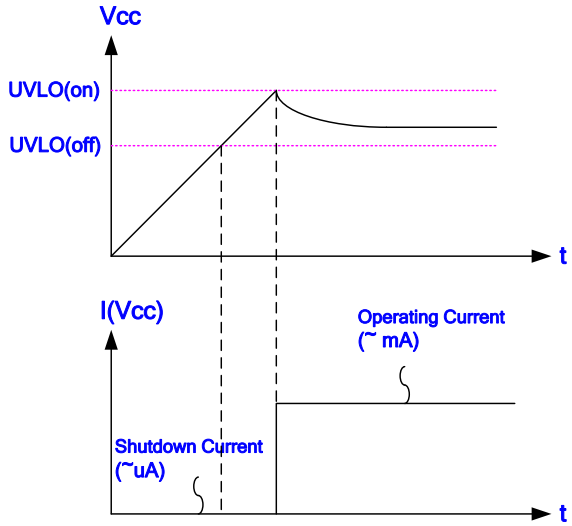



Fig. 7

## LED Open Protection and OVP Trip Point

If there's open in LED string, $V_{OUT}$ will start to boost up OVP voltage. Once it rises over the threshold of around 2.0V, the MOSFET will disable drive output (DRV).

$$V_{OVP} = 2.0 \times \frac{R_B + R_A}{R_B}$$

Place the bypass capacitor ($C_{OVP}$) between OVP and signal ground as close as possible. It's superior to suppress the noise and protect OVP from abnormal condition.

## Programming the LED Current

Select a proper external current sense resistor ($R_{FB,}$ see below parameter) to set the LED current.

$$R_{FB} = \frac{0.3V}{I_{LED}}$$

## Dimming Output of LED Current

The output current can be achieved by applying a PWM signal to DIM pin, the brightness is adjusted in direct proportion to the width of duty cycles. This frequency of input signal varies in the range from 200Hz to 30KHz . Also the LD5857 can program analog diming with software control. The dimming linearity offset is approaching to 1%( typ.).

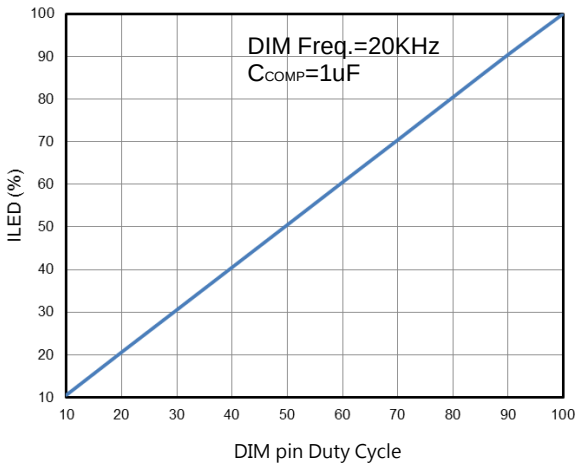



Fig8. The Curve between LED Current and DIM duty

## Current Sensing and Leading-edge Blanking

The LD5857 detects the primary MOSFET current across CS pin for the protection of cycle-by-cycle current limit. The voltage threshold of the current sensing pin is set at 0.45V maximum. The MOSFET peak current can be obtained as below.

$$I_{PEAK(MAX)} = \frac{0.45V}{R_{CS}}$$

A 275ns leading-edge blanking (LEB) time is set in CS pin to prevent the false-triggering from the current spike. The R-C filter is eliminable in those low power applications, for LD5857 features pulse width of the turn-on spikes below 275ns and the negative spike of the CS pin below -0.5V.

However, the pulse width of the turn-on spike is determined according to the output power, circuit design and PCB layout. It is strongly recommended to add a smaller R-C filter for large power application to avoid CS pin from being damaged by the negative turn-on spike.

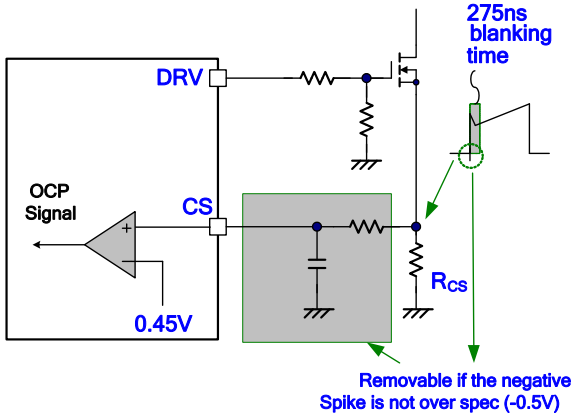



Fig. 9

Select a proper value of $V_{RCS}$ according to the below equation to avoid the output power from being clamped due to the limit of $V_{COMP\_CLAMP}$.

$$1.5 + (1.3 \times Duty_{(\%)}) + (3 \times I_{L(Peak)} \times R_{CS}) < 3.5V$$

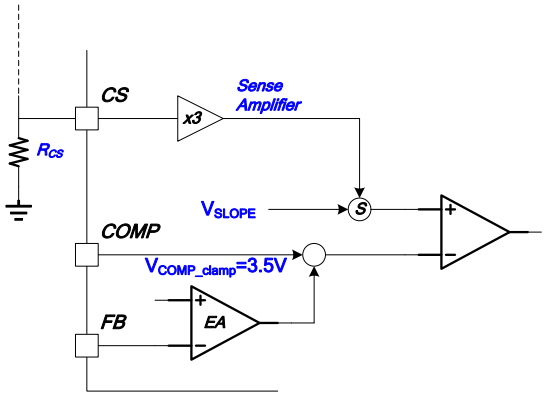



Fig. 10

## Thermal Protection

Thermal protection limits the whole power dissipation in this device. When the junction temperature reaches 150°C, the thermal sensor will send a signal of shutdown logic to disable the device and would not resume operation unless the IC's junction temperature cools down for 30°C

## PCB Layout Guideline

It's recommended to separate the high frequency switching current from the low-level control signals in layout. The high switching current (MOSFET, inductor, gate driver and FB return ends) may disturb the low-level signals in the feedback loop and protection circuitry. As a result, it may cause the control function to behave abnormally. To avoid these side effects, a few guidelines are recommended for the PCB layout as below.

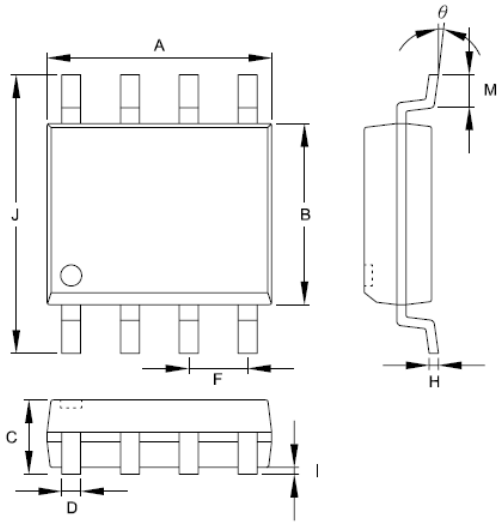
1. Route the VIN bypass capacitor and the signal ground close to the IC as possible. The traces between capacitor and VIN pin should be short as possible to avoid noise interference.

2. Use broader traces for VIN, VOUT and power ground. Those components connected to VIN, VOUT and power ground carry high input/output current, such as power MOSFET and decoupling capacitors. To minimize power loss in these traces, the resistance of traces should be kept as low as possible.

3. Use broader traces between power MOSFET drain, inductor and diode since they often carry high current in these traces. To minimize power loss in these traces, the resistance of traces should be minimized as possible.
4. Keep the gate drive traces short and broad around the IC driver output, DRV pin, and the power MOSFET. The driving traces have a high current spike during inverter operation. To minimize power MOSFET switching loss or oscillation voltage in the gate driver signal, the drive traces should be as broad and short as possible to minimize resistance and parasitic inductance.

# Package Information

## SOP-8




| Symbols | Dimensions in Millimeters | | Dimensions in Inch | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.178 | 0.254 | 0.007 | 0.010 |
| I | 0.102 | 0.254 | 0.004 | 0.010 |
| J | 5.791 | 6.198 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| Rev. | Date | Change Notice |
|---|---|---|
| 00 | 4/15/2014 | Original Specification |