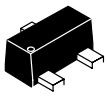
Bias Resistor Transistor

NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

LDTC144TET1G
S-LDTC144TET1G



SC-89

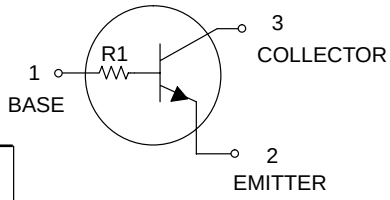
- **Applications**

  Inverter, Interface, Driver

- **Features**

  1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
  2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
  3) Only the on/off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	50	V
Collector-emitter voltage	V_{CEO}	50	V
Emitter-base voltage	V_{EBO}	5	
Collector current	I_C	100	mA
Collector power dissipation	Pc	200	mW
Junction temperature	Tj	150	°C
Storage temperature	Tstg	–55 to +150	°C

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTC144TET1G S-LDTC144TET1G	H5	47	-	3000/Tape & Reel
LDTC144TET3G S-LDTC144TET3G	H5	47	-	10000/Tape & Reel

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	50	–	–	V	I_C=10μA
Collector-emitter breakdown voltage	BV_{CEO}	50	–	–	V	I_C=2.0mA
Emitter-base breakdown voltage	BV_{EBO}	5	–	–	V	I_E=50μA
Collector cutoff current	I_{CBO}	–	–	0.5	μA	V_{CB}=50V
Emitter cutoff current	I_{EBO}	–	–	0.5	μA	V_{EB}=4V
Collector-emitter saturation voltage	$V_{CE(sat)}$	–	–	0.3	V	I_C/I_B=5mA/0.5mA
DC current transfer ratio	h_{FE}	100	250	600	–	V_{CE}=5V, I_C=1mA
Input resistance	R_1	32.9	47	61.1	kΩ	–
Transition frequency	f_T *	–	250	–	MHz	V_{CE}=10V, I_E= –5mA, f=100MHz

Characteristics of built-in transistor

●Electrical characteristic curves

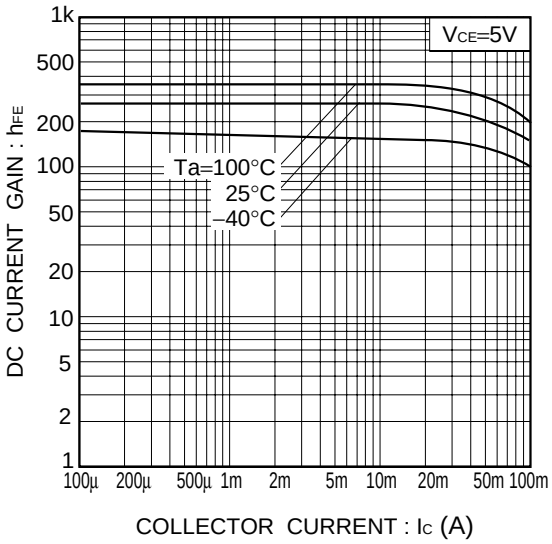


Fig.1 DC current gain vs. collector current

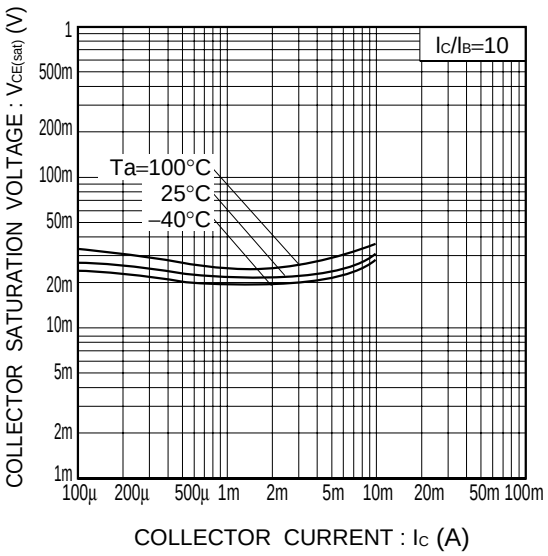


Fig.2 Collector-emitter saturation voltage vs. collector current

LDTC144TET1G;S-LDTC144TET1G

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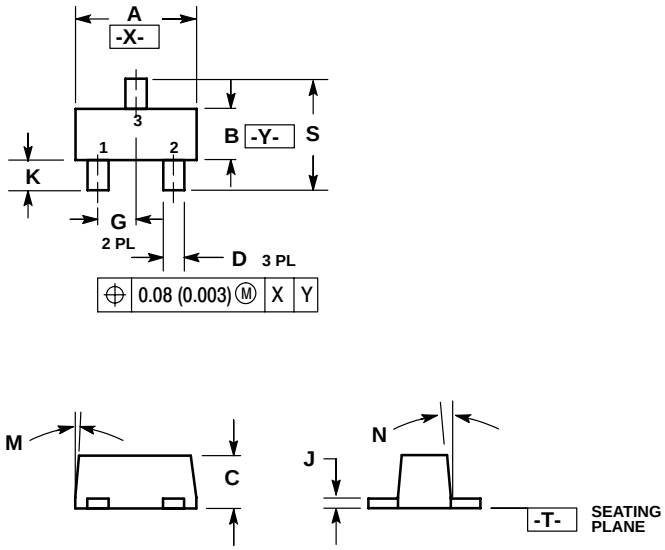
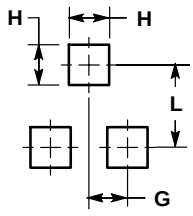


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS