

### Features

- N-Channel enhancement mode device
- DMOS structure
- Lower capacitances for broadband operation
- Common source configuration
- Lower noise floor
- Applications
  - Broadband linear operation
  - 500 MHz to 1200 MHz

### ABSOLUTE MAXIMUM RATINGS AT 25° C

| Parameter            | Symbol        | Rating      | Units |
|----------------------|---------------|-------------|-------|
| Drain-Source Voltage | $V_{DS}$      | 65          | V     |
| Gate-Source Voltage  | $V_{GS}$      | 20          | V     |
| Drain-Source Current | $I_{DS}$      | 2.8         | A     |
| Power Dissipation    | $P_D$         | 26.5        | W     |
| Junction Temperature | $T_J$         | 200         | °C    |
| Storage Temperature  | $T_{STG}$     | -55 to +150 | °C    |
| Thermal Resistance   | $\theta_{JC}$ | 6.6         | °C/W  |

### TYPICAL DEVICE IMPEDANCE

| F (MHz) | $Z_{IN}$ ( $\Omega$ ) | $Z_{LOAD}$ ( $\Omega$ ) |
|---------|-----------------------|-------------------------|
| 500     | 0.60 - j9.5           | 10.0 + j17.0            |
| 1000    | 1.4 - j1.0            | 4.85 + j7.9             |
| 1200    | 1.5 - j3.5            | 5.7 + j5.7              |

$V_{DD} = 28V, I_{DQ} = 100\text{ mA}, P_{OUT} = 10\text{ W}$

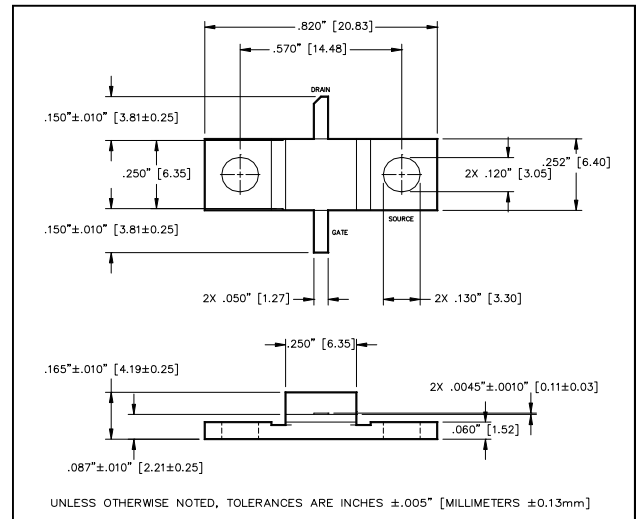
$Z_{IN}$  is the series equivalent input impedance of the device from gate to source.

$Z_{LOAD}$  is the optimum series equivalent load impedance as measured from drain to ground.

### ELECTRICAL CHARACTERISTICS AT 25°C

| Parameter                      | Symbol       | Min | Max  | Units         | Test Conditions   |
|--------------------------------|--------------|-----|------|---------------|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$   | 65  | -    | V             | $V_{GS} = 0.0\text{ V}, I_{DS} = 4.0\text{ mA}$   |
| Drain-Source Leakage Current   | $I_{DSS}$    | -   | 2.0  | mA            | $V_{DS} = 28.0\text{ V}, V_{GS} = 0.0\text{ V}$   |
| Gate-Source Leakage Current    | $I_{GSS}$    | -   | 2.0  | $\mu\text{A}$ | $V_{GS} = 20.0\text{ V}, V_{DS} = 0.0\text{ V}$   |
| Gate Threshold Voltage         | $V_{GS(TH)}$ | 2.0 | 6.0  | V             | $V_{DS} = 10.0\text{ V}, I_{DS} = 20.0\text{ mA}$   |
| Forward Transconductance       | $G_M$        | 160 | -    | mS            | $V_{DS} = 10.0\text{ V}, I_{DS} 200.0\text{ mA}, 80\text{-}30\text{ }\mu\text{s Pulse}$       |
| Input Capacitance              | $C_{ISS}$    | -   | 14   | pF            | $V_{DS} = 28.0\text{ V}, F = 1.0\text{ MHz}$  |
| Output Capacitance             | $C_{OSS}$    | -   | 10   | pF            | $V_{DS} = 28.0\text{ V}, F = 1.0\text{ MHz}$  |
| Reverse Capacitance            | $C_{RSS}$    | -   | 4.8  | pF            | $V_{DS} = 28.0\text{ V}, F = 1.0\text{ MHz}$  |
| Power Gain                     | $G_P$        | 10  | -    | dB            | $V_{DD} = 28.0\text{ V}, I_{DQ} = 100\text{ mA}, P_{OUT} = 10.0\text{ W}, F = 1.0\text{ GHz}$ |
| Drain Efficiency               | $\eta_D$     | 50  | -    | %             | $V_{DD} = 28.0\text{ V}, I_{DQ} = 100\text{ mA}, P_{OUT} = 10.0\text{ W}, F = 1.0\text{ GHz}$ |
| Load Mismatch Tolerance        | VSWR-T       | -   | 20:1 | -             | $V_{DD} = 28.0\text{ V}, I_{DQ} = 100\text{ mA}, P_{OUT} = 10.0\text{ W}, F = 1.0\text{ GHz}$ |

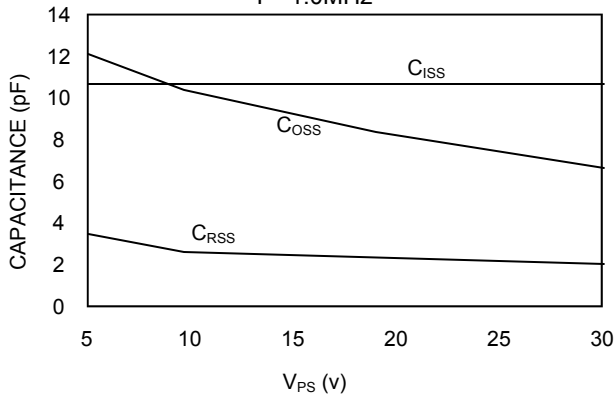
### Package Outline



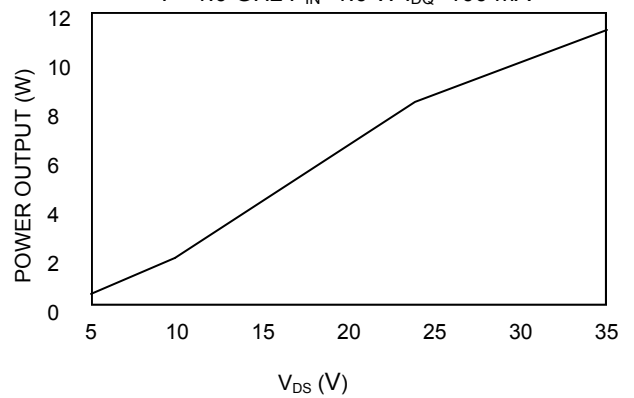
| LETTER | MILLIMETERS |       | INCHES |      |
|--------|-------------|-------|--------|------|
|        | MIN         | MAX   | MIN    | MAX  |
| A      | 20.70       | 20.96 | .815   | .825 |
| B      | 14.35       | 14.61 | .565   | .575 |
| C      | 13.72       | 14.22 | .540   | .560 |
| D      | 6.27        | 6.53  | .247   | .257 |
| E      | 6.22        | 6.48  | .245   | .255 |
| F      | 6.22        | 6.48  | .245   | .255 |
| G      | 1.14        | 1.40  | .045   | .055 |
| H      | 2.92        | 3.18  | .115   | .125 |
| J      | 1.40        | 1.65  | .055   | .065 |
| K      | 1.96        | 2.46  | .077   | .097 |
| L      | 3.61        | 4.37  | .142   | .172 |
| M      | .08         | .15   | .003   | .006 |

**Typical Broadband Performance Curves**

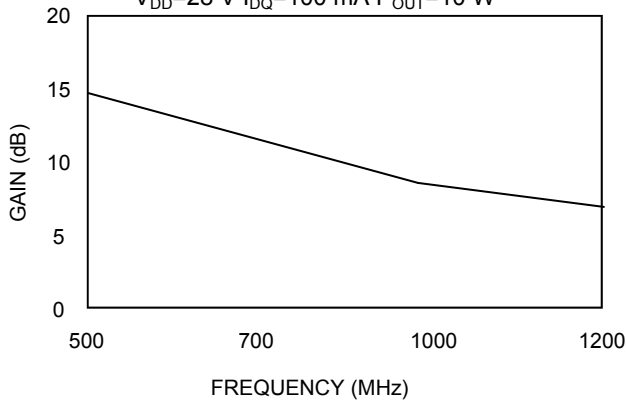
**CAPACITANCES vs VOLTAGE**  
 $F = 1.0\text{MHz}$



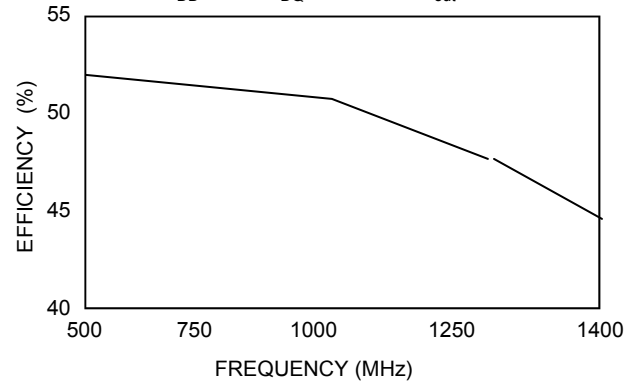
**POWER OUTPUT vs VOLTAGE**  
 $F = 1.0\text{ GHz } P_{IN} = 1.0\text{ W } I_{DQ} = 100\text{ mA}$



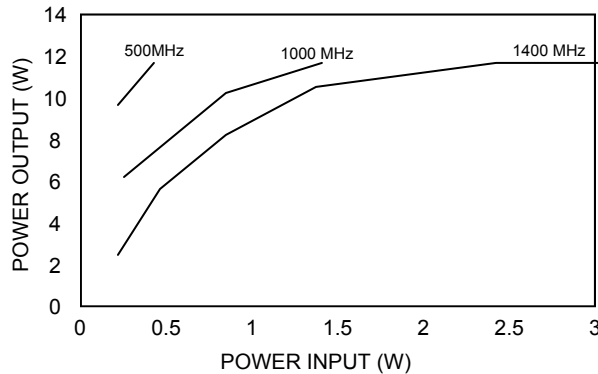
**GAIN vs FREQUENCY**  
 $V_{DD} = 28\text{ V } I_{DQ} = 100\text{ mA } P_{OUT} = 10\text{ W}$



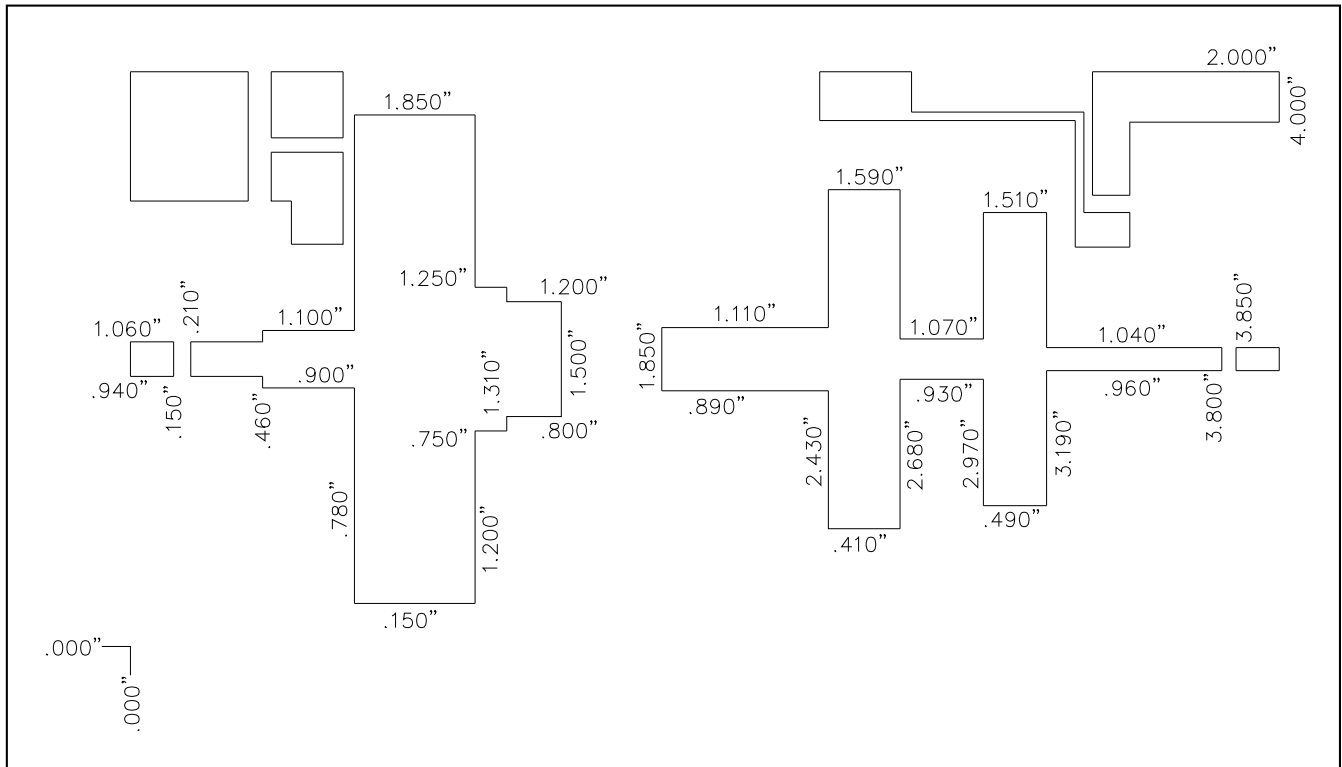
**EFFICIENCY vs FREQUENCY**  
 $V_{DD} = 28\text{ V } I_{DQ} = 100\text{ mA } P_{out} = 10\text{ W}$



**POWER OUTPUT vs POWER INPUT**  
 $V_{DD} = 28\text{ V } I_{DQ} = 50\text{ mA}$



**TEST FIXTURE CIRCUIT DIMENSIONS**



**TEST FIXTURE ASSEMBLY**

