



LatticeECP/EC Family Data Sheet

Version 01.3

Features

■ Extensive Density and Package Options

- 1.5K to 41K LUT4s
- 65 to 576 I/Os
- Density migration supported

■ sysDSP™ Block (LatticeECP™ Versions)

- High performance multiply and accumulate
- 4 to 10 blocks
 - 4 to 10 36x36 multipliers or
 - 16 to 40 18x18 multipliers or
 - 32 to 80 9x9 multipliers

■ Embedded and Distributed Memory

- 18 Kbits to 645 Kbits sysMEM™ Embedded Block RAM (EBR)
- Up to 163 Kbits distributed RAM
- Flexible memory resources:
 - Distributed and block memory

■ Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:

- LVCMOS 3.3/2.5/1.8/1.5/1.2
- LVTTTL
- SSTL 3/2 Class I, II, SSTL18 Class I
- HSTL 18 Class I, II, III, HSTL15 Class I, III
- PCI
- LVDS, Bus-LVDS, LVPECL, RSDS

■ Dedicated DDR Memory Support

- Implements interface up to DDR400 (200MHz)

■ sysCLOCK™ PLLs

- Up to 4 analog PLLs per device
- Clock multiply, divide and phase shifting

■ System Level Support

- IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
- SPI boot flash interface
- 1.2V power supply

■ Low Cost FPGA

- Features optimized for mainstream applications
- Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

| Device | LFEC1 | LFEC3 | LFEC6/ LFCEP6 | LFEC10/ LFCEP10 | LFEC15/ LFCEP15 | LFEC20/ LFCEP20 | LFEC33/ LFCEP33 | LFEC40/ LFCEP40 |
|---------------------------------------|-------|-------|------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| PFU/PFF Rows | 12 | 16 | 24 | 32 | 40 | 44 | 64 | 64 |
| PFU/PFF Columns | 16 | 24 | 32 | 40 | 48 | 56 | 64 | 80 |
| PFUs/PFFs | 192 | 384 | 768 | 1280 | 1920 | 2464 | 4096 | 5120 |
| LUTs (K) | 1.5 | 3.1 | 6.1 | 10.2 | 15.4 | 19.7 | 32.8 | 41.0 |
| Distributed RAM (Kbits) | 6 | 12 | 25 | 41 | 61 | 79 | 131 | 164 |
| EBR SRAM (Kbits) | 18 | 55 | 92 | 277 | 350 | 424 | 535 | 645 |
| EBR SRAM Blocks | 2 | 6 | 10 | 30 | 38 | 46 | 58 | 70 |
| sysDSP Blocks ¹ | — | — | 4 | 5 | 6 | 7 | 8 | 10 |
| 18x18 Multipliers ¹ | — | — | 16 | 20 | 24 | 28 | 32 | 40 |
| V _{CC} Voltage (V) | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| Number of PLLs | 2 | 2 | 2 | 4 | 4 | 4 | 4 | 4 |
| Packages and I/O Combinations: | | | | | | | | |
| 100-pin TQFP (14 x 14 mm) | 67 | 67 | | | | | | |
| 144-pin TQFP (20 x 20 mm) | 97 | 97 | 97 | | | | | |
| 208-pin PQFP (28 x 28 mm) | 112 | 145 | 147 | 147 | | | | |
| 256-ball fpBGA (17 x 17 mm) | | 160 | 195 | 195 | 195 | | | |
| 484-ball fpBGA (23 x 23 mm) | | | 224 | 288 | 352 | 360 | 360 | |
| 672-ball fpBGA (27 x 27 mm) | | | | | | 400 | 496 | 496 |
| 900-ball fpBGA (31 x 31 mm) | | | | | | | | 576 |

1. LatticeECP devices only.

Introduction

The LatticeECP/EC family of FPGA devices has been optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The LatticeECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC family of FPGA devices. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Architecture Overview

The LatticeECP™-DSP and LatticeEC™ architectures contain an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) as shown in Figures 2-1 and 2-2. In addition, LatticeECP-DSP supports an additional row of DSP blocks as shown in Figure 2-2.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeECP/EC architecture provides up to four PLLs per device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The LatticeECP/EC devices use 1.2V as their core voltage.

Figure 2-1. Simplified Block Diagram, LatticeECP/EC Device (Top Level)

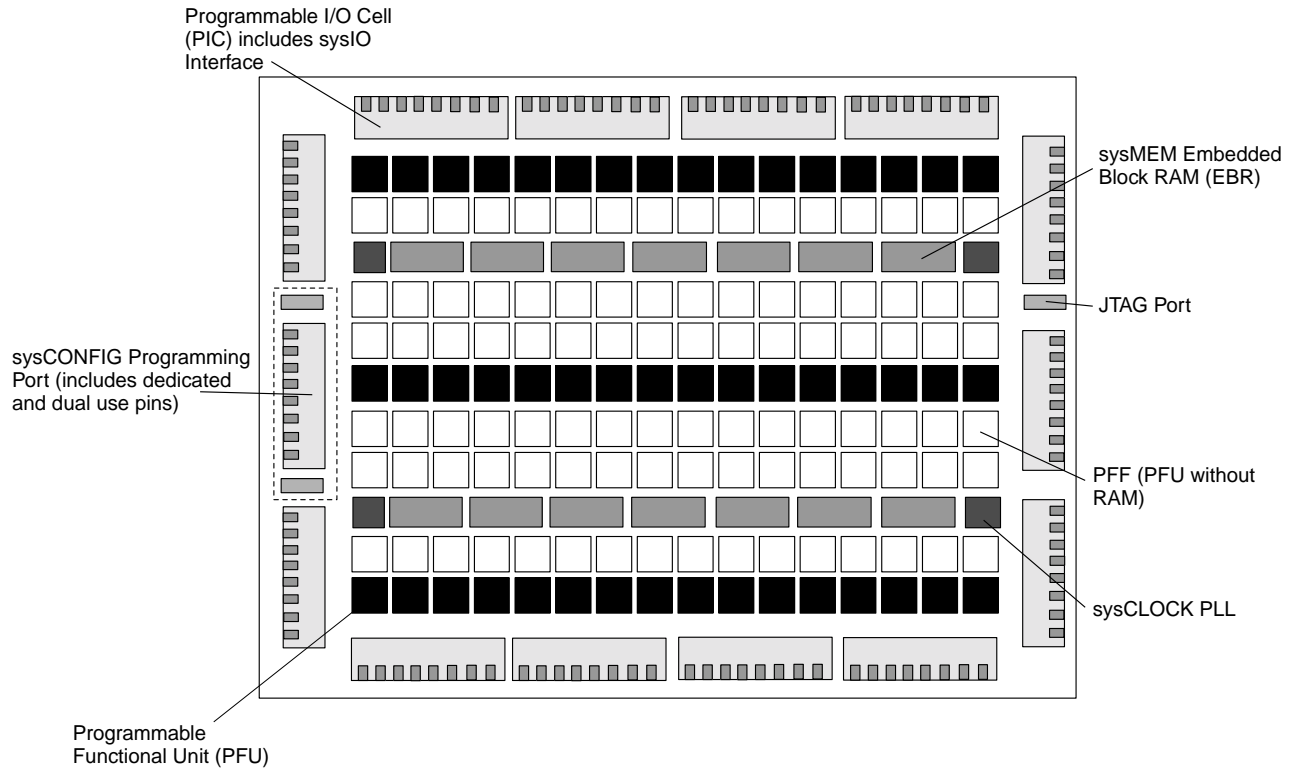
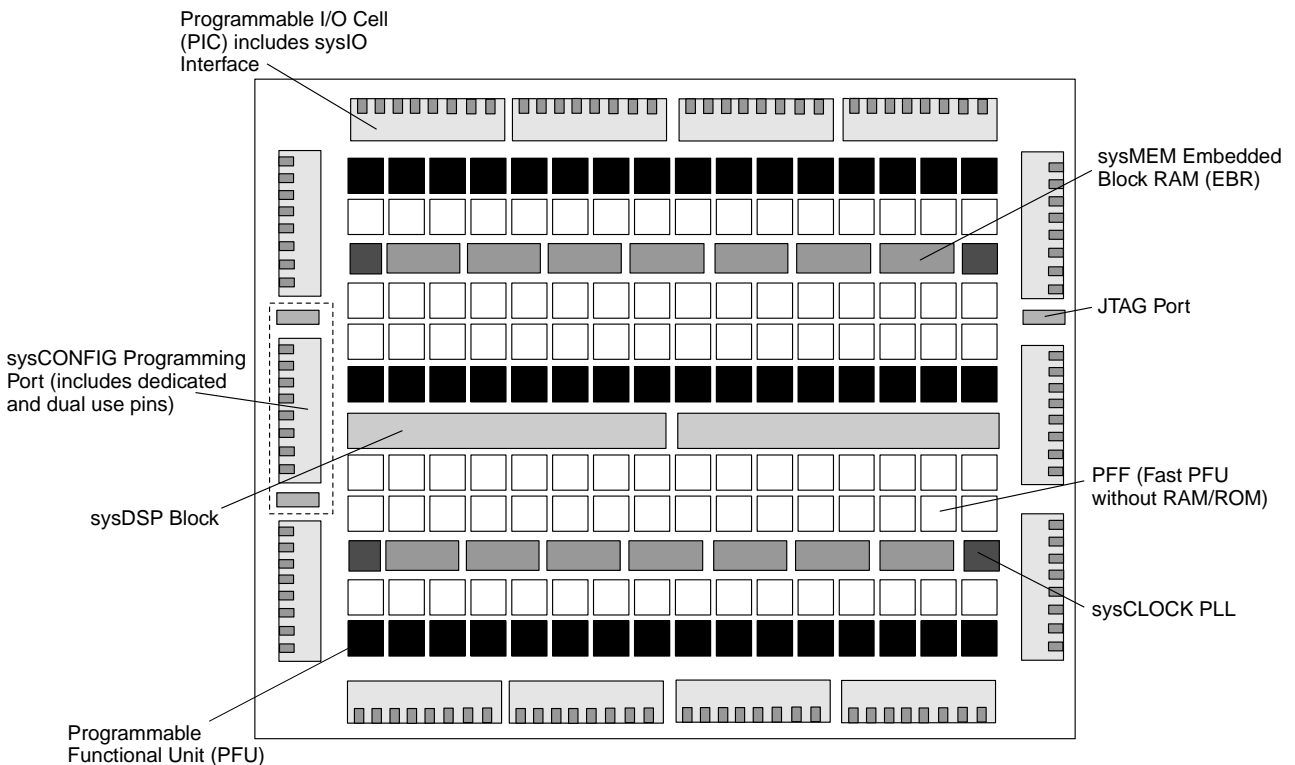


Figure 2-2. Simplified Block Diagram, LatticeECP-DSP Device (Top Level)

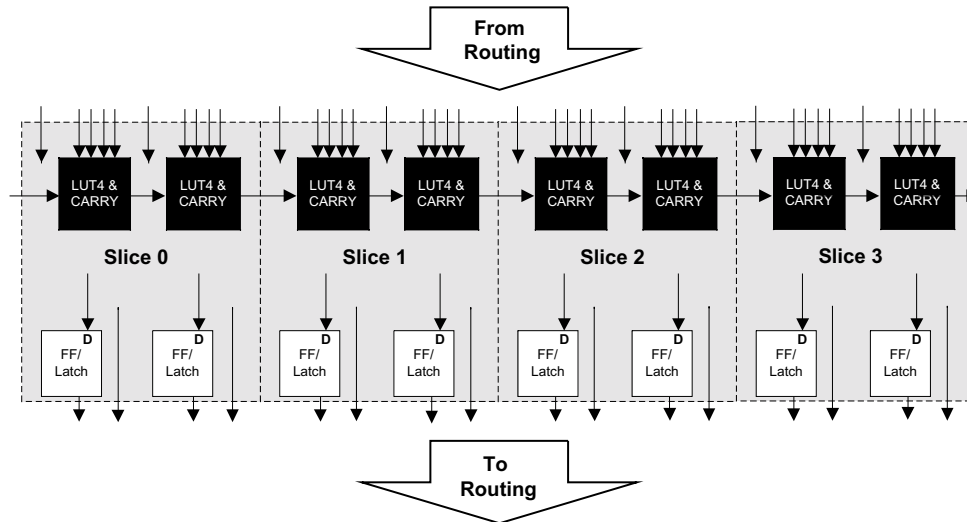


PFU and PFF Blocks

The core of the LatticeECP/EC devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-4. Slice Diagram

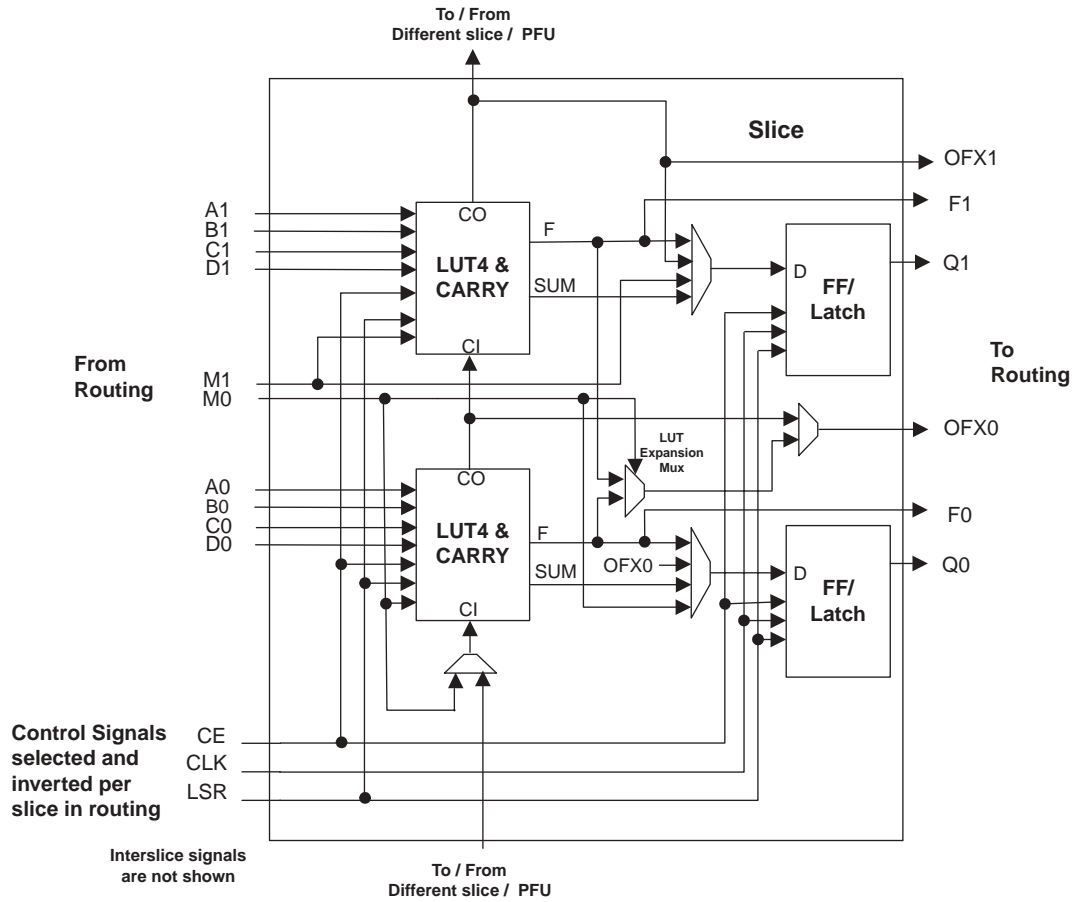


Table 2-1. Slice Signal Descriptions

| Function | Type | Signal Names | Description |
|----------|------------------|----------------|--|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCIN | Fast Carry In ¹ |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register Outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice |
| Output | Inter-PFU signal | FCO | For the right most PFU the fast carry chain output ¹ |

1. See Figure 2-3 for connection details.

2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

| | Logic | Ripple | RAM | ROM |
|-----------|--------------------|-----------------------|---------|-------------|
| PFU Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | SPR16x2 | ROM16x1 x 2 |
| PFF Slice | LUT 4x2 or LUT 5x1 | 2-bit Arithmetic Unit | N/A | ROM16x1 x 2 |

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

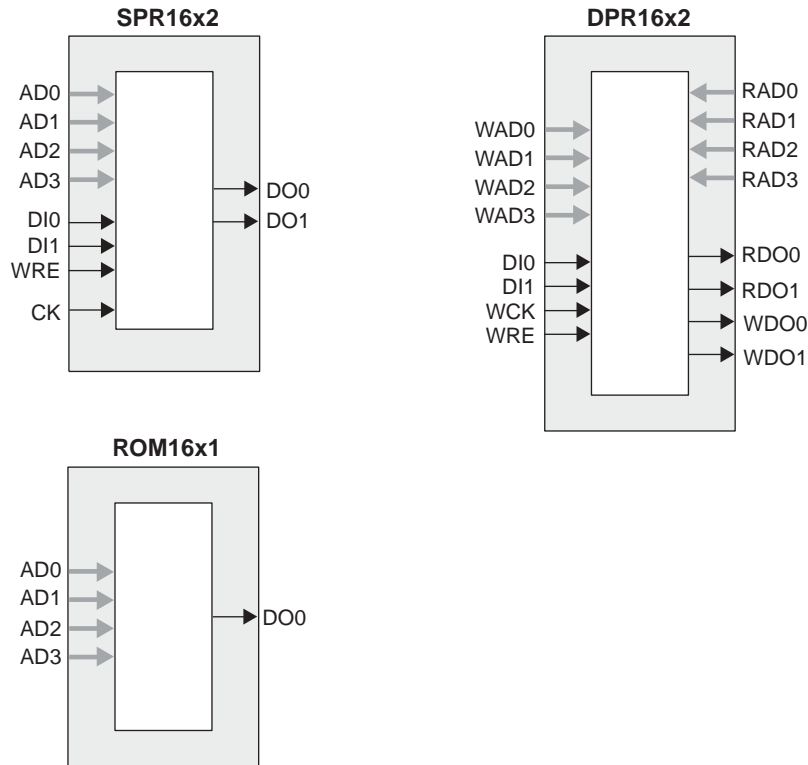
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-5 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on using RAM in LatticeECP/EC devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

| | SPR16x2 | DPR16x2 |
|------------------|---------|---------|
| Number of slices | 1 | 2 |

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-5. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

| Logic | Ripple | RAM ¹ | ROM |
|----------------------------|-------------------|----------------------------|-------------|
| LUT 4x8 or MUX 2x1 x 8 | 2-bit Add x 4 | SPR16x2 x 4 DPR16x2 x 2 | ROM16x1 x 8 |
| LUT 5x4 or MUX 4x1 x 4 | 2-bit Sub x 4 | SPR16x4 x 2 DPR16x4 x 1 | ROM16x2 x 4 |
| LUT 6x 2 or MUX 8x1 x 2 | 2-bit Counter x 4 | SPR16x8 x 1 | ROM16x4 x 2 |
| LUT 7x1 or MUX 16x1 x 1 | 2-bit Comp x 4 | | ROM16x8 x 1 |

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeECP/EC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

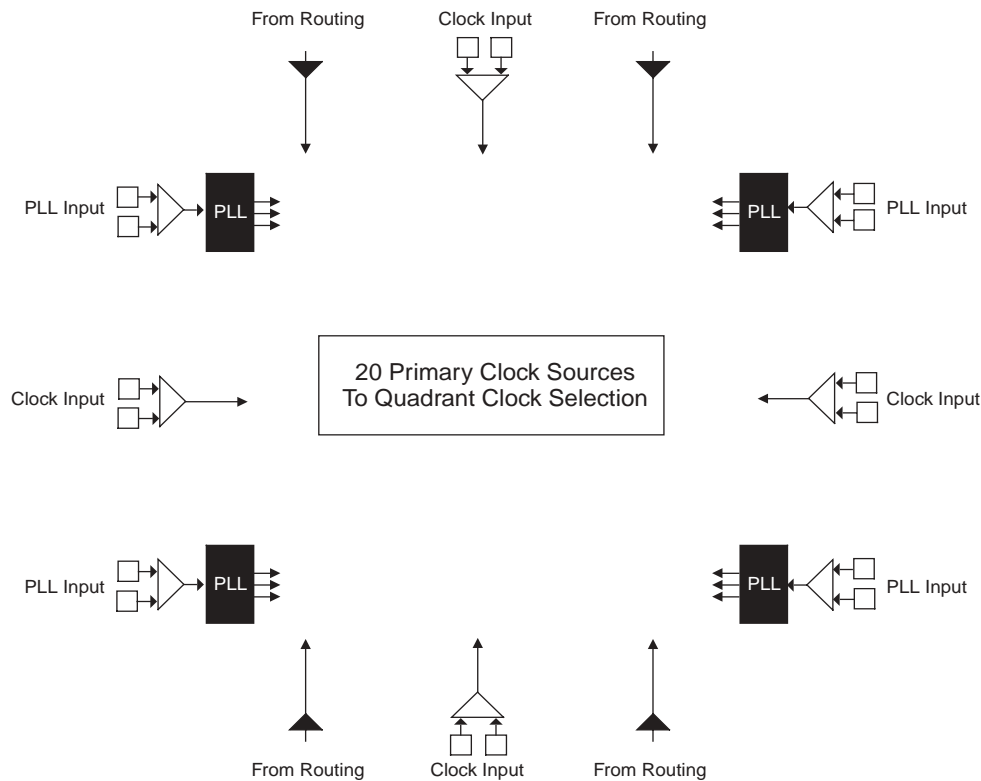
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeECP/EC devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeECP/EC devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-6 shows the 20 primary clock sources.

Figure 2-6. Primary Clock Sources

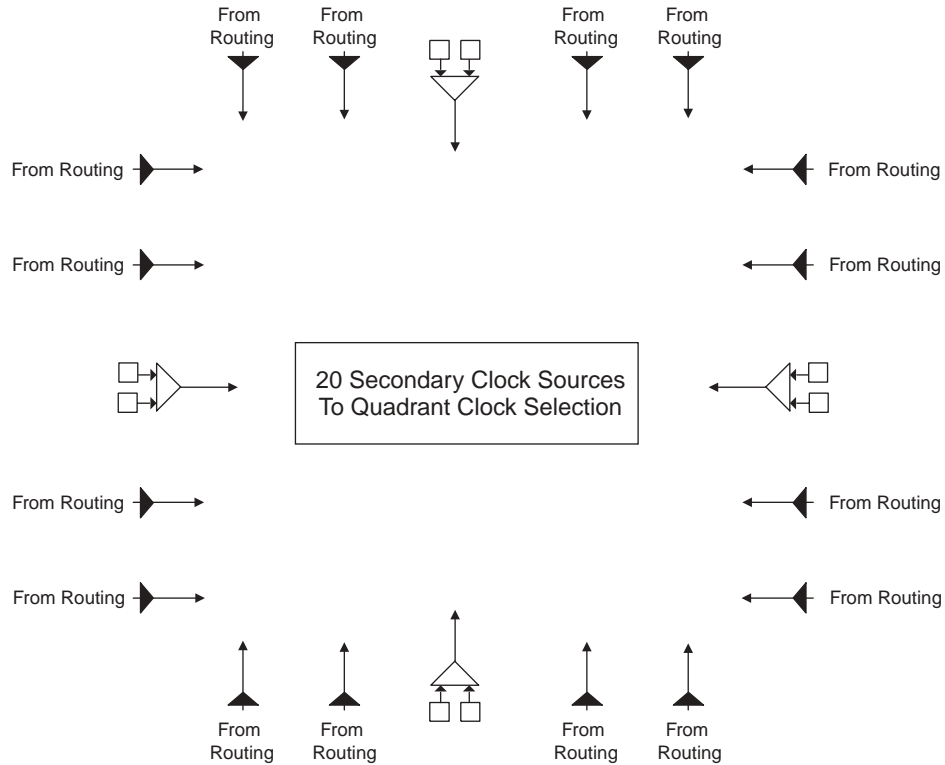


Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeECP/EC devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-7.

Figure 2-7. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeECP/EC devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-8 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-9. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-10.

Figure 2-8. Per Quadrant Primary Clock Selection

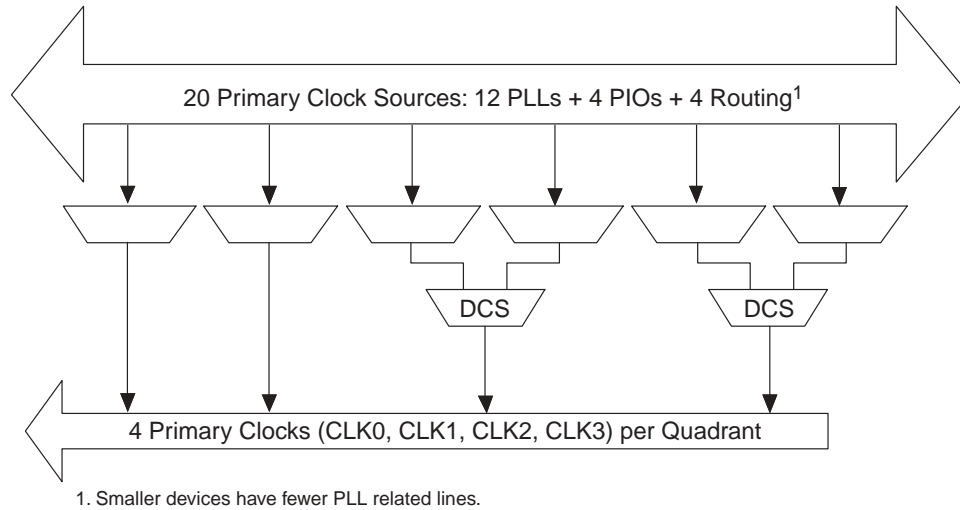


Figure 2-9. Per Quadrant Secondary Clock Selection

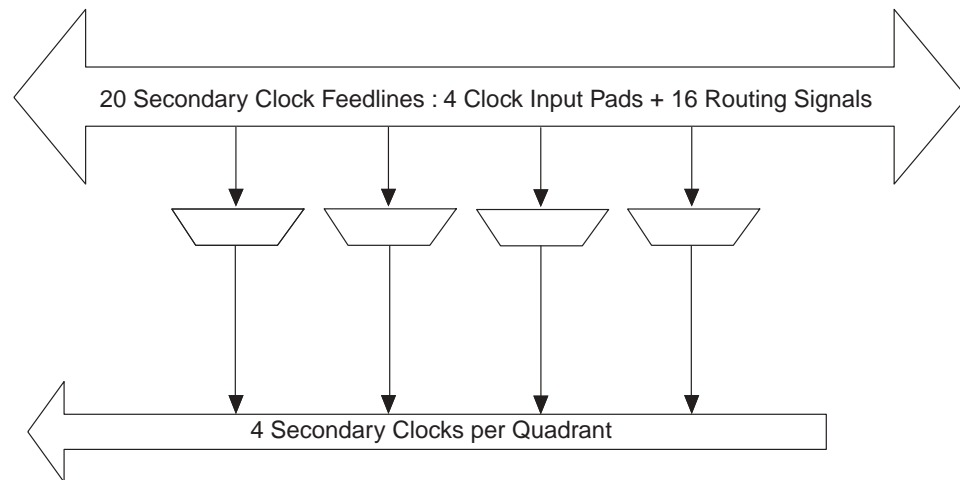
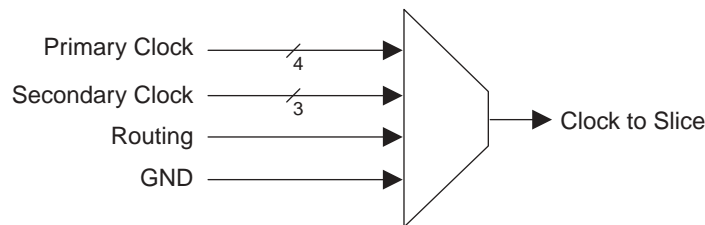


Figure 2-10. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are three sources of feedback signal to the feedback divider: from the CLKOP, from the clock net, or from an external pin. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after

adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, post scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-11. PLL Diagram

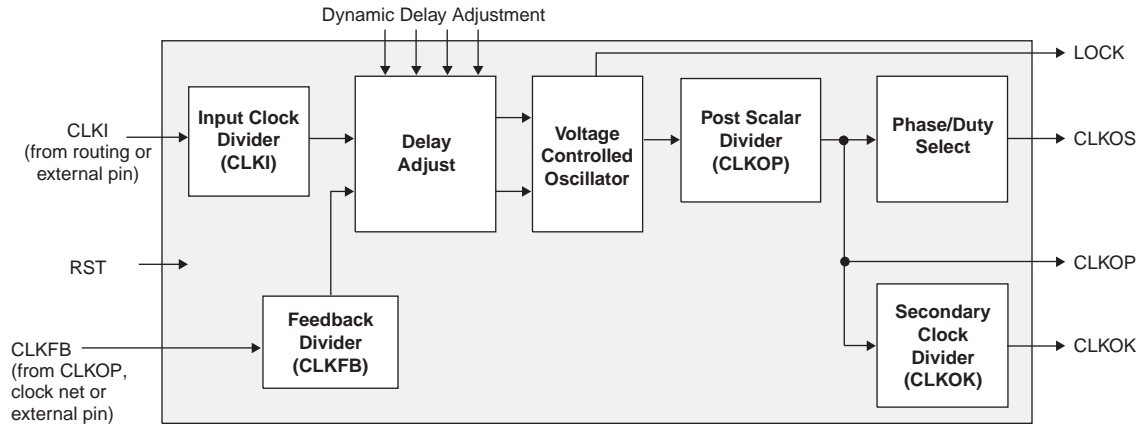


Figure 2-12 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-12. PLL Primitive

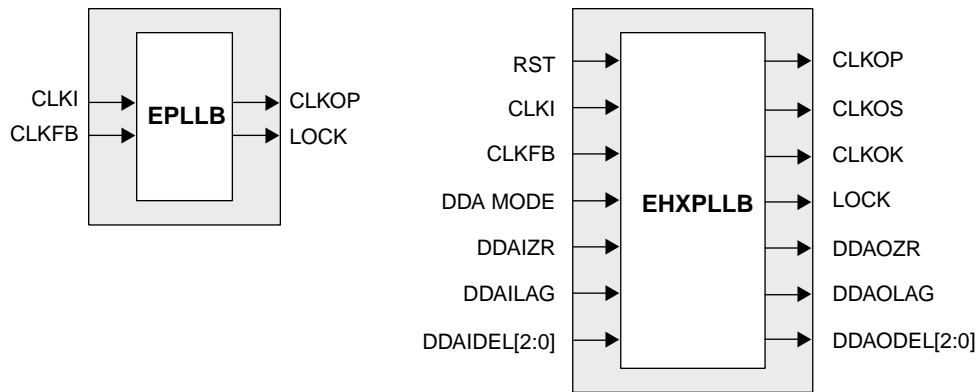


Table 2-5. PLL Signal Descriptions

| Signal | I/O | Description |
|--------------|-----|--|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP, clocknet, or external pin |
| RST | I | "1" to reset PLL |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (No phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| LOCK | O | "1" indicates PLL LOCK to CLKI |
| DDAMODE | I | Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static) |
| DDAIZR | I | Dynamic Delay Zero. "1": delay = 0, "0": delay = on |
| DDAILAG | I | Dynamic Delay Lag/Lead. "1": Lead, "0": Lag |
| DDAIDEL[2:0] | I | Dynamic Delay Input |
| DDAOZR | O | Dynamic Delay Zero Output |
| DDAOLAG | O | Dynamic Delay Lag/Lead Output |
| DDAODEL[2:0] | O | Dynamic Delay Output |

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-13 illustrates the DCS Block Macro.

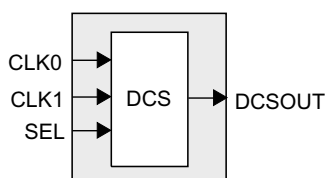
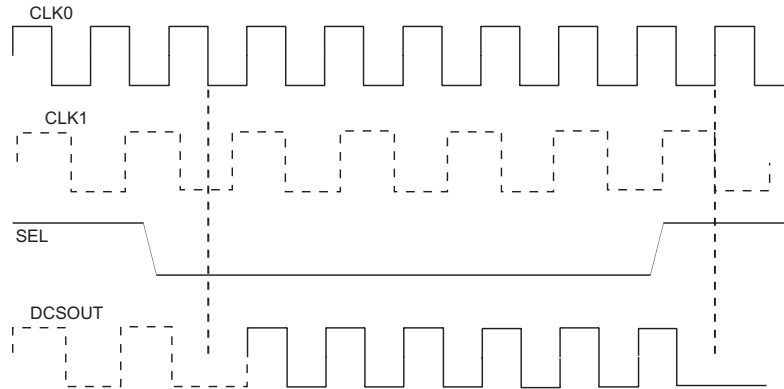
Figure 2-13. DCS Block Primitive

Figure 2-14 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-14. DCS Waveforms



sysMEM Memory

The LatticeECP/EC family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Table 2-6. sysMEM Block Configurations

| Memory Mode | Configurations |
|------------------|----------------|
| Single Port | 8,192 x 1 |
| | 4,096 x 2 |
| | 2,048 x 4 |
| | 1,024 x 9 |
| | 512 x 18 |
| | 256 x 36 |
| True Dual Port | 8,192 x 1 |
| | 4,096 x 2 |
| | 2,048 x 4 |
| | 1,024 x 9 |
| | 512 x 18 |
| Pseudo Dual Port | 8,192 x 1 |
| | 4,096 x 2 |
| | 2,048 x 4 |
| | 1,024 x 9 |
| | 512 x 18 |
| | 256 x 36 |

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

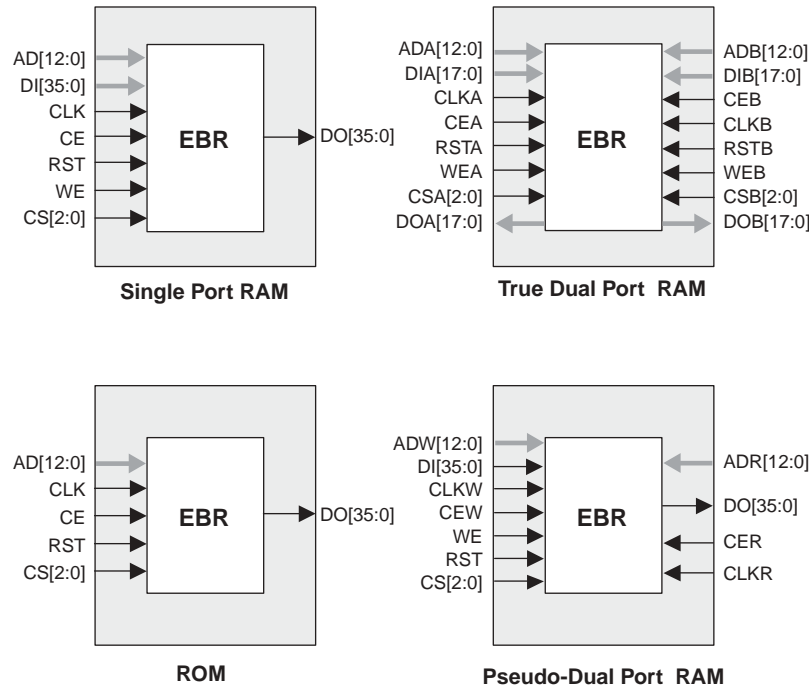
Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-15 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-15. sysMEM EBR Primitives



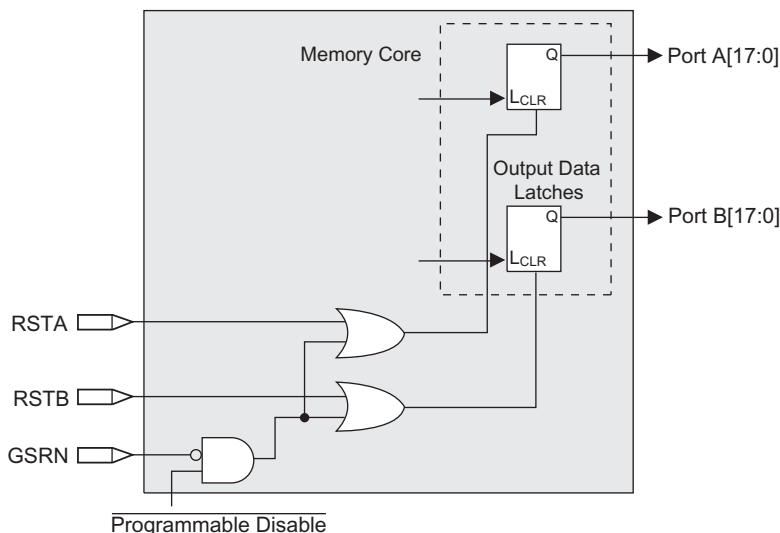
The EBR memory supports three forms of write behavior for single port or dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output.
2. **Write Through** – a copy of the input data appears at the output of the same port, during a write cycle.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-16.

Figure 2-16. Memory Core Reset



For further information on sysMEM EBR block, please see the details of additional technical documentation at the end of this data sheet.

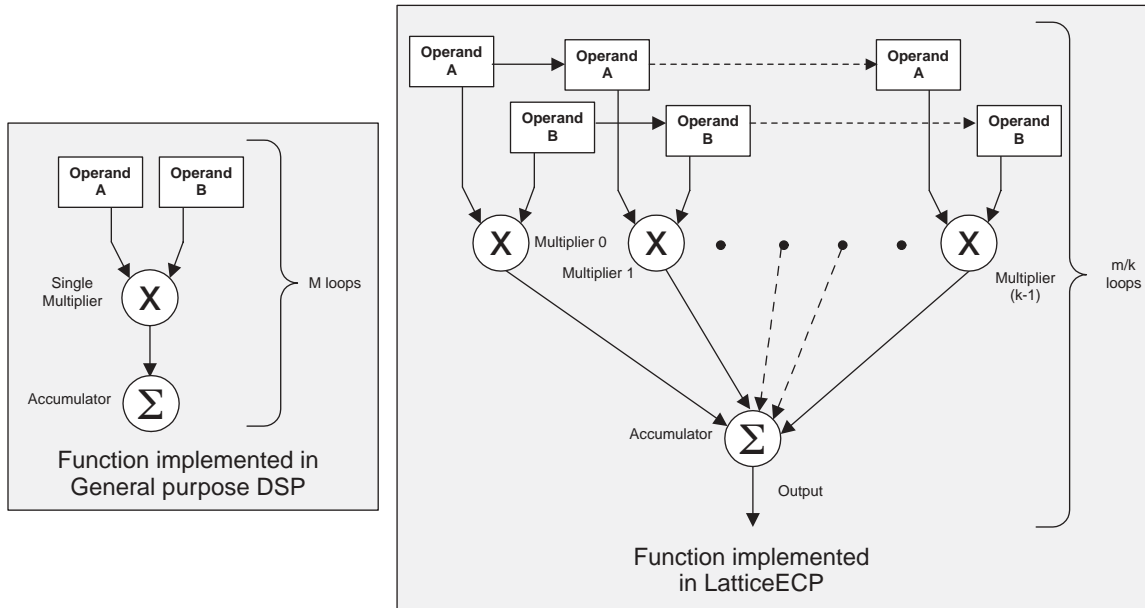
sysDSP Block

The LatticeECP-DSP family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters; Fast Fourier Transforms (FFT) functions, correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate level of parallelism. Figure 2-17 compares the serial and the parallel implementations.

Figure 2-17. Comparison of General DSP and LatticeECP-DSP Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP-DSP family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP-DSP family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADD (Multiply, Addition/Subtraction)
- MULTADDSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends in the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-1 shows the capabilities of the block.

Table 2-7. Maximum Number of Elements in a Block

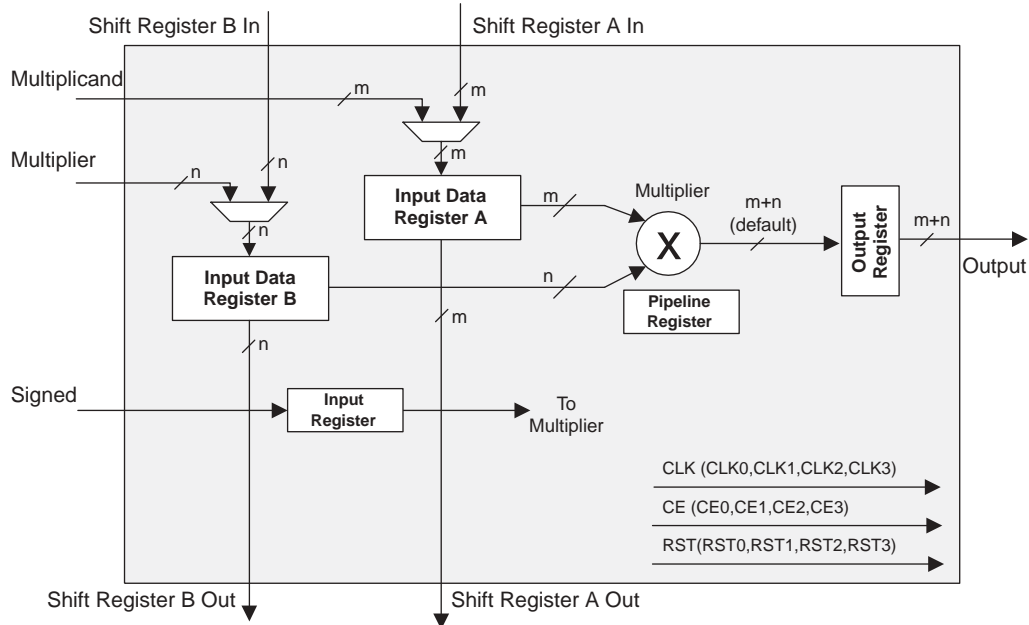
| Width of Multiply | x9 | x18 | x36 |
|-------------------|----|-----|-----|
| MULT | 8 | 4 | 1 |
| MAC | 4 | 2 | — |
| MULTADD | 4 | 2 | — |
| MULTADDSUM | 2 | 1 | — |

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. In addition by selecting 'dynamic operation' in the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle. Similarly by selecting 'Dynamic operation' in the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-18 shows the MULT sysDSP element.

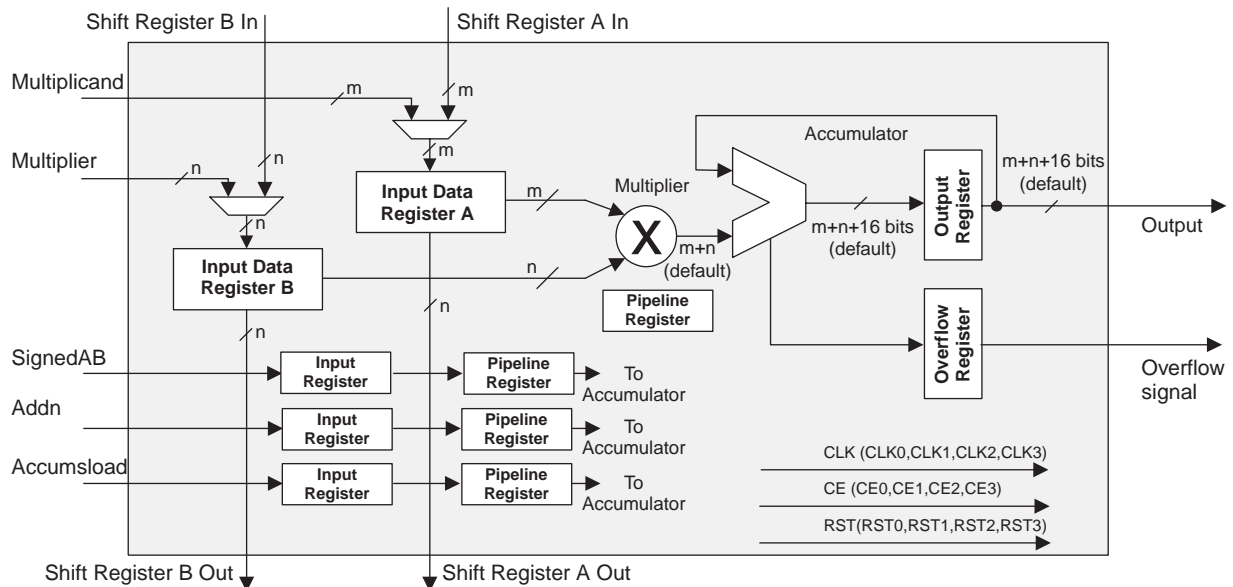
Figure 2-18. MULT sysDSP Element



MAC sysDSP Element

In this case the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-19 shows the MAC sysDSP element.

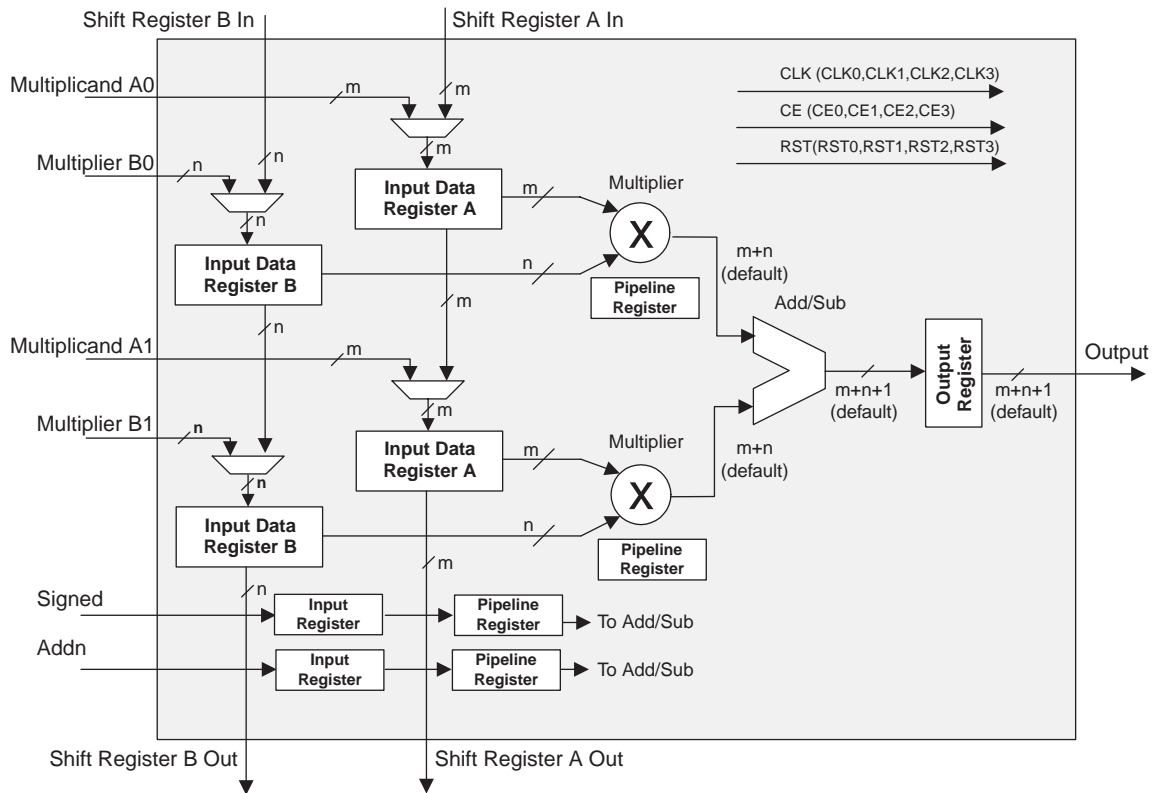
Figure 2-19. MAC sysDSP Element



MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-20 shows the MULTADD sysDSP element.

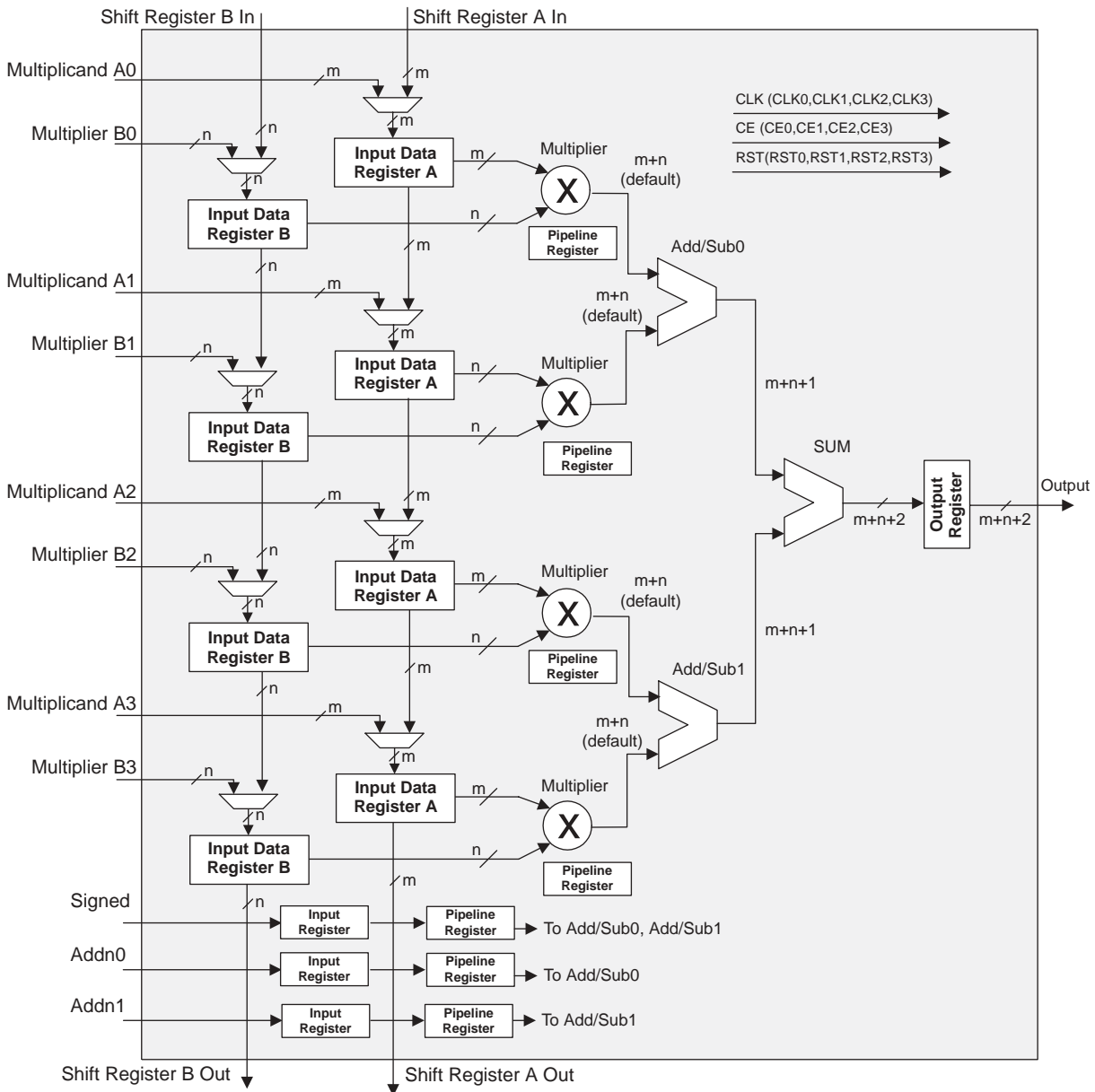
Figure 2-20. MULTADD



MULTADDSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-21 shows the MULTADDSUM sysDSP element.

Figure 2-21. MULTADDSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

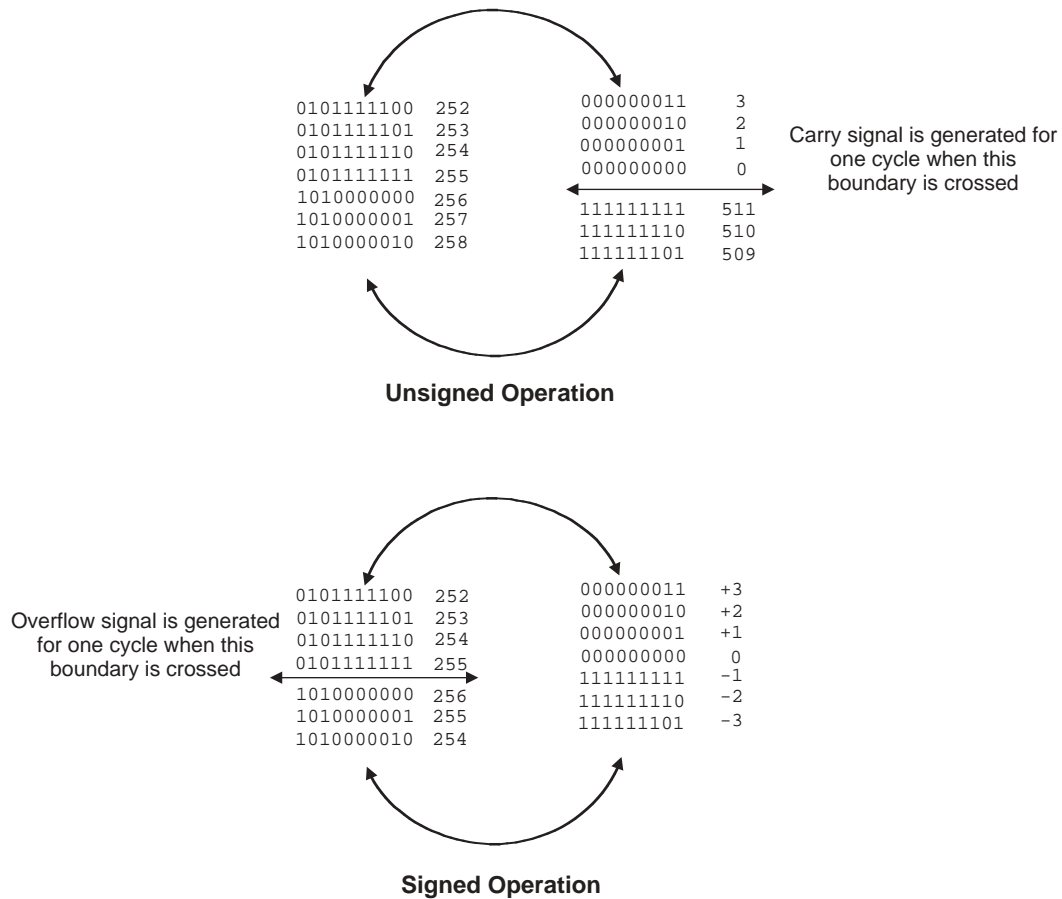
Table 2-8. An Example of Sign Extension

| Number | Unsigned | Unsigned 9-bit | Unsigned 18-bit | Signed | Two's Complement Signed 9-Bits | Two's Complement Signed 18-bits |
|--------|----------|----------------|---------------------|--------|--------------------------------|---------------------------------|
| +5 | 0101 | 000000101 | 0000000000000000101 | 0101 | 000000101 | 0000000000000000101 |
| -6 | 0110 | 000000110 | 0000000000000000110 | 1010 | 111111010 | 1111111111111111010 |

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number then accumulator roll over is said to occur and overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator “roll-over” is said to have occurred and an overflow signal is indicated. Note when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signal for signed and unsigned operands are listed in Figure 2-22.

Figure 2-22. Accumulator Overflow/Underflow Conditions



ispLEVER Module Manager

The user can access the sysDSP block via the ispLEVER Module Manager, which has options to configure each DSP module (or group of modules) or through direct HDL instantiation. Additionally Lattice has partnered Mathworks to support instantiation in the Simulink tool, which is a Graphical Simulation Environment. Simulink works with ispLEVER and dramatically shortens the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IPs planned for LatticeECP DSP are: Bit Correlators, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/ Decoder, Turbo Encoder/Decoders and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IPs.

Resources Available in the LatticeECP Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP family. Table 2-10 shows the maximum available EBR RAM Blocks in each of the LatticeECP family. EBR blocks, together with Distributed RAM can be used to store variables locally for the fast DSP operations.

Table 2-9. Number of DSP Blocks in LatticeECP Family

| Device | DSP Block | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|---------|-----------|----------------|------------------|------------------|
| LFCEP6 | 4 | 32 | 16 | 4 |
| LFCEP10 | 5 | 40 | 20 | 5 |
| LFCEP15 | 6 | 48 | 24 | 6 |
| LFCEP20 | 7 | 56 | 28 | 7 |
| LFCEP33 | 8 | 64 | 32 | 8 |
| LFCEP40 | 10 | 80 | 40 | 10 |

Table 2-10. Embedded SRAM in LatticeECP Family

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) |
|---------|----------------|------------------------|
| LFCEP6 | 10 | 92 |
| LFCEP10 | 30 | 276 |
| LFCEP15 | 38 | 350 |
| LFCEP20 | 46 | 424 |
| LFCEP33 | 58 | 535 |
| LFCEP40 | 70 | 645 |

DSP Performance of the LatticeECP Family

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP family.

Table 2-11. DSP Block Performance of LatticeECP Family

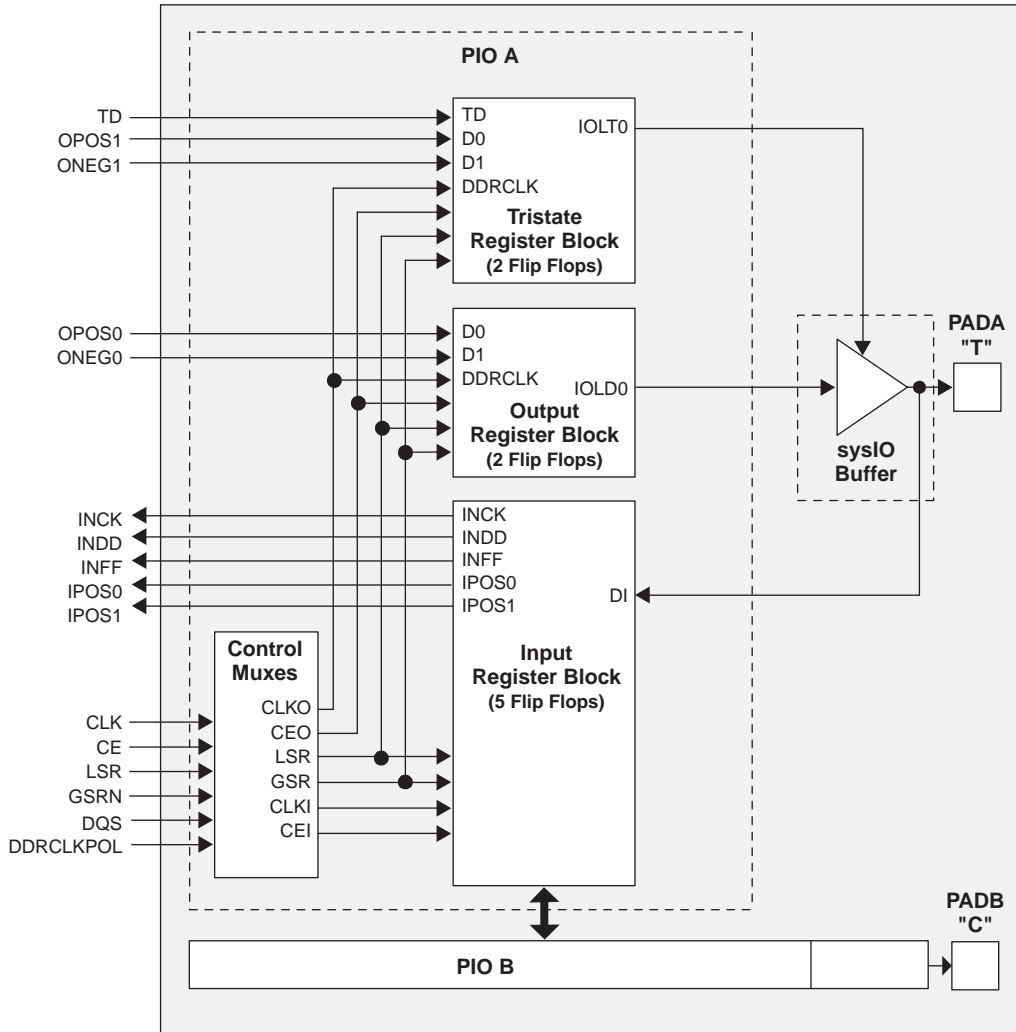
| Device | DSP Block | DSP Performance MMAC |
|---------|-----------|----------------------|
| LFCEP6 | 4 | 3680 |
| LFCEP10 | 5 | 4600 |
| LFCEP15 | 6 | 5520 |
| LFCEP20 | 7 | 6440 |
| LFCEP33 | 8 | 7360 |
| LFCEP40 | 10 | 9200 |

For further information on the sysDSP block, please see details of additional technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-23. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-23. PIC Diagram



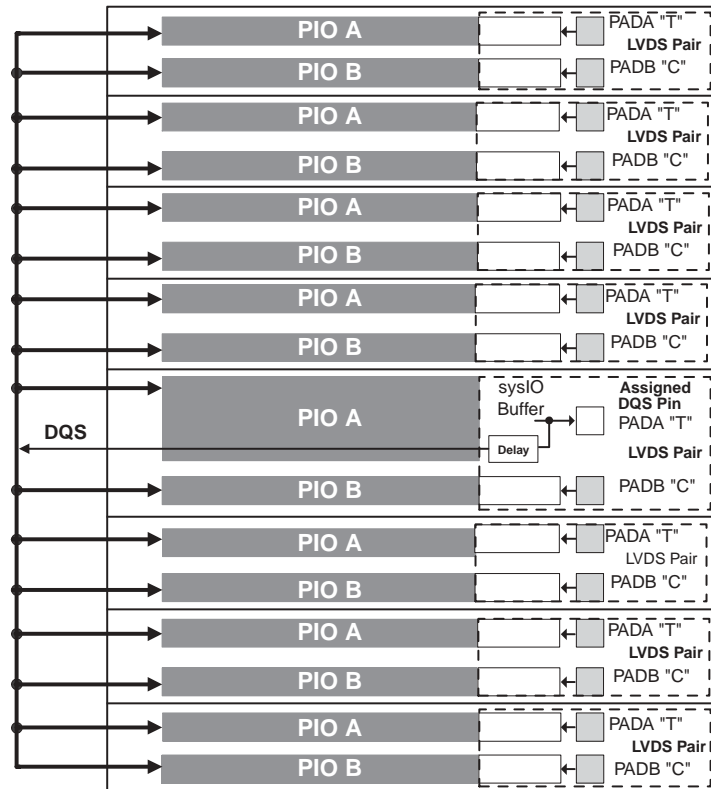
Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C") as shown in Figure 2-24. The PAD Labels "T" and "C" distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-24 shows the assignment of DQS pins in each set of 16 PIOs. The exact DQS pins are shown in a dual function in the Logic Signal Connections table at the end of this data sheet. Additional detail is provided in the Signal Descriptions table at the end of this data sheet. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

Table 2-12. PIO Signal List

| Name | Type | Description |
|--------------|---------------------------------|--|
| CE0, CE1 | Control from the core | Clock enables for input and output block FFs. |
| CLK0, CLK1 | Control from the core | System clocks for input and output blocks. |
| LSR | Control from the core | Local Set/Reset. |
| GSRN | Control from routing | Global Set/Reset (active low). |
| INCK | Input to the core | Input to Primary Clock Network or PLL reference inputs. |
| DQS | Input to PIO | DQS signal from logic (routing) to PIO. |
| INDD | Input to the core | Unregistered data input to core. |
| INFF | Input to the core | Registered input on positive edge of the clock (CLK0). |
| IPOS0, IPOS1 | Input to the core | DDR _X registered inputs to the core. |
| ONEG0 | Control from the core | Output signals from the core for SDR and DDR operation. |
| OPOS0, | Control from the core | Output signals from the core for DDR operation |
| OPOS1 ONEG1 | Tristate control from the core | Signals to Tristate Register block for DDR operation. |
| TD | Tristate control from the core | Tristate signal from the core used in SDR operation. |
| DDRCLKPOL | Control from clock polarity bus | Controls the polarity of the clock (CLK0) that feed the DDR input block. |

Figure 2-24. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-25 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first passes through an optional delay block. This delay, if selected, reduces input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-26 shows the input register waveforms for DDR operation and Figure 2-27 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-25. Input Register Diagram

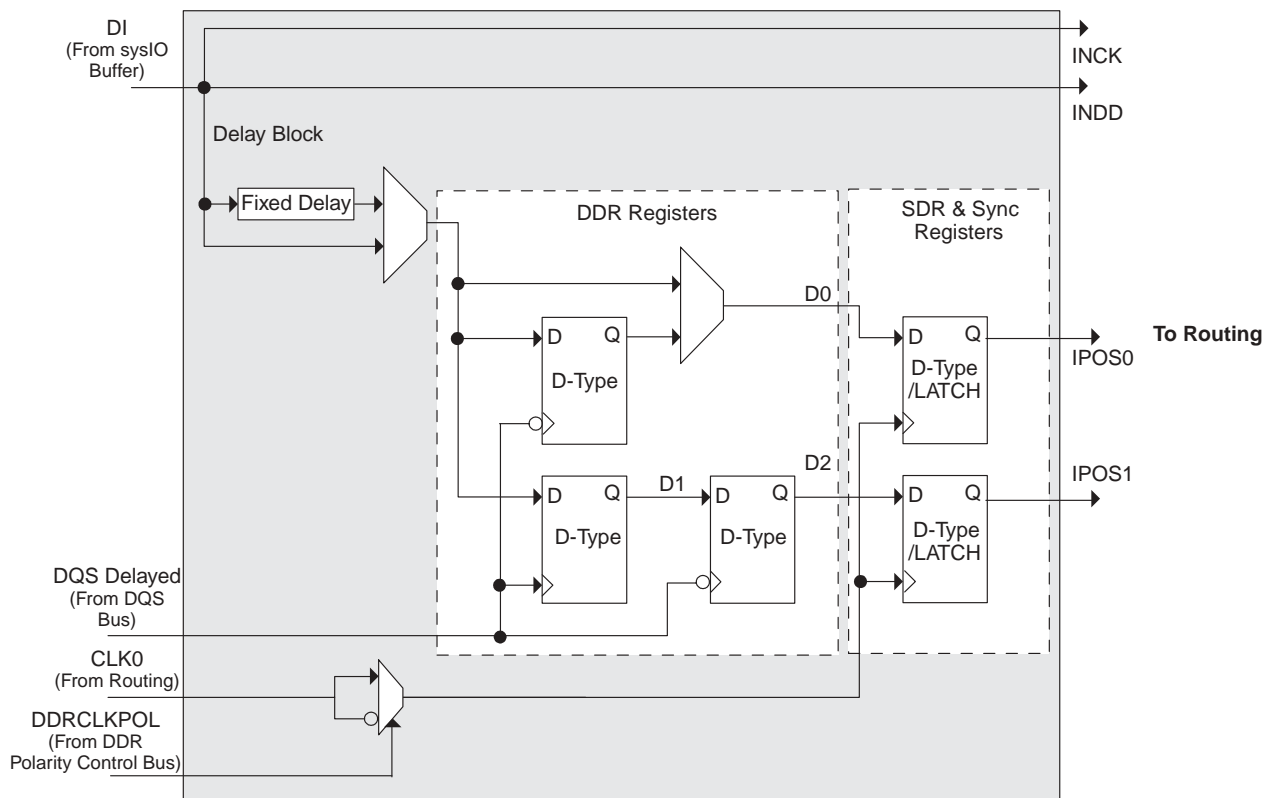


Figure 2-26. Input Register DDR Waveforms

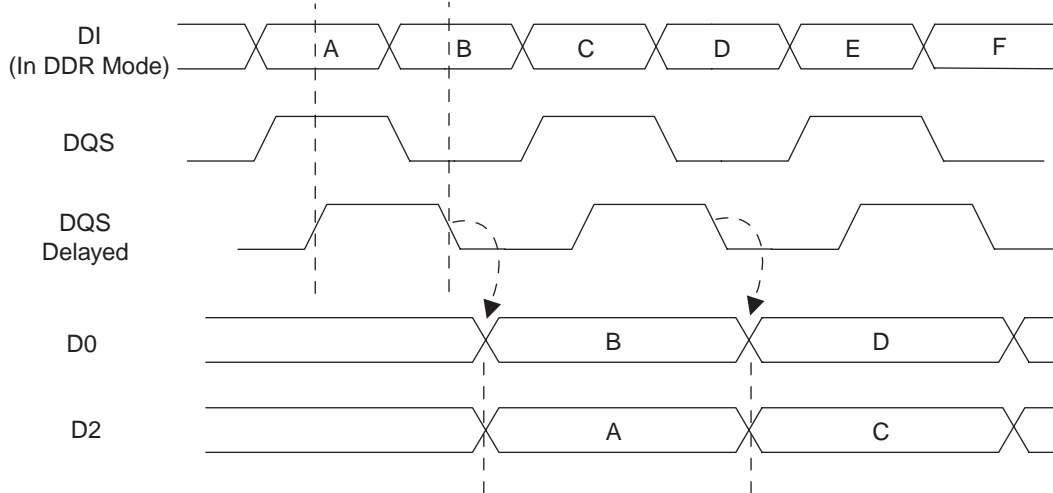
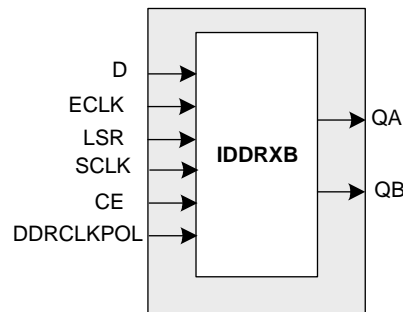


Figure 2-27. INDDRXB Primitive



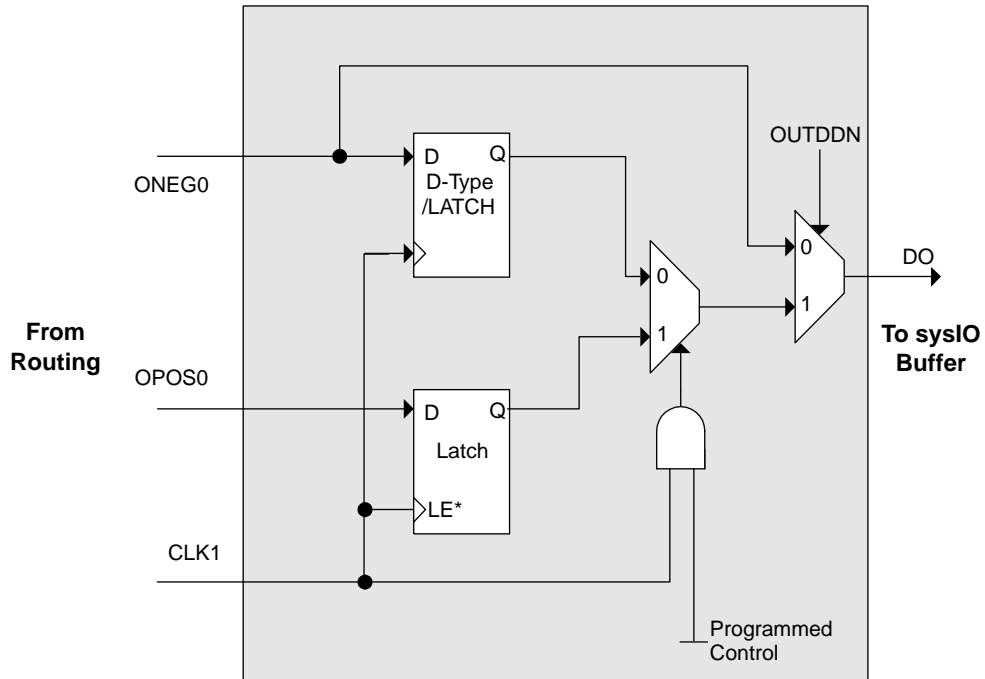
Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-28 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

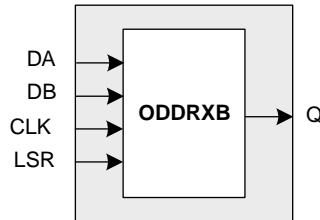
Figure 2-29 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-28. Output Register Block



*Latch is transparent when input is low.

Figure 2-29. ODDRXB Primitive

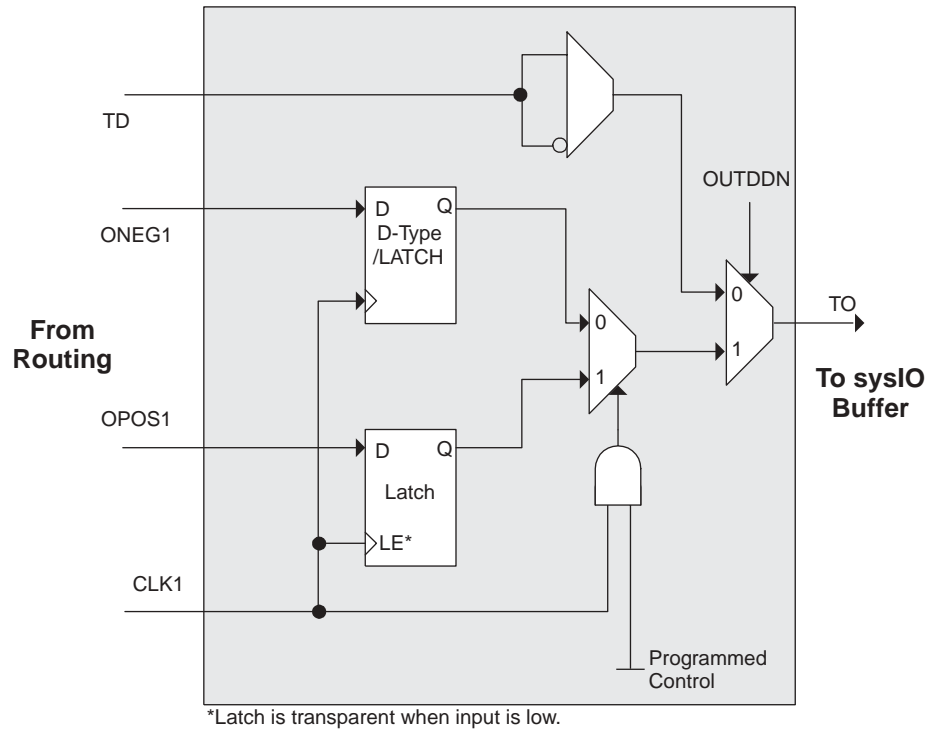


Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-30 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-30. Tristate Register Block



Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the EC devices provide this capability. In addition to these registers, the EC devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-31 and 2-32 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-32. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-31. DQS Local Bus.

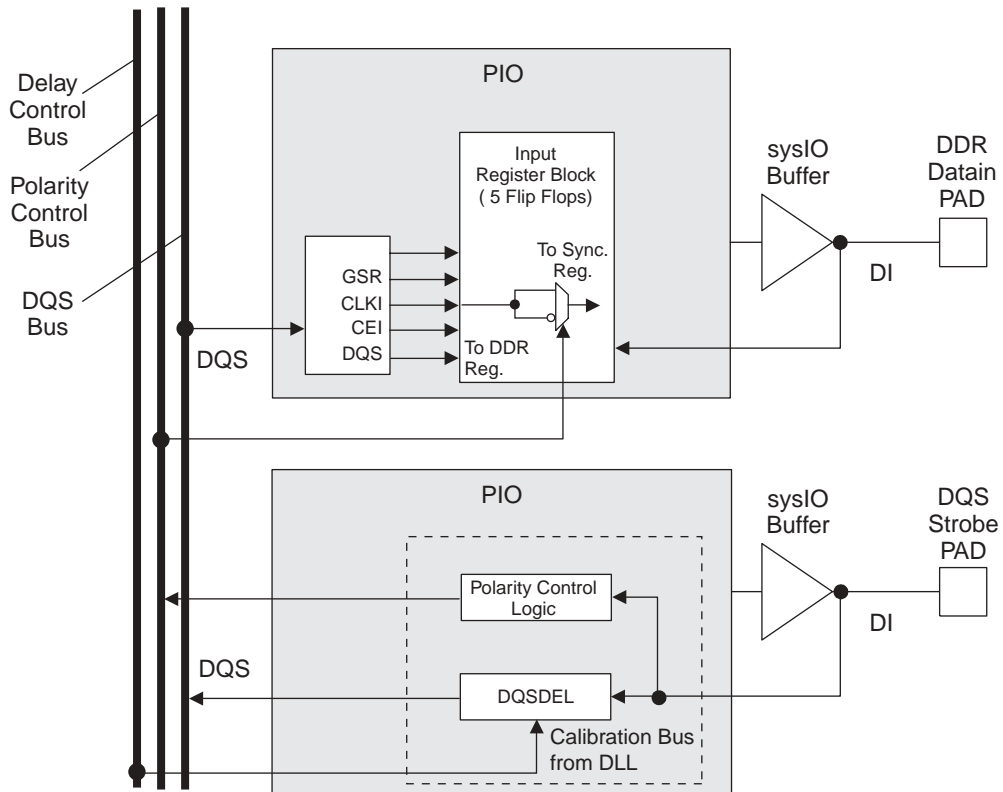
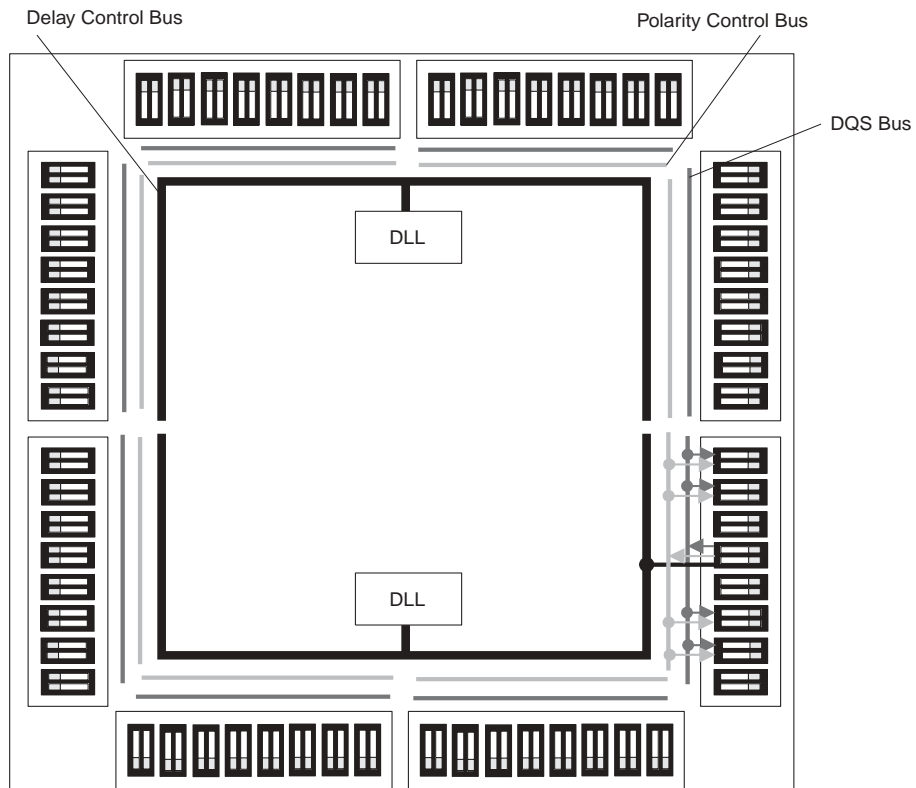


Figure 2-32. DLL Calibration Bus and DQS/DQS Transition Distribution



Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeECP/EC family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

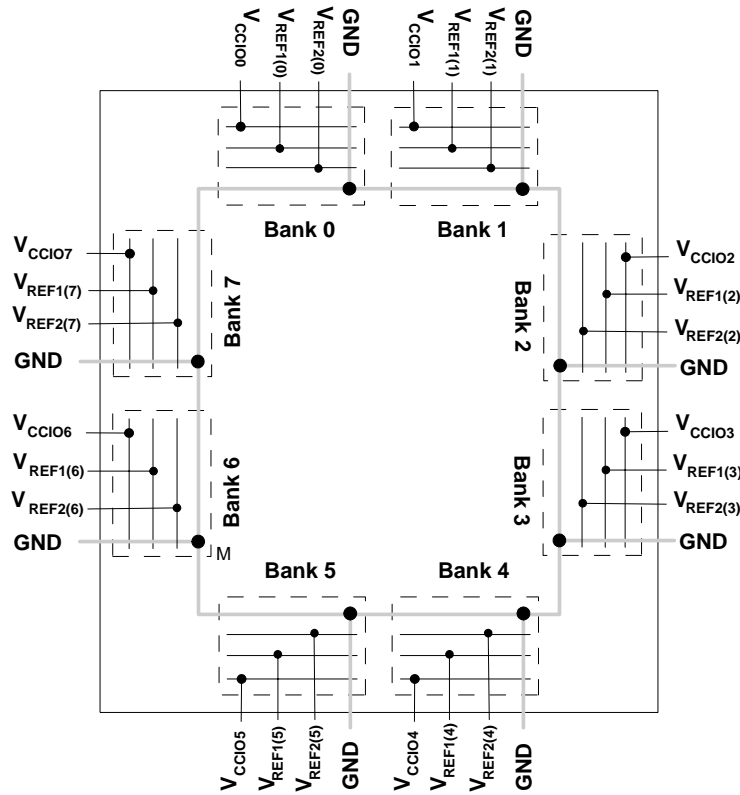
sysIO Buffer Banks

LatticeECP/EC devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-33 shows the eight banks and their associated supplies.

In the LatticeECP/EC devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS, PCI and PCI-X) are powered using V_{CCIO} . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold input independent of V_{CCIO} . In addition to the bank V_{CCIO} supplies, the LatticeECP/EC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeECP/EC devices, some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-33. LatticeECP/EC Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeECP/EC devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**

The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/Os on the top and bottom banks have PCI clamp.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**

The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

Only the left and right banks have LVDS differential output drivers.

Supported Standards

The LatticeECP/EC sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTTL and other standards. The buffers support the LVTTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTTL modes, the buffer has individually configurable

options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by the LatticeECP/EC devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

| Input Standard | V _{REF} (Nom.) | V _{CCIO} ¹ (Nom.) |
|--------------------------------------|-------------------------|---------------------------------------|
| Single Ended Interfaces | | |
| LVTTTL | — | — |
| LVC MOS33 ² | — | — |
| LVC MOS25 ² | — | — |
| LVC MOS18 | — | 1.8 |
| LVC MOS15 | — | 1.5 |
| LVC MOS12 ² | — | — |
| PCI | — | 3.3 |
| HSTL18 Class I, II | 0.9 | — |
| HSTL18 Class III | 1.08 | — |
| HSTL15 Class I | 0.75 | — |
| HSTL15 Class III | 0.9 | — |
| SSTL3 Class I, II | 1.5 | — |
| SSTL2 Class I, II | 1.25 | — |
| SSTL18 Class I | 0.9 | — |
| Differential Interfaces | | |
| Differential SSTL18 Class I | — | — |
| Differential SSTL2 Class I, II | — | — |
| Differential SSTL3 Class I, II | — | — |
| Differential HSTL15 Class I, III | — | — |
| Differential HSTL18 Class I, II, III | — | — |
| LVDS, LVPECL, BLVDS, RSDS | — | — |

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.

2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

Table 2-14. Supported Output Standards

| Output Standard | Drive | V _{CCIO} (Nom.) |
|---------------------------------------|----------------------------|--------------------------|
| Single-ended Interfaces | | |
| LVTTTL | 4mA, 8mA, 12mA, 16mA, 20mA | 3.3 |
| LVC MOS33 | 4mA, 8mA, 12mA 16mA, 20mA | 3.3 |
| LVC MOS25 | 4mA, 8mA, 12mA, 16mA, 20mA | 2.5 |
| LVC MOS18 | 4mA, 8mA, 12mA, 16mA | 1.8 |
| LVC MOS15 | 4mA, 8mA | 1.5 |
| LVC MOS12 | 2mA, 6mA | 1.2 |
| LVC MOS33, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVC MOS25, Open Drain | 4mA, 8mA, 12mA 16mA, 20mA | — |
| LVC MOS18, Open Drain | 4mA, 8mA, 12mA 16mA | — |
| LVC MOS15, Open Drain | 4mA, 8mA | — |
| LVC MOS12, Open Drain | 2mA, 6mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II, III | N/A | 1.8 |
| HSTL15 Class I, III | N/A | 1.5 |
| SSTL3 Class I, II | N/A | 3.3 |
| SSTL2 Class I, II | N/A | 2.5 |
| SSTL18 Class I | N/A | 1.8 |
| Differential Interfaces | | |
| Differential SSTL3, Class I, II | N/A | 3.3 |
| Differential SSTL2, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I | N/A | 1.8 |
| Differential HSTL18, Class I, II, III | N/A | 1.8 |
| Differential HSTL15, Class I, III | N/A | 1.5 |
| LVDS | N/A | 2.5 |
| BLVDS ¹ | N/A | 2.5 |
| LVPECL ¹ | N/A | 3.3 |
| RSDS ¹ | N/A | 2.5 |

1. Emulated with external resistors.

Hot Socketing

The LatticeECP/EC devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeECP/EC ideal for many multiple power supply and hot-swap applications.

Recommended Power Up Sequence: As described in the previous paragraph, the supplies can be sequenced in any order. However, once internal power good is achieved (determined by VCC, VCCAUX, VCCIO bank 5) the part releases I/Os from tri-state and the management of I/Os becomes the designers responsibility. To simplify a system design it is therefore recommended that supplies be sequenced VCCIO, VCC, VCCAUX.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeECP/EC family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP/EC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeECP/EC devices contain two possible ports that can be used for device configuration. The test access port (TAP), which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The TAP supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. There are four configuration options for LatticeECP/EC devices:

1. Industry standard SPI memories.
2. Industry standard byte wide flash and ispMACH 4000 for control/addressing.
3. Configuration from system microprocessor via the configuration bus or TAP.
4. Industry standard FPGA board memory.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next power-up sequence.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Internal Logic Analyzer Capability (ispTRACY)

All LatticeECP/EC devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP/EC devices require a single external, 10K ohm +/- 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

Oscillator

Every LatticeECP/EC device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously. The default value of the master serial clock is 2.5MHz. Table 2-15 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-15. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

| CCLK (MHz) | CCLK (MHz) | CCLK (MHz) |
|------------|------------|------------|
| 2.5* | 13 | 45 |
| 4.3 | 15 | 51 |
| 5.4 | 20 | 55 |
| 6.9 | 26 | 60 |
| 8.1 | 30 | 130 |
| 9.2 | 34 | — |
| 10.0 | 41 | — |

Density Shifting

The LatticeECP/EC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings^{1, 2, 3}

| | |
|---|---------------|
| Supply Voltage V_{CC} | -0.5 to 1.32V |
| Supply Voltage V_{CCAUX} | -0.5 to 3.75V |
| Supply Voltage V_{CCJ} | -0.5 to 3.75V |
| Output Supply Voltage V_{CCIO} | -0.5 to 3.75V |
| Input Voltage Applied ⁴ | -0.5 to 4.25V |
| I/O Tristate Voltage Applied ⁴ | -0.5 to 3.75V |
| Storage Temperature (Ambient) | -65 to 150°C |
| Junction Temp. (Tj) +125°C | |

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|------------------|---|-------|-------|-------|
| V_{CC} | Core Supply Voltage | 1.14 | 1.26 | V |
| V_{CCAUX} | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}^{1,2}$ | I/O Driver Supply Voltage | 1.140 | 3.465 | V |
| V_{CCJ}^1 | Supply Voltage for IEEE 1149.1 Test Access Port | 1.140 | 3.465 | V |
| t_{JCOM} | Junction Commercial Operation | 0 | +85 | °C |
| t_{JIND} | Junction Industrial Operation | -40 | 100 | °C |

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX} .
2. See recommended voltages by I/O standard in subsequent table.

Hot Socketing Specifications^{1, 2, 3, 4}

| Symbol | Parameter | Condition | Min. | Typ. | Max | Units |
|----------|------------------------------|-----------------------------------|------|------|---------|---------|
| I_{DK} | Input or I/O leakage Current | $0 \leq V_{IN} \leq V_{IH} (MAX)$ | — | — | +/-1000 | μA |

1. Insensitive to sequence of V_{CC} , V_{CCAUX} and V_{CCIO} . However, assumes monotonic rise/fall rates for V_{CC} , V_{CCAUX} and V_{CCIO} .
2. $0 \leq V_{CC} \leq V_{CC} (MAX)$, $0 \leq V_{CCIO} \leq V_{CCIO} (MAX)$ or $0 \leq V_{CCAUX} \leq V_{CCAUX} (MAX)$.
3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .
4. LVCMOS and LVTTTL only.

DC Electrical Characteristics

Over Recommended Operating Conditions

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--------------------|--|--|----------------|------|----------------|---------|
| I_{IL}, I_{IH}^1 | Input or I/O Low leakage | $0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$ | — | — | 10 | μA |
| | | $(V_{CCIO} - 0.2V) \leq V_{IN} \leq 3.6V$ | — | — | 40 | μA |
| I_{PU} | I/O Active Pull-up Current | $0 \leq V_{IN} \leq 0.7 V_{CCIO}$ | 30 | — | 150 | μA |
| I_{PD} | I/O Active Pull-down Current | $V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$ | -30 | — | -150 | μA |
| I_{BHLS} | Bus Hold Low sustaining current | $V_{IN} = V_{IL} (MAX)$ | 30 | — | — | μA |
| I_{BHHS} | Bus Hold High sustaining current | $V_{IN} = 0.7V_{CCIO}$ | -30 | — | — | μA |
| I_{BHLO} | Bus Hold Low Overdrive current | $0 \leq V_{IN} \leq V_{IH} (MAX)$ | — | — | 150 | μA |
| I_{BHLH} | Bus Hold High Overdrive current | $0 \leq V_{IN} \leq V_{IH} (MAX)$ | — | — | -150 | μA |
| V_{BHT} | Bus Hold trip Points | $0 \leq V_{IN} \leq V_{IH} (MAX)$ | $V_{IL} (MAX)$ | — | $V_{IH} (MIN)$ | V |
| C1 | I/O Capacitance ² | $V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$ | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance ² | $V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$ | — | 6 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. T_A 25°C, $f = 1.0MHz$

Supply Current (Standby)^{1, 2, 3, 4}

Over Recommended Operating Conditions

| Symbol | Parameter | Devices | Typ. ⁵ | Max. | Units |
|--------------------|--|---|-------------------|------|-------|
| I _{CC} | Core Power Supply Current | LFEC1 | | | mA |
| | | LFEC3 | | | mA |
| | | LFECP6/LFEC6 | | | mA |
| | | LFECP10/LFEC10 | | | mA |
| | | LFECP15/LFEC15 | | | mA |
| | | LFECP20/LFEC20 | 100 | | mA |
| | | LFECP33/LFEC33 | | | mA |
| | LFECP40/LFEC40 | | | mA | |
| I _{CCAUX} | Auxiliary Power Supply Current | LFEC1 | | | mA |
| | | LFEC3 | | | mA |
| | | LFECP6/LFEC6 | | | mA |
| | | LFECP10/LFEC10 | | | mA |
| | | LFECP15/LFEC15 | | | mA |
| | | LFECP20/LFEC20 | 15 | | mA |
| | | LFECP33/LFEC33 | | | mA |
| | LFECP40/LFEC40 | | | mA | |
| I _{CCPLL} | PLL Power Supply Current (per PLL) | LFEC1, LFEC3, LFEC6, LFECP6, LFECP10, LFECP15, LFECP20, LFECP33, LFECP40, LFEC10, LFEC15, LFEC20, LFEC33, LFEC40, | 8 | | mA |
| I _{CCIO} | Bank Power Supply Current ⁶ | | 2 | | mA |
| I _{CCJ} | V _{CCJ} Power Supply Current | | 5 | | mA |

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.
5. T_J=25°C, power supplies at nominal voltage.
6. Per bank.

Initialization Supply Current^{1,2,3,4,5,6}

Over Recommended Operating Conditions

| Symbol | Parameter | Devices | Typ. ⁶ | Max. | Units |
|--------------------|--|---|-------------------|------|-------|
| I _{CC} | Core Power Supply Current | LFEC1 | | | mA |
| | | LFEC3 | | | mA |
| | | LFEC6/LFEC6 | | | mA |
| | | LFEC10/LFEC10 | | | mA |
| | | LFEC15/LFEC15 | | | mA |
| | | LFEC20/LFEC20 | 150 | | mA |
| | | LFEC33/LFEC33 | | | mA |
| | | LFEC40/LFEC40 | | | mA |
| I _{CCAUX} | Auxiliary Power Supply Current | LFEC1 | | | mA |
| | | LFEC3 | | | mA |
| | | LFEC6/LFEC6 | | | mA |
| | | LFEC10/LFEC10 | | | mA |
| | | LFEC15/LFEC15 | | | mA |
| | | LFEC20/LFEC20 | 25 | | mA |
| | | LFEC33/LFEC33 | | | mA |
| | | LFEC40/LFEC40 | | | mA |
| I _{CCPLL} | PLL Power Supply Current (per PLL) | LFEC1, LFEC3, LFEC6, LFEC6, LFEC10, LFEC15, LFEC20, LFEC33, LFEC40, LFEC10, LFEC15, LFEC20, LFEC33, LFEC40, | 12 | | mA |
| I _{CCIO} | Bank Power Supply Current ⁷ | | 5 | | mA |
| I _{CCJ} | V _{CCJ} Power Supply Current | | 10 | | mA |

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. Pattern represents typical design with 65% logic, 55% EBR, 10% routing utilization.
6. T_J=25°C, power supplies at nominal voltage.
7. Per bank.

sysIO Recommended Operating Conditions

| Standard | V _{CCIO} | | | V _{REF} (V) | | |
|---------------------|-------------------|------|-------|----------------------|------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVC MOS 3.3 | 3.135 | 3.3 | 3.465 | — | — | — |
| LVC MOS 2.5 | 2.375 | 2.5 | 2.625 | — | — | — |
| LVC MOS 1.8 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVC MOS 1.5 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVC MOS 1.2 | 1.14 | 1.2 | 1.26 | — | — | — |
| LV TTL | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI | 3.135 | 3.3 | 3.465 | — | — | — |
| SSTL18 Class I | 1.71 | 2.5 | 1.89 | 1.15 | 1.25 | 1.35 |
| SSTL2 Class I, II | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL3 Class I, II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL15 Class I | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL15 Class III | 1.425 | 1.5 | 1.575 | — | 0.9 | — |
| HSTL 18 Class I, II | 1.71 | 1.8 | 1.89 | — | 0.9 | — |
| HSTL 18 Class III | 1.71 | 1.8 | 1.89 | — | 1.08 | — |
| LVDS | 2.375 | 2.5 | 2.625 | — | — | — |
| LVPECL ¹ | 3.135 | 3.3 | 3.465 | — | — | — |
| BLVDS ¹ | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS ¹ | 2.375 | 2.5 | 2.625 | — | — | — |

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

sysIO Single-Ended DC Electrical Characteristics

| Input/Output Standard | V_{IL} | | V_{IH} | | V_{OL} Max. (V) | V_{OH} Min. (V) | I_{OL}^1 (mA) | I_{OH}^1 (mA) |
|-----------------------|----------|-------------------|-------------------|----------|-------------------|-------------------|------------------|-----------------------|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| LVTTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 16, 12, 8, 4 | -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| LVCMOS 1.5 | -0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 8, 4 | -8, -4 |
| | | | | | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| LVCMOS 1.2 | -0.3 | $0.35V_{CC}$ | $0.65V_{CC}$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| PCI | -0.3 | $0.3V_{CCIO}$ | $0.5V_{CCIO}$ | 3.6 | $0.1V_{CCIO}$ | $0.9V_{CCIO}$ | 1.5 | -0.5 |
| SSTL3 class I | -0.3 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 3.6 | 0.7 | $V_{CCIO} - 1.1$ | 8 | -8 |
| SSTL3 class II | -0.3 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 3.6 | 0.5 | $V_{CCIO} - 0.9$ | 16 | -16 |
| SSTL2 class I | -0.3 | $V_{REF} - 0.18$ | $V_{REF} + 0.18$ | 3.6 | 0.54 | $V_{CCIO} - 0.62$ | 7.6 | -7.6 |
| SSTL2 class II | -0.3 | $V_{REF} - 0.18$ | $V_{REF} + 0.18$ | 3.6 | 0.35 | $V_{CCIO} - 0.43$ | 15.2 | -15.2 |
| SSTL18 class I | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 6.7 | -6.7 |
| HSTL15 class I | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL15 class III | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 24 | -8 |
| HSTL18 class I | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 9.6 | -9.6 |
| HSTL18 class II | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL18 class III | -0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 3.6 | 0.4 | $V_{CCIO} - 0.4$ | 24 | -8 |

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

Rev F 0.17

sysIO Differential Electrical Characteristics**LVDS****Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|--------------------|--|--|-------------|------|-------|---------------|
| V_{INP}, V_{INM} | Input voltage | | 0 | — | 2.4 | V |
| V_{THD} | Differential input threshold | | +/-100 | — | — | mV |
| V_{CM} | Input common mode voltage | $100\text{mV} \leq V_{THD}$ | $V_{THD}/2$ | 1.2 | 1.8 | V |
| | | $200\text{mV} \leq V_{THD}$ | $V_{THD}/2$ | 1.2 | 1.9 | V |
| | | $350\text{mV} \leq V_{THD}$ | $V_{THD}/2$ | 1.2 | 2.0 | V |
| I_{IN} | Input current | Power on or power off | — | — | +/-10 | μA |
| V_{OH} | Output high voltage for V_{OP} or V_{OM} | $R_T = 100 \text{ Ohm}$ | — | 1.38 | 1.60 | V |
| V_{OL} | Output low voltage for V_{OP} or V_{OM} | $R_T = 100 \text{ Ohm}$ | 0.9V | 1.03 | — | V |
| V_{OD} | Output voltage differential | $(V_{OP} - V_{OM}), R_T = 100 \text{ Ohm}$ | 250 | 350 | 450 | mV |
| ΔV_{OD} | Change in V_{OD} between high and low | | — | — | 50 | mV |
| V_{OS} | Output voltage offset | $(V_{OP} - V_{OM})/2, R_T = 100 \text{ Ohm}$ | 1.125 | 1.25 | 1.375 | V |
| ΔV_{OS} | Change in V_{OS} between H and L | | — | — | 50 | mV |
| I_{OSD} | Output short circuit current | $V_{OD} = 0\text{V}$ Driver outputs shorted | — | — | 6 | mA |

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

BLVDS

The LatticeECP/EC devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. BLVDS Multi-point Output Example

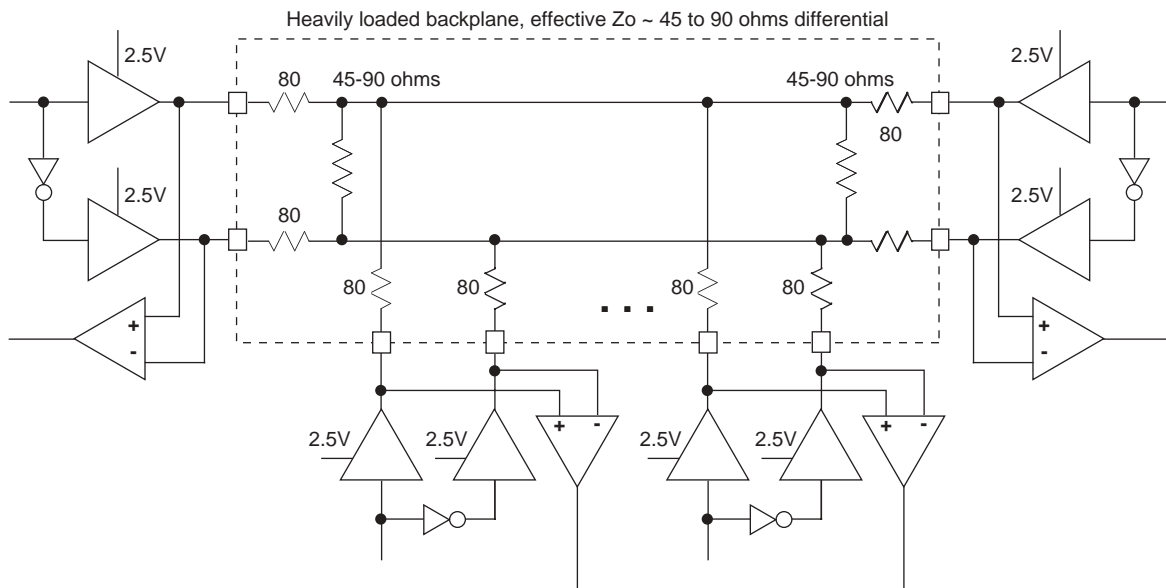


Table 3-1. BLVDS DC Conditions¹

Over Recommended Operating Conditions

| Parameter | Description | Typical | | Units |
|---------------------|-----------------------------|---------|---------|-------|
| | | Zo = 45 | Zo = 90 | |
| Z _{OUT} | Output impedance | 100 | 100 | ohm |
| R _{TLEFT} | Left end termination | 45 | 90 | ohm |
| R _{TRIGHT} | Right end termination | 45 | 90 | ohm |
| V _{OH} | Output high voltage | 1.375 | 1.48 | V |
| V _{OL} | Output low voltage | 1.125 | 1.02 | V |
| V _{OD} | Output differential voltage | 0.25 | 0.46 | V |
| V _{CM} | Output common mode voltage | 1.25 | 1.25 | V |
| I _{DC} | DC output current | 11.2 | 10.2 | mA |

1. For input buffer, see LVDS table.

LVPECL

The LatticeECP/EC devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-2 is one possible solution for point-to-point signals.

Figure 3-2. Differential LVPECL

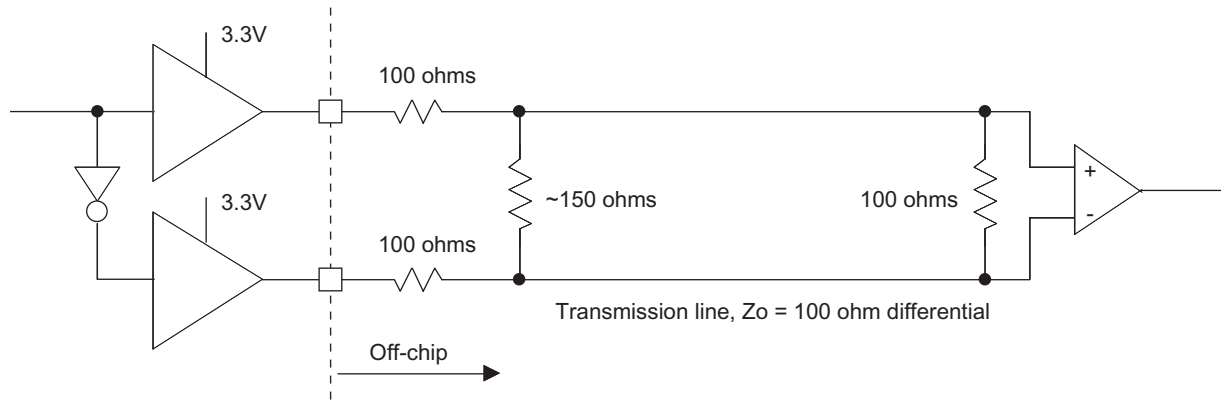


Table 3-2. LVPECL DC Conditions¹

Over Recommended Operating Conditions

| Parameter | Description | Typical | Units |
|-------------------|-----------------------------|---------|-------|
| Z _{OUT} | Output impedance | 100 | ohm |
| R _P | Driver parallel resistor | 150 | ohm |
| R _T | Receiver termination | 100 | ohm |
| V _{OH} | Output high voltage | 2.03 | V |
| V _{OL} | Output low voltage | 1.27 | V |
| V _{OD} | Output differential voltage | 0.76 | V |
| V _{CM} | Output common mode voltage | 1.65 | V |
| Z _{BACK} | Back impedance | 85.7 | ohm |
| I _{DC} | DC output current | 12.7 | mA |

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

RSDS

The LatticeECP/EC devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-3 are industry standard values for 1% resistors.

Figure 3-3. RSDS (Reduced Swing Differential Standard)

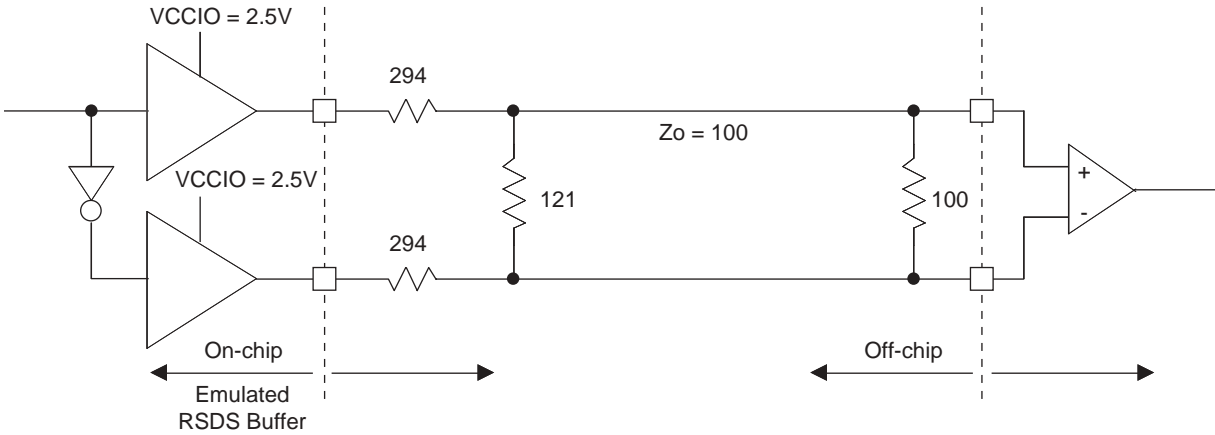


Table 3-3. RSDS DC Conditions

| Parameter | Description | Typical | Units |
|-------------------|-----------------------------|---------|-------|
| Z _{OUT} | Output impedance | 20 | ohm |
| R _S | Driver series resistor | 294 | ohm |
| R _P | Driver parallel resistor | 121 | ohm |
| R _T | Receiver termination | 100 | ohm |
| V _{OH} | Output high voltage | 1.35 | V |
| V _{OL} | Output low voltage | 1.15 | V |
| V _{OD} | Output differential voltage | 0.20 | V |
| V _{CM} | Output common mode voltage | 1.25 | V |
| Z _{BACK} | Back impedance | 101.5 | ohm |
| I _{DC} | DC output current | 3.66 | mA |

5V Tolerant Input Buffer

The input buffers of the LatticeECP/EC family of devices can support 5V signals by using a PCI Clamp and an external series resistor as shown in Figure 3-4.

Figure 3-4. 5 V Tolerant Input Buffer

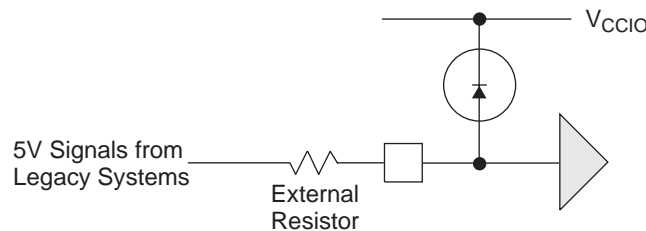
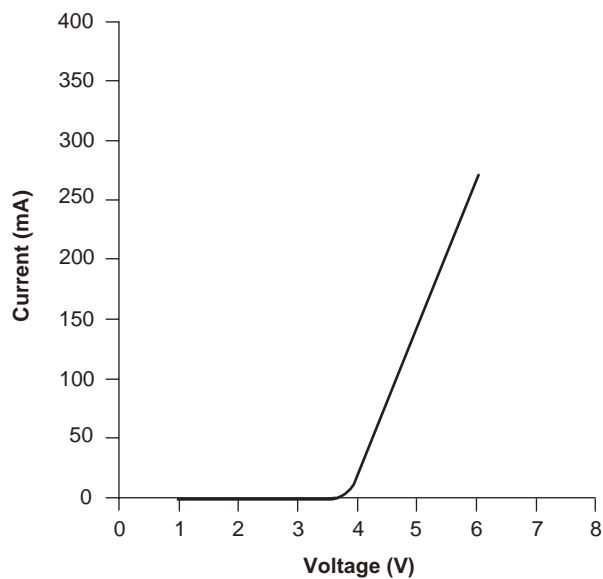


Figure 3-5. Typical PCI Clamp Current



Typical Building Block Function Performance**Pin-to-Pin Performance (LVCMOS25 12mA Drive)**

| Function | -5 Timing | Units |
|-----------------------------------|-----------|-------|
| Basic Functions | | |
| 16 bit decoder | 6.2 | ns |
| 32 bit decoder | 7.2 | ns |
| 64 bit decoder | 7.7 | ns |
| 4:1 MUX | 4.8 | ns |
| 8:1 MUX | 5.1 | ns |
| 16:1 MUX | 6.1 | ns |
| 32:1 MUX | 6.5 | ns |
| Combinatorial (pin to LUT to pin) | 5.3 | ns |

Register-to-Register Performance

| Function | -5 Timing | Units |
|-------------------------------------|-----------|-------|
| Basic Functions | | |
| 16 bit decoder | 331 | MHz |
| 32 bit decoder | 277 | MHz |
| 64 bit decoder | 240 | MHz |
| 4:1 MUX | 727 | MHz |
| 8:1 MUX | 482 | MHz |
| 16:1 MUX | 439 | MHz |
| 32:1 MUX | 382 | MHz |
| 8-bit adder | 391 | MHz |
| 16-bit adder | 337 | MHz |
| 64-bit adder | 190 | MHz |
| 16-bit counter | 410 | MHz |
| 32-bit counter | 315 | MHz |
| 64-bit counter | 215 | MHz |
| 64-bit accumulator | 155 | MHz |
| Embedded Memory Functions | | |
| 256x36 Single Port RAM | 280 | MHz |
| 512x18 True-Dual Port RAM | 280 | MHz |
| Distributed Memory Functions | | |
| 16x2 Single Port RAM | 549 | MHz |
| 64x2 Single Port RAM | 259 | MHz |
| 128x4 Single Port RAM | 205 | MHz |
| 32x2 Pseudo-Dual Port RAM | 360 | MHz |
| 64x4 Pseudo-Dual Port RAM | 301 | MHz |
| DSP Function¹ | | |
| 9x9 Pipelined Multiply/Accumulate | 250 | MHz |
| 18x18 Pipelined Mutiply/Accumulate | 230 | MHz |
| 36x36 Pipelined Mutiply | 210 | MHz |

1. Applies to LatticeECP devices only.

2. The above timing numbers were generated using ispLEVER tool, exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Derating Timing Tables

Logic Timing provided in the following sections of the data sheet and the ispLEVER design tools are worst-case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process, can be much better than the values given in the tables. To calculate logic timing numbers at a particular temperature and voltage multiply the noted numbers with the derating factors provided below.

The junction temperature for the FPGA depends on the power dissipation by the device, the package thermal characteristics (Θ_{JA}), and the ambient temperature, as calculated with the following equation:

$$T_{JMAX} = T_{AMAX} + (\text{Power} * \Theta_{JA})$$

The user must determine this temperature and then use it to determine the derating factor based on the following derating tables: T_J °C.

Table 3-4. Delay Derating Table for Internal Blocks

| T_J °C Commercial | T_J °C Industrial | Power Supply Voltage | | |
|------------------------|------------------------|----------------------|------|-------|
| | | 1.14V | 1.2V | 1.26V |
| — | -40 | 0.82 | 0.77 | 0.71 |
| — | -25 | 0.82 | 0.76 | 0.71 |
| 0 | 20 | 0.89 | 0.83 | 0.78 |
| 25 | 45 | 0.93 | 0.87 | 0.81 |
| 85 | 105 | 1.00 | 0.94 | 0.89 |
| 100 | 115 | 1.00 | 0.95 | 0.90 |
| 110 | — | 1.00 | 0.95 | 0.90 |
| 125 | — | 1.02 | 0.96 | 0.91 |

LatticeECP/EC External Switching Characteristics

Over Recommended Operating Conditions

| Parameter | Description | Device | -5 | | -4 | | -3 | | Units |
|---|--|--------|-------|-------|-------|-------|-------|-------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| General I/O Pin Parameters (Using Primary Clock without PLL)¹ | | | | | | | | | |
| t_{CO} | Clock to Output - PIO Output Register | LFEC20 | — | 5.71 | — | 6.85 | — | 7.99 | ns |
| t_{SU} | Clock to Data Setup - PIO Input Register | LFEC20 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| t_H | Clock to Data Hold - PIO Input Register | LFEC20 | 3.41 | — | 4.09 | — | 4.77 | — | ns |
| t_{SU_DEL} | Clock to Data Setup - PIO Input Register with data input delay | LFEC20 | 3.84 | — | 4.62 | — | 5.38 | — | ns |
| t_{H_DEL} | Clock to Data Hold - PIO Input Register with Input Data Delay | LFEC20 | -0.44 | — | -0.54 | — | -0.61 | — | ns |
| f_{MAX_IO} | LVDS I/O Buffer Frequency | LFEC20 | — | 420 | — | 378 | — | 340 | MHz |
| DDR I/O Pin Parameters^{2,3} | | | | | | | | | |
| t_{DVADQ}^4 | Data Valid After DQS (DDR Read) | LFEC20 | — | 0.192 | — | 0.192 | — | 0.192 | UI |
| t_{DVEDQ}^4 | Data Hold After DQS (DDR Read) | LFEC20 | 0.668 | — | 0.668 | — | 0.668 | — | UI |
| t_{DQVBS} | Data Valid Before DQS | LFEC20 | 0.2 | — | 0.2 | — | 0.2 | — | UI |
| t_{DQVAS} | Data Valid After DQS | LFEC20 | 0.2 | — | 0.2 | — | 0.2 | — | UI |
| f_{MAX_DDR} | DDR Clock Frequency | LFEC20 | 95 | 200 | 95 | 166 | 95 | 133 | MHz |
| Primary and Secondary Clock | | | | | | | | | |
| f_{MAX_PRI} | Frequency for Primary Clock Tree | LFEC20 | — | 420 | — | 378 | — | 340 | MHz |
| t_{W_PRI} | Clock Pulse Width for Primary Clock | LFEC20 | 1.19 | — | 1.19 | — | 1.19 | — | ns |
| t_{SKEW_PRI} | Primary Clock Skew within an I/O Bank | LFEC20 | — | 250 | — | 300 | — | 350 | ps |

1. General timing numbers based on LVCMOS2.5V, 12 mA.

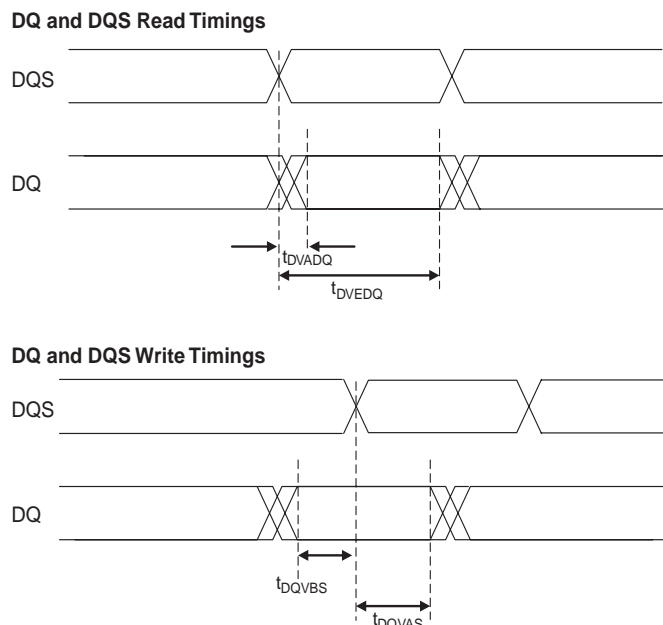
2. DDR timing numbers based on SSTL I/O.

3. DDR specifications are characterized but not tested.

4. UI is average bit period.

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Figure 3-6. DDR Timings



LatticeECP/EC Internal Timing Parameters¹

Over Recommended Operating Conditions

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|---------------------------------------|---|-------|-------|-------|-------|-------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| PFU/PFF Logic Mode Timing | | | | | | | | |
| t _{LUT4_PFU} | LUT4 delay (A to D inputs to F output) | - | 0.25 | - | 0.31 | - | 0.36 | ns |
| t _{LUT6_PFU} | LUT6 delay (A to D inputs to OFX output) | - | 0.55 | - | 0.66 | - | 0.77 | ns |
| t _{LSR_PFU} | Set/Reset to output of PFU | - | 0.81 | - | 0.98 | - | 1.14 | ns |
| t _{SUM_PFU} | Clock to Mux (M0,M1) input setup time | 0.08 | - | 0.10 | - | 0.11 | - | ns |
| t _{HM_PFU} | Clock to Mux (M0,M1) input hold time | -0.06 | - | -0.07 | - | -0.08 | - | ns |
| t _{SUD_PFU} | Clock to D input setup time | 0.11 | - | 0.14 | - | 0.16 | - | ns |
| t _{HD_PFU} | Clock to D input hold time | -0.04 | - | -0.04 | - | -0.05 | - | ns |
| t _{CK2Q_PFU} | Clock to Q delay, D-type register configuration | - | 0.43 | - | 0.51 | - | 0.60 | ns |
| t _{LE2Q_PFU} | Clock to Q delay latch configuration | - | 0.54 | - | 0.65 | - | 0.76 | ns |
| t _{LD2Q_PFU} | D to Q throughput delay when latch is enabled | - | 0.50 | - | 0.60 | - | 0.69 | ns |
| PFU Memory Mode Timing | | | | | | | | |
| t _{CORAM_PFU} | Clock to Output | - | 0.43 | - | 0.51 | - | 0.60 | ns |
| t _{SUDATA_PFU} | Data Setup Time | -0.25 | - | -0.30 | - | -0.34 | - | ns |
| t _{HDATA_PFU} | Data Hold Time | -0.06 | - | -0.07 | - | -0.08 | - | ns |
| t _{SUADDR_PFU} | Address Setup Time | -0.66 | - | -0.79 | - | -0.92 | - | ns |
| t _{HADDR_PFU} | Address Hold Time | -0.27 | - | -0.33 | - | -0.38 | - | ns |
| t _{SUWREN_PFU} | Write/Read Enable Setup Time | -0.30 | - | -0.36 | - | -0.42 | - | ns |
| t _{HWREN_PFU} | Write/Read Enable Hold Time | -0.21 | - | -0.25 | - | -0.29 | - | ns |
| PIC Timing | | | | | | | | |
| PIO Input/Output Buffer Timing | | | | | | | | |
| t _{IN_PIO} | Input Buffer Delay | - | 0.56 | - | 0.67 | - | 0.78 | ns |
| t _{OUT_PIO} | Output Buffer Delay | - | 2.07 | - | 2.49 | - | 2.90 | ns |
| IOLOGIC Input/Output Timing | | | | | | | | |
| t _{SUI_PIO} | Input Register Setup Time (Data Before Clock) | - | 0.12 | - | 0.14 | - | 0.17 | ns |
| t _{HI_PIO} | Input Register Hold Time (Data after Clock) | - | -0.09 | - | -0.11 | - | -0.13 | ns |
| t _{COO_PIO} | Output Register Clock to Output Delay | - | 0.82 | - | 0.98 | - | 1.15 | ns |
| t _{SUCE_PIO} | Input Register Clock Enable Setup Time | - | -0.02 | - | -0.02 | - | -0.03 | ns |
| t _{HCE_PIO} | Input Register Clock Enable Hold Time | - | 0.12 | - | 0.14 | - | 0.17 | ns |
| t _{SULSR_PIO} | Set/Reset Setup Time | 0.10 | - | 0.12 | - | 0.14 | - | ns |
| t _{HLSR_PIO} | Set/Reset Hold Time | -0.24 | - | -0.29 | - | -0.34 | - | ns |
| EBR Timing | | | | | | | | |
| t _{CO_EBR} | Clock to output from Address or Data | - | 3.82 | - | 4.58 | - | 5.34 | ns |
| t _{COO_EBR} | Clock to output from EBR output Register | - | 0.74 | - | 0.88 | - | 1.03 | ns |
| t _{SUDATA_EBR} | Setup Data to EBR Memory | -0.34 | - | -0.41 | - | -0.48 | - | ns |
| t _{HDATA_EBR} | Hold Data to EBR Memory | 0.37 | - | 0.44 | - | 0.52 | - | ns |
| t _{SUADDR_EBR} | Setup Address to EBR Memory | -0.34 | - | -0.41 | - | -0.48 | - | ns |
| t _{HADDR_EBR} | Hold Address to EBR Memory | 0.37 | - | 0.45 | - | 0.52 | - | ns |
| t _{SUWREN_EBR} | Setup Write/Read Enable to PFU Memory | -0.22 | - | -0.26 | - | -0.30 | - | ns |

LatticeECP/EC Internal Timing Parameters¹ (Continued)

Over Recommended Operating Conditions

| Parameter | Description | -5 | | -4 | | -3 | | Units |
|-------------------------------------|---|-------|-------|-------|-------|-------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{HWREN_EBR} | Hold Write/Read Enable to PFU Memory | 0.23 | - | 0.28 | - | 0.33 | - | ns |
| t _{SUCE_EBR} | Clock Enable Setup Time to EBR Output Register | 0.28 | - | 0.34 | - | 0.40 | - | ns |
| t _{HCE_EBR} | Clock Enable Hold Time to EBR Output Register | -0.24 | - | -0.29 | - | -0.34 | - | ns |
| t _{RSTO_EBR} | Reset To Output Delay Time from EBR Output Register | - | 1.00 | - | 1.20 | - | 1.40 | ns |
| PLL Parameters | | | | | | | | |
| t _{RSTREC} | Reset Recovery to Rising Clock | - | - | - | - | - | - | ns |
| t _{RSTSU} | Reset Signal Setup Time | - | - | - | - | - | - | ns |
| t _{RSTW} | Reset Signal Pulse Width | 10.0 | - | 10.0 | - | 10.0 | - | ns |
| DSP Block Timing² | | | | | | | | |
| t _{SUI_DSP} | Input Register Setup Time | - | -0.44 | - | -0.35 | - | -0.27 | ns |
| t _{HI_DSP} | Input Register Hold Time | - | 0.80 | - | 0.96 | - | 1.12 | ns |
| t _{SUP_DSP} | Pipeline Register Setup Time | - | 3.31 | - | 3.98 | - | 4.64 | ns |
| t _{HP_DSP} | Pipeline Register Hold Time | - | 0.80 | - | 0.96 | - | 1.12 | ns |
| t _{SUO_DSP} | Output Register Setup Time | - | 6.72 | - | 8.07 | - | 9.41 | ns |
| t _{HO_DSP} | Output Register Hold Time | - | 0.80 | - | 0.96 | - | 1.12 | ns |
| t _{COI_DSP} | Input Register Clock to Output Time | - | 8.33 | - | 10.35 | - | 12.07 | ns |
| t _{COP_DSP} | Pipeline Register Clock to Output Time | - | 4.80 | - | 5.89 | - | 6.87 | ns |
| t _{COO_DSP} | Output Register Clock to Output Time | - | 1.47 | - | 1.77 | - | 2.06 | ns |
| t _{COVRFL_DSP} | Overflow Register Clock to Output Time | - | 1.47 | - | 1.77 | - | 2.06 | ns |
| t _{SUADSUB} | AdSub Setup Time | - | 3.31 | - | 3.98 | - | 4.64 | ns |
| t _{HADSUB} | AdSub Hold Time | - | 0.71 | - | 0.86 | - | 1.00 | ns |
| t _{SUSIGN} | Sign Setup Time | - | 3.31 | - | 3.98 | - | 4.64 | ns |
| t _{HSIGN} | Sign Hold Time | - | 0.80 | - | 0.96 | - | 1.12 | ns |
| t _{SUACCSLOAD} | Accumulator Load Setup Time | - | 3.31 | - | 3.98 | - | 4.64 | ns |
| t _{HACCSLOAD} | Accumulator Load Hold Time | - | 0.80 | - | 0.96 | - | 1.12 | ns |

1. Internal parameters are characterized but not tested on every device.

2. These parameters apply to LatticeECP devices only.

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Timing Diagrams

PFU Timing Diagrams

Figure 3-7. Slice Single/Dual Port Write Cycle Timing

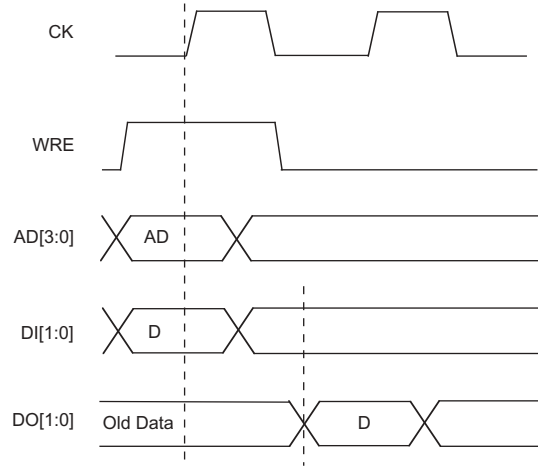
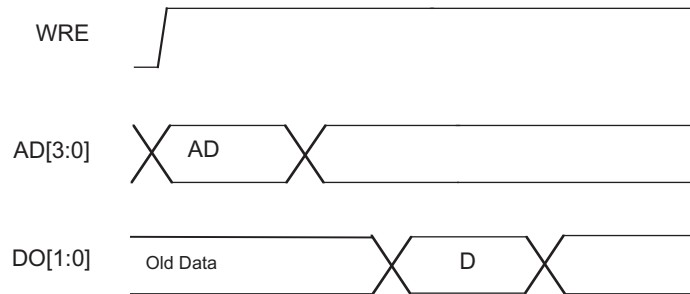
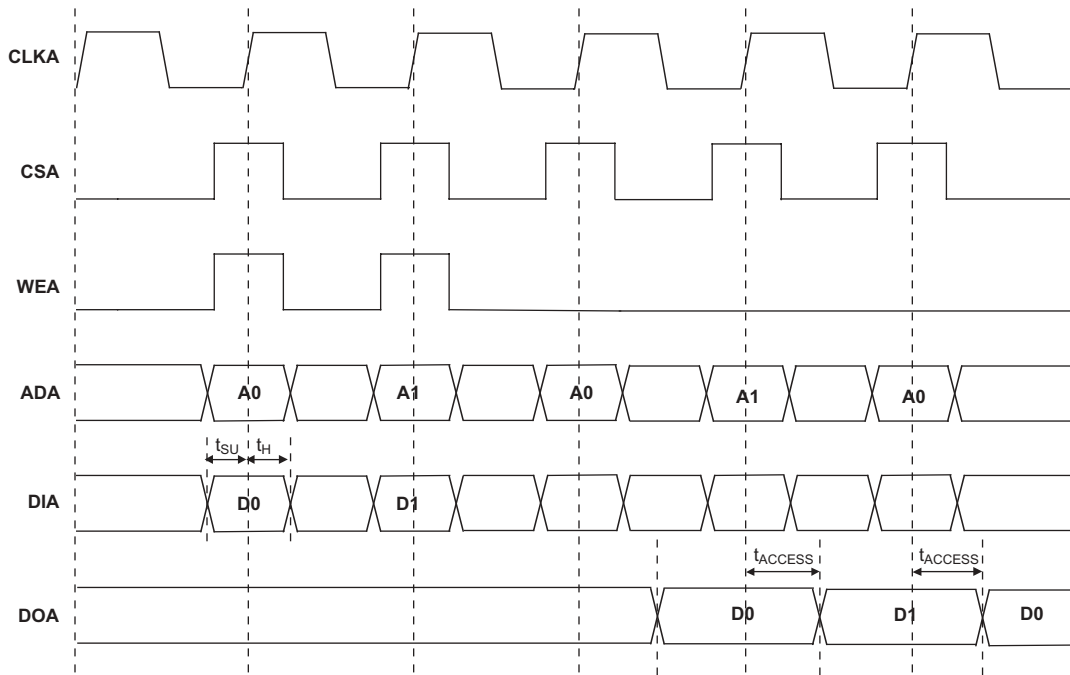


Figure 3-8. Slice Single /Dual Port Read Cycle Timing



EBR Memory Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers

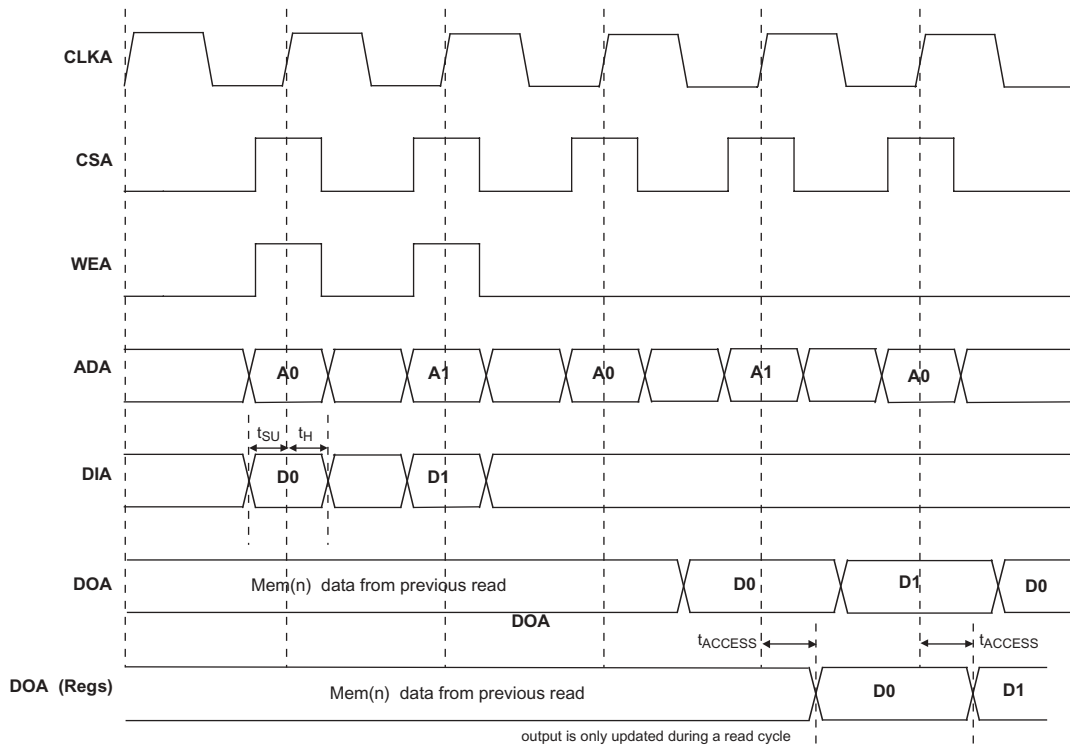
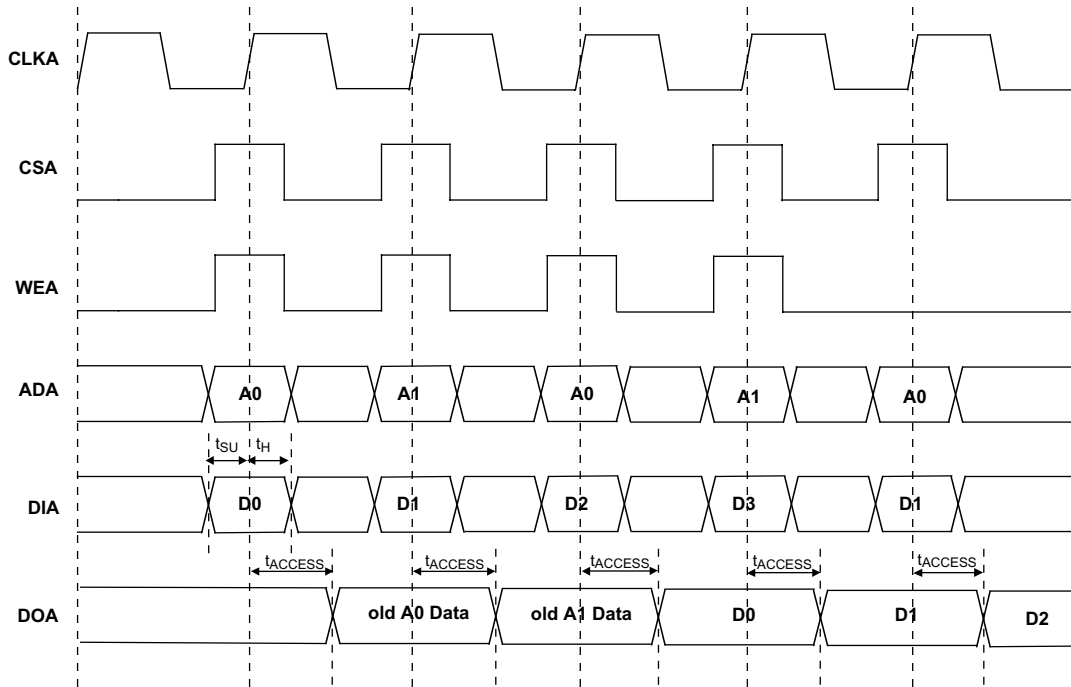
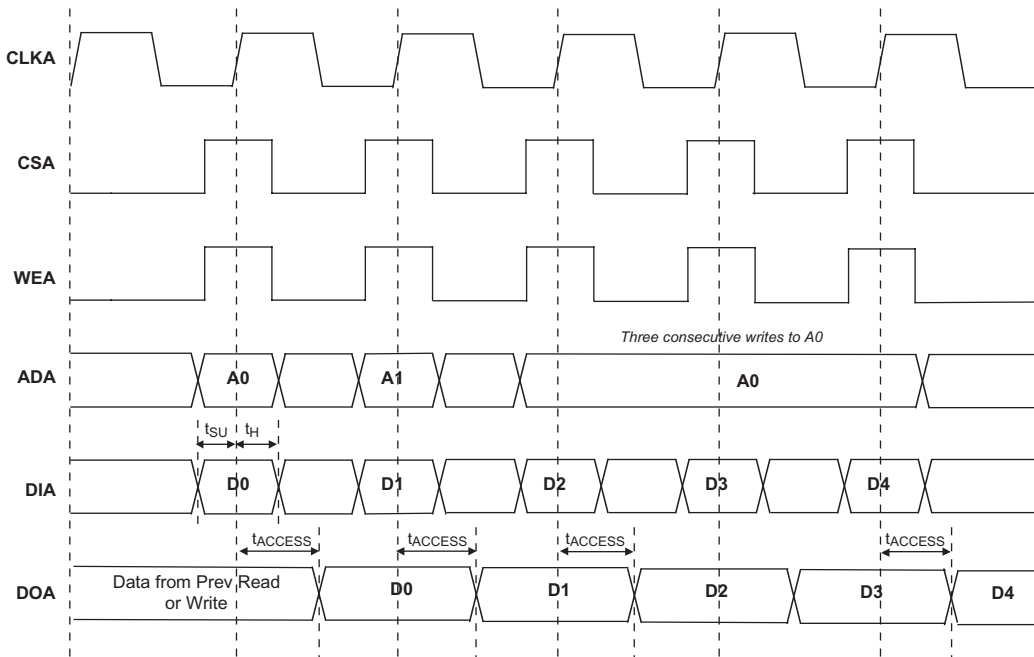


Figure 3-11. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-12. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP/EC Family Timing Adders^{1, 2, 3}**Over Recommended Operating Conditions**

| Buffer Type | Description | -5 | -4 | -3 | Units |
|-------------------------|--------------------------------|-------|-------|-------|-------|
| Input Adjusters | | | | | |
| LVDS25 | LVDS | 0.41 | 0.50 | 0.58 | ns |
| BLVDS25 | BLVDS | 0.41 | 0.50 | 0.58 | ns |
| LVPECL33 | LVPECL | 0.50 | 0.60 | 0.70 | ns |
| HSTL18_I | HSTL_18 class I | 0.41 | 0.49 | 0.57 | ns |
| HSTL18_II | HSTL_18 class II | 0.41 | 0.49 | 0.57 | ns |
| HSTL18_III | HSTL_18 class III | 0.41 | 0.49 | 0.57 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.37 | 0.44 | 0.52 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.37 | 0.44 | 0.52 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.37 | 0.44 | 0.52 | ns |
| HSTL15_I | HSTL_15 class I | 0.40 | 0.48 | 0.56 | ns |
| HSTL15_III | HSTL_15 class III | 0.40 | 0.48 | 0.56 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.37 | 0.44 | 0.51 | ns |
| HSTL15D_III | Differential HSTL 15 class III | 0.37 | 0.44 | 0.51 | ns |
| SSTL33_I | SSTL_3 class I | 0.46 | 0.55 | 0.64 | ns |
| SSTL33_II | SSTL_3 class II | 0.46 | 0.55 | 0.64 | ns |
| SSTL33D_I | Differential SSTL_3 class I | 0.39 | 0.47 | 0.55 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.39 | 0.47 | 0.55 | ns |
| SSTL25_I | SSTL_2 class I | 0.43 | 0.51 | 0.60 | ns |
| SSTL25_II | SSTL_2 class II | 0.43 | 0.51 | 0.60 | ns |
| SSTL25D_I | Differential SSTL_2 class I | 0.38 | 0.45 | 0.53 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.38 | 0.45 | 0.53 | ns |
| SSTL18_I | SSTL_18 class I | 0.40 | 0.48 | 0.56 | ns |
| SSTL18D_I | Differential SSTL_18 class I | 0.37 | 0.44 | 0.51 | ns |
| LVTTTL33 | LVTTTL | 0.07 | 0.09 | 0.10 | ns |
| LVC MOS33 | LVC MOS 3.3 | 0.07 | 0.09 | 0.10 | ns |
| LVC MOS25 | LVC MOS 2.5 | 0.00 | 0.00 | 0.00 | ns |
| LVC MOS18 | LVC MOS 1.8 | 0.07 | 0.09 | 0.10 | ns |
| LVC MOS15 | LVC MOS 1.5 | 0.24 | 0.29 | 0.33 | ns |
| LVC MOS12 | LVC MOS 1.2 | 1.27 | 1.52 | 1.77 | ns |
| PCI33 | PCI | 0.07 | 0.09 | 0.10 | ns |
| Output Adjusters | | | | | |
| LVDS25E | LVDS 2.5 E | -0.03 | -0.04 | -0.04 | ns |
| LVDS25 | LVDS 2.5 | -0.59 | -0.71 | -0.83 | ns |
| BLVDS25 | BLVDS 2.5 | 0.18 | 0.22 | 0.26 | ns |
| LVPECL33 | LVPECL 3.3 | 0.05 | 0.06 | 0.07 | ns |
| HSTL18_I | HSTL_18 class I | -0.25 | -0.30 | -0.35 | ns |
| HSTL18_II | HSTL_18 class II | -0.09 | -0.11 | -0.13 | ns |
| HSTL18_III | HSTL_18 class III | 0.00 | 0.01 | 0.01 | ns |
| HSTL18D_I | Differential HSTL 18 class I | -0.25 | -0.30 | -0.35 | ns |
| HSTL18D_II | Differential HSTL 18 class II | -0.09 | -0.11 | -0.13 | ns |
| HSTL18D_III | Differential HSTL 18 class III | 0.00 | 0.01 | 0.01 | ns |

LatticeECP/EC Family Timing Adders^{1, 2, 3} (Continued)

Over Recommended Operating Conditions

| Buffer Type | Description | -5 | -4 | -3 | Units |
|----------------|--------------------------------|-------|-------|-------|-------|
| HSTL15_I | HSTL_15 class I | -0.07 | -0.08 | -0.09 | ns |
| HSTL15_II | HSTL_15 class II | 0.00 | 0.00 | 0.00 | ns |
| HSTL15_III | HSTL_15 class III | -0.05 | -0.06 | -0.07 | ns |
| HSTL15D_I | Differential HSTL 15 class I | -0.07 | -0.08 | -0.09 | ns |
| HSTL15D_III | Differential HSTL 15 class III | -0.05 | -0.06 | -0.07 | ns |
| SSTL33_I | SSTL_3 class I | -0.20 | -0.24 | -0.28 | ns |
| SSTL33_II | SSTL_3 class II | 0.25 | 0.30 | 0.35 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.20 | -0.24 | -0.28 | ns |
| SSTL33D_II | Differential SSTL_3 class II | 0.25 | 0.30 | 0.35 | ns |
| SSTL25_I | SSTL_2 class I | -0.10 | -0.11 | -0.13 | ns |
| SSTL25_II | SSTL_2 class II | 0.10 | 0.12 | 0.14 | ns |
| SSTL25D_I | Differential SSTL_2 class I | -0.10 | -0.11 | -0.13 | ns |
| SSTL25D_II | Differential SSTL_2 class II | 0.10 | 0.12 | 0.14 | ns |
| SSTL18_I | SSTL_1.8 class I | -0.14 | -0.17 | -0.20 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | -0.14 | -0.17 | -0.20 | ns |
| LVTTTL33_4mA | LVTTTL 4mA drive | -0.06 | -0.07 | -0.09 | ns |
| LVTTTL33_8mA | LVTTTL 8mA drive | -0.05 | -0.07 | -0.08 | ns |
| LVTTTL33_12mA | LVTTTL 12mA drive | -0.06 | -0.07 | -0.08 | ns |
| LVTTTL33_16mA | LVTTTL 16mA drive | -0.05 | -0.07 | -0.08 | ns |
| LVTTTL33_20mA | LVTTTL 20mA drive | -0.07 | -0.09 | -0.10 | ns |
| LVC MOS33_4mA | LVC MOS 3.3 4mA drive | -0.06 | -0.07 | -0.09 | ns |
| LVC MOS33_8mA | LVC MOS 3.3 8mA drive | -0.05 | -0.07 | -0.08 | ns |
| LVC MOS33_12mA | LVC MOS 3.3 12mA drive | -0.06 | -0.07 | -0.08 | ns |
| LVC MOS33_16mA | LVC MOS 3.3 16mA drive | -0.05 | -0.07 | -0.08 | ns |
| LVC MOS33_20mA | LVC MOS 3.3 20mA drive | -0.07 | -0.09 | -0.10 | ns |
| LVC MOS25_4mA | LVC MOS 2.5 4mA drive | 0.04 | 0.05 | 0.05 | ns |
| LVC MOS25_8mA | LVC MOS 2.5 8mA drive | 0.03 | 0.03 | 0.04 | ns |
| LVC MOS25_12mA | LVC MOS 2.5 12mA drive | 0.00 | 0.00 | 0.00 | ns |
| LVC MOS25_16mA | LVC MOS 2.5 16mA drive | 0.03 | 0.03 | 0.04 | ns |
| LVC MOS25_20mA | LVC MOS 2.5 20mA drive | -0.05 | -0.06 | -0.07 | ns |
| LVC MOS18_4mA | LVC MOS 1.8 4mA drive | 0.07 | 0.08 | 0.10 | ns |
| LVC MOS18_8mA | LVC MOS 1.8 8mA drive | 0.07 | 0.08 | 0.09 | ns |
| LVC MOS18_12mA | LVC MOS 1.8 12mA drive | 0.06 | 0.07 | 0.09 | ns |
| LVC MOS18_16mA | LVC MOS 1.8 16mA drive | 0.07 | 0.08 | 0.09 | ns |
| LVC MOS15_4mA | LVC MOS 1.5 4mA drive | 0.12 | 0.14 | 0.16 | ns |
| LVC MOS15_8mA | LVC MOS 1.5 8mA drive | 0.11 | 0.13 | 0.15 | ns |
| LVC MOS12_2mA | LVC MOS 1.2 2mA drive | 0.22 | 0.26 | 0.31 | ns |
| LVC MOS12_6mA | LVC MOS 1.2 6mA drive | 0.21 | 0.25 | 0.29 | ns |
| LVC MOS12_4mA | LVC MOS 1.2 4mA drive | 0.22 | 0.26 | 0.31 | ns |
| PCI33 | PCI33 | 2.00 | 2.40 | 2.80 | ns |

1. Timing adders are characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Conditions table.

3. All other standards according to the appropriate specification.

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sysCLOCK PLL Timing

Over Recommended Operating Conditions

| Parameter | Descriptions | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|---------------------------------------|---|-------|------|---------|-------|
| f_{IN} | Input Clock Frequency (CLKI, CLKFB) | | 25 | — | 420 | MHz |
| f_{OUT} | Output Clock Frequency (CLKOP, CLKOS) | | 25 | — | 420 | MHz |
| f_{OUT2} | K-Divider Output Frequency (CLKOK) | | 0.195 | — | 210 | MHz |
| f_{VCO} | PLL VCO Frequency | | 420 | — | 840 | MHz |
| f_{PFD} | Phase Detector Input Frequency | | 25 | — | — | MHz |
| AC Characteristics | | | | | | |
| t_{DT} | Output Clock Duty Cycle | Default duty cycle elected ³ | 45 | 50 | 55 | % |
| t_{PH}^4 | Output Phase Accuracy | | — | — | TBD | UI |
| t_{OPJIT}^1 | Output Clock Period Jitter | Fout \geq 100MHz | — | — | +/- 125 | ps |
| | | Fout $<$ 100MHz | — | — | 0.02 | UIPP |
| t_{SK} | Input Clock to Output Clock skew | Divider ratio = integer | — | — | +/- 200 | ps |
| t_W | Output Clock Pulse Width | At 90% or 10% ³ | 1 | — | — | ns |
| t_{LOCK}^2 | PLL Lock-in Time | | — | — | 150 | us |
| t_{PA} | Programmable Delay Unit | | 100 | 250 | 400 | ps |
| t_{PJIT} | Input Clock Period Jitter | | — | — | +/- 200 | ps |
| t_{FBKDLY} | External Feedback Delay | | — | — | 10 | ns |
| t_{HI} | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| t_{LO} | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| t_{RST} | RST Pulse Width | | 10 | — | — | ns |

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

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LatticeECP/EC sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

| Parameter | Description | Min | Max | Units |
|--|--|----------|----------|--------|
| sysCONFIG Byte Data Flow | | | | |
| t _{SUCBDI} | Byte D[0:7] Setup Time to CCLK | 7 | — | ns |
| t _{HCBDI} | Byte D[0:7] Hold Time to CCLK | 1 | — | ns |
| t _{CODO} | Clock to Dout in Flowthrough Mode | — | TBD | ns |
| t _{SUCS} | CS[0:1] Setup Time to CCLK | 7 | — | ns |
| t _{HCS} | CS[0:1] Hold Time to CCLK | 1 | — | ns |
| t _{SUWD} | Write Signal Setup Time to CCLK | 7 | — | ns |
| t _{HWD} | Write Signal Hold Time to CCLK | 1 | — | ns |
| t _{DCB} | CCLK to BUSY Delay Time | — | 12 | ns |
| t _{CORD} | Clock to out for read Data | — | 12 | ns |
| sysCONFIG Byte Slave Clocking | | | | |
| t _{BSCH} | Byte Slave Clock Minimum High Pulse | 6 | — | ns |
| t _{BSCL} | Byte Slave Clock Minimum Low Pulse | 6 | — | ns |
| t _{BSCYC} | Byte Slave Clock Cycle Time | 15 | — | ns |
| sysCONFIG Serial (Bit) Data Flow | | | | |
| t _{SUSCDI} | Din Setup Time to CCLK Slave Mode | 7 | — | ns |
| t _{HSCDI} | Din Hold Time to CCLK Slave Mode | 1 | — | ns |
| t _{CODO} | Clock to Dout in Flowthrough Mode | — | 12 | ns |
| t _{SUMCDI} | Din Setup Time to CCLK Master Mode | 7 | — | ns |
| t _{HMCDI} | Din Hold Time to CCLK Master Mode | 1 | — | ns |
| sysCONFIG Serial Slave Clocking | | | | |
| t _{SSCH} | Serial Slave Clock Minimum High Pulse | 6 | — | ns |
| t _{SSCL} | Serial Slave Clock Minimum Low Pulse | 6 | — | ns |
| sysCONFIG POR, Initialization and Wake Up | | | | |
| t _{ICFG} | Minimum V _{CC} to INIT High | — | 50 | ms |
| t _{VMC} | Time from t _{ICFG} to valid Master Clock | — | 2 | us |
| t _{PRGMRJ} | PROGRAMB Pin Pulse Rejection | — | 10 | ns |
| t _{PRGM} | PROGRAMB Low Time to Start Configuration | 25 | — | ns |
| t _{DINIT} | PROGRAMB High to INIT High Delay | — | 1 | ms |
| t _{DPPINIT} | Delay Time from PROGRAMB Low to INIT Low | — | 37 | ns |
| t _{DPPDONE} | Delay Time from PROGRAMB Low to DONE Low | — | 37 | ns |
| t _{IODISS} | User I/O Disable from PROGRAMB Low | — | 25 | ns |
| t _{IOENSS} | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| t _{MWC} | Additional Wake Master Clock Signals after Done Pin High | 120 | — | cycles |
| sysCONFIG SPI Port | | | | |
| t _{CFGX} | Init High to CCLK Low | — | 1 | μs |
| t _{CSSPI} | Init High to CSSPIN Low | — | 2 | us |
| t _{CSCCLK} | CCLK Low before CSSPIN Low | 0 | - | ns |
| t _{SOCDO} | CCLK Low to Output Valid | — | 15 | ns |
| t _{SOE} | CSSPIN Active Setup Time | 300 | — | ns |
| t _{CSPID} | CSSPIN Low to First Clock Edge Setup Time | 300+3cyc | 600+6cyc | ns |
| f _{MAXSPI} | Max Frequency for SPI | — | 20 | MHz |

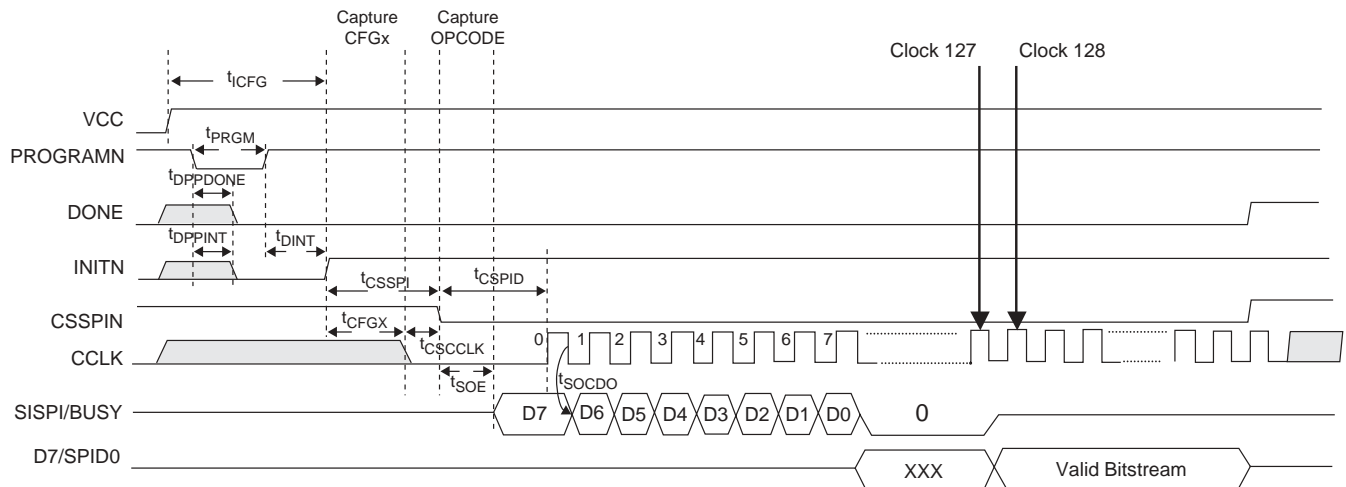
LatticeECP/EC sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

| Parameter | Description | Min | Max | Units |
|------------------------|-----------------------------------|---------------------|---------------------|-------|
| t_{SUSPI} | SOSPI Data Setup Time Before CCLK | 7 | — | ns |
| t_{HSPI} | SOSPI Data Hold Time After CCLK | 2 | — | ns |
| Master Clock Frequency | | Selected value -30% | Selected value +30% | MHz |
| Duty Cycle | | 40 | 60 | % |

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Figure 3-13. sysCONFIG SPI Port Sequence



JTAG Port Timing Specifications

Over Recommended Operating Conditions

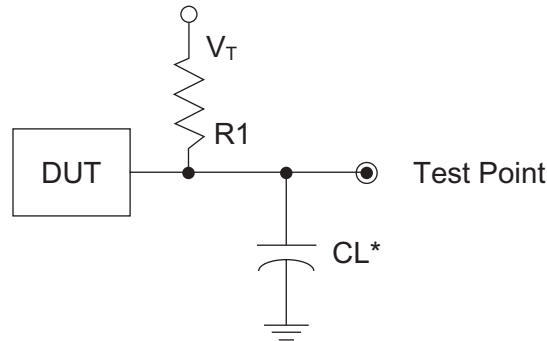
| Symbol | Parameter | Min. | Max. | Units |
|---------------|--|------|------|-------|
| f_{MAX} | TCK Clock Frequency | - | 25 | MHz |
| t_{BTCP} | TCK [BSCAN] clock pulse width | 40 | - | ns |
| t_{BTCPH} | TCK [BSCAN] clock pulse width high | 20 | - | ns |
| t_{BTCPL} | TCK [BSCAN] clock pulse width low | 20 | - | ns |
| t_{BTS} | TCK [BSCAN] setup time | 8 | - | ns |
| t_{BTH} | TCK [BSCAN] hold time | 10 | - | ns |
| t_{BTRF} | TCK [BSCAN] rise/fall time | 50 | - | mV/ns |
| t_{BTCO} | TAP controller falling edge of clock to valid output | - | 10 | ns |
| $t_{BTCODIS}$ | TAP controller falling edge of clock to valid disable | - | 10 | ns |
| t_{BTCOEN} | TAP controller falling edge of clock to valid enable | - | 10 | ns |
| t_{BTCRS} | BSCAN test capture register setup time | 8 | - | ns |
| t_{BTCRH} | BSCAN test capture register hold time | 25 | - | ns |
| t_{BUTCO} | BSCAN test update register, falling edge of clock to valid output | - | 25 | ns |
| t_{BUODIS} | BSCAN test update register, falling edge of clock to valid disable | - | 25 | ns |
| t_{BUPOEN} | BSCAN test update register, falling edge of clock to valid enable | - | 25 | ns |

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Switching Test Conditions

Figure 3-14 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-5.

Figure 3-14. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-5. Test Fixture Required Components, Non-Terminated Interfaces

| Test Condition | R ₁ | C _L | Timing Ref. | V _T |
|---|----------------|----------------|-----------------------------------|-----------------|
| LVTTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | 0pF | LVCMOS 3.3 = 1.5V | — |
| | | | LVCMOS 2.5 = V _{CCIO} /2 | — |
| | | | LVCMOS 1.8 = V _{CCIO} /2 | — |
| | | | LVCMOS 1.5 = V _{CCIO} /2 | — |
| | | | LVCMOS 1.2 = V _{CCIO} /2 | — |
| LVCMOS 2.5 I/O (Z -> H) | 188Ω | 0pF | V _{CCIO} /2 | V _{OL} |
| LVCMOS 2.5 I/O (Z -> L) | | | V _{CCIO} /2 | V _{OH} |
| LVCMOS 2.5 I/O (H -> Z) | | | V _{OH} - 0.15 | V _{OL} |
| LVCMOS 2.5 I/O (L -> Z) | | | V _{OL} + 0.15 | V _{OH} |

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|-----|---|
| General Purpose | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | <p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected.</p> <p>Some of these user-programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic.</p> <p>During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p> |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| GND | — | Ground. Dedicated pins. |
| V _{CC} | — | Power supply pins for core logic. Dedicated pins. |
| V _{CCAUX} | — | Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated pins. |
| V _{CCIOx} | — | Power supply pins for I/O bank x. Dedicated pins. |
| V _{REF1_x} , V _{REF2_x} | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are as assigned V _{REF} inputs. When not used, they may be used as I/O pins. |
| XRES | — | 10K ohm +/-1% resistor must be connected between this pad and ground. |
| PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_PLL[T, C]_IN_A | I | Reference clock (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_PLL[T, C]_FB_A | I | Optional feedback (PLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | I | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank. |
| [LOC]DQS[num] | I | DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output. |
| Test and Programming (Dedicated pins) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |

Signal Descriptions (Cont.)

| Signal Name | I/O | Descriptions |
|---|-----|--|
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |
| TDO | O | Output pin. Test Data out pin used to shift data out of device using 1149.1. |
| V _{CCJ} | — | V _{CCJ} - The power supply pin for JTAG Test Access Port. |
| Configuration Pads (used during sysCONFIG) | | |
| CFG[2:0] | I | Mode pins used to specify configuration modes values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins. |
| INITN | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| BUSY/SISPI | I/O | Read control command in SPI3 or SPIX mode. |
| CSN | I | sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. |
| CS1N | I | sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. |
| WRITEN | I | Write Data on Parallel port (Active low). |
| D[7:0]/SPID[0:7] | I/O | sysCONFIG Port Data I/O. |
| DOUT/CSON | O | Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. |
| DI/CSSPIN | I | Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. |

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO Within PIC | DDR Strobe (DQS) and Data (DQ) Pins |
|---------------------------------|----------------|-------------------------------------|
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |

Notes:

1. "n" is a Row/Column PIC number
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. PIC numbering definitions are provided in the "Signal Names" column of the Signal Descriptions table.

Pin Information Summary

| Pin Type | | LFEC6/EC6 | | | | LFEC20/EC20 | |
|---|-----------|-----------|----------|-----------|-----------|-------------|-----------|
| | | 144-TQFP | 208-PQFP | 256-fpBGA | 484-fpBGA | 484-fpBGA | 672-fpBGA |
| Single Ended User I/O | | 97 | 147 | 195 | 224 | 360 | 400 |
| Differential Pair User I/O | | 72 | 97 | 97 | 112 | 180 | 200 |
| Configuration | Dedicated | 13 | 13 | 13 | 13 | 13 | 13 |
| | Muxed | 48 | 48 | 48 | 48 | 56 | 56 |
| TAP | | 5 | 5 | 5 | 5 | 5 | 5 |
| Dedicated (total without supplies) | | 110 | 160 | 208 | 373 | 373 | 509 |
| V _{CC} | | 4 | 4 | 10 | 20 | 20 | 32 |
| V _{CCAUX} | | 2 | 4 | 2 | 12 | 12 | 20 |
| V _{CCIO} | Bank0 | 2 | 3 | 2 | 4 | 4 | 6 |
| | Bank1 | 2 | 2 | 2 | 4 | 4 | 6 |
| | Bank2 | 1 | 2 | 2 | 4 | 4 | 6 |
| | Bank3 | 2 | 2 | 2 | 4 | 4 | 6 |
| | Bank4 | 2 | 2 | 2 | 4 | 4 | 6 |
| | Bank5 | 2 | 3 | 2 | 4 | 4 | 6 |
| | Bank6 | 2 | 2 | 2 | 4 | 4 | 6 |
| | Bank7 | 1 | 2 | 2 | 4 | 4 | 6 |
| GND, GND0-GND7 | | 14 | 18 | 20 | 44 | 44 | 63 |
| NC | | 0 | 4 | 0 | 139 | 3 | 96 |
| Single Ended/ Differential I/O per Bank | Bank0 | 14 | 26 | 32 | 32 | 48 | 64 |
| | Bank1 | 13 | 17 | 18 | 32 | 48 | 48 |
| | Bank2 | 8 | 14 | 16 | 16 | 40 | 40 |
| | Bank3 | 13 | 16 | 32 | 32 | 44 | 48 |
| | Bank4 | 14 | 17 | 17 | 32 | 48 | 48 |
| | Bank5 | 13 | 26 | 32 | 32 | 48 | 64 |
| | Bank6 | 14 | 16 | 32 | 32 | 44 | 48 |
| | Bank7 | 8 | 15 | 16 | 16 | 40 | 40 |
| V _{CCJ} | | 1 | 1 | 1 | 1 | 1 | 1 |

Note: During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

Power Supply and NC Connections

| Signals | 144 TQFP | 208 PQFP | 256 fpBGA |
|----------------|--|--|--|
| VCC | 11, 13, 92, 99 | 24, 26, 128, 135 | E12, E5, E8, M12, M5, M9, F6, F11, L11, L6 |
| VCCIO0 | 136, 143 | 187, 197, 208 | F7, F8 |
| VCCIO1 | 110, 125 | 157, 176 | F9, F10 |
| VCCIO2 | 108 | 145, 155 | G11, H11 |
| VCCIO3 | 73, 84 | 106, 120 | J11, K11 |
| VCCIO4 | 55, 71 | 85, 104 | L9, L10 |
| VCCIO5 | 38, 44 | 53, 64, 74 | L7, L8 |
| VCCIO6 | 24, 36 | 37, 51 | J6, K6 |
| VCCIO7 | 1 | 2, 13 | G6, H6 |
| VCCJ | 19 | 32 | L4 |
| VCCAUX | 54, 126 | 22, 84, 136, 177 | B15, R2 |
| GND, GND0-GND7 | 12, 15, 28, 37, 52, 63, 72, 80, 96, 98, 109, 117, 128, 144 | 1, 18, 25, 28, 41, 52, 72, 82, 93, 105, 116, 132, 134, 138, 156, 168, 179, 189 | A1, A16, G10, G7, G8, G9, H10, H7, H8, H9, J10, J7, J8, J9, K10, K7, K8, K9, T1, T16 |
| NC | - | - | - |

Power Supply and NC Connections

| Signals | 484 fpBGA | 672 fpBGA |
|----------------|--|--|
| VCC | J6, J7, J16, J17, K6, K7, K16, K17, L6, L17, M6, M17, N6, N7, N16, N17, P6, P7, P16, P17 | H8, H9, H10, H11, H16, H17, H18, H19, J9, J18, K8, K19, L8, L19, M19, N7, R7, R20, T19, U8, U19, V8, V18, V9, W8, W9, W10, W11, W16, W17, W18, W19 |
| VCCIO0 | G11, H9, H10, H11 | H12, H13, J10, J11, J12, J13 |
| VCCIO1 | G12, H12, H13, H14 | H14, H15, J14, J15, J16, J17 |
| VCCIO2 | J15, K15, L15, L16 | K17, K18, L18, M18, N18, N19 |
| VCCIO3 | M15, M16, N15, P15 | P18, P19, R18, R19, T8, U18 |
| VCCIO4 | R12, R13, R14, T12 | V14, V15, V16, V17, W14, W15 |
| VCCIO5 | R9, R10, R11, T11 | V10, V11, V12, V13, W12, W13 |
| VCCIO6 | M7, M8, N8, P8 | P8, P9, R8, R9, T9, U9 |
| VCCIO7 | J8, K8, L7, L8 | K9, L9, M8, M9, N8, N9 |
| VCCJ | U2 | U6 |
| VCCAUX | G7, G8, G15, G16, H7, H16, R7, R16, T7, T8, T15, T16 | G13, H7, H20, J8, J19, K7, L20, M7, M20, N20, P7, P20, T7, T8, T20, V7, V19, W20, Y7, Y13 |
| GND, GND0-GND7 | A1, A22, AB1, AB22, H8, H15, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14, R8, R15 | K10, K11, K12, K13, K14, K15, K16, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17 |
| NC | ECP6/EC6: C3, B2, E5, F5, D3, C2, F4, G4, E3, D2, B1, C1, F3, E2, G5, H6, G3, H4, J5, H5, F2, F1, E1, D1, R6, P5, P3, P4, R1, R2, R5, R4, T1, T2, R3, T3, A2, AB2, A21 ECP/EC20: A2, AB2, A21 | A25, B2, B23, B24, B25, B26, C2, C3, C19, C20, C21, C22, C23, C24, D3, D5, D20, D21, D22, D24, E5, E19, E21, E22, E24, E25, E26, F4, F5, F20, F22, F23, F24, F26, G5, G20, G26, H2, H3, H5, H6, H22, J2, J3, J7, J21, J22, J23, W5, W7, Y5, Y6, Y19, Y20, Y21, Y22, Y23, Y24, AA2, AA3, AA4, AA5, AA21, AA22, AA23, AA24, AB3, AB5, AB19, AB20, AB21, AB22, AB23, AB24, AC2, AC3, AC19, AC20, AC21, AC22, AD1, AD2, AD3, AD19, AD20, AD21, AD22, AD23, AD24, AD25, AD26, AE1, AE24, AE25, AE26, AF25 |

LFCEP6/LFEC6 Logic Signal Connections: 144 TQFP

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|----------------|
| 1 | VCCIO7 | 7 | | |
| 2 | PL2A | 7 | T | VREF2_7 |
| 3 | PL2B | 7 | C | VREF1_7 |
| 4 | PL7A | 7 | T | |
| 5 | PL7B | 7 | C | |
| 6 | PL8A | 7 | T | |
| 7 | PL8B | 7 | C | |
| 8 | PL9A | 7 | T | PCLKT7_0 |
| 9 | PL9B | 7 | C | PCLKC7_0 |
| 10 | XRES | 6 | | |
| 11 | VCC | - | | |
| 12 | GND | - | | |
| 13 | VCC | - | | |
| 14 | TCK | 6 | | |
| 15 | GND | - | | |
| 16 | TDI | 6 | | |
| 17 | TMS | 6 | | |
| 18 | TDO | 6 | | |
| 19 | VCCJ | 6 | | |
| 20 | PL20A | 6 | T | LLM0_PLLT_IN_A |
| 21 | PL20B | 6 | C | LLM0_PLLC_IN_A |
| 22 | PL21A | 6 | T | LLM0_PLLT_FB_A |
| 23 | PL21B | 6 | C | LLM0_PLLC_FB_A |
| 24 | VCCIO6 | 6 | | |
| 25 | PL22A | 6 | T | |
| 26 | PL22B | 6 | C | |
| 27 | PL23A | 6 | T | |
| 28 | GND6 | 6 | | |
| 29 | PL23B | 6 | C | |
| 30 | PL24A | 6 | T | LDQS24 |
| 31 | PL24B | 6 | C | |
| 32 | PL25A | 6 | T | |
| 33 | PL25B | 6 | C | |
| 34 | PL27A | 6 | T | VREF1_6 |
| 35 | PL27B | 6 | C | VREF2_6 |
| 36 | VCCIO6 | 6 | | |
| 37* | GND5, GND6 | | | |
| 38 | VCCIO5 | 5 | | |
| 39 | PB10A | 5 | T | |
| 40 | PB10B | 5 | C | |
| 41 | PB11A | 5 | T | |
| 42 | PB11B | 5 | C | |
| 43 | PB13B | 5 | | |

LFCEP6/LFEC6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|----------------|
| 44 | VCCIO5 | 5 | | |
| 45 | PB14A | 5 | T | BDQS14 |
| 46 | PB14B | 5 | C | |
| 47 | PB15A | 5 | T | |
| 48 | PB15B | 5 | C | |
| 49 | PB16A | 5 | T | VREF2_5 |
| 50 | PB16B | 5 | C | VREF1_5 |
| 51 | PB17A | 5 | T | PCLKT5_0 |
| 52 | GND5 | 5 | | |
| 53 | PB17B | 5 | C | PCLKC5_0 |
| 54 | VCCAUX | - | | |
| 55 | VCCIO4 | 4 | | |
| 56 | PB18A | 4 | T | WRITEN |
| 57 | PB18B | 4 | C | CS1N |
| 58 | PB19A | 4 | T | VREF1_4 |
| 59 | PB19B | 4 | C | CSN |
| 60 | PB20A | 4 | T | VREF2_4 |
| 61 | PB20B | 4 | C | D0/SPID7 |
| 62 | PB21A | 4 | T | D2/SPID5 |
| 63 | GND4 | 4 | | |
| 64 | PB21B | 4 | C | D1/SPID6 |
| 65 | PB22A | 4 | T | BDQS22 |
| 66 | PB22B | 4 | C | D3/SPID4 |
| 67 | PB23A | 4 | T | |
| 68 | PB23B | 4 | C | D4/SPID3 |
| 69 | PB24B | 4 | | D5/SPID2 |
| 70 | PB25B | 4 | | D6/SPID1 |
| 71 | VCCIO4 | 4 | | |
| 72* | GND3, GND4 | | | |
| 73 | VCCIO3 | 3 | | |
| 74 | PR27A | 3 | | VREF1_3 |
| 75 | PR25B | 3 | C | |
| 76 | PR25A | 3 | T | |
| 77 | PR24B | 3 | C | |
| 78 | PR24A | 3 | T | RDQS24 |
| 79 | PR23B | 3 | C | RLM0_PLLC_FB_A |
| 80 | GND3 | 3 | | |
| 81 | PR23A | 3 | T | RLM0_PLLT_FB_A |
| 82 | PR22B | 3 | C | RLM0_PLLC_IN_A |
| 83 | PR22A | 3 | T | RLM0_PLLT_IN_A |
| 84 | VCCIO3 | 3 | | |
| 85 | PR21B | 3 | C | DI/CSSPIN |
| 86 | PR21A | 3 | T | DOUT/CSON |
| 87 | PR20B | 3 | C | BUSY/SISPI |

LFCEP6/LFEC6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|---------------|
| 88 | PR20A | 3 | T | D7/SPID0 |
| 89 | CFG2 | 3 | | |
| 90 | CFG1 | 3 | | |
| 91 | CFG0 | 3 | | |
| 92 | VCC | - | | |
| 93 | PROGRAMN | 3 | | |
| 94 | CCLK | 3 | | |
| 95 | INITN | 3 | | |
| 96 | GND | - | | |
| 97 | DONE | 3 | | |
| 98 | GND | - | | |
| 99 | VCC | - | | |
| 100 | PR9B | 2 | C | PCLKC2_0 |
| 101 | PR9A | 2 | T | PCLKT2_0 |
| 102 | PR8B | 2 | C | |
| 103 | PR8A | 2 | T | |
| 104 | PR7B | 2 | C | |
| 105 | PR7A | 2 | T | |
| 106 | PR2B | 2 | C | VREF1_2 |
| 107 | PR2A | 2 | T | VREF2_2 |
| 108 | VCCIO2 | 2 | | |
| 109* | GND1, GND2 | | | |
| 110 | VCCIO1 | 1 | | |
| 111 | PT25B | 1 | C | |
| 112 | PT25A | 1 | T | |
| 113 | PT23A | 1 | | |
| 114 | PT22B | 1 | C | |
| 115 | PT22A | 1 | T | TDQS22 |
| 116 | PT21B | 1 | C | |
| 117 | GND1 | 1 | | |
| 118 | PT21A | 1 | T | |
| 119 | PT20B | 1 | C | |
| 120 | PT20A | 1 | T | |
| 121 | PT19B | 1 | C | VREF2_1 |
| 122 | PT19A | 1 | T | VREF1_1 |
| 123 | PT18B | 1 | C | |
| 124 | PT18A | 1 | T | |
| 125 | VCCIO1 | 1 | | |
| 126 | VCCAUX | - | | |
| 127 | PT17B | 0 | C | PCLKC0_0 |
| 128 | GND0 | 0 | | |
| 129 | PT17A | 0 | T | PCLKT0_0 |
| 130 | PT16B | 0 | C | VREF1_0 |
| 131 | PT16A | 0 | T | VREF2_0 |

LFCEP6/LFEC6 Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|---------------|
| 132 | PT15B | 0 | C | |
| 133 | PT15A | 0 | T | |
| 134 | PT14B | 0 | C | |
| 135 | PT14A | 0 | T | TDQS14 |
| 136 | VCCIO0 | 0 | | |
| 137 | PT13B | 0 | C | |
| 138 | PT13A | 0 | T | |
| 139 | PT12B | 0 | C | |
| 140 | PT12A | 0 | T | |
| 141 | PT10B | 0 | C | |
| 142 | PT10A | 0 | T | |
| 143 | VCCIO0 | 0 | | |
| 144* | GND0, GND7 | | | |

* Double bonded to the pin.

LFCEP6/LFEC6 Logic Signal Connections: 208 PQFP

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|----------------|
| 1* | GND0, GND7 | | | |
| 2 | VCCIO7 | 7 | | |
| 3 | PL2A | 7 | T | VREF2_7 |
| 4 | PL2B | 7 | C | VREF1_7 |
| 5 | NC | - | | |
| 6 | NC | - | | |
| 7 | PL3B | 7 | | |
| 8 | PL4A | 7 | T | |
| 9 | PL4B | 7 | C | |
| 10 | PL5A | 7 | T | |
| 11 | PL5B | 7 | C | |
| 12 | PL6A | 7 | T | LDQS6 |
| 13 | VCCIO7 | 7 | | |
| 14 | PL6B | 7 | C | |
| 15 | PL7A | 7 | T | |
| 16 | PL7B | 7 | C | |
| 17 | PL8A | 7 | T | |
| 18 | GND7 | 7 | | |
| 19 | PL8B | 7 | C | |
| 20 | PL9A | 7 | T | PCLKT7_0 |
| 21 | PL9B | 7 | C | PCLKC7_0 |
| 22 | VCCAUX | - | | |
| 23 | XRES | 6 | | |
| 24 | VCC | - | | |
| 25 | GND | - | | |
| 26 | VCC | - | | |
| 27 | TCK | 6 | | |
| 28 | GND | - | | |
| 29 | TDI | 6 | | |
| 30 | TMS | 6 | | |
| 31 | TDO | 6 | | |
| 32 | VCCJ | 6 | | |
| 33 | PL20A | 6 | T | LLM0_PLLT_IN_A |
| 34 | PL20B | 6 | C | LLM0_PLLC_IN_A |
| 35 | PL21A | 6 | T | LLM0_PLLT_FB_A |
| 36 | PL21B | 6 | C | LLM0_PLLC_FB_A |
| 37 | VCCIO6 | 6 | | |
| 38 | PL22A | 6 | T | |
| 39 | PL22B | 6 | C | |
| 40 | PL23A | 6 | T | |
| 41 | GND6 | 6 | | |
| 42 | PL23B | 6 | C | |
| 43 | PL24A | 6 | T | LDQS24 |

LFCEP6/LFEC6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|---------------|
| 44 | PL24B | 6 | C | |
| 45 | PL25A | 6 | T | |
| 46 | PL25B | 6 | C | |
| 47 | PL26A | 6 | T | |
| 48 | PL26B | 6 | C | |
| 49 | PL27A | 6 | T | VREF1_6 |
| 50 | PL27B | 6 | C | VREF2_6 |
| 51 | VCCIO6 | 6 | | |
| 52* | GND5, GND6 | | | |
| 53 | VCCIO5 | 5 | | |
| 54 | PB2A | 5 | T | |
| 55 | PB2B | 5 | C | |
| 56 | PB3A | 5 | T | |
| 57 | PB3B | 5 | C | |
| 58 | PB4A | 5 | T | |
| 59 | PB4B | 5 | C | |
| 60 | PB5A | 5 | T | |
| 61 | PB5B | 5 | C | |
| 62 | PB6A | 5 | T | BDQS6 |
| 63 | PB6B | 5 | C | |
| 64 | VCCIO5 | 5 | | |
| 65 | PB10A | 5 | T | |
| 66 | PB10B | 5 | C | |
| 67 | PB11A | 5 | T | |
| 68 | PB11B | 5 | C | |
| 69 | PB12A | 5 | T | |
| 70 | PB12B | 5 | C | |
| 71 | PB13A | 5 | T | |
| 72 | GND5 | 5 | | |
| 73 | PB13B | 5 | C | |
| 74 | VCCIO5 | 5 | | |
| 75 | PB14A | 5 | T | BDQS14 |
| 76 | PB14B | 5 | C | |
| 77 | PB15A | 5 | T | |
| 78 | PB15B | 5 | C | |
| 79 | PB16A | 5 | T | VREF2_5 |
| 80 | PB16B | 5 | C | VREF1_5 |
| 81 | PB17A | 5 | T | PCLKT5_0 |
| 82 | GND5 | 5 | | |
| 83 | PB17B | 5 | C | PCLKC5_0 |
| 84 | VCCAUX | - | | |
| 85 | VCCIO4 | 4 | | |
| 86 | PB18A | 4 | T | WRITEN |
| 87 | PB18B | 4 | C | CS1N |

LFCEP6/LFEC6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|----------------|
| 88 | PB19A | 4 | T | VREF1_4 |
| 89 | PB19B | 4 | C | CSN |
| 90 | PB20A | 4 | T | VREF2_4 |
| 91 | PB20B | 4 | C | D0/SPID7 |
| 92 | PB21A | 4 | T | D2/SPID5 |
| 93 | GND4 | 4 | | |
| 94 | PB21B | 4 | C | D1/SPID6 |
| 95 | PB22A | 4 | T | BDQS22 |
| 96 | PB22B | 4 | C | D3/SPID4 |
| 97 | PB23A | 4 | T | |
| 98 | PB23B | 4 | C | D4/SPID3 |
| 99 | PB24A | 4 | T | |
| 100 | PB24B | 4 | C | D5/SPID2 |
| 101 | PB25A | 4 | T | |
| 102 | PB25B | 4 | C | D6/SPID1 |
| 103 | PB33A | 4 | | |
| 104 | VCCIO4 | 4 | | |
| 105* | GND3, GND4 | | | |
| 106 | VCCIO3 | 3 | | |
| 107 | PR27B | 3 | C | VREF2_3 |
| 108 | PR27A | 3 | T | VREF1_3 |
| 109 | PR26B | 3 | C | |
| 110 | PR26A | 3 | T | |
| 111 | PR25B | 3 | C | |
| 112 | PR25A | 3 | T | |
| 113 | PR24B | 3 | C | |
| 114 | PR24A | 3 | T | RDQS24 |
| 115 | PR23B | 3 | C | RLM0_PLLC_FB_A |
| 116 | GND3 | 3 | | |
| 117 | PR23A | 3 | T | RLM0_PLLT_FB_A |
| 118 | PR22B | 3 | C | RLM0_PLLC_IN_A |
| 119 | PR22A | 3 | T | RLM0_PLLT_IN_A |
| 120 | VCCIO3 | 3 | | |
| 121 | PR21B | 3 | C | DI/CSSPIN |
| 122 | PR21A | 3 | T | DOUC/CSN |
| 123 | PR20B | 3 | C | BUSY/SISPI |
| 124 | PR20A | 3 | T | D7/SPID0 |
| 125 | CFG2 | 3 | | |
| 126 | CFG1 | 3 | | |
| 127 | CFG0 | 3 | | |
| 128 | VCC | - | | |
| 129 | PROGRAMN | 3 | | |
| 130 | CCLK | 3 | | |
| 131 | INITN | 3 | | |

LFCEP6/LFEC6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|---------------|
| 132 | GND | - | | |
| 133 | DONE | 3 | | |
| 134 | GND | - | | |
| 135 | VCC | - | | |
| 136 | VCCAUX | - | | |
| 137 | PR9B | 2 | C | PCLKC2_0 |
| 138 | GND2 | 2 | | |
| 139 | PR9A | 2 | T | PCLKT2_0 |
| 140 | PR8B | 2 | C | |
| 141 | PR8A | 2 | T | |
| 142 | PR7B | 2 | C | |
| 143 | PR7A | 2 | T | |
| 144 | PR6B | 2 | C | |
| 145 | VCCIO2 | 2 | | |
| 146 | PR6A | 2 | T | RDQS6 |
| 147 | PR5B | 2 | C | |
| 148 | PR5A | 2 | T | |
| 149 | PR4B | 2 | C | |
| 150 | PR4A | 2 | T | |
| 151 | NC | - | | |
| 152 | NC | - | | |
| 153 | PR2B | 2 | C | VREF1_2 |
| 154 | PR2A | 2 | T | VREF2_2 |
| 155 | VCCIO2 | 2 | | |
| 156* | GND1, GND2 | | | |
| 157 | VCCIO1 | 1 | | |
| 158 | PT33A | 1 | | |
| 159 | PT25B | 1 | C | |
| 160 | PT25A | 1 | T | |
| 161 | PT24B | 1 | C | |
| 162 | PT24A | 1 | T | |
| 163 | PT23B | 1 | C | |
| 164 | PT23A | 1 | T | |
| 165 | PT22B | 1 | C | |
| 166 | PT22A | 1 | T | TDQS22 |
| 167 | PT21B | 1 | C | |
| 168 | GND1 | 1 | | |
| 169 | PT21A | 1 | T | |
| 170 | PT20B | 1 | C | |
| 171 | PT20A | 1 | T | |
| 172 | PT19B | 1 | C | VREF2_1 |
| 173 | PT19A | 1 | T | VREF1_1 |
| 174 | PT18B | 1 | C | |
| 175 | PT18A | 1 | T | |

LFCEP6/LFEC6 Logic Signal Connections: 208 PQFP (Cont.)

| Pin Number | Pin Function | Bank | LVDS | Dual Function |
|------------|--------------|------|------|---------------|
| 176 | VCCIO1 | 1 | | |
| 177 | VCCAUX | - | | |
| 178 | PT17B | 0 | C | PCLKC0_0 |
| 179 | GND0 | 0 | | |
| 180 | PT17A | 0 | T | PCLKT0_0 |
| 181 | PT16B | 0 | C | VREF1_0 |
| 182 | PT16A | 0 | T | VREF2_0 |
| 183 | PT15B | 0 | C | |
| 184 | PT15A | 0 | T | |
| 185 | PT14B | 0 | C | |
| 186 | PT14A | 0 | T | TDQS14 |
| 187 | VCCIO0 | 0 | | |
| 188 | PT13B | 0 | C | |
| 189 | GND0 | 0 | | |
| 190 | PT13A | 0 | T | |
| 191 | PT12B | 0 | C | |
| 192 | PT12A | 0 | T | |
| 193 | PT11B | 0 | C | |
| 194 | PT11A | 0 | T | |
| 195 | PT10B | 0 | C | |
| 196 | PT10A | 0 | T | |
| 197 | VCCIO0 | 0 | | |
| 198 | PT6B | 0 | C | |
| 199 | PT6A | 0 | T | TDQS6 |
| 200 | PT5B | 0 | C | |
| 201 | PT5A | 0 | T | |
| 202 | PT4B | 0 | C | |
| 203 | PT4A | 0 | T | |
| 204 | PT3B | 0 | C | |
| 205 | PT3A | 0 | T | |
| 206 | PT2B | 0 | C | |
| 207 | PT2A | 0 | T | |
| 208 | VCCIO0 | 0 | | |

* Double bonded to the pin.

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| GND | GND7 | 7 | | |
| D4 | PL2A | 7 | T | VREF2_7 |
| D3 | PL2B | 7 | C | VREF1_7 |
| C3 | PL3A | 7 | T | |
| C2 | PL3B | 7 | C | |
| B1 | PL4A | 7 | T | |
| C1 | PL4B | 7 | C | |
| E3 | PL5A | 7 | T | |
| E4 | PL5B | 7 | C | |
| F4 | PL6A | 7 | T | LDQS6 |
| F5 | PL6B | 7 | C | |
| G4 | PL7A | 7 | T | |
| G3 | PL7B | 7 | C | |
| D2 | PL8A | 7 | T | |
| GND | GND7 | 7 | | |
| D1 | PL8B | 7 | C | |
| E1 | PL9A | 7 | T | PCLKT7_0 |
| E2 | PL9B | 7 | C | PCLKC7_0 |
| F3 | XRES | 6 | | |
| G5 | PL11A | 6 | T | |
| H5 | PL11B | 6 | C | |
| F2 | PL12A | 6 | T | |
| F1 | PL12B | 6 | C | |
| H4 | PL13A | 6 | T | |
| H3 | PL13B | 6 | C | |
| G2 | PL14A | 6 | T | |
| GND | GND6 | 6 | | |
| G1 | PL14B | 6 | C | |
| J4 | PL15A | 6 | T | LDQS15 |
| J3 | PL15B | 6 | C | |
| J5 | PL16A | 6 | T | |
| K5 | PL16B | 6 | C | |
| H2 | PL17A | 6 | T | |
| H1 | PL17B | 6 | C | |
| J2 | PL18A | 6 | T | |
| GND | GND6 | 6 | | |
| J1 | PL18B | 6 | C | |
| K4 | TCK | 6 | | |
| K3 | TDI | 6 | | |
| L3 | TMS | 6 | | |
| L5 | TDO | 6 | | |
| L4 | VCCJ | 6 | | |
| K2 | PL20A | 6 | T | LLM0_PLLT_IN_A |

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| K1 | PL20B | 6 | C | LLM0_PLLC_IN_A |
| L2 | PL21A | 6 | T | LLM0_PLLT_FB_A |
| L1 | PL21B | 6 | C | LLM0_PLLC_FB_A |
| M2 | PL22A | 6 | T | |
| M1 | PL22B | 6 | C | |
| N1 | PL23A | 6 | T | |
| GND | GND6 | 6 | | |
| N2 | PL23B | 6 | C | |
| M4 | PL24A | 6 | T | LDQS24 |
| M3 | PL24B | 6 | C | |
| P1 | PL25A | 6 | T | |
| R1 | PL25B | 6 | C | |
| P2 | PL26A | 6 | T | |
| P3 | PL26B | 6 | C | |
| N3 | PL27A | 6 | T | VREF1_6 |
| N4 | PL27B | 6 | C | VREF2_6 |
| GND | GND6 | 6 | | |
| GND | GND5 | 5 | | |
| P4 | PB2A | 5 | T | |
| N5 | PB2B | 5 | C | |
| P5 | PB3A | 5 | T | |
| P6 | PB3B | 5 | C | |
| R4 | PB4A | 5 | T | |
| R3 | PB4B | 5 | C | |
| T2 | PB5A | 5 | T | |
| T3 | PB5B | 5 | C | |
| R5 | PB6A | 5 | T | BDQS6 |
| R6 | PB6B | 5 | C | |
| T4 | PB7A | 5 | T | |
| T5 | PB7B | 5 | C | |
| N6 | PB8A | 5 | T | |
| M6 | PB8B | 5 | C | |
| T6 | PB9A | 5 | T | |
| GND | GND5 | 5 | | |
| T7 | PB9B | 5 | C | |
| P7 | PB10A | 5 | T | |
| N7 | PB10B | 5 | C | |
| R7 | PB11A | 5 | T | |
| R8 | PB11B | 5 | C | |
| M7 | PB12A | 5 | T | |
| M8 | PB12B | 5 | C | |
| T8 | PB13A | 5 | T | |
| GND | GND5 | 5 | | |
| T9 | PB13B | 5 | C | |

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| P8 | PB14A | 5 | T | BDQS14 |
| N8 | PB14B | 5 | C | |
| R9 | PB15A | 5 | T | |
| R10 | PB15B | 5 | C | |
| P9 | PB16A | 5 | T | VREF2_5 |
| N9 | PB16B | 5 | C | VREF1_5 |
| T10 | PB17A | 5 | T | PCLKT5_0 |
| GND | GND5 | 5 | | |
| T11 | PB17B | 5 | C | PCLKC5_0 |
| T12 | PB18A | 4 | T | WRITEN |
| T13 | PB18B | 4 | C | CS1N |
| P10 | PB19A | 4 | T | VREF1_4 |
| N10 | PB19B | 4 | C | CSN |
| T14 | PB20A | 4 | T | VREF2_4 |
| T15 | PB20B | 4 | C | D0/SPID7 |
| M10 | PB21A | 4 | T | D2/SPID5 |
| GND | GND4 | 4 | | |
| M11 | PB21B | 4 | C | D1/SPID6 |
| R11 | PB22A | 4 | T | BDQS22 |
| P11 | PB22B | 4 | C | D3/SPID4 |
| R13 | PB23A | 4 | T | |
| R14 | PB23B | 4 | C | D4/SPID3 |
| P12 | PB24A | 4 | T | |
| P13 | PB24B | 4 | C | D5/SPID2 |
| N11 | PB25A | 4 | T | |
| GND | GND4 | 4 | | |
| N12 | PB25B | 4 | C | D6/SPID1 |
| R12 | PB26A | 4 | | |
| GND | GND4 | 4 | | |
| GND | GND4 | 4 | | |
| GND | GND3 | 3 | | |
| N13 | PR27B | 3 | C | VREF2_3 |
| N14 | PR27A | 3 | T | VREF1_3 |
| P14 | PR26B | 3 | C | |
| P15 | PR26A | 3 | T | |
| R15 | PR25B | 3 | C | |
| R16 | PR25A | 3 | T | |
| M13 | PR24B | 3 | C | |
| M14 | PR24A | 3 | T | RDQS24 |
| P16 | PR23B | 3 | C | RLM0_PLLC_FB_A |
| GND | GND3 | 3 | | |
| N16 | PR23A | 3 | T | RLM0_PLLT_FB_A |
| N15 | PR22B | 3 | C | RLM0_PLLC_IN_A |
| M15 | PR22A | 3 | T | RLM0_PLLT_IN_A |

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| M16 | PR21B | 3 | C | DI/CSSPIN |
| L16 | PR21A | 3 | T | DOUT/CSON |
| K16 | PR20B | 3 | C | BUSY/SISPI |
| J16 | PR20A | 3 | T | D7/SPID0 |
| L12 | CFG2 | 3 | | |
| L14 | CFG1 | 3 | | |
| L13 | CFG0 | 3 | | |
| K13 | PROGRAMN | 3 | | |
| L15 | CCLK | 3 | | |
| K15 | INITN | 3 | | |
| K14 | DONE | 3 | | |
| H16 | PR18B | 3 | C | |
| GND | GND3 | 3 | | |
| H15 | PR18A | 3 | T | |
| G16 | PR17B | 3 | C | |
| G15 | PR17A | 3 | T | |
| K12 | PR16B | 3 | C | |
| J12 | PR16A | 3 | T | |
| J14 | PR15B | 3 | C | |
| J15 | PR15A | 3 | T | RDQS15 |
| F16 | PR14B | 3 | C | |
| GND | GND3 | 3 | | |
| F15 | PR14A | 3 | T | |
| J13 | PR13B | 3 | C | |
| H13 | PR13A | 3 | T | |
| H14 | PR12B | 3 | C | |
| G14 | PR12A | 3 | T | |
| E16 | PR11B | 3 | C | |
| E15 | PR11A | 3 | T | |
| H12 | PR9B | 2 | C | PCLKC2_0 |
| GND | GND2 | 2 | | |
| G12 | PR9A | 2 | T | PCLKT2_0 |
| G13 | PR8B | 2 | C | |
| F13 | PR8A | 2 | T | |
| F12 | PR7B | 2 | C | |
| E13 | PR7A | 2 | T | |
| D16 | PR6B | 2 | C | |
| D15 | PR6A | 2 | T | RDQS6 |
| F14 | PR5B | 2 | C | |
| E14 | PR5A | 2 | T | |
| C16 | PR4B | 2 | C | |
| B16 | PR4A | 2 | T | |
| C15 | PR3B | 2 | C | |
| C14 | PR3A | 2 | T | |

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| D14 | PR2B | 2 | C | VREF1_2 |
| D13 | PR2A | 2 | T | VREF2_2 |
| GND | GND2 | 2 | | |
| GND | GND1 | 1 | | |
| GND | GND1 | 1 | | |
| B13 | PT26B | 1 | C | |
| C13 | PT26A | 1 | T | |
| GND | GND1 | 1 | | |
| C12 | PT25B | 1 | C | |
| D12 | PT25A | 1 | T | |
| A15 | PT24B | 1 | C | |
| B14 | PT24A | 1 | T | |
| D11 | PT23B | 1 | C | |
| C11 | PT23A | 1 | T | |
| E10 | PT22B | 1 | C | |
| E11 | PT22A | 1 | T | TDQS22 |
| A14 | PT21B | 1 | C | |
| GND | GND1 | 1 | | |
| A13 | PT21A | 1 | T | |
| D10 | PT20B | 1 | C | |
| C10 | PT20A | 1 | T | |
| A12 | PT19B | 1 | C | VREF2_1 |
| B12 | PT19A | 1 | T | VREF1_1 |
| A11 | PT18B | 1 | C | |
| B11 | PT18A | 1 | T | |
| A10 | PT17B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | |
| B10 | PT17A | 0 | T | PCLKT0_0 |
| C9 | PT16B | 0 | C | VREF1_0 |
| B9 | PT16A | 0 | T | VREF2_0 |
| E9 | PT15B | 0 | C | |
| D9 | PT15A | 0 | T | |
| D8 | PT14B | 0 | C | |
| C8 | PT14A | 0 | T | TDQS14 |
| A9 | PT13B | 0 | C | |
| GND | GND0 | 0 | | |
| A8 | PT13A | 0 | T | |
| B8 | PT12B | 0 | C | |
| B7 | PT12A | 0 | T | |
| D7 | PT11B | 0 | C | |
| C7 | PT11A | 0 | T | |
| A7 | PT10B | 0 | C | |
| A6 | PT10A | 0 | T | |
| E7 | PT9B | 0 | C | |

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| GND | GND0 | 0 | | |
| E6 | PT9A | 0 | T | |
| D6 | PT8B | 0 | C | |
| C6 | PT8A | 0 | T | |
| B6 | PT7B | 0 | C | |
| B5 | PT7A | 0 | T | |
| A5 | PT6B | 0 | C | |
| A4 | PT6A | 0 | T | TDQS6 |
| A3 | PT5B | 0 | C | |
| A2 | PT5A | 0 | T | |
| B2 | PT4B | 0 | C | |
| B3 | PT4A | 0 | T | |
| D5 | PT3B | 0 | C | |
| C5 | PT3A | 0 | T | |
| C4 | PT2B | 0 | C | |
| B4 | PT2A | 0 | T | |
| GND | GND0 | 0 | | |
| A1 | GND | - | | |
| A16 | GND | - | | |
| G10 | GND | - | | |
| G7 | GND | - | | |
| G8 | GND | - | | |
| G9 | GND | - | | |
| H10 | GND | - | | |
| H7 | GND | - | | |
| H8 | GND | - | | |
| H9 | GND | - | | |
| J10 | GND | - | | |
| J7 | GND | - | | |
| J8 | GND | - | | |
| J9 | GND | - | | |
| K10 | GND | - | | |
| K7 | GND | - | | |
| K8 | GND | - | | |
| K9 | GND | - | | |
| T1 | GND | - | | |
| T16 | GND | - | | |
| E12 | VCC | - | | |
| E5 | VCC | - | | |
| E8 | VCC | - | | |
| M12 | VCC | - | | |
| M5 | VCC | - | | |
| M9 | VCC | - | | |
| B15 | VCCAUX | - | | |

LFCEP6/LFEC6 Logic Signal Connections: 256 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| R2 | VCCAUX | - | | |
| F7 | VCCIO0 | 0 | | |
| F8 | VCCIO0 | 0 | | |
| F10 | VCCIO1 | 1 | | |
| F9 | VCCIO1 | 1 | | |
| G11 | VCCIO2 | 2 | | |
| H11 | VCCIO2 | 2 | | |
| J11 | VCCIO3 | 3 | | |
| K11 | VCCIO3 | 3 | | |
| L10 | VCCIO4 | 4 | | |
| L9 | VCCIO4 | 4 | | |
| L7 | VCCIO5 | 5 | | |
| L8 | VCCIO5 | 5 | | |
| J6 | VCCIO6 | 6 | | |
| K6 | VCCIO6 | 6 | | |
| G6 | VCCIO7 | 7 | | |
| H6 | VCCIO7 | 7 | | |
| F6 | VCC | - | | |
| F11 | VCC | - | | |
| L11 | VCC | - | | |
| L6 | VCC | - | | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|----------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| D4 | PL2A | 7 | T | VREF2_7 | D4 | PL2A | 7 | T | VREF2_7 |
| E4 | PL2B | 7 | C | VREF1_7 | E4 | PL2B | 7 | C | VREF1_7 |
| C3 | NC | - | | | C3 | PL3A | 7 | T | |
| B2 | NC | - | | | B2 | PL3B | 7 | C | |
| E5 | NC | - | | | E5 | PL4A | 7 | T | |
| F5 | NC | - | | | F5 | PL4B | 7 | C | |
| D3 | NC | - | | | D3 | PL5A | 7 | T | |
| C2 | NC | - | | | C2 | PL5B | 7 | C | |
| F4 | NC | - | | | F4 | PL6A | 7 | T | LDQS6 |
| G4 | NC | - | | | G4 | PL6B | 7 | C | |
| E3 | NC | - | | | E3 | PL7A | 7 | T | |
| D2 | NC | - | | | D2 | PL7B | 7 | C | |
| B1 | NC | - | | | B1 | PL8A | 7 | T | LUM0_PLLT_IN_A |
| C1 | NC | - | | | C1 | PL8B | 7 | C | LUM0_PLLC_IN_A |
| F3 | NC | - | | | F3 | PL9A | 7 | T | LUM0_PLLT_FB_A |
| - | - | - | | | GND | GND7 | 7 | | |
| E2 | NC | - | | | E2 | PL9B | 7 | C | LUM0_PLLC_FB_A |
| G5 | NC | - | | | G5 | PL11A | 7 | T | |
| H6 | NC | - | | | H6 | PL11B | 7 | C | |
| G3 | NC | - | | | G3 | PL12A | 7 | T | |
| H4 | NC | - | | | H4 | PL12B | 7 | C | |
| J5 | NC | - | | | J5 | PL13A | 7 | T | |
| H5 | NC | - | | | H5 | PL13B | 7 | C | |
| F2 | NC | - | | | F2 | PL14A | 7 | T | |
| - | - | - | | | GND | GND7 | 7 | | |
| F1 | NC | - | | | F1 | PL14B | 7 | C | |
| E1 | NC | - | | | E1 | PL15A | 7 | T | |
| D1 | NC | - | | | D1 | PL15B | 7 | C | |
| H3 | PL3A | 7 | T | | H3 | PL16A | 7 | T | |
| G2 | PL3B | 7 | C | | G2 | PL16B | 7 | C | |
| H2 | PL4A | 7 | T | | H2 | PL17A | 7 | T | |
| G1 | PL4B | 7 | C | | G1 | PL17B | 7 | C | |
| J4 | PL5A | 7 | T | | J4 | PL18A | 7 | T | |
| - | - | - | | | GND | GND7 | 7 | | |
| J3 | PL5B | 7 | C | | J3 | PL18B | 7 | C | |
| J2 | PL6A | 7 | T | LDQS6 | J2 | PL19A | 7 | T | LDQS19 |
| H1 | PL6B | 7 | C | | H1 | PL19B | 7 | C | |
| K4 | PL7A | 7 | T | | K4 | PL20A | 7 | T | |
| K5 | PL7B | 7 | C | | K5 | PL20B | 7 | C | |
| K3 | PL8A | 7 | T | | K3 | PL21A | 7 | T | |
| K2 | PL8B | 7 | C | | K2 | PL21B | 7 | C | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| J1 | PL9A | 7 | T | PCLKT7_0 | J1 | PL22A | 7 | T | PCLKT7_0 |
| GND | GND7 | 7 | | | GND | GND7 | 7 | | |
| K1 | PL9B | 7 | C | PCLKC7_0 | K1 | PL22B | 7 | C | PCLKC7_0 |
| L3 | XRES | 6 | | | L3 | XRES | 6 | | |
| L4 | PL11A | 6 | T | | L4 | PL24A | 6 | T | |
| L5 | PL11B | 6 | C | | L5 | PL24B | 6 | C | |
| L2 | PL12A | 6 | T | | L2 | PL25A | 6 | T | |
| L1 | PL12B | 6 | C | | L1 | PL25B | 6 | C | |
| M4 | PL13A | 6 | T | | M4 | PL26A | 6 | T | |
| M5 | PL13B | 6 | C | | M5 | PL26B | 6 | C | |
| M1 | PL14A | 6 | T | | M1 | PL27A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| M2 | PL14B | 6 | C | | M2 | PL27B | 6 | C | |
| N3 | PL15A | 6 | T | LDQS15 | N3 | PL28A | 6 | T | LDQS28 |
| M3 | PL15B | 6 | C | | M3 | PL28B | 6 | C | |
| N5 | PL16A | 6 | T | | N5 | PL29A | 6 | T | |
| N4 | PL16B | 6 | C | | N4 | PL29B | 6 | C | |
| N1 | PL17A | 6 | T | | N1 | PL30A | 6 | T | |
| N2 | PL17B | 6 | C | | N2 | PL30B | 6 | C | |
| P1 | PL18A | 6 | T | | P1 | PL31A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| P2 | PL18B | 6 | C | | P2 | PL31B | 6 | C | |
| R6 | NC | - | | | R6 | PL32A | 6 | T | |
| P5 | NC | - | | | P5 | PL32B | 6 | C | |
| P3 | NC | - | | | P3 | PL33A | 6 | T | |
| P4 | NC | - | | | P4 | PL33B | 6 | C | |
| R1 | NC | - | | | R1 | PL34A | 6 | T | |
| R2 | NC | - | | | R2 | PL34B | 6 | C | |
| R5 | NC | - | | | R5 | PL35A | 6 | T | |
| - | - | - | | | GND | GND6 | 6 | | |
| R4 | NC | - | | | R4 | PL35B | 6 | C | |
| T1 | NC | - | | | T1 | PL36A | 6 | T | LDQS36 |
| T2 | NC | - | | | T2 | PL36B | 6 | C | |
| R3 | NC | - | | | R3 | PL37A | 6 | T | |
| T3 | NC | - | | | T3 | PL37B | 6 | C | |
| | | | | | | PL38A | 6 | T | |
| | | | | | | PL38B | 6 | C | |
| | | | | | | PL39A | 6 | T | |
| - | - | - | | | GND | GND6 | 6 | | |
| | | | | | | PL39B | 6 | C | |
| T5 | TCK | 6 | | | T5 | TCK | 6 | | |
| U5 | TDI | 6 | | | U5 | TDI | 6 | | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|----------------|----------------|---------------|------|------|----------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| T4 | TMS | 6 | | | T4 | TMS | 6 | | |
| U1 | TDO | 6 | | | U1 | TDO | 6 | | |
| U2 | VCCJ | 6 | | | U2 | VCCJ | 6 | | |
| V1 | PL20A | 6 | T | LLM0_PLLT_IN_A | V1 | PL41A | 6 | T | LLM0_PLLT_IN_A |
| V2 | PL20B | 6 | C | LLM0_PLLC_IN_A | V2 | PL41B | 6 | C | LLM0_PLLC_IN_A |
| U3 | PL21A | 6 | T | LLM0_PLLT_FB_A | U3 | PL42A | 6 | T | LLM0_PLLT_FB_A |
| V3 | PL21B | 6 | C | LLM0_PLLC_FB_A | V3 | PL42B | 6 | C | LLM0_PLLC_FB_A |
| U4 | PL22A | 6 | T | | U4 | PL43A | 6 | T | |
| V5 | PL22B | 6 | C | | V5 | PL43B | 6 | C | |
| W1 | PL23A | 6 | T | | W1 | PL44A | 6 | T | |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| W2 | PL23B | 6 | C | | W2 | PL44B | 6 | C | |
| Y1 | PL24A | 6 | T | LDQS24 | Y1 | PL45A | 6 | T | LDQS45 |
| Y2 | PL24B | 6 | C | | Y2 | PL45B | 6 | C | |
| AA1 | PL25A | 6 | T | | AA1 | PL46A | 6 | T | |
| AA2 | PL25B | 6 | C | | AA2 | PL46B | 6 | C | |
| W4 | PL26A | 6 | T | | W4 | PL47A | 6 | T | |
| V4 | PL26B | 6 | C | | V4 | PL47B | 6 | C | |
| W3 | PL27A | 6 | T | VREF1_6 | W3 | PL48A | 6 | T | VREF1_6 |
| Y3 | PL27B | 6 | C | VREF2_6 | Y3 | PL48B | 6 | C | VREF2_6 |
| GND | GND6 | 6 | | | GND | GND6 | 6 | | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| | | | | | | PB2A | 5 | T | |
| | | | | | | PB2B | 5 | C | |
| | | | | | | PB3A | 5 | T | |
| | | | | | | PB3B | 5 | C | |
| | | | | | | PB4A | 5 | T | |
| | | | | | | PB4B | 5 | C | |
| | | | | | | PB5A | 5 | T | |
| | | | | | | PB5B | 5 | C | |
| | | | | | | PB6A | 5 | T | |
| | | | | | | PB6B | 5 | C | |
| | | | | | | PB7A | 5 | T | |
| | | | | | | PB7B | 5 | C | |
| | | | | | | PB8A | 5 | T | |
| | | | | | | PB8B | 5 | C | |
| | | | | | | PB9A | 5 | T | |
| - | - | - | | | GND | GND5 | 5 | | |
| | | | | | | PB9B | 5 | C | |
| V7 | NC | - | | | V7 | PB10A | 5 | T | |
| T6 | NC | - | | | T6 | PB10B | 5 | C | |
| V8 | NC | - | | | V8 | PB11A | 5 | T | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| U7 | NC | - | | | U7 | PB11B | 5 | C | |
| W5 | NC | - | | | W5 | PB12A | 5 | T | |
| U6 | NC | - | | | U6 | PB12B | 5 | C | |
| AA3 | NC | - | | | AA3 | PB13A | 5 | T | |
| - | - | - | | | GND | GND5 | 5 | | |
| AB3 | NC | - | | | AB3 | PB13B | 5 | C | |
| Y6 | NC | - | | | Y6 | PB14A | 5 | T | BDQS14 |
| V6 | NC | - | | | V6 | PB14B | 5 | C | |
| AA5 | NC | - | | | AA5 | PB15A | 5 | T | |
| W6 | NC | - | | | W6 | PB15B | 5 | C | |
| Y5 | NC | - | | | Y5 | PB16A | 5 | T | |
| Y4 | NC | - | | | Y4 | PB16B | 5 | C | |
| AA4 | NC | - | | | AA4 | PB17A | 5 | T | |
| - | - | - | | | GND | GND5 | 5 | | |
| AB4 | NC | - | | | AB4 | PB17B | 5 | C | |
| Y7 | PB2A | 5 | T | | Y7 | PB18A | 5 | T | |
| W8 | PB2B | 5 | C | | W8 | PB18B | 5 | C | |
| W7 | PB3A | 5 | T | | W7 | PB19A | 5 | T | |
| U8 | PB3B | 5 | C | | U8 | PB19B | 5 | C | |
| W9 | PB4A | 5 | T | | W9 | PB20A | 5 | T | |
| U9 | PB4B | 5 | C | | U9 | PB20B | 5 | C | |
| Y8 | PB5A | 5 | T | | Y8 | PB21A | 5 | T | |
| - | - | - | | | GND | GND5 | 5 | | |
| Y9 | PB5B | 5 | C | | Y9 | PB21B | 5 | C | |
| V9 | PB6A | 5 | T | BDQS6 | V9 | PB22A | 5 | T | BDQS22 |
| T9 | PB6B | 5 | C | | T9 | PB22B | 5 | C | |
| W10 | PB7A | 5 | T | | W10 | PB23A | 5 | T | |
| U10 | PB7B | 5 | C | | U10 | PB23B | 5 | C | |
| V10 | PB8A | 5 | T | | V10 | PB24A | 5 | T | |
| T10 | PB8B | 5 | C | | T10 | PB24B | 5 | C | |
| AA6 | PB9A | 5 | T | | AA6 | PB25A | 5 | T | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AB5 | PB9B | 5 | C | | AB5 | PB25B | 5 | C | |
| AA8 | PB10A | 5 | T | | AA8 | PB26A | 5 | T | |
| AA7 | PB10B | 5 | C | | AA7 | PB26B | 5 | C | |
| AB6 | PB11A | 5 | T | | AB6 | PB27A | 5 | T | |
| AB7 | PB11B | 5 | C | | AB7 | PB27B | 5 | C | |
| Y10 | PB12A | 5 | T | | Y10 | PB28A | 5 | T | |
| W11 | PB12B | 5 | C | | W11 | PB28B | 5 | C | |
| AB8 | PB13A | 5 | T | | AB8 | PB29A | 5 | T | |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AB9 | PB13B | 5 | C | | AB9 | PB29B | 5 | C | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| AA10 | PB14A | 5 | T | BDQS14 | AA10 | PB30A | 5 | T | BDQS30 |
| AA9 | PB14B | 5 | C | | AA9 | PB30B | 5 | C | |
| Y11 | PB15A | 5 | T | | Y11 | PB31A | 5 | T | |
| AA11 | PB15B | 5 | C | | AA11 | PB31B | 5 | C | |
| V11 | PB16A | 5 | T | VREF2_5 | V11 | PB32A | 5 | T | VREF2_5 |
| V12 | PB16B | 5 | C | VREF1_5 | V12 | PB32B | 5 | C | VREF1_5 |
| AB10 | PB17A | 5 | T | PCLKT5_0 | AB10 | PB33A | 5 | T | PCLKT5_0 |
| GND | GND5 | 5 | | | GND | GND5 | 5 | | |
| AB11 | PB17B | 5 | C | PCLKC5_0 | AB11 | PB33B | 5 | C | PCLKC5_0 |
| Y12 | PB18A | 4 | T | WRITEN | Y12 | PB34A | 4 | T | WRITEN |
| U11 | PB18B | 4 | C | CS1N | U11 | PB34B | 4 | C | CS1N |
| W12 | PB19A | 4 | T | VREF1_4 | W12 | PB35A | 4 | T | VREF1_4 |
| U12 | PB19B | 4 | C | CSN | U12 | PB35B | 4 | C | CSN |
| W13 | PB20A | 4 | T | VREF2_4 | W13 | PB36A | 4 | T | VREF2_4 |
| U13 | PB20B | 4 | C | D0/SPID7 | U13 | PB36B | 4 | C | D0/SPID7 |
| AA12 | PB21A | 4 | T | D2/SPID5 | AA12 | PB37A | 4 | T | D2/SPID5 |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AB12 | PB21B | 4 | C | D1/SPID6 | AB12 | PB37B | 4 | C | D1/SPID6 |
| T13 | PB22A | 4 | T | BDQS22 | T13 | PB38A | 4 | T | BDQS38 |
| V13 | PB22B | 4 | C | D3/SPID4 | V13 | PB38B | 4 | C | D3/SPID4 |
| W14 | PB23A | 4 | T | | W14 | PB39A | 4 | T | |
| U14 | PB23B | 4 | C | D4/SPID3 | U14 | PB39B | 4 | C | D4/SPID3 |
| Y13 | PB24A | 4 | T | | Y13 | PB40A | 4 | T | |
| V14 | PB24B | 4 | C | D5/SPID2 | V14 | PB40B | 4 | C | D5/SPID2 |
| AA13 | PB25A | 4 | T | | AA13 | PB41A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AB13 | PB25B | 4 | C | D6/SPID1 | AB13 | PB41B | 4 | C | D6/SPID1 |
| AA14 | PB26A | 4 | T | | AA14 | PB42A | 4 | T | |
| Y14 | PB26B | 4 | C | | Y14 | PB42B | 4 | C | |
| Y15 | PB27A | 4 | T | | Y15 | PB43A | 4 | T | |
| W15 | PB27B | 4 | C | | W15 | PB43B | 4 | C | |
| V15 | PB28A | 4 | T | | V15 | PB44A | 4 | T | |
| T14 | PB28B | 4 | C | | T14 | PB44B | 4 | C | |
| AB14 | PB29A | 4 | T | | AB14 | PB45A | 4 | T | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| AB15 | PB29B | 4 | C | | AB15 | PB45B | 4 | C | |
| AB16 | PB30A | 4 | T | BDQS30 | AB16 | PB46A | 4 | T | BDQS46 |
| AA15 | PB30B | 4 | C | | AA15 | PB46B | 4 | C | |
| AB17 | PB31A | 4 | T | | AB17 | PB47A | 4 | T | |
| AA16 | PB31B | 4 | C | | AA16 | PB47B | 4 | C | |
| AB18 | PB32A | 4 | T | | AB18 | PB48A | 4 | T | |
| AA17 | PB32B | 4 | C | | AA17 | PB48B | 4 | C | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|----------------|----------------|---------------|------|------|----------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| AB19 | PB33A | 4 | T | | AB19 | PB49A | 4 | T | |
| - | - | - | | | GND | GND4 | 4 | | |
| AA18 | PB33B | 4 | C | | AA18 | PB49B | 4 | C | |
| W16 | NC | - | | | W16 | PB50A | 4 | T | |
| U15 | NC | - | | | U15 | PB50B | 4 | C | |
| V16 | NC | - | | | V16 | PB51A | 4 | T | |
| U16 | NC | - | | | U16 | PB51B | 4 | C | |
| Y17 | NC | - | | | Y17 | PB52A | 4 | T | |
| V17 | NC | - | | | V17 | PB52B | 4 | C | |
| AB20 | NC | - | | | AB20 | PB53A | 4 | T | |
| - | - | - | | | GND | GND4 | 4 | | |
| AA19 | NC | - | | | AA19 | PB53B | 4 | C | |
| Y16 | NC | - | | | Y16 | PB54A | 4 | T | BDQS54 |
| W17 | NC | - | | | W17 | PB54B | 4 | C | |
| AA20 | NC | - | | | AA20 | PB55A | 4 | T | |
| Y19 | NC | - | | | Y19 | PB55B | 4 | C | |
| Y18 | NC | - | | | Y18 | PB56A | 4 | T | |
| W18 | NC | - | | | W18 | PB56B | 4 | C | |
| T17 | NC | - | | | T17 | PB57A | 4 | T | |
| U17 | NC | - | | | U17 | PB57B | 4 | C | |
| GND | GND4 | 4 | | | GND | GND4 | 4 | | |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| W20 | PR27B | 3 | C | VREF2_3 | W20 | PR48B | 3 | C | VREF2_3 |
| Y20 | PR27A | 3 | T | VREF1_3 | Y20 | PR48A | 3 | T | VREF1_3 |
| AA21 | PR26B | 3 | C | | AA21 | PR47B | 3 | C | |
| AB21 | PR26A | 3 | T | | AB21 | PR47A | 3 | T | |
| W19 | PR25B | 3 | C | | W19 | PR46B | 3 | C | |
| V19 | PR25A | 3 | T | | V19 | PR46A | 3 | T | |
| Y21 | PR24B | 3 | C | | Y21 | PR45B | 3 | C | |
| AA22 | PR24A | 3 | T | RDQS24 | AA22 | PR45A | 3 | T | RDQS45 |
| V20 | PR23B | 3 | C | RLM0_PLLC_FB_A | V20 | PR44B | 3 | C | RLM0_PLLC_IN_A |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| U20 | PR23A | 3 | T | RLM0_PLLT_FB_A | U20 | PR44A | 3 | T | RLM0_PLLT_IN_A |
| W21 | PR22B | 3 | C | RLM0_PLLC_IN_A | W21 | PR43B | 3 | C | RLM0_PLLC_FB_A |
| Y22 | PR22A | 3 | T | RLM0_PLLT_IN_A | Y22 | PR43A | 3 | T | RLM0_PLLT_FB_A |
| V21 | PR21B | 3 | C | DI/CSSPIN | V21 | PR42B | 3 | C | DI/CSSPIN |
| W22 | PR21A | 3 | T | DOUT/CSON | W22 | PR42A | 3 | T | DOUT/CSON |
| U21 | PR20B | 3 | C | BUSY/SISPI | U21 | PR41B | 3 | C | BUSY/SISPI |
| V22 | PR20A | 3 | T | D7/SPID0 | V22 | PR41A | 3 | T | D7/SPID0 |
| T19 | CFG2 | 3 | | | T19 | CFG2 | 3 | | |
| U19 | CFG1 | 3 | | | U19 | CFG1 | 3 | | |
| U18 | CFG0 | 3 | | | U18 | CFG0 | 3 | | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| V18 | PROGRAMN | 3 | | | V18 | PROGRAMN | 3 | | |
| T20 | CCLK | 3 | | | T20 | CCLK | 3 | | |
| T21 | INITN | 3 | | | T21 | INITN | 3 | | |
| R20 | DONE | 3 | | | R20 | DONE | 3 | | |
| | | | | | | PR39B | 3 | C | |
| - | - | - | | | GND | GND3 | 3 | | |
| | | | | | | PR39A | 3 | T | |
| | | | | | | PR38B | 3 | C | |
| | | | | | | PR38A | 3 | T | |
| T18 | NC | - | | | T18 | PR37B | 3 | C | |
| R17 | NC | - | | | R17 | PR37A | 3 | T | |
| R19 | NC | - | | | R19 | PR36B | 3 | C | |
| R18 | NC | - | | | R18 | PR36A | 3 | T | RDQS36 |
| U22 | NC | - | | | U22 | PR35B | 3 | C | |
| - | - | - | | | GND | GND3 | 3 | | |
| T22 | NC | - | | | T22 | PR35A | 3 | T | |
| R21 | NC | - | | | R21 | PR34B | 3 | C | |
| R22 | NC | - | | | R22 | PR34A | 3 | T | |
| P20 | NC | - | | | P20 | PR33B | 3 | C | |
| N20 | NC | - | | | N20 | PR33A | 3 | T | |
| P19 | NC | - | | | P19 | PR32B | 3 | C | |
| P18 | NC | - | | | P18 | PR32A | 3 | T | |
| P21 | PR18B | 3 | C | | P21 | PR31B | 3 | C | |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| P22 | PR18A | 3 | T | | P22 | PR31A | 3 | T | |
| N21 | PR17B | 3 | C | | N21 | PR30B | 3 | C | |
| N22 | PR17A | 3 | T | | N22 | PR30A | 3 | T | |
| N19 | PR16B | 3 | C | | N19 | PR29B | 3 | C | |
| N18 | PR16A | 3 | T | | N18 | PR29A | 3 | T | |
| M21 | PR15B | 3 | C | | M21 | PR28B | 3 | C | |
| L20 | PR15A | 3 | T | RDQS15 | L20 | PR28A | 3 | T | RDQS28 |
| L21 | PR14B | 3 | C | | L21 | PR27B | 3 | C | |
| GND | GND3 | 3 | | | GND | GND3 | 3 | | |
| M20 | PR14A | 3 | T | | M20 | PR27A | 3 | T | |
| M18 | PR13B | 3 | C | | M18 | PR26B | 3 | C | |
| M19 | PR13A | 3 | T | | M19 | PR26A | 3 | T | |
| M22 | PR12B | 3 | C | | M22 | PR25B | 3 | C | |
| L22 | PR12A | 3 | T | | L22 | PR25A | 3 | T | |
| K22 | PR11B | 3 | C | | K22 | PR24B | 3 | C | |
| K21 | PR11A | 3 | T | | K21 | PR24A | 3 | T | |
| J22 | PR9B | 2 | C | PCLKC2_0 | J22 | PR22B | 2 | C | PCLKC2_0 |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|----------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| J21 | PR9A | 2 | T | PCLKT2_0 | J21 | PR22A | 2 | T | PCLKT2_0 |
| H22 | PR8B | 2 | C | | H22 | PR21B | 2 | C | |
| H21 | PR8A | 2 | T | | H21 | PR21A | 2 | T | |
| L19 | PR7B | 2 | C | | L19 | PR20B | 2 | C | |
| L18 | PR7A | 2 | T | | L18 | PR20A | 2 | T | |
| K20 | PR6B | 2 | C | | K20 | PR19B | 2 | C | |
| J20 | PR6A | 2 | T | RDQS6 | J20 | PR19A | 2 | T | RDQS19 |
| K19 | PR5B | 2 | C | | K19 | PR18B | 2 | C | |
| - | - | - | | | GND | GND2 | 2 | | |
| K18 | PR5A | 2 | T | | K18 | PR18A | 2 | T | |
| G22 | PR4B | 2 | C | | G22 | PR17B | 2 | C | |
| F22 | PR4A | 2 | T | | F22 | PR17A | 2 | T | |
| F21 | PR3B | 2 | C | | F21 | PR16B | 2 | C | |
| E22 | PR3A | 2 | T | | E22 | PR16A | 2 | T | |
| E21 | NC | - | | | E21 | PR15B | 2 | C | |
| D22 | NC | - | | | D22 | PR15A | 2 | T | |
| G21 | NC | - | | | G21 | PR14B | 2 | C | |
| G20 | NC | - | | | G20 | PR14A | 2 | T | |
| - | - | - | | | GND | GND2 | 2 | | |
| J18 | NC | - | | | J18 | PR13B | 2 | C | |
| H19 | NC | - | | | H19 | PR13A | 2 | T | |
| J19 | NC | - | | | J19 | PR12B | 2 | C | |
| H20 | NC | - | | | H20 | PR12A | 2 | T | |
| H17 | NC | - | | | H17 | PR11B | 2 | C | |
| H18 | NC | - | | | H18 | PR11A | 2 | T | |
| D21 | NC | - | | | D21 | PR9B | 2 | C | RUM0_PLLC_FB_A |
| - | - | - | | | GND | GND2 | 2 | | |
| C22 | NC | - | | | C22 | PR9A | 2 | T | RUM0_PLLT_FB_A |
| G19 | NC | - | | | G19 | PR8B | 2 | C | RUM0_PLLC_IN_A |
| G18 | NC | - | | | G18 | PR8A | 2 | T | RUM0_PLLT_IN_A |
| F20 | NC | - | | | F20 | PR7B | 2 | C | |
| F19 | NC | - | | | F19 | PR7A | 2 | T | |
| E20 | NC | - | | | E20 | PR6B | 2 | C | |
| D20 | NC | - | | | D20 | PR6A | 2 | T | RDQS6 |
| C21 | NC | - | | | C21 | PR5B | 2 | C | |
| C20 | NC | - | | | C20 | PR5A | 2 | T | |
| F18 | NC | - | | | F18 | PR4B | 2 | C | |
| E18 | NC | - | | | E18 | PR4A | 2 | T | |
| B22 | NC | - | | | B22 | PR3B | 2 | C | |
| B21 | NC | - | | | B21 | PR3A | 2 | T | |
| E19 | PR2B | 2 | C | VREF1_2 | E19 | PR2B | 2 | C | VREF1_2 |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| D19 | PR2A | 2 | T | VREF2_2 | D19 | PR2A | 2 | T | VREF2_2 |
| GND | GND2 | 2 | | | GND | GND2 | 2 | | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| G17 | NC | - | | | G17 | PT57B | 1 | C | |
| F17 | NC | - | | | F17 | PT57A | 1 | T | |
| D18 | NC | - | | | D18 | PT56B | 1 | C | |
| C18 | NC | - | | | C18 | PT56A | 1 | T | |
| C19 | NC | - | | | C19 | PT55B | 1 | C | |
| B20 | NC | - | | | B20 | PT55A | 1 | T | |
| D17 | NC | - | | | D17 | PT54B | 1 | C | |
| C16 | NC | - | | | C16 | PT54A | 1 | T | TDQS54 |
| B19 | NC | - | | | B19 | PT53B | 1 | C | |
| - | - | - | | | GND | GND1 | 1 | | |
| A20 | NC | - | | | A20 | PT53A | 1 | T | |
| E17 | NC | - | | | E17 | PT52B | 1 | C | |
| C17 | NC | - | | | C17 | PT52A | 1 | T | |
| F16 | NC | - | | | F16 | PT51B | 1 | C | |
| E16 | NC | - | | | E16 | PT51A | 1 | T | |
| F15 | NC | - | | | F15 | PT50B | 1 | C | |
| D16 | NC | - | | | D16 | PT50A | 1 | T | |
| B18 | PT33B | 1 | C | | B18 | PT49B | 1 | C | |
| - | - | - | | | GND | GND1 | 1 | | |
| A19 | PT33A | 1 | T | | A19 | PT49A | 1 | T | |
| B17 | PT32B | 1 | C | | B17 | PT48B | 1 | C | |
| A18 | PT32A | 1 | T | | A18 | PT48A | 1 | T | |
| B16 | PT31B | 1 | C | | B16 | PT47B | 1 | C | |
| A17 | PT31A | 1 | T | | A17 | PT47A | 1 | T | |
| B15 | PT30B | 1 | C | | B15 | PT46B | 1 | C | |
| A16 | PT30A | 1 | T | TDQS30 | A16 | PT46A | 1 | T | TDQS46 |
| A15 | PT29B | 1 | C | | A15 | PT45B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| A14 | PT29A | 1 | T | | A14 | PT45A | 1 | T | |
| G14 | PT28B | 1 | C | | G14 | PT44B | 1 | C | |
| E15 | PT28A | 1 | T | | E15 | PT44A | 1 | T | |
| D15 | PT27B | 1 | C | | D15 | PT43B | 1 | C | |
| C15 | PT27A | 1 | T | | C15 | PT43A | 1 | T | |
| C14 | PT26B | 1 | C | | C14 | PT42B | 1 | C | |
| B14 | PT26A | 1 | T | | B14 | PT42A | 1 | T | |
| A13 | PT25B | 1 | C | | A13 | PT41B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B13 | PT25A | 1 | T | | B13 | PT41A | 1 | T | |
| E14 | PT24B | 1 | C | | E14 | PT40B | 1 | C | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| C13 | PT24A | 1 | T | | C13 | PT40A | 1 | T | |
| F14 | PT23B | 1 | C | | F14 | PT39B | 1 | C | |
| D14 | PT23A | 1 | T | | D14 | PT39A | 1 | T | |
| E13 | PT22B | 1 | C | | E13 | PT38B | 1 | C | |
| G13 | PT22A | 1 | T | TDQS22 | G13 | PT38A | 1 | T | TDQS38 |
| A12 | PT21B | 1 | C | | A12 | PT37B | 1 | C | |
| GND | GND1 | 1 | | | GND | GND1 | 1 | | |
| B12 | PT21A | 1 | T | | B12 | PT37A | 1 | T | |
| F13 | PT20B | 1 | C | | F13 | PT36B | 1 | C | |
| D13 | PT20A | 1 | T | | D13 | PT36A | 1 | T | |
| F12 | PT19B | 1 | C | VREF2_1 | F12 | PT35B | 1 | C | VREF2_1 |
| D12 | PT19A | 1 | T | VREF1_1 | D12 | PT35A | 1 | T | VREF1_1 |
| F11 | PT18B | 1 | C | | F11 | PT34B | 1 | C | |
| C12 | PT18A | 1 | T | | C12 | PT34A | 1 | T | |
| A11 | PT17B | 0 | C | PCLKC0_0 | A11 | PT33B | 0 | C | PCLKC0_0 |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A10 | PT17A | 0 | T | PCLKT0_0 | A10 | PT33A | 0 | T | PCLKT0_0 |
| E12 | PT16B | 0 | C | VREF1_0 | E12 | PT32B | 0 | C | VREF1_0 |
| E11 | PT16A | 0 | T | VREF2_0 | E11 | PT32A | 0 | T | VREF2_0 |
| B11 | PT15B | 0 | C | | B11 | PT31B | 0 | C | |
| C11 | PT15A | 0 | T | | C11 | PT31A | 0 | T | |
| B9 | PT14B | 0 | C | | B9 | PT30B | 0 | C | |
| B10 | PT14A | 0 | T | TDQS14 | B10 | PT30A | 0 | T | TDQS30 |
| A9 | PT13B | 0 | C | | A9 | PT29B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A8 | PT13A | 0 | T | | A8 | PT29A | 0 | T | |
| D11 | PT12B | 0 | C | | D11 | PT28B | 0 | C | |
| C10 | PT12A | 0 | T | | C10 | PT28A | 0 | T | |
| A7 | PT11B | 0 | C | | A7 | PT27B | 0 | C | |
| A6 | PT11A | 0 | T | | A6 | PT27A | 0 | T | |
| B7 | PT10B | 0 | C | | B7 | PT26B | 0 | C | |
| B8 | PT10A | 0 | T | | B8 | PT26A | 0 | T | |
| A5 | PT9B | 0 | C | | A5 | PT25B | 0 | C | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| B6 | PT9A | 0 | T | | B6 | PT25A | 0 | T | |
| G10 | PT8B | 0 | C | | G10 | PT24B | 0 | C | |
| E10 | PT8A | 0 | T | | E10 | PT24A | 0 | T | |
| F10 | PT7B | 0 | C | | F10 | PT23B | 0 | C | |
| D10 | PT7A | 0 | T | | D10 | PT23A | 0 | T | |
| G9 | PT6B | 0 | C | | G9 | PT22B | 0 | C | |
| E9 | PT6A | 0 | T | TDQS6 | E9 | PT22A | 0 | T | TDQS22 |
| C9 | PT5B | 0 | C | | C9 | PT21B | 0 | C | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| - | - | - | | | GND | GND0 | 0 | | |
| C8 | PT5A | 0 | T | | C8 | PT21A | 0 | T | |
| F9 | PT4B | 0 | C | | F9 | PT20B | 0 | C | |
| D9 | PT4A | 0 | T | | D9 | PT20A | 0 | T | |
| F8 | PT3B | 0 | C | | F8 | PT19B | 0 | C | |
| D7 | PT3A | 0 | T | | D7 | PT19A | 0 | T | |
| D8 | PT2B | 0 | C | | D8 | PT18B | 0 | C | |
| C7 | PT2A | 0 | T | | C7 | PT18A | 0 | T | |
| GND | GND0 | 0 | | | GND | GND0 | 0 | | |
| A4 | NC | - | | | A4 | PT17B | 0 | C | |
| B4 | NC | - | | | B4 | PT17A | 0 | T | |
| C4 | NC | - | | | C4 | PT16B | 0 | C | |
| C5 | NC | - | | | C5 | PT16A | 0 | T | |
| D6 | NC | - | | | D6 | PT15B | 0 | C | |
| B5 | NC | - | | | B5 | PT15A | 0 | T | |
| E6 | NC | - | | | E6 | PT14B | 0 | C | |
| C6 | NC | - | | | C6 | PT14A | 0 | T | TDQS14 |
| A3 | NC | - | | | A3 | PT13B | 0 | C | |
| - | - | - | | | GND | GND0 | 0 | | |
| B3 | NC | - | | | B3 | PT13A | 0 | T | |
| F6 | NC | - | | | F6 | PT12B | 0 | C | |
| D5 | NC | - | | | D5 | PT12A | 0 | T | |
| F7 | NC | - | | | F7 | PT11B | 0 | C | |
| E8 | NC | - | | | E8 | PT11A | 0 | T | |
| G6 | NC | - | | | G6 | PT10B | 0 | C | |
| E7 | NC | - | | | E7 | PT10A | 0 | T | |
| | | | | | | PR9B | C | | |
| - | - | - | | | GND | GND0 | 0 | | |
| | | | | | | PT9A | 0 | T | |
| | | | | | | PR8B | 0 | C | |
| | | | | | | PT8A | 0 | T | |
| | | | | | | PT7B | 0 | C | |
| | | | | | | PT7A | 0 | T | |
| | | | | | | PT6A | 0 | C | |
| | | | | | | PT6A | 0 | T | |
| | | | | | | PT5B | 0 | C | |
| | | | | | | PT5A | 0 | T | |
| | | | | | | PT4B | 0 | C | |
| | | | | | | PT4A | 0 | T | |
| | | | | | | PT3B | 0 | C | |
| | | | | | | PT3A | 0 | T | |
| | | | | | | PT2B | 0 | C | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| | | | | | | PT2A | 0 | T | |
| - | - | - | | | GND | GND0 | | | |
| A1 | GND | - | | | A1 | GND | - | | |
| A22 | GND | - | | | A22 | GND | - | | |
| AB1 | GND | - | | | AB1 | GND | - | | |
| AB22 | GND | - | | | AB22 | GND | - | | |
| H15 | GND | - | | | H15 | GND | - | | |
| H8 | GND | - | | | H8 | GND | - | | |
| J10 | GND | - | | | J10 | GND | - | | |
| J11 | GND | - | | | J11 | GND | - | | |
| J12 | GND | - | | | J12 | GND | - | | |
| J13 | GND | - | | | J13 | GND | - | | |
| J14 | GND | - | | | J14 | GND | - | | |
| J9 | GND | - | | | J9 | GND | - | | |
| K10 | GND | - | | | K10 | GND | - | | |
| K11 | GND | - | | | K11 | GND | - | | |
| K12 | GND | - | | | K12 | GND | - | | |
| K13 | GND | - | | | K13 | GND | - | | |
| K14 | GND | - | | | K14 | GND | - | | |
| K9 | GND | - | | | K9 | GND | - | | |
| L10 | GND | - | | | L10 | GND | - | | |
| L11 | GND | - | | | L11 | GND | - | | |
| L12 | GND | - | | | L12 | GND | - | | |
| L13 | GND | - | | | L13 | GND | - | | |
| L14 | GND | - | | | L14 | GND | - | | |
| L9 | GND | - | | | L9 | GND | - | | |
| M10 | GND | - | | | M10 | GND | - | | |
| M11 | GND | - | | | M11 | GND | - | | |
| M12 | GND | - | | | M12 | GND | - | | |
| M13 | GND | - | | | M13 | GND | - | | |
| M14 | GND | - | | | M14 | GND | - | | |
| M9 | GND | - | | | M9 | GND | - | | |
| N10 | GND | - | | | N10 | GND | - | | |
| N11 | GND | - | | | N11 | GND | - | | |
| N12 | GND | - | | | N12 | GND | - | | |
| N13 | GND | - | | | N13 | GND | - | | |
| N14 | GND | - | | | N14 | GND | - | | |
| N9 | GND | - | | | N9 | GND | - | | |
| P10 | GND | - | | | P10 | GND | - | | |
| P11 | GND | - | | | P11 | GND | - | | |
| P12 | GND | - | | | P12 | GND | - | | |
| P13 | GND | - | | | P13 | GND | - | | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| P14 | GND | - | | | P14 | GND | - | | |
| P9 | GND | - | | | P9 | GND | - | | |
| R15 | GND | - | | | R15 | GND | - | | |
| R8 | GND | - | | | R8 | GND | - | | |
| J16 | VCC | - | | | J16 | VCC | - | | |
| J7 | VCC | - | | | J7 | VCC | - | | |
| K16 | VCC | - | | | K16 | VCC | - | | |
| K17 | VCC | - | | | K17 | VCC | - | | |
| K6 | VCC | - | | | K6 | VCC | - | | |
| K7 | VCC | - | | | K7 | VCC | - | | |
| L17 | VCC | - | | | L17 | VCC | - | | |
| L6 | VCC | - | | | L6 | VCC | - | | |
| M17 | VCC | - | | | M17 | VCC | - | | |
| M6 | VCC | - | | | M6 | VCC | - | | |
| N16 | VCC | - | | | N16 | VCC | - | | |
| N17 | VCC | - | | | N17 | VCC | - | | |
| N6 | VCC | - | | | N6 | VCC | - | | |
| N7 | VCC | - | | | N7 | VCC | - | | |
| P16 | VCC | - | | | P16 | VCC | - | | |
| P7 | VCC | - | | | P7 | VCC | - | | |
| G11 | VCCIO0 | 0 | | | G11 | VCCIO0 | 0 | | |
| H10 | VCCIO0 | 0 | | | H10 | VCCIO0 | 0 | | |
| H11 | VCCIO0 | 0 | | | H11 | VCCIO0 | 0 | | |
| H9 | VCCIO0 | 0 | | | H9 | VCCIO0 | 0 | | |
| G12 | VCCIO1 | 1 | | | G12 | VCCIO1 | 1 | | |
| H12 | VCCIO1 | 1 | | | H12 | VCCIO1 | 1 | | |
| H13 | VCCIO1 | 1 | | | H13 | VCCIO1 | 1 | | |
| H14 | VCCIO1 | 1 | | | H14 | VCCIO1 | 1 | | |
| J15 | VCCIO2 | 2 | | | J15 | VCCIO2 | 2 | | |
| K15 | VCCIO2 | 2 | | | K15 | VCCIO2 | 2 | | |
| L15 | VCCIO2 | 2 | | | L15 | VCCIO2 | 2 | | |
| L16 | VCCIO2 | 2 | | | L16 | VCCIO2 | 2 | | |
| M15 | VCCIO3 | 3 | | | M15 | VCCIO3 | 3 | | |
| M16 | VCCIO3 | 3 | | | M16 | VCCIO3 | 3 | | |
| N15 | VCCIO3 | 3 | | | N15 | VCCIO3 | 3 | | |
| P15 | VCCIO3 | 3 | | | P15 | VCCIO3 | 3 | | |
| R12 | VCCIO4 | 4 | | | R12 | VCCIO4 | 4 | | |
| R13 | VCCIO4 | 4 | | | R13 | VCCIO4 | 4 | | |
| R14 | VCCIO4 | 4 | | | R14 | VCCIO4 | 4 | | |
| T12 | VCCIO4 | 4 | | | T12 | VCCIO4 | 4 | | |
| R10 | VCCIO5 | 5 | | | R10 | VCCIO5 | 5 | | |
| R11 | VCCIO5 | 5 | | | R11 | VCCIO5 | 5 | | |

LFCEP6/LFEC6, LFCEP20/LFEC20 Logic Signal Connections: 484 fpBGA

| LFCEP6/LFEC6 | | | | | LFCEP20/LFEC20 | | | | |
|--------------|---------------|------|------|---------------|----------------|---------------|------|------|---------------|
| Ball Number | Ball Function | Bank | LVDS | Dual Function | Ball Number | Ball Function | Bank | LVDS | Dual Function |
| R9 | VCCIO5 | 5 | | | R9 | VCCIO5 | 5 | | |
| T11 | VCCIO5 | 5 | | | T11 | VCCIO5 | 5 | | |
| M7 | VCCIO6 | 6 | | | M7 | VCCIO6 | 6 | | |
| M8 | VCCIO6 | 6 | | | M8 | VCCIO6 | 6 | | |
| N8 | VCCIO6 | 6 | | | N8 | VCCIO6 | 6 | | |
| P8 | VCCIO6 | 6 | | | P8 | VCCIO6 | 6 | | |
| J8 | VCCIO7 | 7 | | | J8 | VCCIO7 | 7 | | |
| K8 | VCCIO7 | 7 | | | K8 | VCCIO7 | 7 | | |
| L7 | VCCIO7 | 7 | | | L7 | VCCIO7 | 7 | | |
| L8 | VCCIO7 | 7 | | | L8 | VCCIO7 | 7 | | |
| G15 | VCCAUX | - | | | G15 | VCCAUX | - | | |
| G16 | VCCAUX | - | | | G16 | VCCAUX | - | | |
| G7 | VCCAUX | - | | | G7 | VCCAUX | - | | |
| G8 | VCCAUX | - | | | G8 | VCCAUX | - | | |
| H16 | VCCAUX | - | | | H16 | VCCAUX | - | | |
| H7 | VCCAUX | - | | | H7 | VCCAUX | - | | |
| R16 | VCCAUX | - | | | R16 | VCCAUX | - | | |
| R7 | VCCAUX | - | | | R7 | VCCAUX | - | | |
| T15 | VCCAUX | - | | | T15 | VCCAUX | - | | |
| T16 | VCCAUX | - | | | T16 | VCCAUX | - | | |
| T7 | VCCAUX | - | | | T7 | VCCAUX | - | | |
| T8 | VCCAUX | - | | | T8 | VCCAUX | - | | |
| J6 | VCC | - | | | J6 | VCC | - | | |
| J17 | VCC | - | | | J17 | VCC | - | | |
| P6 | VCC | - | | | P6 | VCC | - | | |
| P17 | VCC | - | | | P17 | VCC | - | | |
| A2 | NC | - | | | A2 | NC | - | | |
| AB2 | NC | - | | | AB2 | NC | - | | |
| A21 | NC | - | | | A21 | NC | - | | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| E3 | PL2A | 7 | T | VREF2_7 |
| E4 | PL2B | 7 | C | VREF1_7 |
| B1 | PL3A | 7 | T | |
| C1 | PL3B | 7 | C | |
| F3 | PL4A | 7 | T | |
| G3 | PL4B | 7 | C | |
| D2 | PL5A | 7 | T | |
| E2 | PL5B | 7 | C | |
| D1 | PL6A | 7 | T | LDQS6 |
| E1 | PL6B | 7 | C | |
| F2 | PL7A | 7 | T | |
| G2 | PL7B | 7 | C | |
| F6 | PL8A | 7 | T | LUM0_PLLT_IN_A |
| G6 | PL8B | 7 | C | LUM0_PLLC_IN_A |
| H4 | PL9A | 7 | T | LUM0_PLLT_FB_A |
| GND | GND07 | | | |
| G4 | PL9B | 7 | C | LUM0_PLLC_FB_A |
| J4 | PL11A | 7 | T | |
| J5 | PL11B | 7 | C | |
| K4 | PL12A | 7 | T | |
| K5 | PL12B | 7 | C | |
| J6 | PL13A | 7 | T | |
| K6 | PL13B | 7 | C | |
| F1 | PL14A | 7 | T | |
| GND | GND07 | | | |
| G1 | PL14B | 7 | C | |
| H1 | PL15A | 7 | T | |
| J1 | PL15B | 7 | C | |
| K2 | PL16A | 7 | T | |
| K1 | PL16B | 7 | C | |
| K3 | PL17A | 7 | T | |
| L3 | PL17B | 7 | C | |
| L2 | PL18A | 7 | T | |
| GND | GND07 | | | |
| L1 | PL18B | 7 | C | |
| M3 | PL19A | 7 | T | LDQS19 |
| M4 | PL19B | 7 | C | |
| M1 | PL20A | 7 | T | |
| M2 | PL20B | 7 | C | |
| L4 | PL21A | 7 | T | |
| L5 | PL21B | 7 | C | |
| N2 | PL22A | 7 | T | PCLKT7_0 |
| GND | GND07 | | | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| N1 | PL22B | 7 | C | PCLKC7_0 |
| N3 | XRES | 6 | | |
| P1 | PL24A | 6 | T | |
| P2 | PL24B | 6 | C | |
| L7 | PL25A | 6 | T | |
| L6 | PL25B | 6 | C | |
| N4 | PL26A | 6 | T | |
| N5 | PL26B | 6 | C | |
| R1 | PL27A | 6 | T | |
| GND | GND06 | | | |
| R2 | PL27B | 6 | C | |
| P4 | PL28A | 6 | T | LDQS28 |
| P3 | PL28B | 6 | C | |
| M5 | PL29A | 6 | T | |
| M6 | PL29B | 6 | C | |
| T1 | PL30A | 6 | T | |
| T2 | PL30B | 6 | C | |
| R4 | PL31A | 6 | T | |
| GND | GND06 | | | |
| R3 | PL31B | 6 | C | |
| N6 | PL32A | 6 | T | |
| P5 | PL32B | 6 | C | |
| P6 | PL33A | 6 | T | |
| R5 | PL33B | 6 | C | |
| U1 | PL34A | 6 | T | |
| U2 | PL34B | 6 | C | |
| T3 | PL35A | 6 | T | |
| GND | GND06 | | | |
| T4 | PL35B | 6 | C | |
| R6 | PL36A | 6 | T | LDQS36 |
| T5 | PL36B | 6 | C | |
| T6 | PL37A | 6 | T | |
| U5 | PL37B | 6 | C | |
| U3 | PL38A | 6 | T | |
| U4 | PL38B | 6 | C | |
| V1 | PL39A | 6 | T | |
| GND | GND06 | | | |
| V2 | PL39B | 6 | C | |
| U7 | TCK | 6 | | |
| V4 | TDI | 6 | | |
| V5 | TMS | 6 | | |
| V3 | TDO | 6 | | |
| U6 | VCCJ | 6 | | |
| W1 | PL41A | 6 | T | LLM0_PLLT_IN_A |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| W2 | PL41B | 6 | C | LLM0_PLLC_IN_A |
| V6 | PL42A | 6 | T | LLM0_PLLT_FB_A |
| W6 | PL42B | 6 | C | LLM0_PLLC_FB_A |
| Y1 | PL43A | 6 | T | |
| Y2 | PL43B | 6 | C | |
| W3 | PL44A | 6 | T | |
| GND | GND06 | | | |
| W4 | PL44B | 6 | C | |
| AA1 | PL45A | 6 | T | LDQS45 |
| AB1 | PL45B | 6 | C | |
| Y4 | PL46A | 6 | T | |
| Y3 | PL46B | 6 | C | |
| AC1 | PL47A | 6 | T | |
| AB2 | PL47B | 6 | C | |
| AB4 | PL48A | 6 | T | VREF1_6 |
| AC4 | PL48B | 6 | C | VREF2_6 |
| GND | GND06 | | | |
| GND | GND05 | | | |
| AB6 | PB2A | 5 | T | |
| AA6 | PB2B | 5 | C | |
| AC7 | PB3A | 5 | T | |
| Y8 | PB3B | 5 | C | |
| AB7 | PB4A | 5 | T | |
| AA7 | PB4B | 5 | C | |
| AC6 | PB5A | 5 | T | |
| AC5 | PB5B | 5 | C | |
| AB8 | PB6A | 5 | T | BDQS6 |
| AC8 | PB6B | 5 | C | |
| AE2 | PB7A | 5 | T | |
| AA8 | PB7B | 5 | C | |
| AF2 | PB8A | 5 | T | |
| Y9 | PB8B | 5 | C | |
| AD5 | PB9A | 5 | T | |
| GND | GND05 | | | |
| AD4 | PB9B | 5 | C | |
| AD8 | PB10A | 5 | T | |
| AC9 | PB10B | 5 | C | |
| AE3 | PB11A | 5 | T | |
| AB9 | PB11B | 5 | C | |
| AF3 | PB12A | 5 | T | |
| AD9 | PB12B | 5 | C | |
| AE4 | PB13A | 5 | T | |
| GND | GND05 | | | |
| AF4 | PB13B | 5 | C | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| AE5 | PB14A | 5 | T | BDQS14 |
| AA9 | PB14B | 5 | C | |
| AF5 | PB15A | 5 | T | |
| Y10 | PB15B | 5 | C | |
| AD6 | PB16A | 5 | T | |
| AC10 | PB16B | 5 | C | |
| AF6 | PB17A | 5 | T | |
| GND | GND05 | | | |
| AE6 | PB17B | 5 | C | |
| AF7 | PB18A | 5 | T | |
| AB10 | PB18B | 5 | C | |
| AE7 | PB19A | 5 | T | |
| AD10 | PB19B | 5 | C | |
| AD7 | PB20A | 5 | T | |
| AA10 | PB20B | 5 | C | |
| AF8 | PB21A | 5 | T | |
| GND | GND05 | | | |
| AF9 | PB21B | 5 | C | |
| AD11 | PB22A | 5 | T | BDQS22 |
| Y11 | PB22B | 5 | C | |
| AE8 | PB23A | 5 | T | |
| AC11 | PB23B | 5 | C | |
| AF10 | PB24A | 5 | T | |
| AB11 | PB24B | 5 | C | |
| AE10 | PB25A | 5 | T | |
| GND | GND05 | | | |
| AE9 | PB25B | 5 | C | |
| AA11 | PB26A | 5 | T | |
| Y12 | PB26B | 5 | C | |
| AE11 | PB27A | 5 | T | |
| AF11 | PB27B | 5 | C | |
| AF12 | PB28A | 5 | T | |
| AE12 | PB28B | 5 | C | |
| AD12 | PB29A | 5 | T | |
| GND | GND05 | | | |
| AC12 | PB29B | 5 | C | |
| AA12 | PB30A | 5 | T | BDQS30 |
| AB12 | PB30B | 5 | C | |
| AE13 | PB31A | 5 | T | |
| AF13 | PB31B | 5 | C | |
| AD13 | PB32A | 5 | T | VREF2_5 |
| AC13 | PB32B | 5 | C | VREF1_5 |
| AF14 | PB33A | 5 | T | PCLKT5_0 |
| GND | GND05 | | | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| AE14 | PB33B | 5 | C | PCLKC5_0 |
| AA13 | PB34A | 4 | T | WRITEN |
| AB13 | PB34B | 4 | C | CS1N |
| AD14 | PB35A | 4 | T | VREF1_4 |
| AA14 | PB35B | 4 | C | CSN |
| AC14 | PB36A | 4 | T | VREF2_4 |
| AB14 | PB36B | 4 | C | D0/SPID7 |
| AF15 | PB37A | 4 | T | D2/SPID5 |
| GND | GND04 | | | |
| AE15 | PB37B | 4 | C | D1/SPID6 |
| AD15 | PB38A | 4 | T | BDQS38 |
| AC15 | PB38B | 4 | C | D3/SPID4 |
| AF16 | PB39A | 4 | T | |
| Y14 | PB39B | 4 | C | D4/SPID3 |
| AE16 | PB40A | 4 | T | |
| AB15 | PB40B | 4 | C | D5/SPID2 |
| AF17 | PB41A | 4 | T | |
| GND | GND04 | | | |
| AE17 | PB41B | 4 | C | D6/SPID1 |
| Y15 | PB42A | 4 | T | |
| AA15 | PB42B | 4 | C | |
| AD17 | PB43A | 4 | T | |
| Y16 | PB43B | 4 | C | |
| AD18 | PB44A | 4 | T | |
| AC16 | PB44B | 4 | C | |
| AE18 | PB45A | 4 | T | |
| GND | GND04 | | | |
| AF18 | PB45B | 4 | C | |
| AD16 | PB46A | 4 | T | BDQS46 |
| AB16 | PB46B | 4 | C | |
| AF19 | PB47A | 4 | T | |
| AA16 | PB47B | 4 | C | |
| AA17 | PB48A | 4 | T | |
| Y17 | PB48B | 4 | C | |
| AF21 | PB49A | 4 | T | |
| GND | GND04 | | | |
| AF20 | PB49B | 4 | C | |
| AE21 | PB50A | 4 | T | |
| AC17 | PB50B | 4 | C | |
| AF22 | PB51A | 4 | T | |
| AB17 | PB51B | 4 | C | |
| AE22 | PB52A | 4 | T | |
| AA18 | PB52B | 4 | C | |
| AE19 | PB53A | 4 | T | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| GND | GND04 | | | |
| AE20 | PB53B | 4 | C | |
| AA19 | PB54A | 4 | T | BDQS54 |
| Y18 | PB54B | 4 | C | |
| AF23 | PB55A | 4 | T | |
| AA20 | PB55B | 4 | C | |
| AC18 | PB56A | 4 | T | |
| AB18 | PB56B | 4 | C | |
| AF24 | PB57A | 4 | T | |
| AE23 | PB57B | 4 | C | |
| GND | GND04 | | | |
| GND | GND03 | | | |
| AC23 | PR48B | 3 | C | VREF2_3 |
| AC24 | PR48A | 3 | T | VREF1_3 |
| AC25 | PR47B | 3 | C | |
| AC26 | PR47A | 3 | T | |
| AB25 | PR46B | 3 | C | |
| AA25 | PR46A | 3 | T | |
| AB26 | PR45B | 3 | C | |
| AA26 | PR45A | 3 | T | RDQS45 |
| W23 | PR44B | 3 | C | RLM0_PLLC_IN_A |
| GND | GND03 | | | |
| W24 | PR44A | 3 | T | RLM0_PLLT_IN_A |
| W22 | PR43B | 3 | C | RLM0_PLLC_FB_A |
| W21 | PR43A | 3 | T | RLM0_PLLT_FB_A |
| Y25 | PR42B | 3 | C | DI/CSSPIN |
| Y26 | PR42A | 3 | T | DOUT/CSON |
| W25 | PR41B | 3 | C | BUSY/SISPI |
| W26 | PR41A | 3 | T | D7/SPID0 |
| V24 | CFG2 | 3 | | |
| V21 | CFG1 | 3 | | |
| V23 | CFG0 | 3 | | |
| V22 | PROGRAMN | 3 | | |
| V20 | CCLK | 3 | | |
| V25 | INITN | 3 | | |
| U20 | DONE | 3 | | |
| V26 | PR39B | 3 | C | |
| GND | GND03 | | | |
| U26 | PR39A | 3 | T | |
| U24 | PR38B | 3 | C | |
| U25 | PR38A | 3 | T | |
| U23 | PR37B | 3 | C | |
| U22 | PR37A | 3 | T | |
| U21 | PR36B | 3 | C | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| T21 | PR36A | 3 | T | RDQS36 |
| T25 | PR35B | 3 | C | |
| GND | GND03 | | | |
| T26 | PR35A | 3 | T | |
| T22 | PR34B | 3 | C | |
| T23 | PR34A | 3 | T | |
| T24 | PR33B | 3 | C | |
| R23 | PR33A | 3 | T | |
| R25 | PR32B | 3 | C | |
| R24 | PR32A | 3 | T | |
| R26 | PR31B | 3 | C | |
| GND | GND03 | | | |
| P26 | PR31A | 3 | T | |
| R21 | PR30B | 3 | C | |
| R22 | PR30A | 3 | T | |
| P25 | PR29B | 3 | C | |
| P24 | PR29A | 3 | T | |
| P23 | PR28B | 3 | C | |
| P22 | PR28A | 3 | T | RDQS28 |
| N26 | PR27B | 3 | C | |
| GND | GND03 | | | |
| M26 | PR27A | 3 | T | |
| N21 | PR26B | 3 | C | |
| P21 | PR26A | 3 | T | |
| N23 | PR25B | 3 | C | |
| N22 | PR25A | 3 | T | |
| N25 | PR24B | 3 | C | |
| N24 | PR24A | 3 | T | |
| L26 | PR22B | 2 | C | PCLKC2_0 |
| GND | GND02 | | | |
| K26 | PR22A | 2 | T | PCLKT2_0 |
| M22 | PR21B | 2 | C | |
| M23 | PR21A | 2 | T | |
| M25 | PR20B | 2 | C | |
| M24 | PR20A | 2 | T | |
| M21 | PR19B | 2 | C | |
| L21 | PR19A | 2 | T | RDQS19 |
| L22 | PR18B | 2 | C | |
| GND | GND02 | | | |
| L23 | PR18A | 2 | T | |
| L25 | PR17B | 2 | C | |
| L24 | PR17A | 2 | T | |
| K25 | PR16B | 2 | C | |
| J25 | PR16A | 2 | T | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|----------------|
| J26 | PR15B | 2 | C | |
| H26 | PR15A | 2 | T | |
| H25 | PR14B | 2 | C | |
| J24 | PR14A | 2 | T | |
| GND | GND02 | | | |
| K21 | PR13B | 2 | C | |
| K22 | PR13A | 2 | T | |
| K20 | PR12B | 2 | C | |
| J20 | PR12A | 2 | T | |
| K23 | PR11B | 2 | C | |
| K24 | PR11A | 2 | T | |
| F25 | PR9B | 2 | C | RUM0_PLLC_FB_A |
| GND | GND02 | | | |
| G25 | PR9A | 2 | T | RUM0_PLLT_FB_A |
| H23 | PR8B | 2 | C | RUM0_PLLC_IN_A |
| H24 | PR8A | 2 | T | RUM0_PLLT_IN_A |
| H21 | PR7B | 2 | C | |
| G21 | PR7A | 2 | T | |
| D26 | PR6B | 2 | C | |
| D25 | PR6A | 2 | T | RDQS6 |
| F21 | PR5B | 2 | C | |
| G22 | PR5A | 2 | T | |
| G24 | PR4B | 2 | C | |
| G23 | PR4A | 2 | T | |
| C26 | PR3B | 2 | C | |
| C25 | PR3A | 2 | T | |
| E23 | PR2B | 2 | C | VREF1_2 |
| D23 | PR2A | 2 | T | VREF2_2 |
| GND | GND02 | | | |
| GND | GND01 | | | |
| A24 | PT57B | 1 | C | |
| A23 | PT57A | 1 | T | |
| E18 | PT56B | 1 | C | |
| D19 | PT56A | 1 | T | |
| F19 | PT55B | 1 | C | |
| B22 | PT55A | 1 | T | |
| G19 | PT54B | 1 | C | |
| B21 | PT54A | 1 | T | TDQS54 |
| D18 | PT53B | 1 | C | |
| GND | GND01 | | | |
| C18 | PT53A | 1 | T | |
| F18 | PT52B | 1 | C | |
| A22 | PT52A | 1 | T | |
| G18 | PT51B | 1 | C | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| A21 | PT51A | 1 | T | |
| E17 | PT50B | 1 | C | |
| B17 | PT50A | 1 | T | |
| C17 | PT49B | 1 | C | |
| GND | GND01 | | | |
| D17 | PT49A | 1 | T | |
| F17 | PT48B | 1 | C | |
| E20 | PT48A | 1 | T | |
| G17 | PT47B | 1 | C | |
| B20 | PT47A | 1 | T | |
| E16 | PT46B | 1 | C | |
| A20 | PT46A | 1 | T | TDQS46 |
| A19 | PT45B | 1 | C | |
| GND | GND01 | | | |
| B19 | PT45A | 1 | T | |
| D16 | PT44B | 1 | C | |
| C16 | PT44A | 1 | T | |
| F16 | PT43B | 1 | C | |
| A18 | PT43A | 1 | T | |
| G16 | PT42B | 1 | C | |
| B18 | PT42A | 1 | T | |
| A17 | PT41B | 1 | C | |
| GND | GND01 | | | |
| A16 | PT41A | 1 | T | |
| D15 | PT40B | 1 | C | |
| B16 | PT40A | 1 | T | |
| E15 | PT39B | 1 | C | |
| C15 | PT39A | 1 | T | |
| F15 | PT38B | 1 | C | |
| G15 | PT38A | 1 | T | TDQS38 |
| B15 | PT37B | 1 | C | |
| GND | GND01 | | | |
| A15 | PT37A | 1 | T | |
| E14 | PT36B | 1 | C | |
| G14 | PT36A | 1 | T | |
| D14 | PT35B | 1 | C | VREF2_1 |
| E13 | PT35A | 1 | T | VREF1_1 |
| F14 | PT34B | 1 | C | |
| C14 | PT34A | 1 | T | |
| B14 | PT33B | 0 | C | PCLKC0_0 |
| GND | GND01 | | | |
| A14 | PT33A | 0 | T | PCLKT0_0 |
| D13 | PT32B | 0 | C | VREF1_0 |
| C13 | PT32A | 0 | T | VREF2_0 |

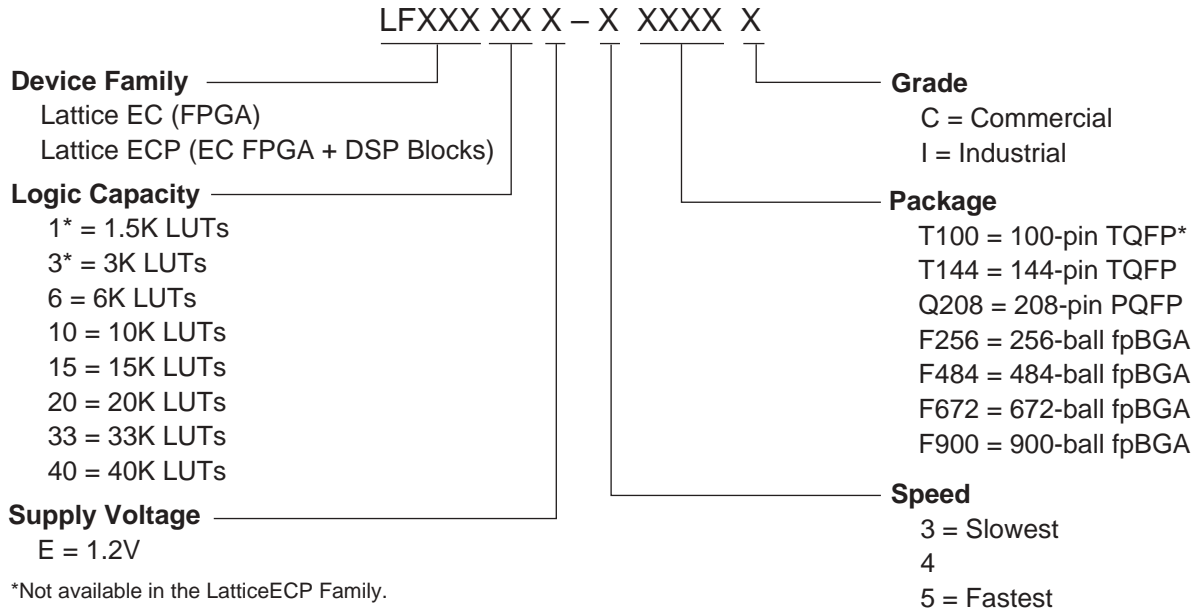
LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| A13 | PT31B | 0 | C | |
| B13 | PT31A | 0 | T | |
| F13 | PT30B | 0 | C | |
| F12 | PT30A | 0 | T | TDQS30 |
| A12 | PT29B | 0 | C | |
| GND | GND00 | | | |
| B12 | PT29A | 0 | T | |
| A11 | PT28B | 0 | C | |
| B11 | PT28A | 0 | T | |
| D12 | PT27B | 0 | C | |
| C12 | PT27A | 0 | T | |
| B10 | PT26B | 0 | C | |
| A10 | PT26A | 0 | T | |
| G12 | PT25B | 0 | C | |
| GND | GND00 | | | |
| A9 | PT25A | 0 | T | |
| E12 | PT24B | 0 | C | |
| B9 | PT24A | 0 | T | |
| F11 | PT23B | 0 | C | |
| A8 | PT23A | 0 | T | |
| D11 | PT22B | 0 | C | |
| C11 | PT22A | 0 | T | TDQS22 |
| B8 | PT21B | 0 | C | |
| GND | GND00 | | | |
| B7 | PT21A | 0 | T | |
| E11 | PT20B | 0 | C | |
| A7 | PT20A | 0 | T | |
| G11 | PT19B | 0 | C | |
| C7 | PT19A | 0 | T | |
| G10 | PT18B | 0 | C | |
| C6 | PT18A | 0 | T | |
| C10 | PT17B | 0 | C | |
| GND | GND00 | | | |
| D10 | PT17A | 0 | T | |
| F10 | PT16B | 0 | C | |
| A6 | PT16A | 0 | T | |
| E10 | PT15B | 0 | C | |
| C9 | PT15A | 0 | T | |
| G9 | PT14B | 0 | C | |
| D9 | PT14A | 0 | T | TDQS14 |
| A5 | PT13B | 0 | C | |
| GND | GND00 | | | |
| A4 | PT13A | 0 | T | |
| F9 | PT12B | 0 | C | |

LFCEP20/LFEC20 Logic Signal Connections: 672 fpBGA (Cont.)

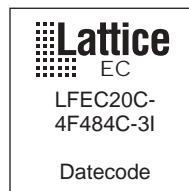
| Ball Number | Ball Function | Bank | LVDS | Dual Function |
|-------------|---------------|------|------|---------------|
| B6 | PT12A | 0 | T | |
| E9 | PT11B | 0 | C | |
| C8 | PT11A | 0 | T | |
| G8 | PT10B | 0 | C | |
| B5 | PT10A | 0 | T | |
| A3 | PT9B | 0 | C | |
| GND | GND00 | | | |
| A2 | PT9A | 0 | T | |
| F8 | PT8B | 0 | C | |
| B4 | PT8A | 0 | T | |
| E8 | PT7B | 0 | C | |
| B3 | PT7A | 0 | T | |
| D8 | PT6B | 0 | C | |
| G7 | PT6A | 0 | T | TDQS6 |
| C4 | PT5B | 0 | C | |
| C5 | PT5A | 0 | T | |
| E7 | PT4B | 0 | C | |
| D4 | PT4A | 0 | T | |
| F7 | PT3B | 0 | C | |
| D6 | PT3A | 0 | T | |
| D7 | PT2B | 0 | C | |
| E6 | PT2A | 0 | T | |
| GND | GND00 | | | |

Part Number Description



Ordering Information

Note: LatticeECP/EC devices are dual marked. For example, the commercial speed grade LFEC20E-4F484C is also marked with industrial grade -3I (LFEC20E-3F484I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:



LatticeEC Commercial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC1E-3Q208C | 112 | -3 | PQFP | 208 | COM | 1.5K |
| LFEC1E-4Q208C | 112 | -4 | PQFP | 208 | COM | 1.5K |
| LFEC1E-5Q208C | 112 | -5 | PQFP | 208 | COM | 1.5K |
| LFEC1E-3T144C | 97 | -3 | TQFP | 144 | COM | 1.5K |
| LFEC1E-4T144C | 97 | -4 | TQFP | 144 | COM | 1.5K |
| LFEC1E-5T144C | 97 | -5 | TQFP | 144 | COM | 1.5K |
| LFEC1E-3T100C | 67 | -3 | TQFP | 100 | COM | 1.5K |

LatticeEC Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC1E-4T100C | 67 | -4 | TQFP | 100 | COM | 1.5K |
| LFEC1E-5T100C | 67 | -5 | TQFP | 100 | COM | 1.5K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC3E-3F256C | 160 | -3 | fpBGA | 256 | COM | 3.1K |
| LFEC3E-4F256C | 160 | -4 | fpBGA | 256 | COM | 3.1K |
| LFEC3E-5F256C | 160 | -5 | fpBGA | 256 | COM | 3.1K |
| LFEC3E-3Q208C | 145 | -3 | PQFP | 208 | COM | 3.1K |
| LFEC3E-4Q208C | 145 | -4 | PQFP | 208 | COM | 3.1K |
| LFEC3E-5Q208C | 145 | -5 | PQFP | 208 | COM | 3.1K |
| LFEC3E-3T144C | 97 | -3 | TQFP | 144 | COM | 3.1K |
| LFEC3E-4T144C | 97 | -4 | TQFP | 144 | COM | 3.1K |
| LFEC3E-5T144C | 97 | -5 | TQFP | 144 | COM | 3.1K |
| LFEC3E-3T100C | 67 | -3 | TQFP | 100 | COM | 3.1K |
| LFEC3E-4T100C | 67 | -4 | TQFP | 100 | COM | 3.1K |
| LFEC3E-5T100C | 67 | -5 | TQFP | 100 | COM | 3.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC6E-3F484C | 224 | -3 | fpBGA | 484 | COM | 6.1K |
| LFEC6E-4F484C | 224 | -4 | fpBGA | 484 | COM | 6.1K |
| LFEC6E-5F484C | 224 | -5 | fpBGA | 484 | COM | 6.1K |
| LFEC6E-3F256C | 195 | -3 | fpBGA | 256 | COM | 6.1K |
| LFEC6E-4F256C | 195 | -4 | fpBGA | 256 | COM | 6.1K |
| LFEC6E-5F256C | 195 | -5 | fpBGA | 256 | COM | 6.1K |
| LFEC6E-3Q208C | 147 | -3 | PQFP | 208 | COM | 6.1K |
| LFEC6E-4Q208C | 147 | -4 | PQFP | 208 | COM | 6.1K |
| LFEC6E-5Q208C | 147 | -5 | PQFP | 208 | COM | 6.1K |
| LFEC6E-3T144C | 97 | -3 | TQFP | 144 | COM | 6.1K |
| LFEC6E-4T144C | 97 | -4 | TQFP | 144 | COM | 6.1K |
| LFEC6E-5T144C | 97 | -5 | TQFP | 144 | COM | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC10E-3F484C | 288 | -3 | fpBGA | 484 | COM | 10.2K |
| LFEC10E-4F484C | 288 | -4 | fpBGA | 484 | COM | 10.2K |
| LFEC10E-5F484C | 288 | -5 | fpBGA | 484 | COM | 10.2K |
| LFEC10E-3F256C | 195 | -3 | fpBGA | 256 | COM | 10.2K |
| LFEC10E-4F256C | 195 | -4 | fpBGA | 256 | COM | 10.2K |
| LFEC10E-5F256C | 195 | -5 | fpBGA | 256 | COM | 10.2K |
| LFEC10E-3Q208C | 147 | -3 | PQFP | 208 | COM | 10.2K |
| LFEC10E-4Q208C | 147 | -4 | PQFP | 208 | COM | 10.2K |
| LFEC10E-5Q208C | 147 | -5 | PQFP | 208 | COM | 10.2K |

LatticeEC Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC15E-3F484C | 352 | -3 | fpBGA | 484 | COM | 15.3K |
| LFEC15E-4F484C | 352 | -4 | fpBGA | 484 | COM | 15.3K |
| LFEC15E-5F484C | 352 | -5 | fpBGA | 484 | COM | 15.3K |
| LFEC15E-3F256C | 195 | -3 | fpBGA | 256 | COM | 15.3K |
| LFEC15E-4F256C | 195 | -4 | fpBGA | 256 | COM | 15.3K |
| LFEC15E-5F256C | 195 | -5 | fpBGA | 256 | COM | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC20E-3F672C | 400 | -3 | fpBGA | 672 | COM | 19.7K |
| LFEC20E-4F672C | 400 | -4 | fpBGA | 672 | COM | 19.7K |
| LFEC20E-5F672C | 400 | -5 | fpBGA | 672 | COM | 19.7K |
| LFEC20E-3F484C | 360 | -3 | fpBGA | 484 | COM | 19.7K |
| LFEC20E-4F484C | 360 | -4 | fpBGA | 484 | COM | 19.7K |
| LFEC20E-5F484C | 360 | -5 | fpBGA | 484 | COM | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC33E-3F672C | 496 | -3 | fpBGA | 672 | COM | 32.8K |
| LFEC33E-4F672C | 496 | -4 | fpBGA | 672 | COM | 32.8K |
| LFEC33E-5F672C | 496 | -5 | fpBGA | 672 | COM | 32.8K |
| LFEC33E-3F484C | 360 | -3 | fpBGA | 484 | COM | 32.8K |
| LFEC33E-4F484C | 360 | -4 | fpBGA | 484 | COM | 32.8K |
| LFEC33E-5F484C | 360 | -5 | fpBGA | 484 | COM | 32.8K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC40E-3F900C | 576 | -3 | fpBGA | 900 | COM | 40.9K |
| LFEC40E-4F900C | 576 | -4 | fpBGA | 900 | COM | 40.9K |
| LFEC40E-5F900C | 576 | -5 | fpBGA | 900 | COM | 40.9K |
| LFEC40E-3F672C | 496 | -3 | fpBGA | 672 | COM | 40.9K |
| LFEC40E-4F672C | 496 | -4 | fpBGA | 672 | COM | 40.9K |
| LFEC40E-5F672C | 496 | -5 | fpBGA | 672 | COM | 40.9K |

LatticeECP Commercial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC6E-3F484C | 224 | -3 | fpBGA | 484 | COM | 6.1K |
| LFEC6E-4F484C | 224 | -4 | fpBGA | 484 | COM | 6.1K |
| LFEC6E-5F484C | 224 | -5 | fpBGA | 484 | COM | 6.1K |
| LFEC6E-3F256C | 195 | -3 | fpBGA | 256 | COM | 6.1K |
| LFEC6E-4F256C | 195 | -4 | fpBGA | 256 | COM | 6.1K |
| LFEC6E-5F256C | 195 | -5 | fpBGA | 256 | COM | 6.1K |
| LFEC6E-3Q208C | 147 | -3 | PQFP | 208 | COM | 6.1K |
| LFEC6E-4Q208C | 147 | -4 | PQFP | 208 | COM | 6.1K |
| LFEC6E-5Q208C | 147 | -5 | PQFP | 208 | COM | 6.1K |
| LFEC6E-3T144C | 97 | -3 | TQFP | 144 | COM | 6.1K |

LatticeECP Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|------|
| LFCEP6E-4T144C | 97 | -4 | TQFP | 144 | COM | 6.1K |
| LFCEP6E-5T144C | 97 | -5 | TQFP | 144 | COM | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP10E-3F484C | 288 | -3 | fpBGA | 484 | COM | 10.2K |
| LFCEP10E-4F484C | 288 | -4 | fpBGA | 484 | COM | 10.2K |
| LFCEP10E-5F484C | 288 | -5 | fpBGA | 484 | COM | 10.2K |
| LFCEP10E-3F256C | 195 | -3 | fpBGA | 256 | COM | 10.2K |
| LFCEP10E-4F256C | 195 | -4 | fpBGA | 256 | COM | 10.2K |
| LFCEP10E-5F256C | 195 | -5 | fpBGA | 256 | COM | 10.2K |
| LFCEP10E-3Q208C | 147 | -3 | PQFP | 208 | COM | 10.2K |
| LFCEP10E-4Q208C | 147 | -4 | PQFP | 208 | COM | 10.2K |
| LFCEP10E-5Q208C | 147 | -5 | PQFP | 208 | COM | 10.2K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP15E-3F484C | 352 | -3 | fpBGA | 484 | COM | 15.3K |
| LFCEP15E-4F484C | 352 | -4 | fpBGA | 484 | COM | 15.3K |
| LFCEP15E-5F484C | 352 | -5 | fpBGA | 484 | COM | 15.3K |
| LFCEP15E-3F256C | 195 | -3 | fpBGA | 256 | COM | 15.3K |
| LFCEP15E-4F256C | 195 | -4 | fpBGA | 256 | COM | 15.3K |
| LFCEP15E-5F256C | 195 | -5 | fpBGA | 256 | COM | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP20E-3F672C | 400 | -3 | fpBGA | 672 | COM | 19.7K |
| LFCEP20E-4F672C | 400 | -4 | fpBGA | 672 | COM | 19.7K |
| LFCEP20E-5F672C | 400 | -5 | fpBGA | 672 | COM | 19.7K |
| LFCEP20E-3F484C | 360 | -3 | fpBGA | 484 | COM | 19.7K |
| LFCEP20E-4F484C | 360 | -4 | fpBGA | 484 | COM | 19.7K |
| LFCEP20E-5F484C | 360 | -5 | fpBGA | 484 | COM | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP33E-3F672C | 496 | -3 | fpBGA | 672 | COM | 32.8K |
| LFCEP33E-4F672C | 496 | -4 | fpBGA | 672 | COM | 32.8K |
| LFCEP33E-5F672C | 496 | -5 | fpBGA | 672 | COM | 32.8K |
| LFCEP33E-3F484C | 360 | -3 | fpBGA | 484 | COM | 32.8K |
| LFCEP33E-4F484C | 360 | -4 | fpBGA | 484 | COM | 32.8K |
| LFCEP33E-5F484C | 360 | -5 | fpBGA | 484 | COM | 32.8K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP40E-3F900C | 576 | -3 | fpBGA | 900 | COM | 40.9K |
| LFCEP40E-4F900C | 576 | -4 | fpBGA | 900 | COM | 40.9K |
| LFCEP40E-5F900C | 576 | -5 | fpBGA | 900 | COM | 40.9K |
| LFCEP40E-3F672C | 496 | -3 | fpBGA | 672 | COM | 40.9K |

LatticeECP Commercial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFECP40E-4F672C | 496 | -4 | fpBGA | 672 | COM | 40.9K |
| LFECP40E-5F672C | 496 | -5 | fpBGA | 672 | COM | 40.9K |

LatticeEC Industrial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC1E-3Q208I | 112 | -3 | PQFP | 208 | IND | 1.5K |
| LFEC1E-4Q208I | 112 | -4 | PQFP | 208 | IND | 1.5K |
| LFEC1E-3T144I | 97 | -3 | TQFP | 144 | IND | 1.5K |
| LFEC1E-4T144I | 97 | -4 | TQFP | 144 | IND | 1.5K |
| LFEC1E-3T100I | 67 | -3 | TQFP | 100 | IND | 1.5K |
| LFEC1E-4T100I | 67 | -4 | TQFP | 100 | IND | 1.5K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC3E-3F256I | 160 | -3 | fpBGA | 256 | IND | 3.1K |
| LFEC3E-4F256I | 160 | -4 | fpBGA | 256 | IND | 3.1K |
| LFEC3E-3Q208I | 145 | -3 | PQFP | 208 | IND | 3.1K |
| LFEC3E-4Q208I | 145 | -4 | PQFP | 208 | IND | 3.1K |
| LFEC3E-3T144I | 97 | -3 | TQFP | 144 | IND | 3.1K |
| LFEC3E-4T144I | 97 | -4 | TQFP | 144 | IND | 3.1K |
| LFEC3E-3T100I | 67 | -3 | TQFP | 100 | IND | 3.1K |
| LFEC3E-4T100I | 67 | -4 | TQFP | 100 | IND | 3.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC6E-3F484I | 224 | -3 | fpBGA | 484 | IND | 6.1K |
| LFEC6E-4F484I | 224 | -4 | fpBGA | 484 | IND | 6.1K |
| LFEC6E-3F256I | 195 | -3 | fpBGA | 256 | IND | 6.1K |
| LFEC6E-4F256I | 195 | -4 | fpBGA | 256 | IND | 6.1K |
| LFEC6E-3Q208I | 147 | -3 | PQFP | 208 | IND | 6.1K |
| LFEC6E-4Q208I | 147 | -4 | PQFP | 208 | IND | 6.1K |
| LFEC6E-3T144I | 97 | -3 | TQFP | 144 | IND | 6.1K |
| LFEC6E-4T144I | 97 | -4 | TQFP | 144 | IND | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFEC10E-3F484I | 288 | -3 | fpBGA | 484 | IND | 10.2K |
| LFEC10E-4F484I | 288 | -4 | fpBGA | 484 | IND | 10.2K |
| LFEC10E-3F256I | 195 | -3 | fpBGA | 256 | IND | 10.2K |
| LFEC10E-4F256I | 195 | -4 | fpBGA | 256 | IND | 10.2K |
| LFEC10E-3 P208I | 147 | -3 | PQFP | 208 | IND | 10.2K |
| LFEC10E-4 P208I | 147 | -4 | PQFP | 208 | IND | 10.2K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC15E-3F484I | 352 | -3 | fpBGA | 484 | IND | 15.3K |
| LFEC15E-4F484I | 352 | -4 | fpBGA | 484 | IND | 15.3K |

LatticeEC Industrial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC15E-3F256I | 195 | -3 | fpBGA | 256 | IND | 15.3K |
| LFEC15E-4F256I | 195 | -4 | fpBGA | 256 | IND | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC20E-3F672I | 400 | -3 | fpBGA | 672 | IND | 19.7K |
| LFEC20E-4F672I | 400 | -4 | fpBGA | 672 | IND | 19.7K |
| LFEC20E-3F484I | 360 | -3 | fpBGA | 484 | IND | 19.7K |
| LFEC20E-4F484I | 360 | -4 | fpBGA | 484 | IND | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|---------------|------|-------|---------|------|-------|------|
| LFEC33-3F672I | 496 | -3 | fpBGA | 672 | IND | 32.8 |
| LFEC33-4F672I | 496 | -4 | fpBGA | 672 | IND | 32.8 |
| LFEC33-3F484I | 360 | -3 | fpBGA | 484 | IND | 32.8 |
| LFEC33-4F484I | 360 | -4 | fpBGA | 484 | IND | 32.8 |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFEC40E-3F900I | 576 | -3 | fpBGA | 900 | IND | 40.9K |
| LFEC40E-4F900I | 576 | -4 | fpBGA | 900 | IND | 40.9K |
| LFEC40E-3F672I | 496 | -3 | fpBGA | 672 | IND | 40.9K |
| LFEC40E-4F672I | 496 | -4 | fpBGA | 672 | IND | 40.9K |

LatticeECP Industrial

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|------|
| LFCEP6E-3F484I | 224 | -3 | fpBGA | 484 | IND | 6.1K |
| LFCEP6E-4F484I | 224 | -4 | fpBGA | 484 | IND | 6.1K |
| LFCEP6E-3F256I | 195 | -3 | fpBGA | 256 | IND | 6.1K |
| LFCEP6E-4F256I | 195 | -4 | fpBGA | 256 | IND | 6.1K |
| LFCEP6E-3Q208I | 147 | -3 | PQFP | 208 | IND | 6.1K |
| LFCEP6E-4Q208I | 147 | -4 | PQFP | 208 | IND | 6.1K |
| LFCEP6E-3T144I | 97 | -3 | TQFP | 144 | IND | 6.1K |
| LFCEP6E-4T144I | 97 | -4 | TQFP | 144 | IND | 6.1K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP10E-3F484I | 288 | -3 | fpBGA | 484 | IND | 10.2K |
| LFCEP10E-4F484I | 288 | -4 | fpBGA | 484 | IND | 10.2K |
| LFCEP10E-3F256I | 195 | -3 | fpBGA | 256 | IND | 10.2K |
| LFCEP10E-4F256I | 195 | -4 | fpBGA | 256 | IND | 10.2K |
| LFCEP10E-3Q208I | 147 | -3 | PQFP | 208 | IND | 10.2K |
| LFCEP10E-4Q208I | 147 | -4 | PQFP | 208 | IND | 10.2K |

LatticeECP Industrial (Continued)

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP15E-3F484I | 352 | -3 | fpBGA | 484 | IND | 15.3K |
| LFCEP15E-4F484I | 352 | -4 | fpBGA | 484 | IND | 15.3K |
| LFCEP15E-3F256I | 195 | -3 | fpBGA | 256 | IND | 15.3K |
| LFCEP15E-4F256I | 195 | -4 | fpBGA | 256 | IND | 15.3K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP20E-3F672I | 400 | -3 | fpBGA | 672 | IND | 19.7K |
| LFCEP20E-4F672I | 400 | -4 | fpBGA | 672 | IND | 19.7K |
| LFCEP20E-3F484I | 360 | -3 | fpBGA | 484 | IND | 19.7K |
| LFCEP20E-4F484I | 360 | -4 | fpBGA | 484 | IND | 19.7K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|----------------|------|-------|---------|------|-------|-------|
| LFCEP33-3F672I | 496 | -3 | fpBGA | 672 | IND | 32.8K |
| LFCEP33-4F672I | 496 | -4 | fpBGA | 672 | IND | 32.8K |
| LFCEP33-3F484I | 360 | -3 | fpBGA | 484 | IND | 32.8K |
| LFCEP33-4F484I | 360 | -4 | fpBGA | 484 | IND | 32.8K |

| Part Number | I/Os | Grade | Package | Pins | Temp. | LUTs |
|-----------------|------|-------|---------|------|-------|-------|
| LFCEP40E-3F900I | 576 | -3 | fpBGA | 900 | IND | 40.9K |
| LFCEP40E-4F900I | 576 | -4 | fpBGA | 900 | IND | 40.9K |
| LFCEP40E-3F672I | 496 | -3 | fpBGA | 672 | IND | 40.9K |
| LFCEP40E-4F672I | 496 | -4 | fpBGA | 672 | IND | 40.9K |

For Further Information

A variety of technical notes for the LatticeECP/EC family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP/EC sysIO Usage Guide (TN1056)
- ispTRACY Internal Logic Analyzer Guide (TN1054)
- LatticeECP/EC sysCLOCK PLL Design and Usage Guide (TN1049)
- Memory Usage Guide for LatticeECP/EC Devices (TN1051)
- LatticeECP/EC DDR Usage Guide (TN1050)
- Estimating Power Using Power Calculator for LatticeECP/EC Devices (TN1052)
- sysDSP/MAC Usage Guide (TN1057)
- LatticeECP/EC sysCONFIG Usage Guide (TN1053)
- IEEE 1149.1 Boundary Scan Testability in Lattice Devices

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com