LH28F008SC

8M (1M × 8) Flash Memory

FEATURES

- High-Density Symmetrically-Blocked Architecture
  - Sixteen 64K Erasable Blocks
- High-Performance
  - 85 ns Read Access Time
- Enhanced Automated Suspend Options
  - Byte Write Suspend to Read
  - Block Erase Suspend to Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Absolute Protection with V_{PP} = GND
  - Flexible Block Locking
  - Block Erase/Byte Write Lockout during Power Transitions
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
  - 1.6 Million Block Erase Cycles/Chip
- Low Power Management
  - Deep Power-Down Mode
  - Automatic Power Saving Mode Decreases I_{CC} in Static Mode
- Automated Byte Write and Block Erase
  - Command User Interface
  - Status Register
- SmartVoltage Technology
  - 3.3 V or 5 V V_{CC}
  - 3.3 V, 5 V, or 12 V V_{PP}
- SRAM - Compatible Write Interface
- ETOX™ V Nonvolatile Flash Technology
- Industry - Standard Packaging
  - 42-Pin, .67 mm × 8 mm^2 CSP Package
  - 40-Pin, 1.2 mm × 10 mm × 20 mm TSOP (Type I) Package
  - 44-Pin, 600-mil, SOP Package

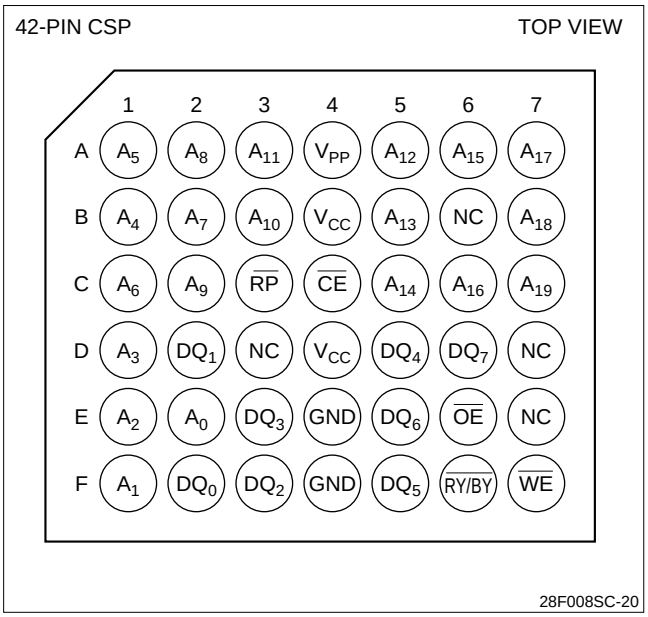


Figure 1. CSP 42-Pin Configuration

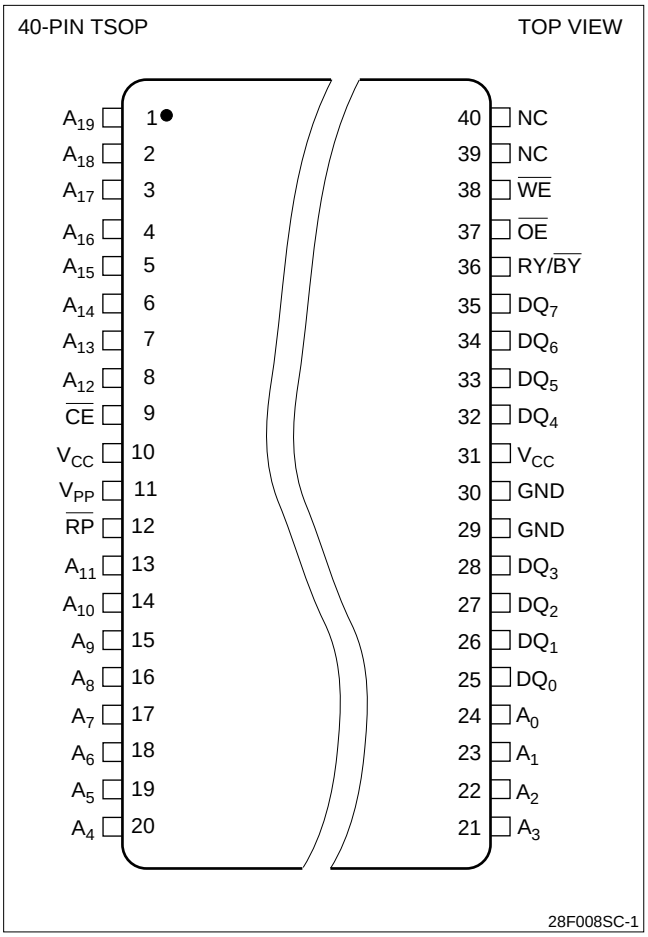


Figure 2. TSOP 40-Pin Configuration

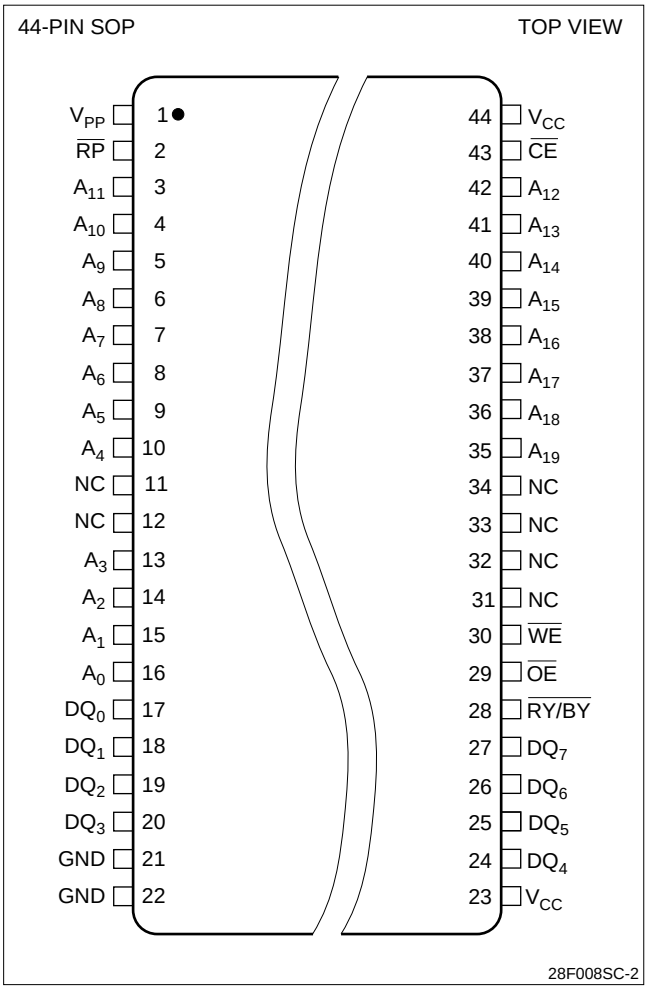


Figure 3. SOP 44-Pin Configuration

INTRODUCTION

SHARP'S LH28F008SC FlashFile™ memory with SmartVoltage technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code and data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F008SC offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F008SC is manufactured on SHARP's 0.4 µm ETOX™ V process technology. It comes in industry-standard packages: the 40-pin TSOP, ideal for board constrained applications, and the rugged 44-pin SOP. Based on the 28F008SA architecture, the LH28F008SC enables quick and easy upgrades for designs demanding the state-of-the art.

New Features

The LH28F008SC SmartVoltage FlashFile memory maintains backwards-compatiblity with SHARP'S 28F008SA. Key enhancements over the 28F008SA include:

- SmartVoltage Technology
- Enhanced Suspend Capabilities
- In-System Block Locking

Both devices share a compatible pinout, status register, and software command set. These similarities enable a clean upgrade from the 28F008SA to LH28F008SC. When upgrading, it is important to note the following differences:

- Because of new feature support, the two devices have different device codes. This allows for software optimization.
- V_{PPLK} has been lowered from 6.5 V to 1.5 V to support 3.3 V and 5 V block erase, byte write, and lock-bit configuration operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- To take advantage of SmartVoltage technology, allow V_{PP} connection to 3.3 V or 5 V.

DESCRIPTION

The LH28F008SC is a high-performance 8M SmartVoltage FlashFile memory organized as 1M of 8 bits. The 1M of data is arranged in sixteen 64K blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 5.

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in the Voltage Combinations Table, to meet system performance and power expectations. 3.3 V V_{CC} consumes approximately one-fourth the power of 5 V V_{CC}. But, 5 V V_{CC} provides the highest read performance. V_{PP} at 3.3 V and 5 V eliminates the need for a separate 12 V converter, while V_{PP} = 12 V maximizes block erase and byte write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

V_{CC} and V_{PP} Voltage Combinations Offered by SmartVoltage Technology

V_{CC} VOLTAGE	V_{PP} VOLTAGE
3.3 V	3.3 V, 5 V, 12 V
5 V	5 V, 12 V

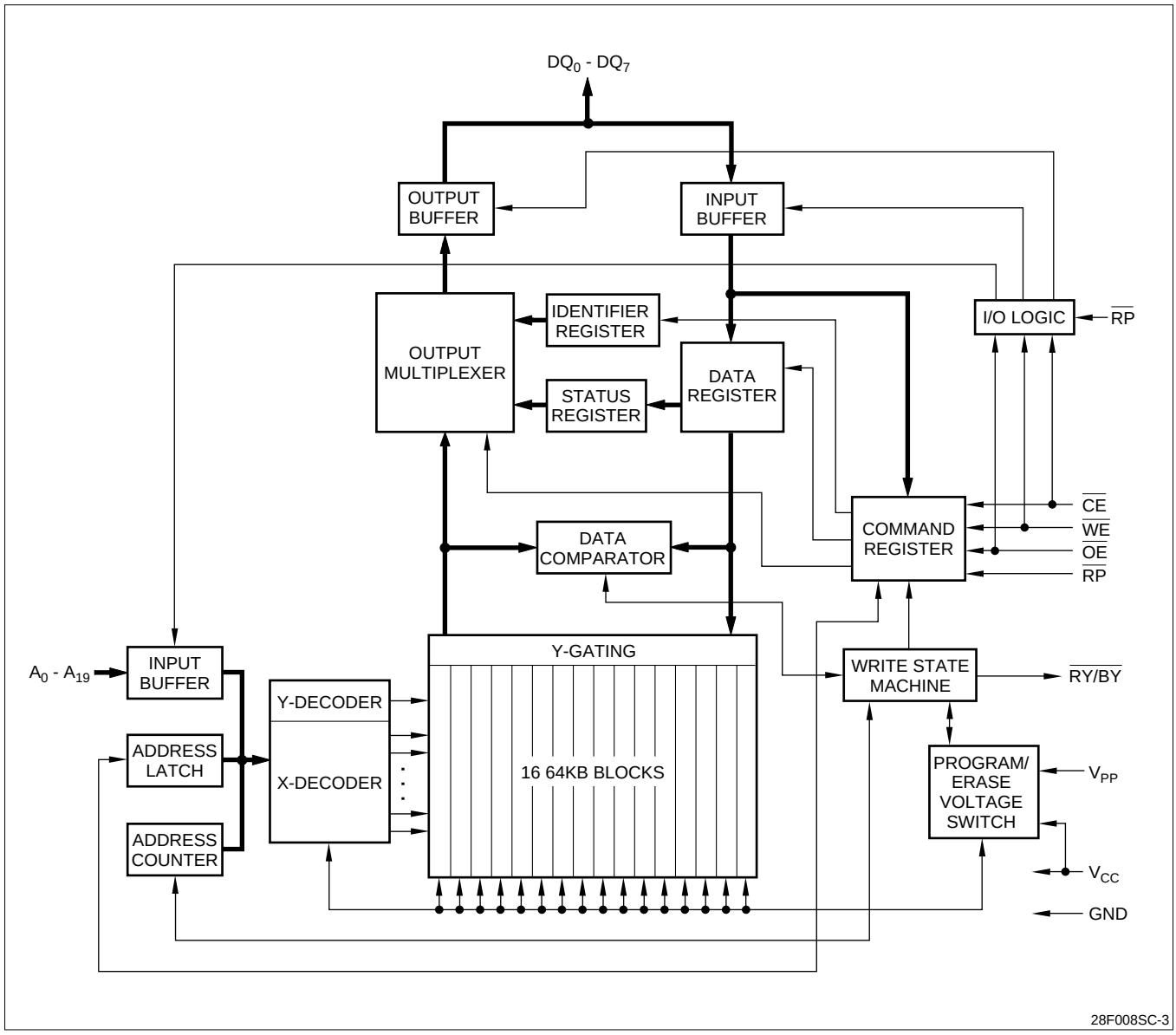


Figure 4. LH28F008SC Block Diagram

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An Internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, byte write, and lock-bit configuration operations.

A block erase operation erases one of the device's 64K blocks typically within 1 second (5 V V_{CC}, 12 V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times (1.6 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in byte increments typically within 6 µs (5 V V_{CC}, 12 V V_{PP}). Byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, sixteen block lock-bits and a master lock-bit, to lock and unlock blocks. Block lock-bits gate block erase and byte write operations, while the master lock-bit gates block lock-bit modification. Lock-bit configuration operations (Set Block, Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, byte write, or lock-bit configuration operation is finished.

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A_0 - A_{19}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
DQ_0 - DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUTS:** Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic input buffers, decoders, and sense amplifiers. $\overline{CE}$ high deselects the device and reduces power consumption to standby levels.
$\overline{RP}$	INPUT	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. $\overline{RP}$ high enables normal operation. When driven low, $\overline{RP}$ inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. $\overline{RP}$ at V_{HH} enables setting of the master lock-bit and enables configuration of block lock-bits when the master lock-bit is set. $\overline{RP}$ = V_{HH} overrides block lock-bits thereby enabling block erase and byte write operation to locked memeory blocks. Block erase, byte write, or lock-bit configuration with V_{IH} < $\overline{RP}$ < V_{HH} produce spurious results and should not be attempted.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the $\overline{WE}$ Pulse.
$\overline{RY}/\overline{BY}$	OUTPUT	**READY/BUSY:** Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, byte write, or lock-bit configuration). $\overline{RY}/\overline{BY}$ high indicates that the WSM is ready for new commands, block erase is suspended, and byte write is inactive, byte write is suspended, or the device is in deep power-down mode. $\overline{RY}/\overline{BY}$ is always active and does not float when the chip is deselected or data outputs are disabled.
V_{PP}	SUPPLY	**BLOCK ERASE/BYTE WRITE, LOCK-BIT CONFIGURATION POWER SUPPLY:** For erasing array blocks, writing bytes, or configuring lock-bits. With $V_{PP} \le V_{LKO}$, memory contents cannot be altered. Block erase, byte write, and lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Internal detection configures the device for 3.3 V or 5 V operation. To switch from one voltage to another, ramp V_{CC} down to GND and then ramp V_{CC} to the new voltage. Do not float any power pins. With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND:** Do not float any pins
NC		**NO CONNECT:** Lead is not internal connected; it may be driven or floated.

The $\overline{RY}/\overline{BY}$ output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using $\overline{RY}/\overline{BY}$ minimizes both CPU overhead and system power consumption. When low, $\overline{RY}/\overline{BY}$ indicates that the WSM is performing a block erase, byte write, or lock-bit configuration. $\overline{RY}/\overline{BY}$ high indicates that the WSM is ready for a new command, block erase is suspended (and byte write is inactive), byte write is suspended, or the device is in deep power-down mode.

The access time is 85 ns (t_{AVAV}) over the commercial temperature range (0°C to +70°C) and V_{CC} supply voltage range of 4.75 V - 5.25 V. At lower V_{CC} voltages, the access times are 90 ns (4.5 V - 5.5 V) and 120 ns (3.0 V - 3.6 V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1 mA at 5 V V_{CC}.

When $\overline{CE}$ and $\overline{RP}$ pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the $\overline{RP}$ pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from $\overline{RP}$ switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from $\overline{RP}$-high until writes to the CUI are recognized. With $\overline{RP}$ at GND, the WSM is reset and the status register is cleared.

The device is available in 40-pin TSOP (Thin Small Outline Package, 1.2 mm thick) and 44-pin SOP (Small Outline Package). Pinouts are shown in Figures 1 and 2.

PRINCIPLES OF OPERATION

The LH28F008SC SmartVoltage FlashFile memory includes an on-chip WSM to manage block erase, byte write, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, byte write, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure, byte writing, and lock-bit configuration. All functions associated with altering memory contents–block erase, byte write, Lock-bit configuration, status, and identifier codes are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, byte write, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase, byte write, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows sytem software to suspend a block. Byte write suspend allows system software to suspend a byte write to read data from any other flash memory array location.

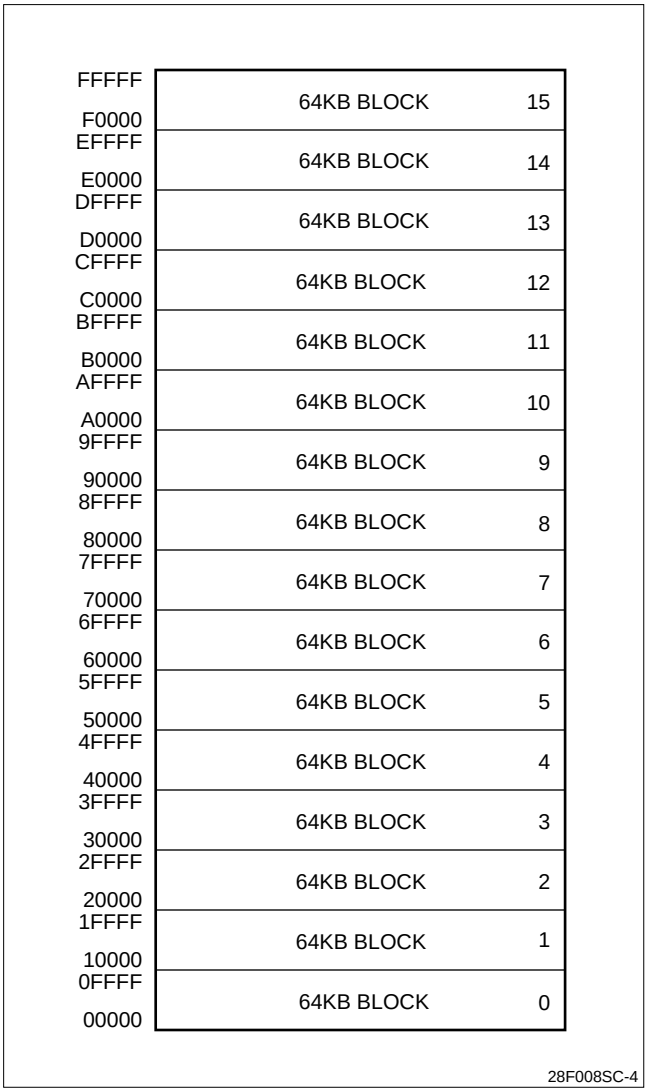


Figure 4. Memory Map

Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases, byte writes, or lock-bit configurations are required) or hardwired to $V_{PPH1/2/3}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase, byte write, or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and byte write operations.

BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Read

Information can be read from any block, identifier codes, or status register independent of the V_{PP} voltage. $\overline{RP}$ can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read, Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Four control pins dictate the data flow in and out of the component: $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and $\overline{RP}$. $\overline{CE}$ and $\overline{OE}$ must be driven active to obtain data at the outputs. $\overline{CE}$ is the device selection control, and when active enables the selected memory device. $\overline{OE}$ is the data output (DQ_0 - DQ_7) control and when active drives the selected memory data onto the I/O bus. $\overline{WE}$ must be at V_{IH} and $\overline{RP}$ must be at V_{IH} or V_{HH}. Figure 15 illustrates a read cycle.

Output Disable

With $\overline{OE}$ at a logic-high level (V_{IH}), the device otuputs are disabled. Output pins DQ_0 - DQ_7 are placed in a high-impedance state.

Standby

$\overline{CE}$ at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0 - DQ_7 outputs are placed in a high-impedance state independent of $\overline{OE}$. If deselected during block erase, byte write, or lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

Deep Power-Down

$\overline{RP}$ at V_{IL} initiates the deep power-down mode.

In read modes, $\overline{RP}$-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. $\overline{RP}$ must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, byte write, or lock-bit configuration modes, $\overline{RP}$-low will abort the operation. $\overline{RY}/\overline{BY}$ remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after $\overline{RP}$ goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert $\overline{RP}$ during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, byte write, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the $\overline{RP}$ input. In this application, $\overline{RP}$ is controlled by the same $\overline{RESET}$ signal that resets the system CPU.

Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the master lock configuration code (see Figure 5). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

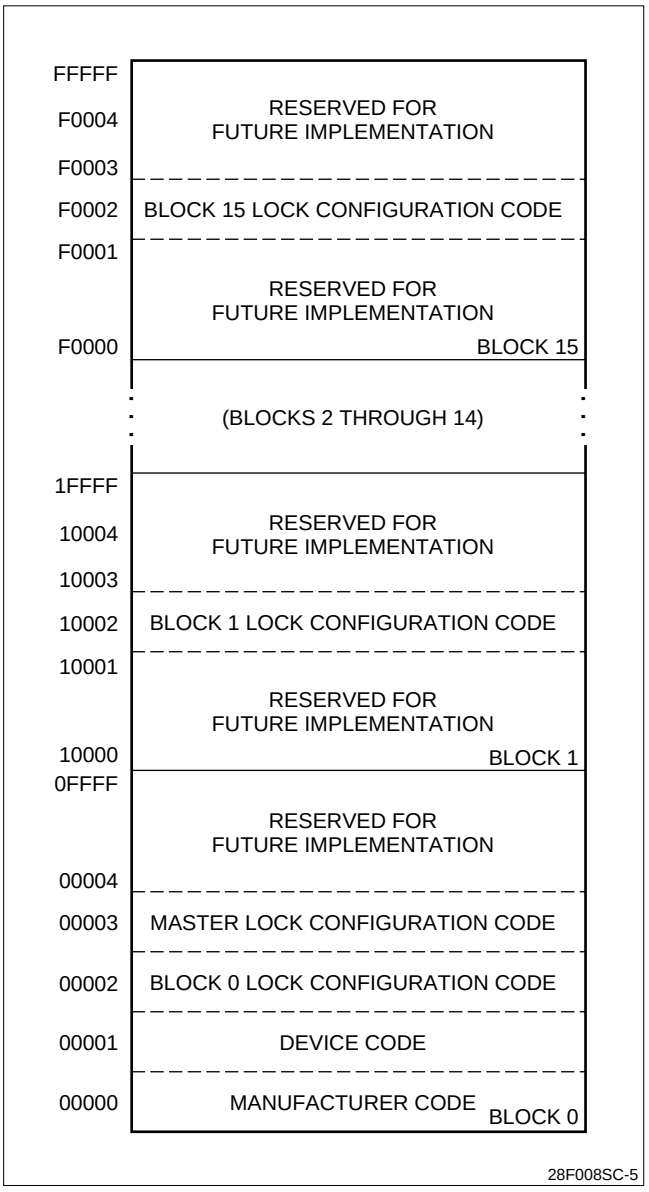


Figure 5. Device Identifier Code Memory Map

Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{PP} = V_{PPH1/2/3}$, the CUI additionally controls block erasure, byte write, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte Write command requires the command and address of the location to be written. Set Master and Block Lock-Bit commands require the command and address within the device (Master Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when $\overline{WE}$ and $\overline{CE}$ are active. The address and data needed to execute a command are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first). Standard microprocessor write timings are used. Figures 16 and 17 illustrate $\overline{WE}$ and $\overline{CE}$ controlled write operations.

COMMAND DEFINITIONS

When the V_{PP} voltage $\leq V_{PPLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{PPH1/2/3}$ on V_{PP} enables successful block erase, byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. The Command Definitions Table defines these commands.

Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and $\overline{RP}$ can be V_{IH} or V_{HH}.

BUS OPERATIONS

MODE	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	V_{PP}	DQ_0 - DQ_7	$\overline{RY}/\overline{BY}$	NOTE
Read	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X	1, 2, 3
Output Disable	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High-Z	X	3
Standby	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High-Z	X	3
Deep Power Down	V_{IL}	X	X	X	X	X	High-Z	V_{OH}	4
Read Identifier Codes	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 5	X	Note 5	V_{OH}	
Write	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X	3, 6, 7

NOTES:
1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2/3}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2/3}$ voltages.
3. $\overline{RY}/\overline{BY}$ is V_{OL} when the WSM is executing internal block erase, byte write, or lock-bit configuration algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with byte write inactive), byte write suspend mode, or deep power-down mode.
4. $\overline{RP}$ at GND ± 0.2 V ensures the lowest deep power-down current.
5. See Read Identifier Codes Command Section for read identifier code data.
6. Command writes involving block erase, write, or lock-bit configuration are reliably executed when $V_{PP} = V_{PPH1/2/3}$ and $V_{CC} = V_{CC1/2/3}$. Block erase, byte write, or lock-bit configuration with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.
7. Refer to Command Definitions Table for valid D_{IN} during a write operation.

Command Definitions[9]

COMMAND	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE			NOTE
		OPER.[1]	ADDRESS[2]	DATA[3]	OPER.[1]	ADDRESS[2]	DATA[3]	
Read Array/Reset	1	Write	X	FFH				
Read Identifier Codes	≥ 2	Write	X	90H	Read	IA	ID	4
Read Status Register	2	Write	X	70H	Read	X	SRD	
Clear Status Register	1	Write	X	50H				
Block Erase	2	Write	BA	20H	Write	BA	D0H	5
Byte Write	2	Write	WA	40H or 10H	Write		WD	5, 6
Block Erase and Byte Write Suspend	1	Write	X	B0H		WA		5
Block Erase and Byte Write Resume	1	Write	X	D0H				5
Set Block Lock-Bit	2	Write	BA	60H	Write	BA	01H	7
Set Master Lock-Bit	2	Write	X	60H	Write	X	F1H	7
Clear Block Lock Bits	2	Write	X	60H	Write	X	D0H	8

NOTES:
1. Bus operations are defined in Bus Definition Table.
2. X = Any valid address within the device.
   IA = Idendifier Code Address: see Figure 5.
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from status register. See Status Register for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first).
   ID = Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Read Identifier Code Command Section for read identifier code data.
5. If the block is locked, $\overline{RP}$ must be at V_{HH} to enable block erase or byte write operations. Attempts to issue a block erase or byte write to locked block while $\overline{RP}$ is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the byte write setup.
7. If the master lock-bit is set, $\overline{RP}$ must be at V_{HH} to set a block lock-bit. $\overline{RP}$ must be at V_{HH} to set the master lock-bit. If the master lock-bit is not set, a block lock-bit can be set while $\overline{RP}$ is V_{IH}.
8. If the master lock-bit is set, $\overline{RP}$ must be at V_{HH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while $\overline{RP}$ is V_{IH}.
9. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 5 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Identifier Code Table for code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} and $\overline{RP}$ can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Identifier Codes

CODE	ADDRESS	DATA
Manufacturer Code	00000	89
Device Code	00001	A6
Block Lock Configurations	X0002[1]	
• Block is Unlocked		$DQ_0 = 0$
• Block is Locked		$DQ_0 = 1$
• Reserved for Future Use		DQ_1 - DQ_7
Master Lock Configuration	00003	
• Device is Unlocked		$DQ_0 = 0$
• Device is Locked		$DQ_0 = 1$
• Reserved for Future Use		DQ_1 - DQ_7

NOTE:
1. X selects the specific block lock configuration code to be read. See Figure 5 for the device identifier code memory map.

Read Status Register Command

The status register may be read to determine when a block erase, byte write, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs. $\overline{OE}$ or $\overline{CE}$ must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. $\overline{RP}$ can be V_{IH} or V_{HH}.

Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 are set to '1' by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Status Register). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. $\overline{RP}$ can be V_{IH} or V_{HH}. This command is not functional during block erase or byte write suspend modes.

Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the output data of the $\overline{RY}/\overline{BY}$ or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to '1'. Also, reliable block erasure can only occur when $V_{CC} = V_{CC1/2/3}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to '1'. Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that $\overline{RP} = V_{HH}$. If block erase is attempted when the corresponding block lock-bit is set and $\overline{RP} = V_{IH}$, SR.1 and SR.5 will be set to '1'. Block erase operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

Byte Write Command

Byte write is executed by a two-cycle command sequence. Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of $\overline{WE}$). The WSM then takes over, controlling the byte write and write verify algorithms internally. After the byte write sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the byte write event by analyzing the $\overline{RY}/\overline{BY}$ pin or status register bit SR.7.

When byte write is complete, status register bit SR.4 should be checked. If byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for '1's that do not successfully write to '0's. The CUI remains in read status register mode until it receives another command.

Reliable byte writes can only occur when $V_{CC} = V_{CC1/2/3}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against byte writes. If byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.4 and SR.5 will be set to '1'. Successful byte write requires that the corresponding block lock-bit be cleared or, if set, that $\overline{RP} = V_{HH}$. If byte write is attempted when the corresponding block lock-bit is set and $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1'. Byte write operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or byte-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to '1'). $\overline{RY}/\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Byte Write Suspend command (see Byte Write Suspend Command Section), a byte write operation can also be suspended. During a byte write operation with block erase suspended, status register bit SR.7 will return to '0' and the $\overline{RY}/\overline{BY}$ output will transition to V_{OL}. However, SR.6 will remain '1' to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and $\overline{RY}/\overline{BY}$ will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for block erase). Block erase cannot resume until byte write operations initiated during block erase suspend have completed.

Byte Write Suspend Command

The Byte Write Suspend command allows byte write interruption to read data in other flash memory locations. Once the byte write process starts, writing the Byte Write Suspend command resquests that the WSM suspend the byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the byte write operation has been suspended (both will be set to '1'). $\overline{RY}/\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRH1} defines the byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while byte write is suspended are Read Status Register and Byte Write Resume. After Byte Write Resume command is written to the flash memory, the WSM will continue the byte write process. Status register bits SR.2 and SR.7 will automatically clear and $\overline{RY}/\overline{BY}$ will return to V_{OL}. After the Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 9). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for byte write) while in byte write suspend mode. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for byte write).

Set Block and Master Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits and a master lock-bit. The block lock-bits gate program and erase operations while the master lock-bit gates block-lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with $\overline{RP} = V_{HH}$, sets the master lock-bit. After the master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and V_{HH} on the $\overline{RP}$ pin. See Write Protection Analysis Table for a summary of hardware and software write protection options.

Set block lock-bit and master lock-bit are executed by a two-cycle command sequence. The set block or master lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set master lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 10). The CPU can detect the completion of the set lock-bit event by analyzing the $\overline{RY}/\overline{BY}$ pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register, bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to '1'. Also, reliable operations occur only when $V_{CC} = V_{CC1/2/3}$ and $V_{PP} = V_{PPH1/2/3}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the master lock-bit be cleared or, if the master lock-bit is set, that $\overline{RP} = V_{HH}$. If it is attempted with the master lock-bit set and $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1' and the operation will fail. Set block lock-bit operations while $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted. A successful set master lock-bit operation requires that $\overline{RP} = V_{HH}$. If it is attempted with $\overline{RP} = V_{IH}$, SR.1 and SR.4 will be set to '1' and the operation will fail. Set master lock-bit operations with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the master lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the master lock-bit is set, clearing block lock-bits requires both the Clear Block Lock-Bits command and V_{HH} on the $\overline{RP}$ pin. See Write Protection Analysis Table for a summary of hardware and software white protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect completion of the clear block lock-bits event by analyzing the $\overline{RY}/\overline{BY}$ Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to “1”. Also, a reliable clear block lock bits operation can only occur when $V_{CC} = V_{CC1/2/3}$ and $V_{PP} = V_{PPH1/2/3}$. If a clear block lock-bits operation is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to '1'. In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the master lock-bit is not set or, if the master lock-bit is set, that $\overline{RP} = V_{HH}$. If it is attempted with the master lock-bit set and $\overline{RP} = V_{IH}$, SR.1 and SR.5 will be set to '1' and the operation will fail. A clear block lock-bits operation with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or $\overline{RP}$ active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known value. Once the master lock-bit is set, it cannont be cleared.

Write Protection Alternatives

OPERATION	MASTER LOCK-BIT	BLOCK LOCK-BIT	RP#	EFFECT
Block Erase or Byte Write	X	0	V_{IH} or V_{HH}	Block Erase and Byte Write Enabled.
		1	V_{IH}	Block is locked. Block Erase and Byte Write Disabled.
			V_{HH}	Block Lock-Bit Override. Block Erase and Byte Write Enabled.
Set Block Lock Bit	0	X	V_{IH} or V_{HH}	Set Block Lock-Bit Enabled.
	1	X	V_{IH}	Master Lock-Bit is Set. Set Block Lock-Bit Disabled.
			V_{HH}	Master Lock-Bit Override. Set Block Lock-Bit Enabled.
Set Master Lock-Bit	X	X	V_{IH}	Set Master Lock-Bit Disabled.
			V_{HH}	Set Master Lock-Bit Enabled.
Clear Block Lock-Bits	0	X	V_{IH} or V_{HH}	Clear Block Lock-Bits Enable.
	1	X	V_{IH}	Master Lock-Bit is Set. Clear Block Lock-Bits Disabled.
			V_{HH}	Master Lock-Bit Override. Clear Block Lock-Bits Enabled.

Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR LOCK-BIT STATUS
1 = Error in Block Erasure or Clear Lock-Bits
0 = Successful Block Erase or Clear Lock-Bits

SR.4 = BYTE WRITE AND SET LOCK-BIT STATUS
1 = Error in Byte Write or Set Master/Block Lock Bit
0 = Successful Byte Write or Set Master/Block Lock-Bit

SR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

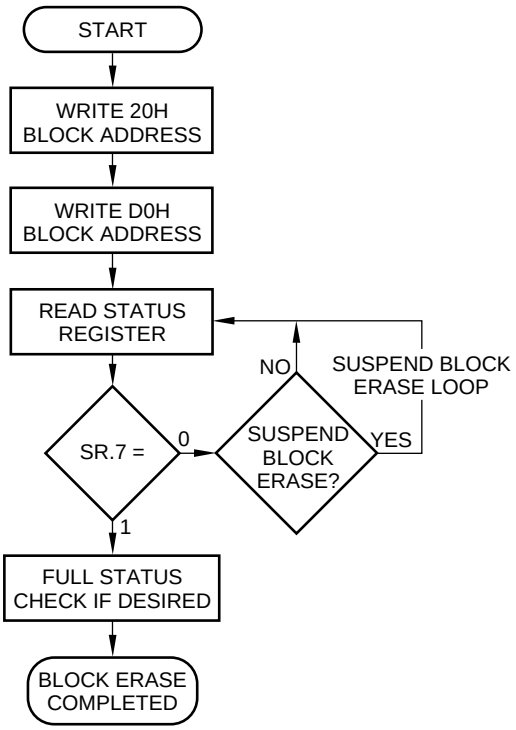
SR.2 = BYTE WRITE SUSPEND STATUS
1 = Byte Write Suspended
0 = Byte Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Master Lock-Bit, Block Lock-Bit and/or $\overline{RP}$ Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

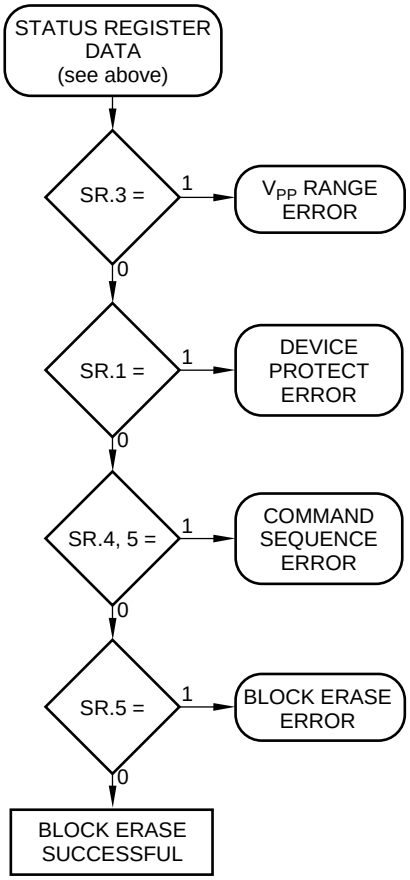
NOTES:

1. Check $\overline{RY}/\overline{BY}$ or SR.7 to determine block erase, byte write, or lock-bit configuration completion. SR.6 - SR.0 are invalid while SR.7 = '0'.
2. If both SR.5 and SR.4 are '1's after a block erase or lock-bit configuration attempt, an improper command sequence was entered.
3. SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Byte Write, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences. SR.3 is not guaranteed to report accurate feedback only when $V_{PP} = V_{PPH1/2/3}$.
4. SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and $\overline{RP}$ only after Block Erase, Byte Write, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or $\overline{RP}$ is not V_{HH}. Reading the block lock and master lock configuration codes after writing the Read identifier Codes command indicates master and block lock-bit status.
5. SR.0 is reserved for future use and should be masked out when polling the status register.



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Setup	Data = 20H Addr = Within block to be erased
Write	Erase Confirm	Data = D0H Addr = Within block to be erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.1 1 = Device Protect Detect RP = V_{IH} Block Lock-Bit is Set Only required for systems implemening lock-bit configuration
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

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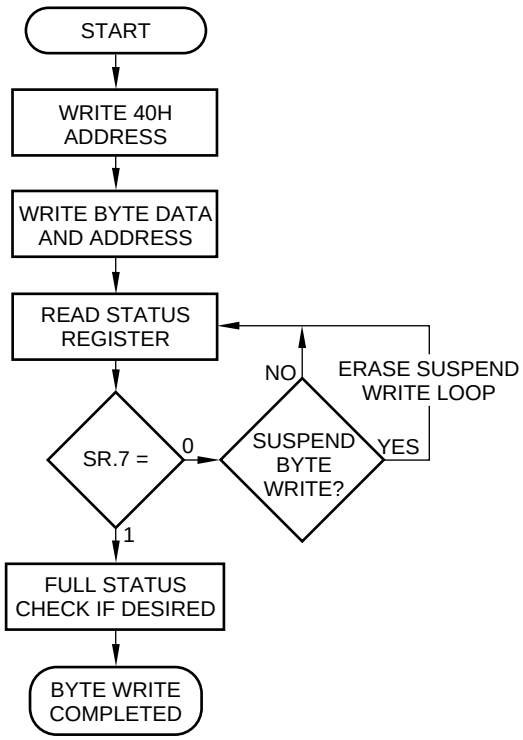
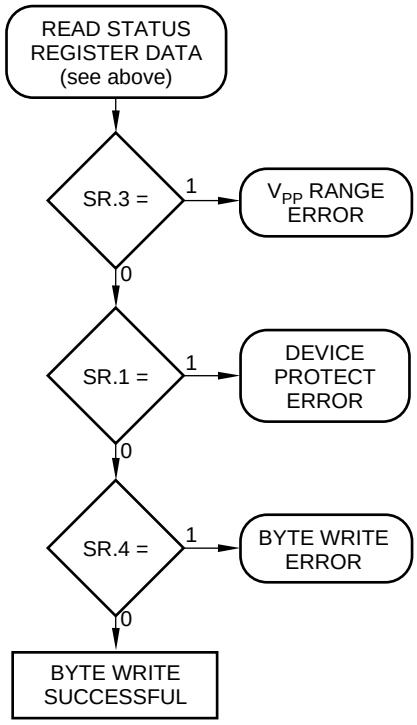
Figure 6. Automated Block Erase Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Setup Byte Write	Data = 40H Addr = Location to be written
Write	Byte Write	Data = Data to be written Addr = Location to be written
Read		Status Register Data
Standy		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent byte writes. SR full status check can be done after each byte write or after a sequence of byte writes. Write FFH after the last byte write operation to place device in read array mode.		

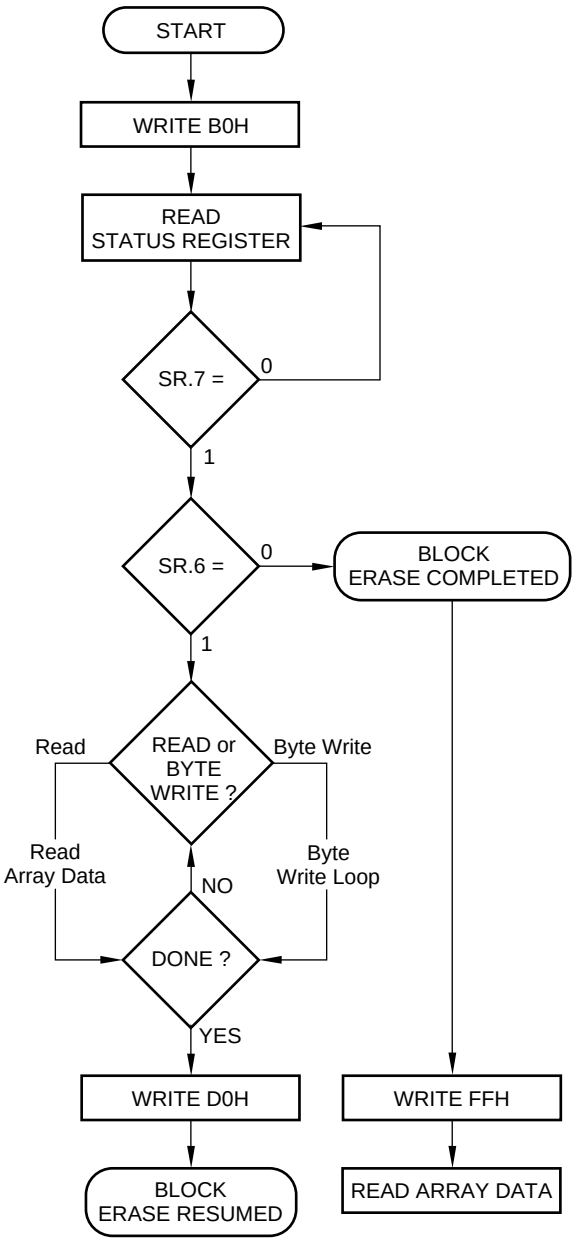
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH} Block Lock-Bit is Set Only required for systems implemening lock-bit configuration
Standby		Check SR.4 1 = Data Write Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

28F008SC-7

Figure 7. Automated Byte Write Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Erase Resume	D = D0H Addr = X

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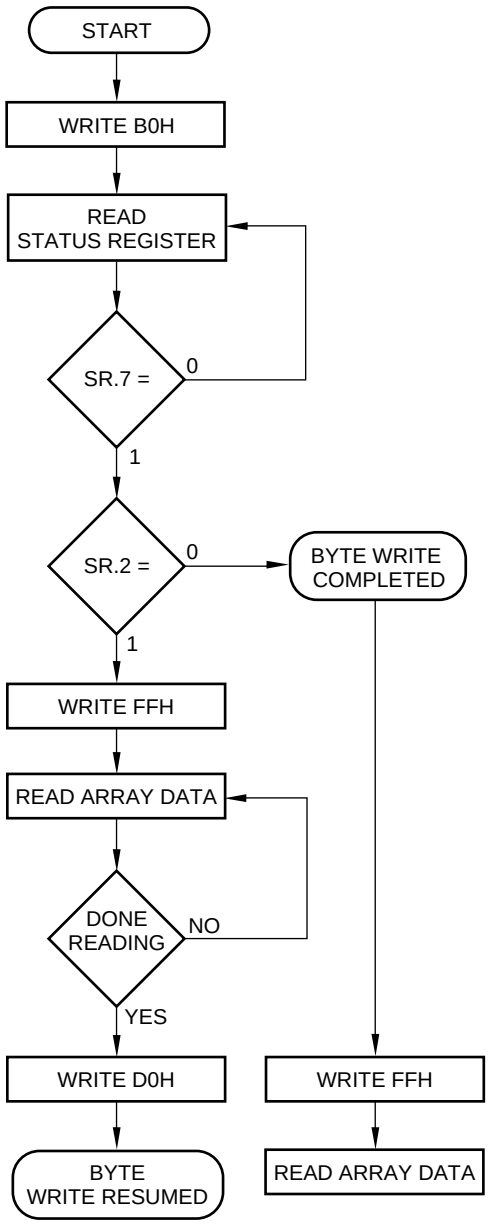
Figure 7. Block Erase Suspend/Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Byte Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Byte Write Suspended 0 = Byte Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array locations other than that being written.
Write	Byte Write Resume	Data = D0H Addr = X

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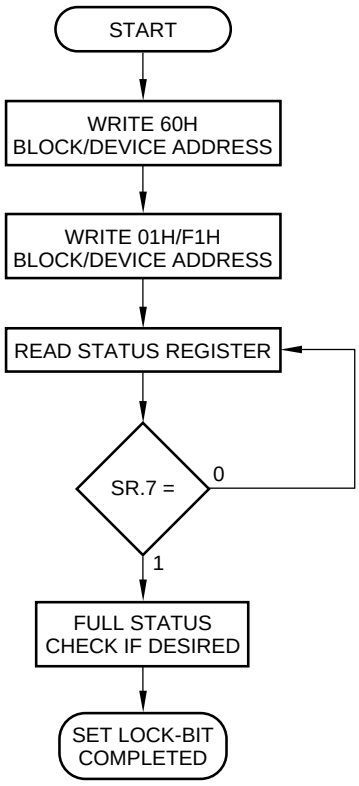
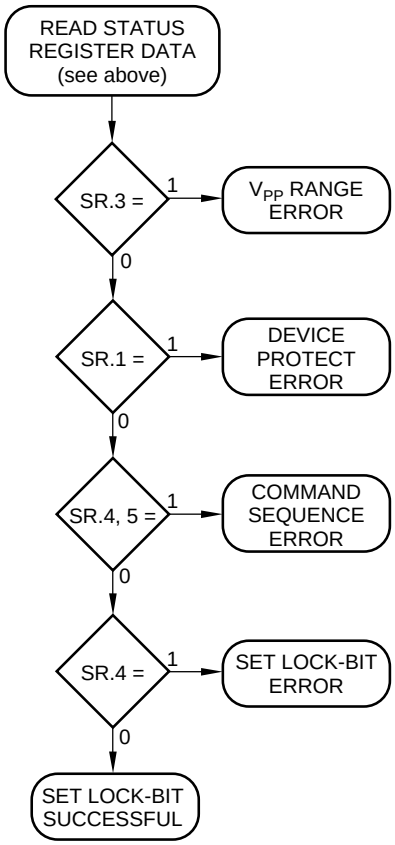
Figure 9. Byte Write Suspend/Resume Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Set Block/Master Lock-Bit Setup	Data = 60H Addr = Block Address (Block), Device Address (Master)
Write	Set Block or Master Lock-Bit Confirm	Data = 01H (Block) F1H (Master) Addr = Block Address (Block), Device Address (Master)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent lock-bit set operations. Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations. Write FFH after the last lock-bit set operation to place device in read array mode.		

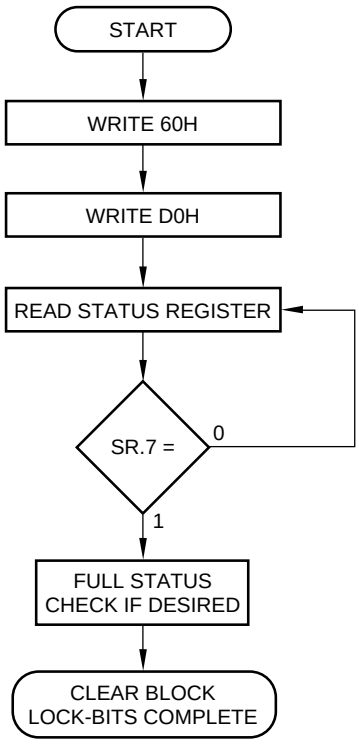
FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH} (Set Master Lock-Bit Operation) RP = V_{IH}, Master Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked. If error is detected clear the Status Register before attempting retry or other error recovery.		

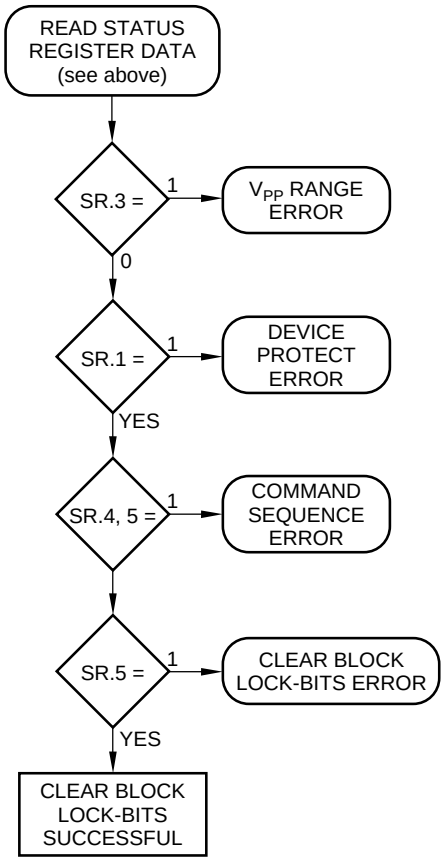
28F008SC-10

Figure 10. Set Block and Master Lock-Bit Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect $\overline{RP}$ = V_{IH}, Master Lock-Bit is Set
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bit Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attemping retry or other error recovery.		

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Figure 11. Clear Block Lock-Bits Flowchart

DESIGN CONSIDERATIONS

Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- Lowest possible memory power dissipation
- Complete assurance that data bus contention will not occur.

To use these control input efficiently, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. $\overline{RP}$ should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

$\overline{RY}/\overline{BY}$ and Block Erase, Byte Write, and Lock-Bit Configuration Polling

$\overline{RY}/\overline{BY}$ is a full CMOS output that provides a hardware method of detecting block erase, byte write and block-bit configuration completion. It transitions low after lock erase, byte write, or lock-bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

$\overline{RY}/\overline{BY}$ can be connected to an interrupt input of the system CPU or controller. It is active at all times. $\overline{RY}/\overline{BY}$ is also V_{OH} when the device is in block erase suspend (with byte write inactive), byte write suspend or deep power-down modes.

Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of $\overline{CE}$ and $\overline{OE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{CC}, V_{PP}, $\overline{RP}$ Transitions

Block erase, byte write and lock-bit configuration are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2/3}$ range, V_{CC} falls outside of a valid $V_{CC1/2/3}$ range, or $\overline{RP} \neq V_{IH}$ or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to '1' along with SR.4 or SR.5, depending on the attempted operation. If $\overline{RP}$ transitions to V_{IL} during block erase, byte write, or lock-bit configuration, $\overline{RY}/\overline{BY}$ will remain low until the reset operation is complete. Then, the opration will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or $\overline{RP}$ transiitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase, byte write, or lock-bit configuration, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, byte writing, or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence archiecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while $\overline{RP} = V_{IL}$ regardless of its control inputs state.

Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering $\overline{RP}$ to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after $\overline{RP}$ is first raised to V_{IH}. See AC Characteristics - Read Only and Write Operations and Figures 16 and 17 for more information.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Commercial Operating Temperature
during Read, Block Erase, Byte Write,
and Lock-Bit Configuration ..... 0°C to +70°C[1]

Temperature under Bias ..... -10°C to +80°C

Storage Temperature: ..... 65°C to +125°C

Voltage On Any Pin
(except V_{CC}, V_{PP} and $\overline{RP}$) ..... -2 V to +7.0 V[2]

V_{CC} Supply Voltage ..... -2.0 V to +7.0 V[2]

V_{PP} Update Voltage during Block Erase,
Byte Write,and Lock-Bit
Configuration ..... -2.0 V to +14.0 V[2, 3]

$\overline{RP}$ Voltage with Respect to GND
during Lock-Bit Configuration
Operations ..... -2.0 V to +14.0 V[2, 3]

Output Short Circuit Current ..... 100 mA[4]

NOTICE: This datasheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Veryify with your local SHARP sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} + 5.0 V which, during transitions, may overshoot to V_{CC} + 2.0 V for periods < 20 ns.
3. Maximum DC voltage on V_{PP} and $\overline{RP}$ may overshoot to +14.0 V for periods < 20 ns.
4. Output shorted for no more than on second. No more than one output shorted at a time.

Operating Conditions

Temperature and V_{CC} Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITION
T_A	Operating Temperature	0	+70	°C	Ambient Temperature
V_{CC}^1	V_{CC} Supply Voltage (3.3 V ± 0.3 V)	3.0	3.6	V	
V_{CC}^2	V_{CC} Supply Voltage (5 V ± 5%)	4.75	5.25	V	
V_{CC}^3	V_{CC} Supply Voltage (5 V ± 10%)	4.50	5.50	V	

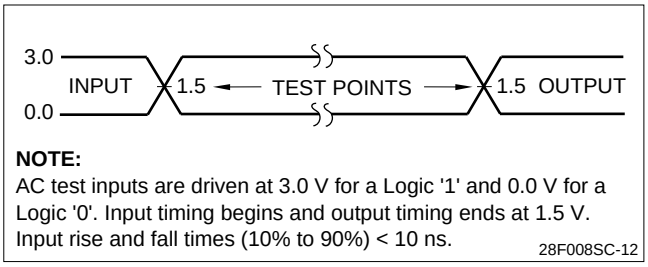
Capacitance

T_A = +25°C, f = 1 MHz

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	CONDITIONS
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

NOTE:
1. Sampled, not 100% tested.

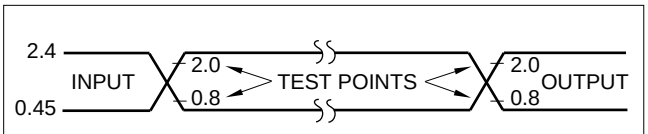
AC INPUT/OUTPUT TEST CONDITIONS



NOTE:
AC test inputs are driven at 3.0 V for a Logic '1' and 0.0 V for a Logic '0'. Input timing begins and output timing ends at 1.5 V. Input rise and fall times (10% to 90%) < 10 ns.

28F008SC-12

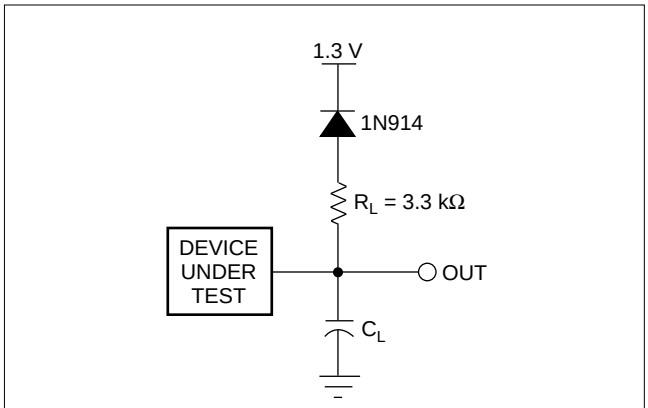
Figure 12. Transient Input/Output Reference Waveform for V_{CC} = 3.3 V ±0.3 V and V_{CC} = 5 V ±5% (High Speed Testing Configuration)



NOTE:
AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic '1' and V_{OL} (0.45 V_{TTL}) for a Logic '0'. Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) < 10 ns.

28F008SC-13

Figure 13. Transient Input/Output Reference Waveform for V_{CC} = 5 V ±10% (Standard Testing Configuration)



NOTE: C_L Includes Jig Capacitance

28F008SC-14

Figure 14. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	C_L (pF)
V_{CC} = 3.3 V ± 0.3 V	50
V_{CC} = 5 V ± 0.5%	30
V_{CC} = 5 V ± 10%	100

DC CHARACTERISTICS

SYM.	PARAMETER	V_{CC} = 3.3 V		V_{CC} = 5 V		UNIT	TEST CONDITIONS	NOTE
		TYP.	MAX.	TYP.	MAX.			
I_{LI}	Input Load Current		±0.5		±1	µA	$V_{CC} = V_{CC}$ MAX., $V_{IN} = V_{CC}$ or GND	1
I_{LO}	Output Leakage Current		±0.5		±10	µA	$V_{CC} = V_{CC}$ MAX., $V_{OUT} = V_{CC}$ or GND	1
I_{CCS}	V_{CC} Standby Current		100		100	µA	CMOS Inputs, $V_{CC} = V_{CC}$ MAX. $\overline{CE} = \overline{RP} = V_{CC}$ ±0.2 V	1, 3, 6
			2		2	mA	TTL Inputs, $V_{CC} = V_{CC}$ MAX. $\overline{CE} = \overline{RP} = V_{IH}$	
I_{CCD}	V_{CC} Deep Power-Down Current		10		10	µA	$\overline{RP}$ = GND ±0.2 V I_{OUT} ($\overline{RY}/\overline{BY}$) = 0 mA	1
I_{CCR}	V_{CC} Read Current		12		35	mA	CMOS Inputs $V_{CC} = V_{CC}$ MAX., $\overline{CE}$ = GND, f = 5 MHz (3.3 V), f = 8 MHz (5 V), I_{OUT} = 0 mA	1, 5, 6
			14		50	mA	TTL Inputs, $V_{CC} = V_{CC}$ MAX., $\overline{CE} = V_{IH}$, f = 5 MHz (3.3 V), f = 8 MHz, (5 V) I_{OUT} = 0 mA	
I_{CCW}	V_{CC} Byte Write or Set Lock-Bit Current		17			mA	V_{PP} = 3.3 V ±0.3 V	1, 7
			17		35	mA	V_{PP} = 5.0 V ±10%	
			12		30	mA	V_{PP} = 12.0 V ± 5%	
I_{CCE}	V_{CC} Block Erase or Clear Block Lock-Bits Current		17			mA	V_{PP} = 3.3 V ±0.3 V	1, 7
			17		30	mA	V_{PP} = 5.0 V ±10%	
			12		25	mA	V_{PP} = 12.0 V ±5%	
I_{CCWS} I_{CCES}	V_{CC} Byte Write or Block Erase Suspend Current		6		10	mA	$\overline{CE} = V_{IH}$	1, 2
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current		±15		±15	µA	$V_{PP} \leq V_{CC}$	1
			200		200	µA	$V_{PP} > V_{CC}$	
I_{PPD}	V_{PP} Deep Power-Down Current		5		5	µA	$\overline{RP}$ = GND ± 0.2V	1
I_{PPW}	V_{PP} Byte Write or Set Lock-Bit Current		40			mA	V_{PP} = 3.3 V ± 0.3 V	1, 7
			40		40	mA	V_{PP} = 5.0 V ±10%	
			15		15	mA	V_{PP} = 12.0 V ±5%	
I_{PPE}	V_{PP} Block Erase or Clear Lock-Bit Current		20			mA	V_{PP} = 3.3 V ± 0.3 V	1, 7
			20		20	mA	V_{PP} = 5.0 V ± 105	
			15		15	mA	V_{PP} = 12.0 V ±5%	
I_{PPWS} I_{PPES}	V_{PP} Byte Write or Block Erase Suspend Current		200		200	µA	$V_{PP} = V_{PPH1/2/3}$	1

DC CHARACTERISTICS (Continued)

SYM.	PARAMETER	V_{CC} = 3.3 V		V_{CC} = 5 V		UNIT	TEST CONDITIONS	NOTE
		MIN.	MAX.	MIN.	MAX.			
V_{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	V		7
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V		7
V_{OL}	Output Low Voltage		0.4		0.45	V	V_{CC} = V_{CC} MIN., I_{OL} = 5.8 mA	3, 7
V_{OH}^1	Output High Voltage (TTL)	2.4		2.4		V	V_{CC} = V_{CC} MIN., I_{OH} = 2.5 mA	3, 7
V_{OH}^2	Output High Voltage (CMOS)	0.85 V_{CC}		0.85 V_{CC}		V	V_{CC} = V_{CC} MIN., I_{OH} = 2.5 µA	4, 7
		V_{CC} - 0.4		V_{CC} - 0.4		V	V_{CC} = V_{CC} MIN., I_{OH} = 100 µA	
V_{PPLK}	V_{PP} Lockout during Normal Operations		1.5		1.5	V		
V_{PPH}^1	V_{PP} during Byte Write, Block Erase, or Lock-Bit Operations	3.0	3.6			V		
V_{PPH}^2	V_{PP} during Byte Write, Block Erase, or Lock-Bit Operations	4.5	5.5	4.5	5.5	V		
V_{PPH}^3	V_{PP} during Byte Write, Block Erase, or Lock-Bit Operations	11.4	12.6	11.4	12.6	V		
V_{LKO}	V_{CC} Lockout Voltage	2.0		2.0		V		
V_{HH}	$\overline{RP}$ Unlock Voltage	11.4	12.6	11.4	12.6	V	Set Master Lock-Bit Override Master and Block Lock-Bit	8

NOTES:

1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact SHARP's Application Support Hotline or your local sales office for information about typical specifications.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes $\overline{RY}/\overline{BY}$.
4. Block erases, byte writes, and lock-bit configurations are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (MAX.) and V_{PPH}^1(MIN.), between V_{PPH}^1(MAX.) and V_{PPH}^2 (MIN.), between V_{PPH}^2 (MAX.) and V_{PPH}^3 (MIN.), and above V_{PPH}^3 (MAX.).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 1mA at 5 V V_{CC} and 3 mA at 3.3 V V_{CC} in static operation.
6. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, but not 100% tested.
8. Master lock-bit set operations are inhibited when $\overline{RP}$ = V_{IH}. Block lock-bit configuration operations are inhibited when the master lock bit is set and $\overline{RP}$ = V_{IH}. Block erases and byte writes are inhibited when the corresponding block-lock bit is set and $\overline{RP}$ = V_{IH}. Block erase, byte write, and lock-bit configuration operations are not guaranteed with $V_{IH} < \overline{RP} < V_{HH}$.

AC CHARACTERISTICS - Read Only Operations[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LH28F008SC-120		LH28F008SC-150		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Read Cycle Time	120		150		ns	
t_{AVQV}	Address to Output Delay		120		150	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		120		150	ns	2
t_{PHQV}	$\overline{RP}$ High to Output Delay		600		600	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		50		55	ns	2
t_{ELQX}	$\overline{CE}$ to Output in Low Z	0		0		ns	3
t_{EHQZ}	$\overline{CE}$ High to Output in High Z		55		55	ns	3
t_{GLQX}	$\overline{CE}$ to Output in Low Z	0		0		ns	3
t_{GHQZ}	$\overline{OE}$ High to Output in High Z		20		25	ns	3
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ change, whichever is first	0		0		ns	3

V_{CC} = 5 V ± 0.5 V, 5 V ± 0.25 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LH28F00SC-85[5] V_{CC} ± 5%		LH28F00SC-90[6] V_{CC} ± 10%		LH28F00SA-120[6] V_{CC} ± 10%		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Read Cycle Time	85		90		120		ns	
t_{AVQV}	Address to Output Delay		85		90		120	ns	
t_{ELQV}	$\overline{CE}$ to Output Delay		85		90		120	ns	2
t_{PHQV}	$\overline{RP}$ High to Output Delay		400		400		400	ns	
t_{GLQV}	$\overline{OE}$ to Output Delay		40		45		50	ns	2
t_{ELQX}	$\overline{CE}$ to Output in Low Z	0		0		0		ns	3
t_{EHQZ}	$\overline{CE}$ High to Output in High Z		55		55		55	ns	3
t_{GLQX}	$\overline{CE}$ to Output in Low Z	0		0		0		ns	3
t_{GHQZ}	$\overline{OE}$ High to Output in High Z		10		10		15	ns	3
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ change, whichever is first	0		0		0		ns	3

NOTES:
1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. $\overline{OE}$ may be delayed to to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{CE}$ without inpact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).
5. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Speed Configuration) for testing characteristics.
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.

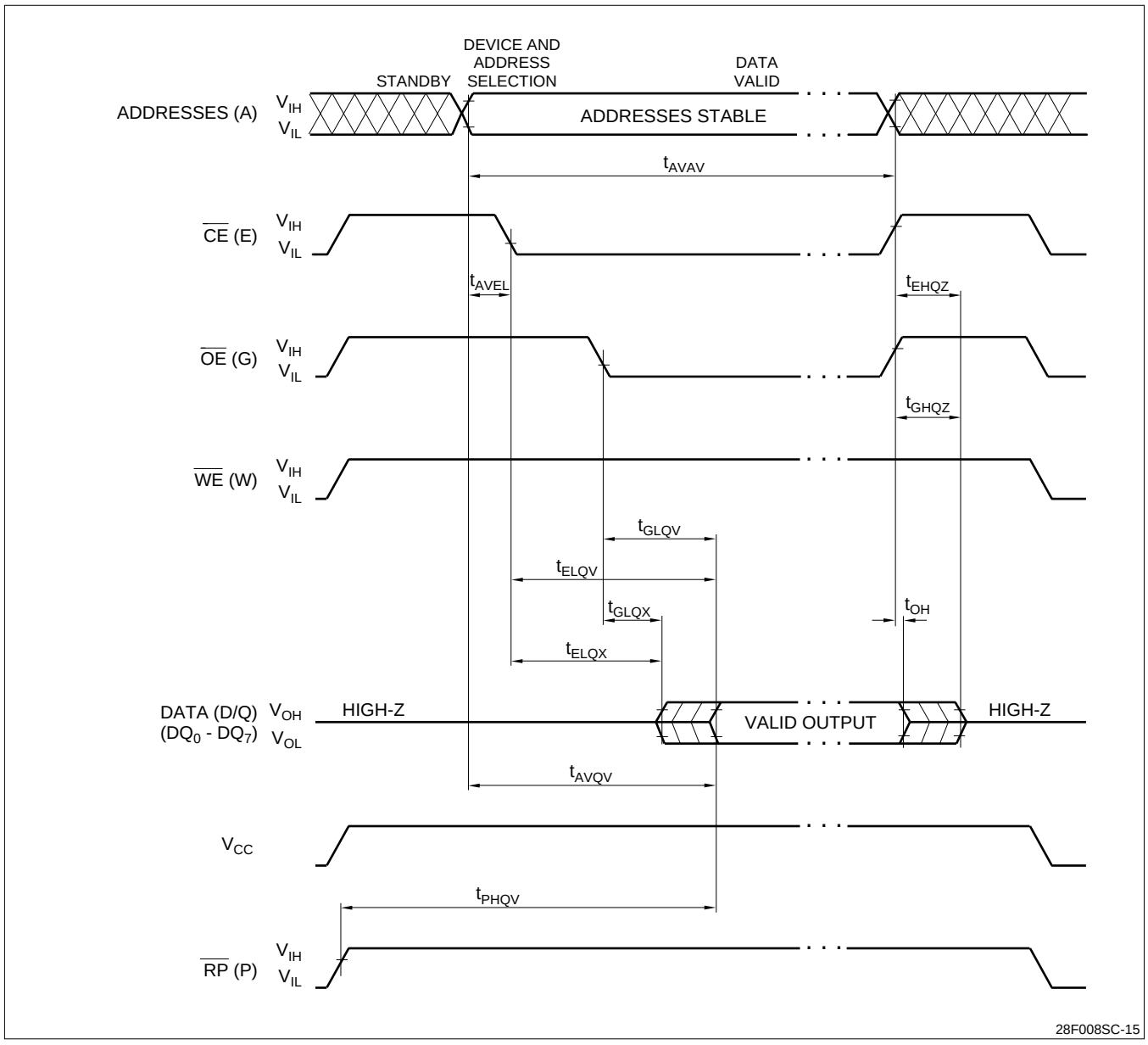


Figure 15. AC Waveforms for Read Operations

AC CHARACTERISTICS - Write Operations[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LH28F008SC-120		LH28F008SC-150		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	120		150		ns	
t_{PHWL}	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	1		1		µs	2
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low	10		10		ns	
t_{WLWH}	$\overline{WE}$ Pulse Width	50		50		ns	
t_{PHHWH}	$\overline{RP}$ V_{HH} Setup to $\overline{WE}$ Going High	100		100		ns	2
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High	100		100		ns	2
t_{AVWH}	Address Setup to $\overline{WE}$ Going High	50		50		ns	3
t_{DVWH}	Data Setup to $\overline{WE}$ Going High	50		50		ns	3
t_{WHDX}	Data Hold from $\overline{WE}$ High	5		5		ns	
t_{WHAX}	Address Hold from $\overline{WE}$ High	5		5		ns	
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High	10		10		ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High	30		30		ns	
t_{WHRL}	$\overline{WE}$ High to $\overline{RY}/\overline{BY}$ Going Low		100		100	ns	
t_{WHGL}	Write Recovery before Read	0		0		ns	
t_{QVVL}	V_{PP} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0		ns	2, 4
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0		ns	2, 4

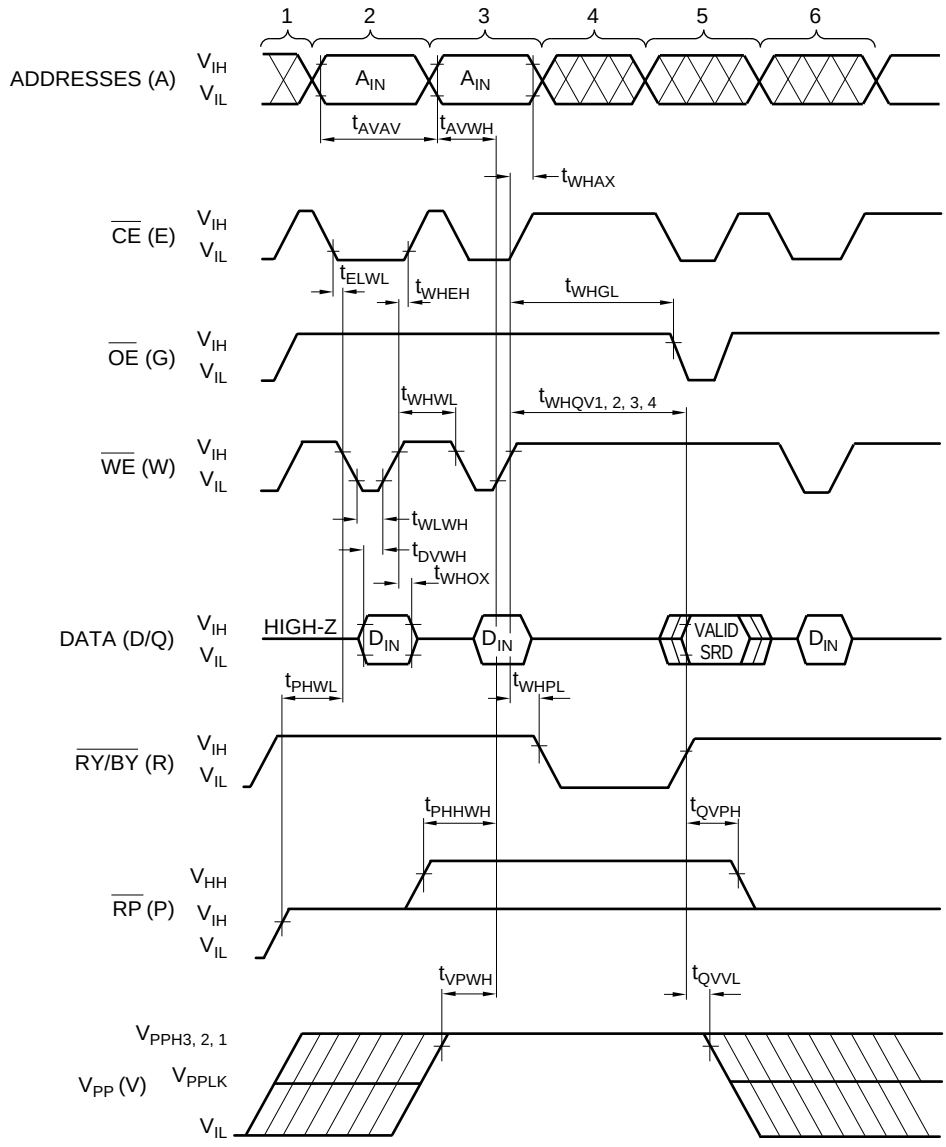
NOTE:
1. See 5 V V_{CC} AC Characteristics - Write Operations for Notes 1 through 5.

AC CHARACTERISTICS - Write Operations[1]

V_{CC} = 5 V ± 0.5 V, 5 V ± 0.25 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LH28F008SC-85[6]		LH28F008SC-90[7]		LH28F008SC-120[8]		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	85		90			120	ns	
t_{PHWL}	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	1		1			1	µs	2
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low	10		10			10	ns	
t_{WLWH}	$\overline{WE}$ Pulse Width	40		40			40	ns	
t_{PHHWH}	$\overline{RP}$ V_{HH} Setup to $\overline{WE}$ Going High	100		100			100	ns	2
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High	100		100			100	ns	2
t_{AVWH}	Address Setup to $\overline{WE}$ Going High	40		40			40	ns	3
t_{DVWH}	Data Setup to $\overline{WE}$ Going High	40		40			40	ns	3
t_{WHDX}	Data Hold from $\overline{WE}$ High	5		5			5	ns	
t_{WHAX}	Address Hold from $\overline{WE}$ High	5		5			5	ns	
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High	10		10			10	ns	
t_{WHWL}	$\overline{WE}$ Pulse Width High	30		30			30	ns	
t_{WHRL}	$\overline{WE}$ High to $\overline{RY}/\overline{BY}$ Going Low		90		90			ns	
t_{WHGL}	Write Recovery before Read	0		0			0	ns	
t_{QVVL}	V_{PP} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0			0	ns	2, 4
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0			0	ns	2, 4

NOTES:
1. Read timing characteristics during block erase, byte write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Command Definitions Table for valid A_{IN} and D_{IN} for block erase, byte write, or lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary $\overline{RP}$ should be held at V_{HH}) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5 = 0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characters.



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or byte write set-up.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

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Figure 16. AC Waveforms for $\overline{WE}$ Controlled Write Operations

ALTERNATIVE $\overline{CE}$ - Controlled Writes[1]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LH28F008SC-120		LH28F008SC-150		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	120		150		ns	
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	1		1		µs	2
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$# Going Low	0		0		ns	
t_{ELEH}	$\overline{CE}$ Pulse Width	70		70		ns	
t_{PHHEH}	$\overline{RP}$ V_{HH} Setup to $\overline{CE}$ Going High	100		100		ns	2
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going High	100		100		ns	2
t_{AVEH}	Address Setup to $\overline{CE}$ Going High	50		50		ns	3
t_{DVEH}	Data Setup to $\overline{CE}$ Going High	50		50		ns	3
t_{EHDX}	Data Hold from $\overline{CE}$ High	5		5		ns	
t_{EHAX}	Address Hold from $\overline{CE}$ High	5		5		ns	
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High	0		0		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width High	25		25		ns	
t_{EHRL}	$\overline{CE}$ High to $\overline{RY}/\overline{BY}$ Going Low		100		100	ns	
t_{EHGL}	Write Recovery before Read	0		0		µs	
t_{QVVL}	V_{PP} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0		ns	2, 4
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0		ns	2, 4

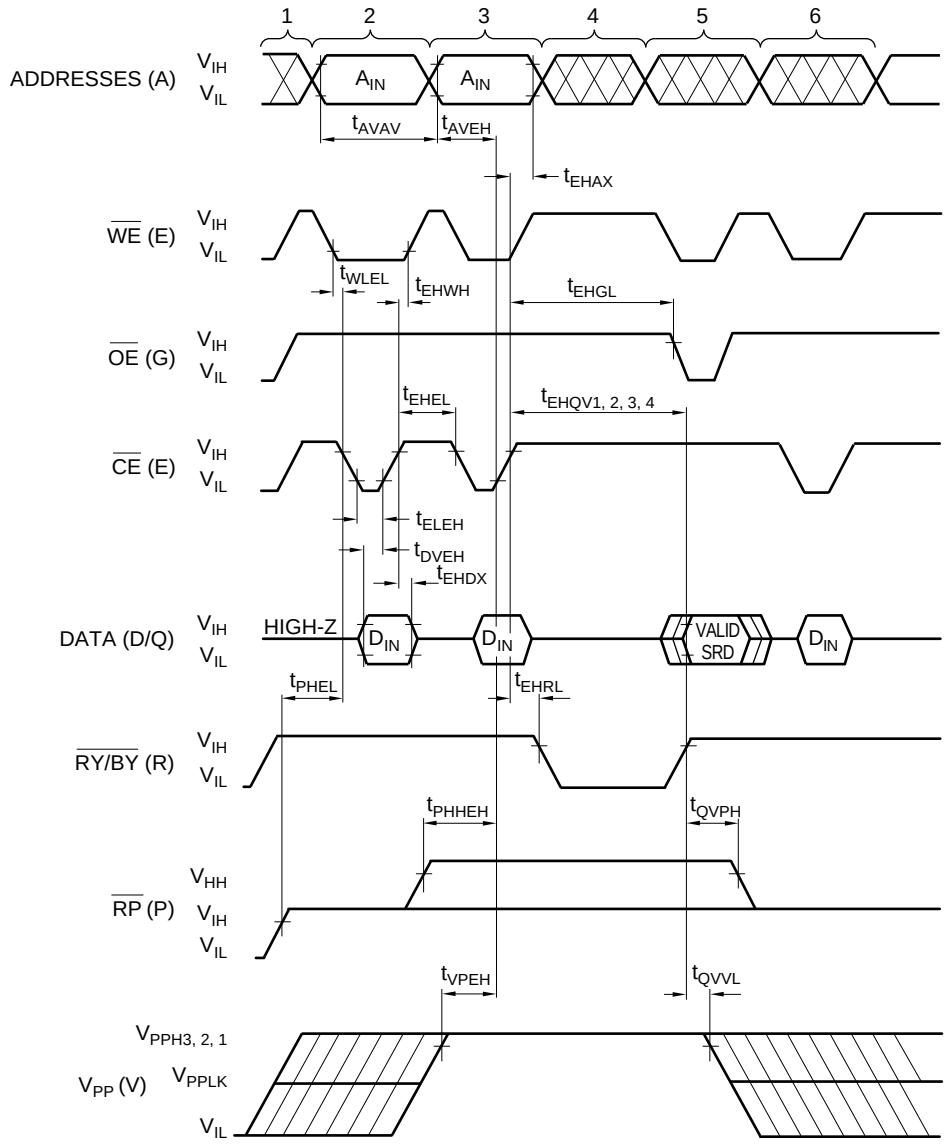
NOTE:
1. See 5 V V_{CC} Alternative $\overline{CE}$ Controlled Writes for Notes 1 through 5.

ALTERNATIVE $\overline{CE}$ - Controlled Writes[1] (Continued)

V_{CC} = 5 V ± 0.5 V, 5 V ± 0.25 V, TA = 0°C to +70°C

SYMBOL	PARAMETER	LH28F008SC-85[6]		LH28F008SC-90[7]		LH28F008SC-120[7]		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AVAV}	Write Cycle Time	85		90		120		ns	
t_{PHEL}	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	1		1		1		µs	2
t_{WLEL}	$\overline{WE}$ Setup to $\overline{CE}$ Going Low	0		0		0		ns	
t_{ELEH}	$\overline{CE}$ Pulse Width	50		50		50		ns	
t_{PHHEH}	$\overline{RP}$ V_{HH} Setup to $\overline{CE}$ Going High	100		100		100		ns	2
t_{VPEH}	V_{PP} Setup to $\overline{CE}$ Going High	100		100		100		ns	2
t_{AVEH}	Address Setup to $\overline{CE}$ Going High	40		40		40		ns	3
t_{DVEH}	Data Setup to $\overline{CE}$ Going High	40		40		40		ns	3
t_{EHDX}	Data Hold from $\overline{CE}$ High	5		5		5		ns	
t_{EHAX}	Address Hold from $\overline{CE}$ High	5		5		5		ns	
t_{EHWH}	$\overline{WE}$ Hold from $\overline{CE}$ High	0		0		0		ns	
t_{EHEL}	$\overline{CE}$ Pulse Width High	25		25		25		ns	
t_{EHRL}	$\overline{CE}$ High to $\overline{RY}/\overline{BY}$ Going Low		90		90		90	ns	
t_{EHGL}	Write Recovery before Read	0		0		0		µs	
t_{QVVL}	V_{PP} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0		0		ns	2, 4
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	0		0		0		ns	2, 4

NOTES:
1. In systems where $\overline{CE}$ defines the write pulse width (within a longer $\overline{WE}$ timing waveform), all setup, hold, and inactive $\overline{WE}$ times should be measured relative to the $\overline{CE}$ waveform.
2. Sampled, not 100% tested.
3. Refer to Command Definitions Table for valid A_{IN} and D_{IN} for block erase, byte write, or lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ (and if necessary $\overline{RP}$ should be held at V_{HH}) until determination of block erase, byte write, or lock-bit configuration success (SR.1/3/4/5 = 0).
5. See Ordering Information for device speeds (valid operational combinations).
6. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (High Seed Configuration) for testing characteristics.
7. See Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit (Standard Configuration) for testing characteristics.



NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or byte write set-up.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

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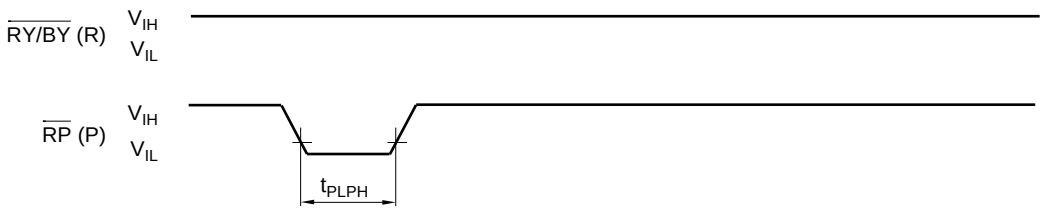
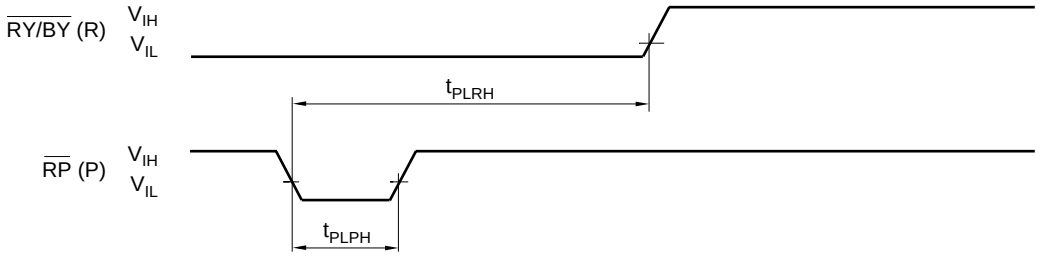
Figure 17. Alternate AC Waveform for $\overline{CE}$ Controlled Write Operations

RESET OPERATIONS



A. Reset During Read Array Mode



B. Reset During Block Erase, Byte Write, or Lock-Bit Configuration

28F008SC-18

Figure 18. AC Waveform for Reset Operation

Reset AC Specifications[1]

SYMBOL	PARAMETER	V_{CC} = 3.3 V		V_{CC} = 5 V		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{PLPH}	$\overline{RP}$ Pulse Low Time (If $\overline{RP}$ is tied to V_{CC}, this specification is not applicable)	100		100		ns	
t_{PLRH}	$\overline{RP}$ Low to Reset during Block Erase, Byte Write, or Lock-Bit Configuration		20		12	µs	2,3

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. If $\overline{RP}$ is asserted while a block erase, byte write, or lock-bit configuration operation is not executing, the reset will complete within 100 ns.
3. A reset time t_{PHQV}, is required from the latter of $\overline{RY}/\overline{BY}$ or $\overline{RP}$ going high until outputs are valid.

BLOCK ERASE, BYTE WRITE AND LOCK-BIT CONFIGURATION PERFORMANCE[3, 4]

V_{CC} = 3.3 V ± 0.3 V, T_A = 0°C to +70°C

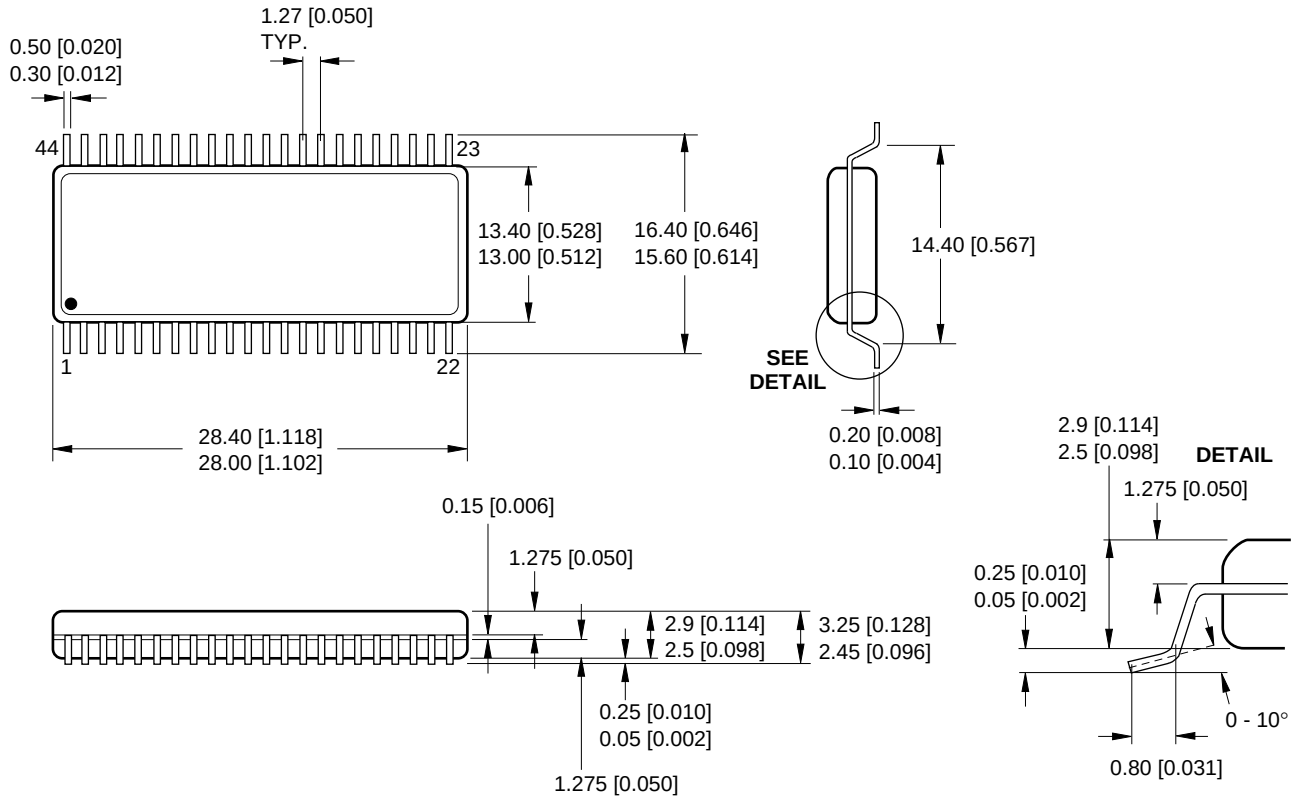
SYM.	PARAMETER	V_{PP} = 3.3 V			V_{PP} = 53 V			V_{PP} = 12 V			UNIT	NOTE
		TYP.[1]	MIN.	MAX.	TYP.[1]	MIN.	MAX.	TYP.[1]	MIN.	MAX.		
t_{WHQV1} t_{EHQV1}	Byte Write Time	17	15	TBD	9.3	8.2	TBD	7.6	6.7	TBD	µs	2
	Block Write Time	1.1	1	TBD	0.6	0.5	TBD	0.5	0.4	TBD	sec	2
t_{WHQV2} t_{EHQV2}	Block Erase Time	1.8	1.5	TBD	1.2	1	TBD	1.1	0.8	TBD	sec	2
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	21	18	TBD	13.3	11.2	TBD	11.6	9.7	TBD	µs	2
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	1.8	1.5	TBD	1.2	1	TBD	1.1	0.8	TBD	sec	2
t_{WHRH1} t_{EHRH1}	Byte Write Suspend Latency Time to Read	6		7	5		7	5		6	µs	
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read	16.2		20	9.6		12	9.6		12	µs	

V_{CC} = 5 V ± 0.5 V, 5 V ± 0.25 V, T_A = 0°C to +70°C

SYM.	PARAMETER	V_{PP} = 53 V			V_{PP} = 12 V			UNIT	NOTE
		TYP.[1]	MIN.	MAX.	TYP.[1]	MIN.	MAX.		
t_{WHQV1} t_{EHQV1}	Byte Write Time	8	6.5	TBD	6	4.8	TBD	µs	2
	Block Write Time	0.5	0.4	TBD	0.4	0.3	TBD	sec	2
t_{WHQV2} t_{EHQV2}	Block Erase Time	1.1	0.9	TBD	1.0	0.3	TBD	sec	2
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time	12	9.5	TBD	10	7.8	TBD	µs	2
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	1.1	0.9	TBD	1.0	0.3	TBD	sec	2
t_{WHRH1} t_{EHRH1}	Byte Write Suspend Latency Time to Read	5		6	4		5	µs	
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read	9.6		12	9.6		12	µs	

NOTES:
1. Typical values measured at T_A = +25°C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

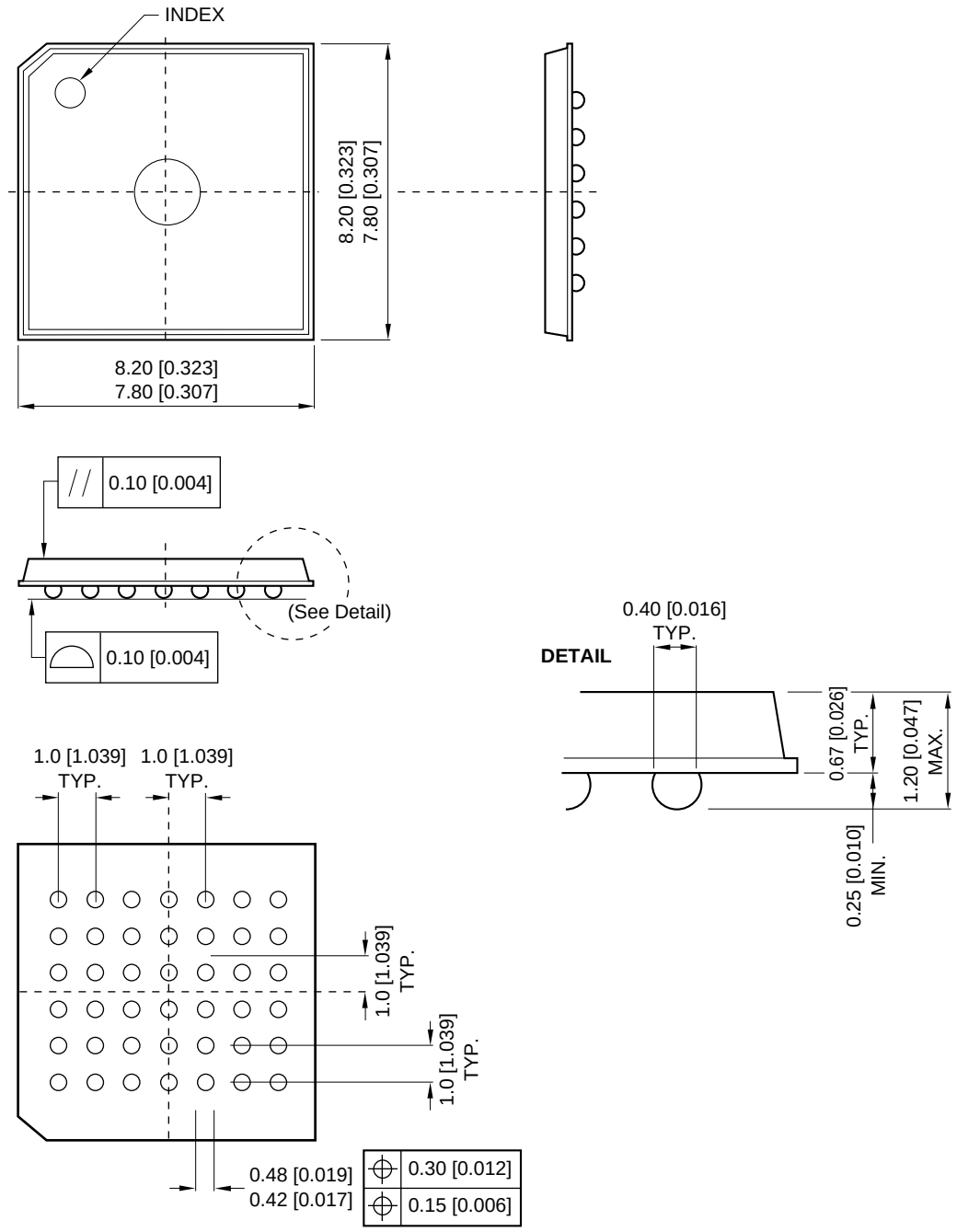
44SOP (SOP044-P-0600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44SOP

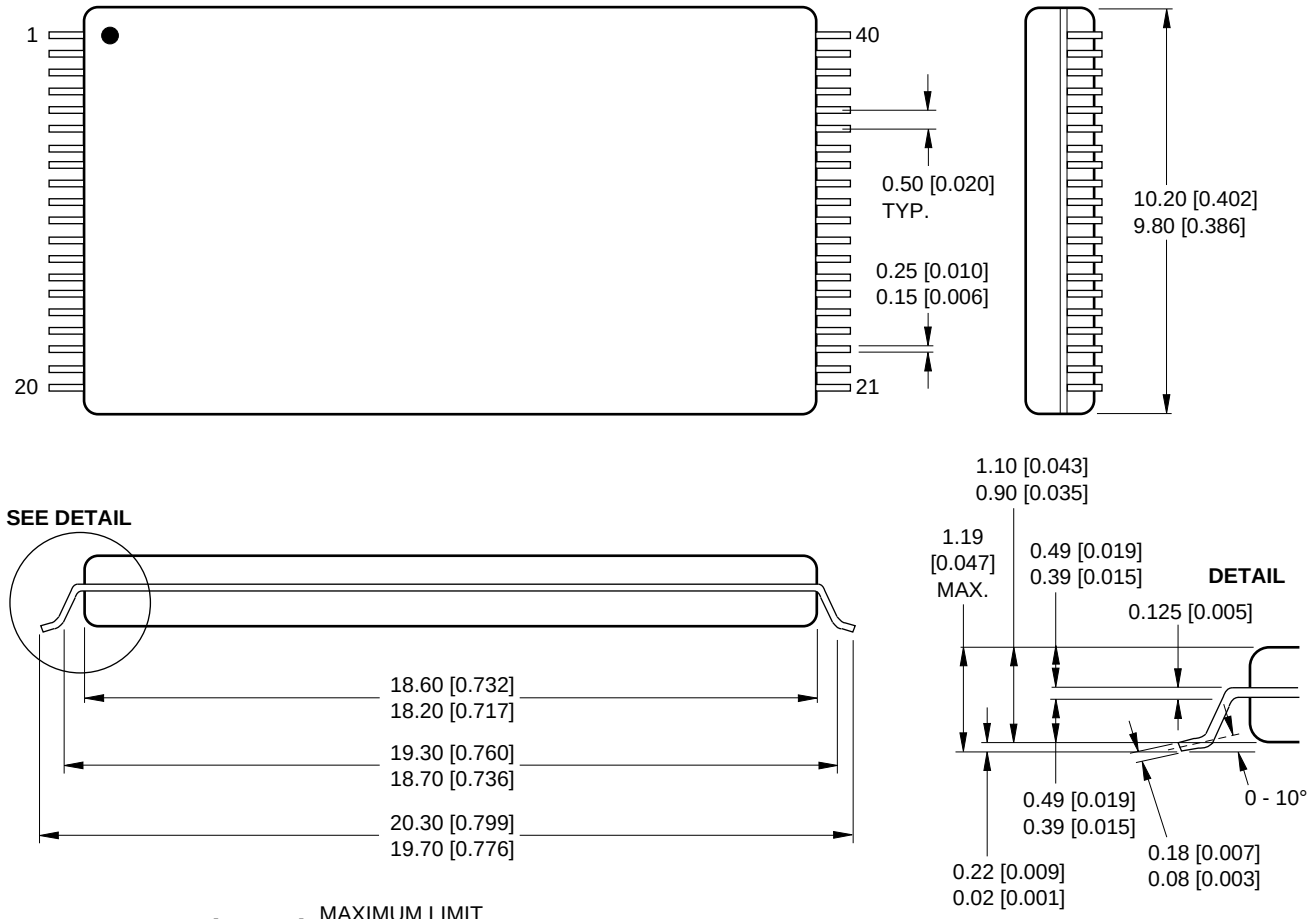
42CSP (CSP042-P-0808)



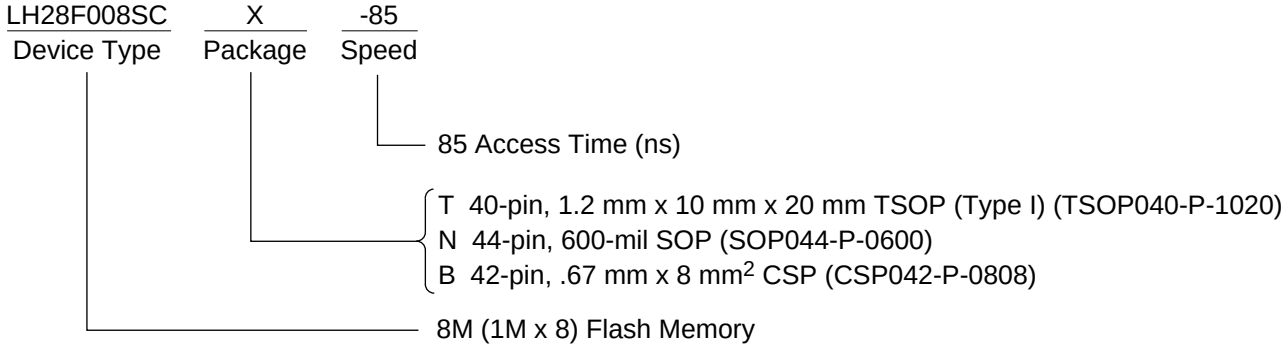
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

42CSP

40TSOP (TSOP040-P-1020)



ORDERING INFORMATION



Example: LH28F008SCT-85 (1M x 8) Flash Memory, 85 ns, 40-pin TSOP)

28F008SC-19

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