

# LH5116S

CMOS 16K (2K × 8) Static RAM

## FEATURES

- 2,048 × 8 bit organization
- Access time: 1000 ns (MAX.)
- Low-power consumption:
  - Operating: 33 mW (MAX.)
  - Standby: 3.3 μW (MAX.)
- Fully-static operation
- Three-state outputs
- Single +3 V power supply
- Package: 24-pin, 450-mil SOP

## DESCRIPTION

The LH5116S is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It operates at a low supply voltage of 3 V ±10%.

## PIN CONNECTIONS

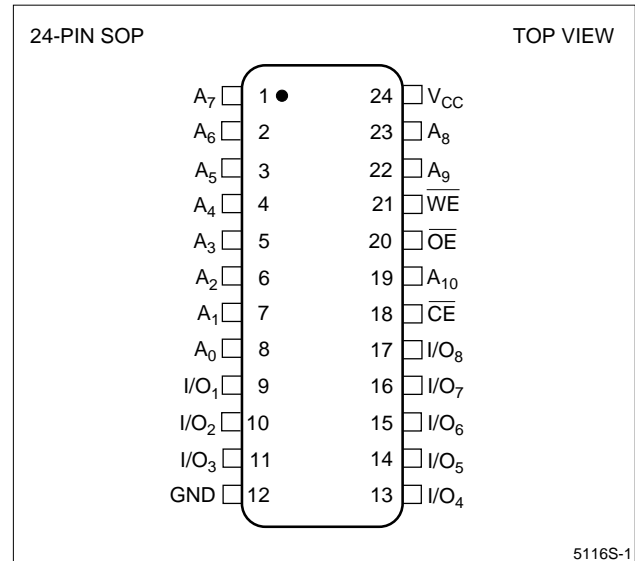


Figure 1. Pin Connections for SOP Package

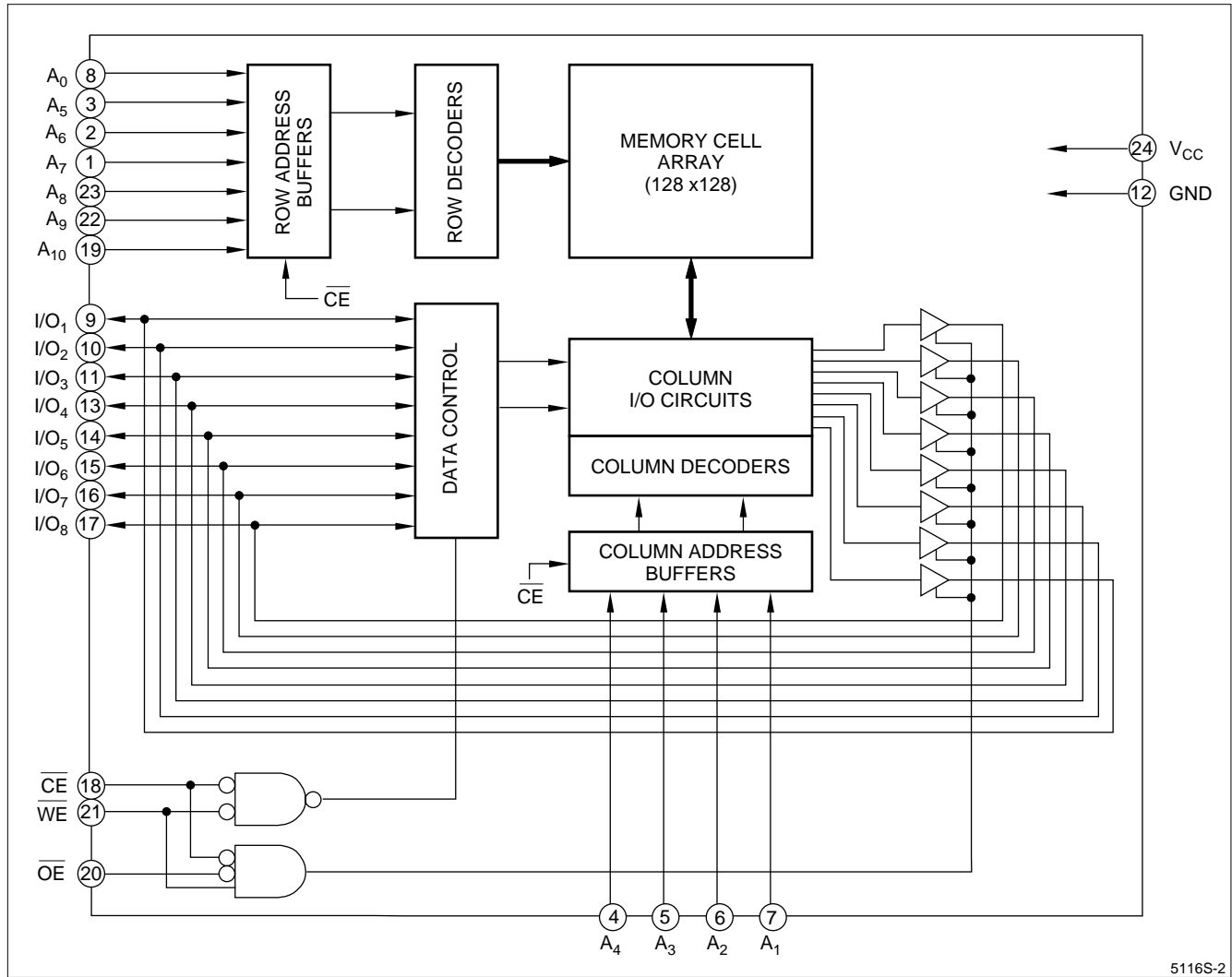


Figure 2. LH5116S Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>10</sub>	Address input
CE	Chip Enable input
OE	Output Enable input
WE	Write Enable input

SIGNAL	PIN NAME
I/O <sub>1</sub> - I/O <sub>8</sub>	Data input/output
V <sub>CC</sub>	Power supply
GND	Ground

**TRUTH TABLE**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
L	X	L	Write	D <sub>IN</sub>	Operating (I <sub>CC</sub> )	1
L	L	H	Read	D <sub>OUT</sub>	Operating (I <sub>CC</sub> )	
H	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
L	H	X	Output disable	High-Z	Operating (I <sub>CC</sub> )	1

**NOTE:**  
 1. X = H or L

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V	1
Operating temperature	T <sub>opr</sub>	0 to +50	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

**NOTE:**

1. The maximum applicable voltage on any pin with respect to GND.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0 to +50°C)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.3	V
Input voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	V
	V <sub>IL</sub>	-0.3		0.8	V

**DC CHARACTERISTICS (V<sub>CC</sub> = 3 V ±10%, T<sub>A</sub> = 0 to +50°C)**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA			0.5	V	
Output 'HIGH' voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> - 0.5			V	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>	-1.0		1.0	μA	
Output leakage current	I <sub>LO</sub>	CE = V <sub>IH</sub> , V <sub>I/O</sub> = 0 V to V <sub>CC</sub>	-1.0		1.0	μA	
Operating current	I <sub>CC1</sub>	Outputs open (OE = V <sub>CC</sub> )		8	10	mA	1
	I <sub>CC2</sub>	Outputs open (OE = V <sub>IH</sub> )		8	10	mA	2
Standby current	I <sub>CCL</sub>	CE ≥ V <sub>CC</sub> - 0.2 V All other input pins = 0 V to V <sub>CC</sub>			1.0	μA	

**NOTES:**

1. CE = 0 V; all other input pins = 0 V to V<sub>CC</sub>
2. CE = V<sub>IL</sub>; all other input pins = V<sub>IL</sub> to V<sub>IH</sub>

**AC CHARACTERISTICS (V<sub>CC</sub> = 3 V ±10%, T<sub>A</sub> = 0 to +50°C)****(1) READ CYCLE**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t <sub>RC</sub>	1000			ns	
Address access time	t <sub>AA</sub>			1000	ns	
Chip enable access time	t <sub>ACE</sub>			1000	ns	
Chip enable Low to output in Low-Z	t <sub>CLZ</sub>	10			ns	1
Output enable access time	t <sub>OE</sub>			100	ns	
Output enable Low to output in Low-Z	t <sub>OLZ</sub>	10			ns	1
Chip disable to output in High-Z	t <sub>CHZ</sub>	0		40	ns	1
Output enable to output in High-Z	t <sub>OHZ</sub>	0		40	ns	1
Output hold time	t <sub>OH</sub>	10			ns	

**NOTE:**

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

**(2) WRITE CYCLE ( $V_{CC} = 3\text{ V} \pm 10\%$ ,  $T_A = 0$  to  $+50^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	$t_{WC}$	1000			ns	
Chip enable to end of write	$t_{CW}$	100			ns	
Address valid time	$t_{AW}$	100			ns	
Address setup time	$t_{AS}$	0			ns	
Write pulse width	$t_{WP}$	100			ns	
Write recovery time	$t_{WR}$	20			ns	
$\overline{WE}$ Low to output in High-Z	$t_{WHZ}$			30	ns	1
Data valid to end of write	$t_{DW}$	50			ns	
Data hold time	$t_{DH}$	20			ns	
Output active from end of write	$t_{OW}$	10			ns	1
Output enable to output in High-Z	$t_{OHZ}$	0		40	ns	1

**NOTE:**

- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 200$  mV transition from steady state levels into the test load.

**AC TEST CONDITIONS**

PARAMETER	MODE	NOTE
Input voltage amplitude	0 to $V_{CC}$	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	$C_L$ (100 pF)	1

**NOTE:**

- Includes scope and jig capacitance.

**DATA RETENTION CHARACTERISTICS ( $T_A = 0$  to  $+50^\circ\text{C}$ )**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	$V_{CCDR}$	$CE \geq V_{CCDR} - 0.2\text{ V}$	2.0			V	
Data retention current	$I_{CCDR}$	$CE \geq V_{CCDR} - 0.2\text{ V}$ , $V_{CCDR} = 2.0\text{ V}$			1.0 0.2	$\mu\text{A}$	1
Chip disable to data retention	$t_{CDR}$		0			ns	
Recovery time	$t_R$		$t_{RC}$			ns	2

**NOTES:**

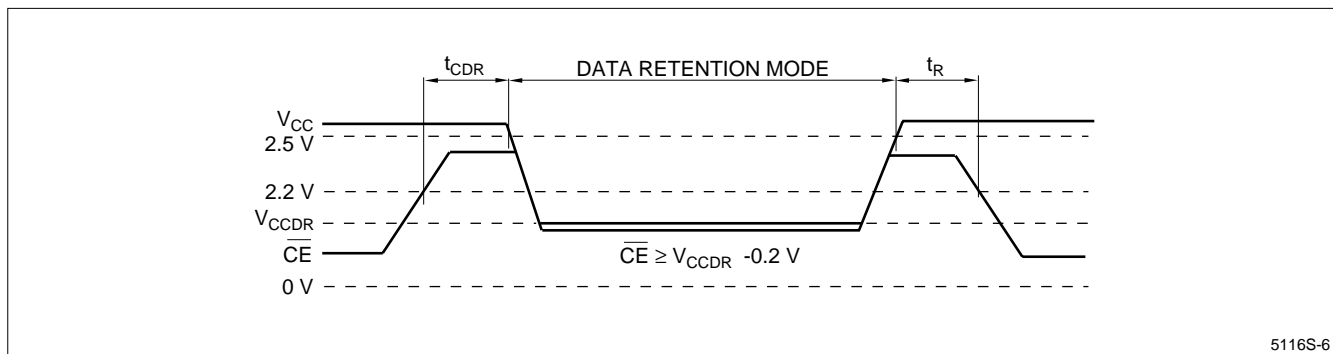
- $T_A = 25^\circ\text{C}$
- $t_{RC}$  = Read cycle time

**CAPACITANCE <sup>1</sup> ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

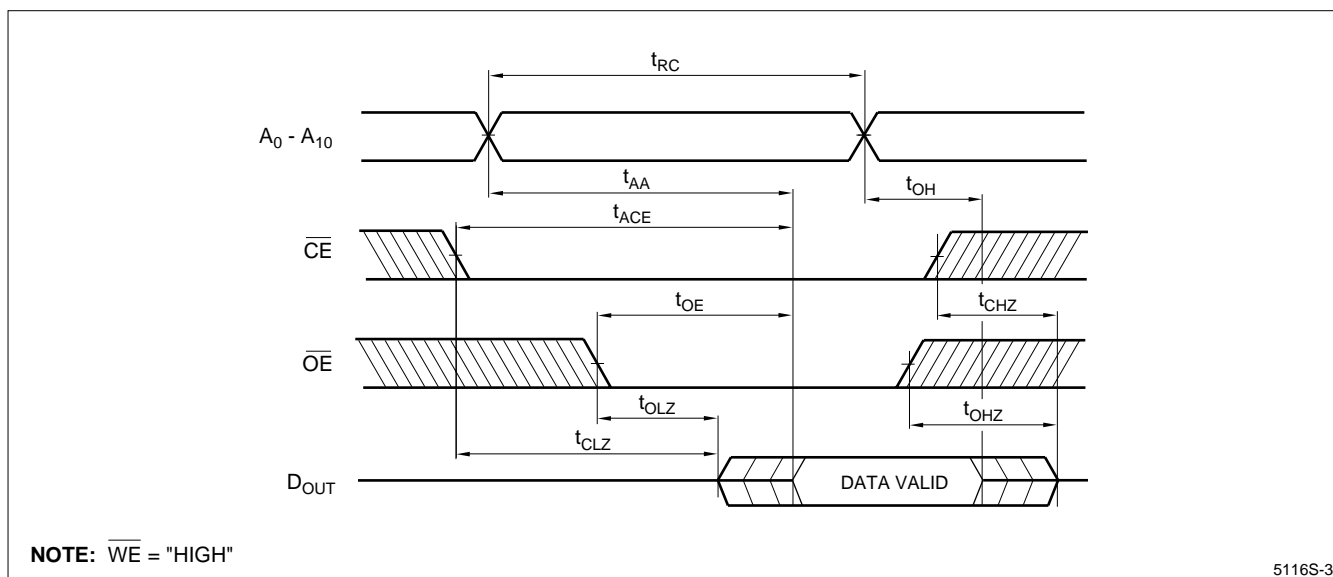
**NOTE:**

- This parameter is sampled and not production tested.



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Figure 3. Low Voltage Data Retention



NOTE:  $\overline{WE}$  = "HIGH"

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Figure 4. Read Cycle

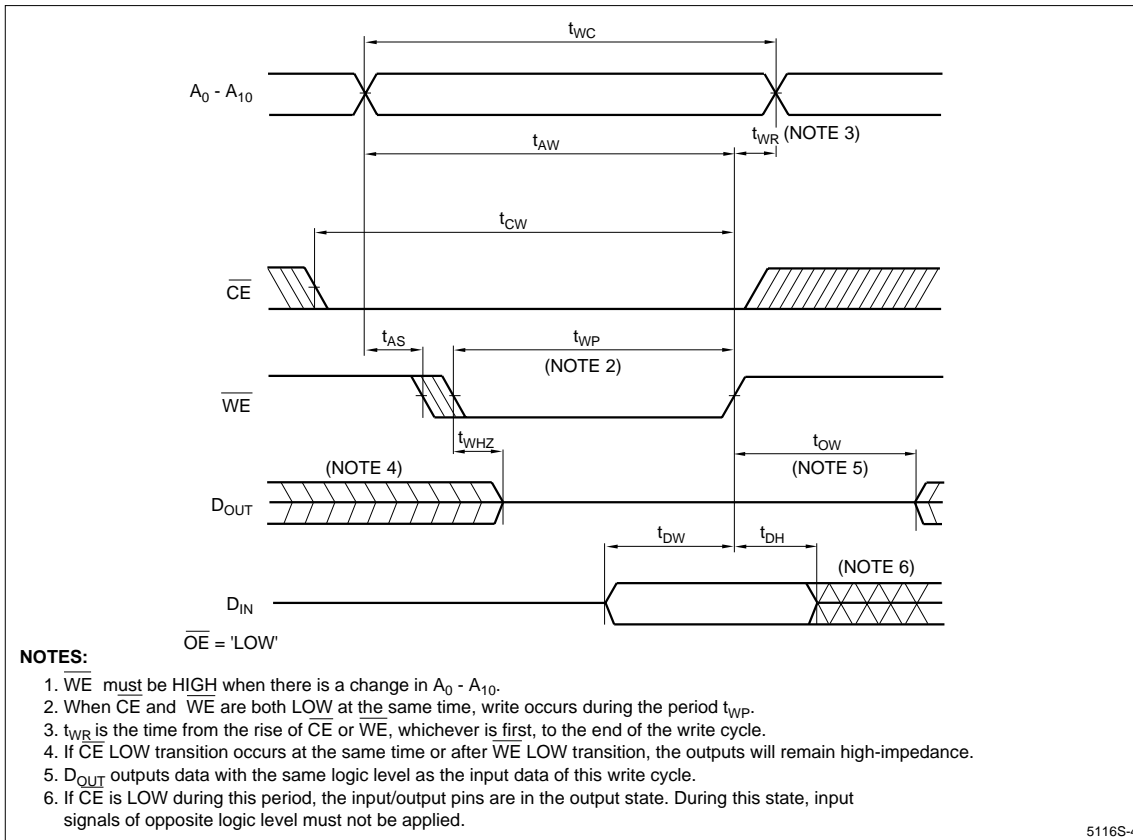


Figure 5. Write Cycle 1 (Note 1)

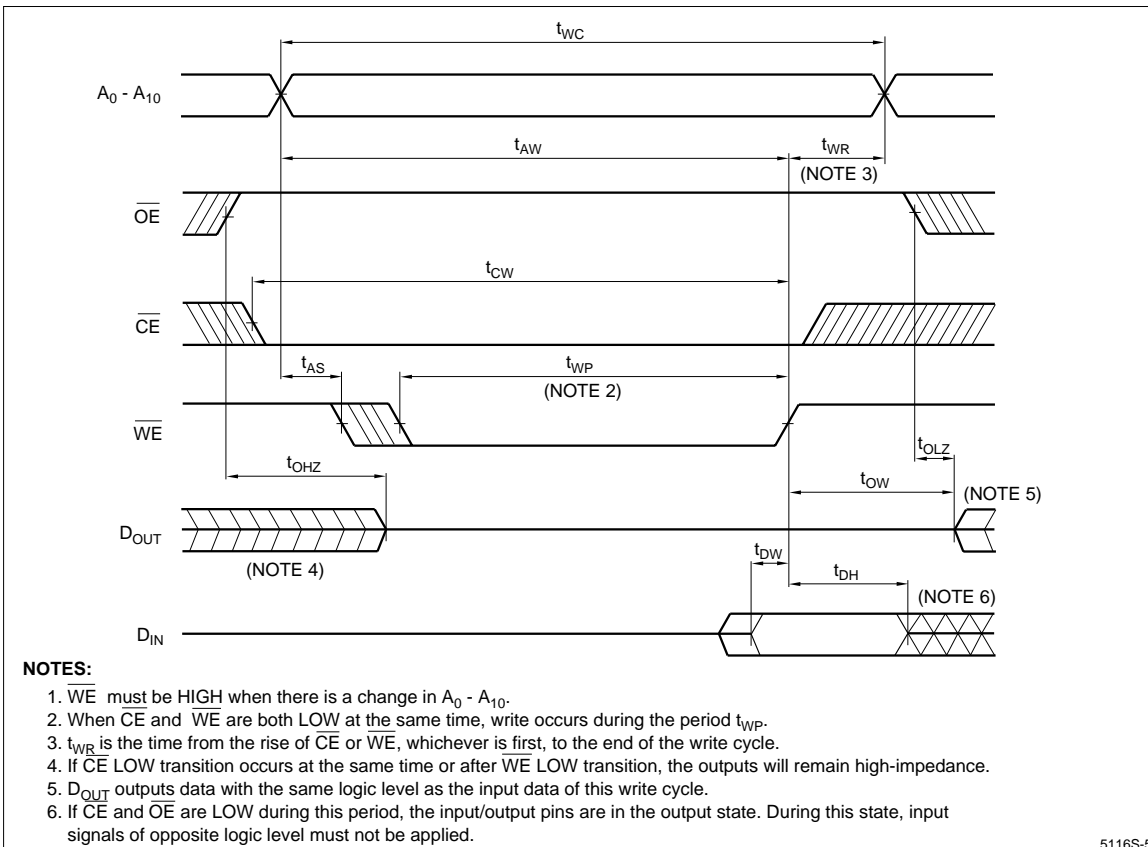
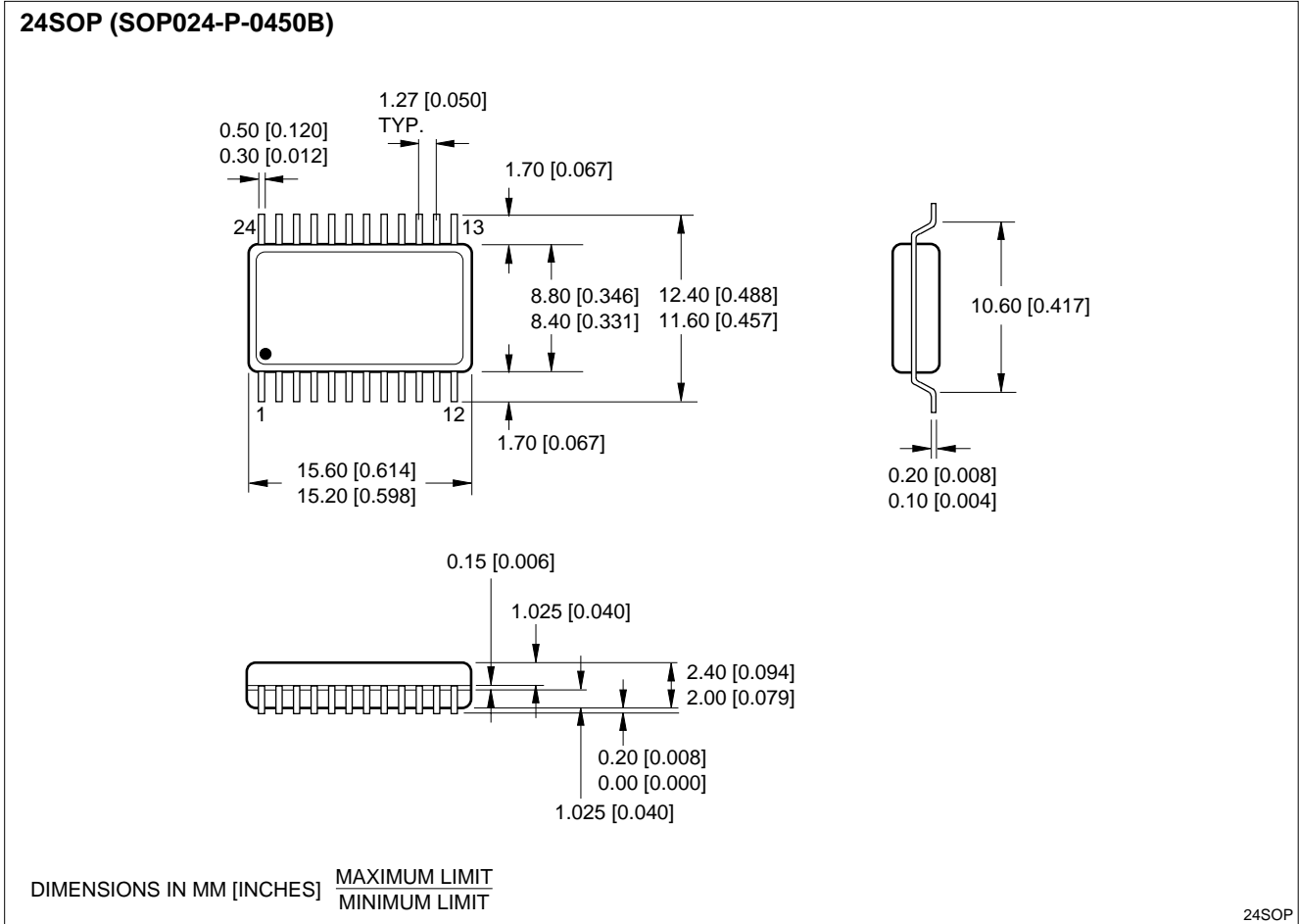


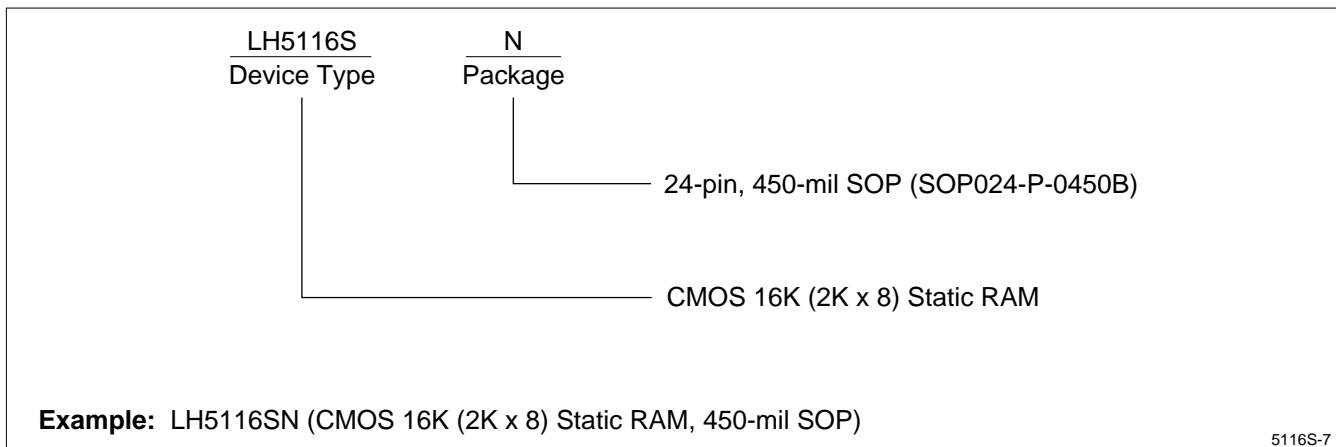
Figure 6. Write Cycle 2 (Note 1)

PACKAGE DIAGRAM



24-pin, 450-mil SOP

ORDERING INFORMATION



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