

LH5164ASH

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access time: 500 ns (MAX.)
- Power consumption:
 - Operating:
 - 60 mW (MAX.) @ 3 V
 - Standby:
 - 3 μW (MAX.) @ 70°C @ 3 V
 - 9 μW (MAX.) @ 85°C @ 3 V
- Fully-static operation
- Three-state outputs
- Wide operating voltage range:
 - 2.5 V to 5.5 V
- TTL compatible I/O
- Wide temp. range
 - t_{OPR}: -40 to +85°C
- Packages:
 - 28-pin, 450-mil SOP
 - 28-pin, 8 × 13 mm² TSOP (Type I)

DESCRIPTION

The LH5164ASH is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

It is designed for 2.5 to 5.5 V low voltage operation and wide temperature range from -40 to +85°C.

PIN CONNECTIONS

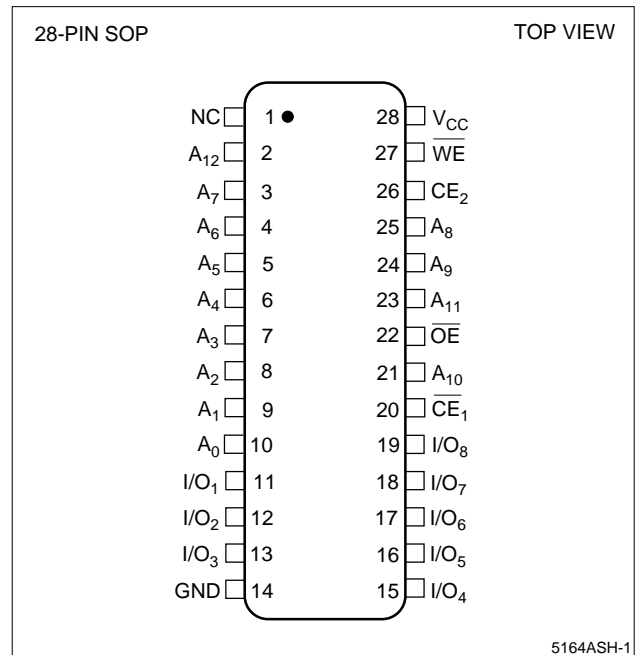


Figure 1. Pin Connections for SOP Package

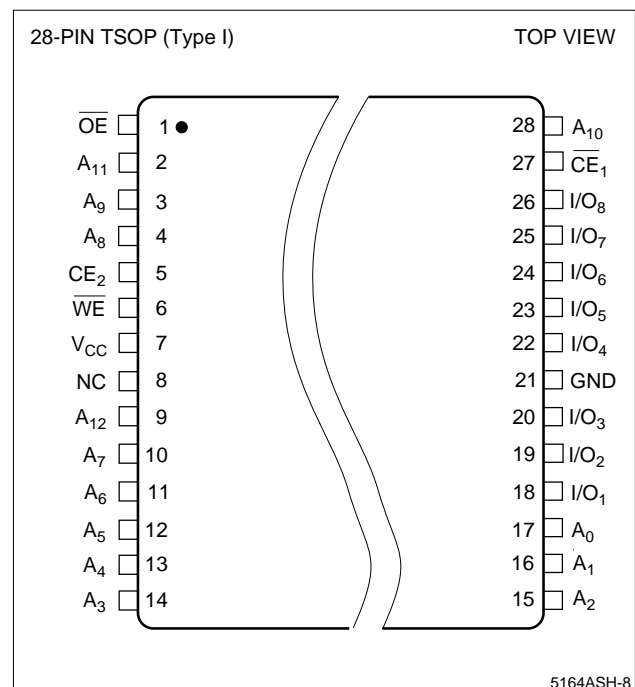


Figure 2. Pin Connections for TSOP Package

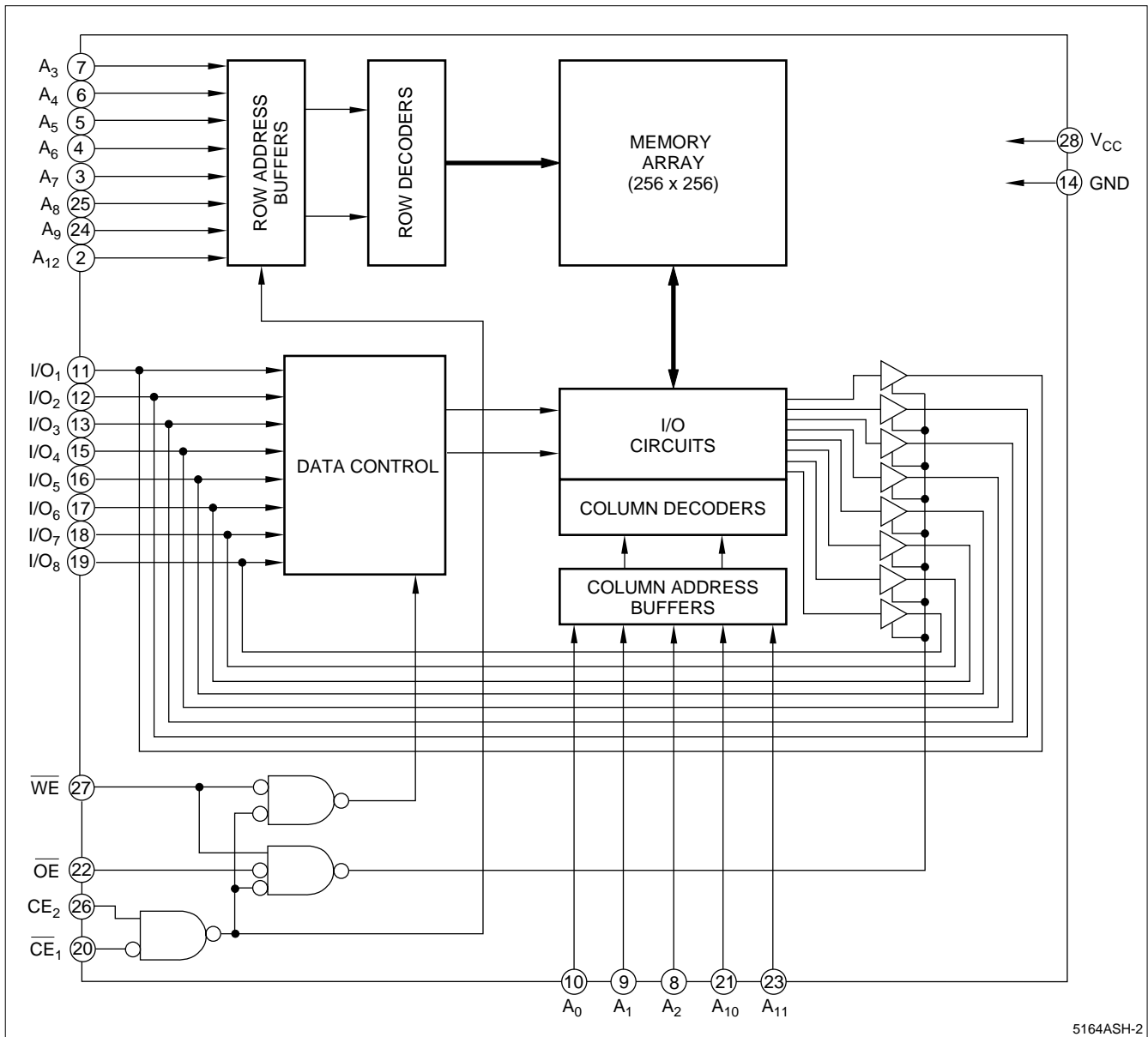


Figure 3. LH5164ASH Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₂	Address inputs
CE ₁ - CE ₂	Chip Enable input
WE	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data inputs and outputs
V _{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I _{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I _{SB})	1
L	H	L	X	Write	D _{IN}	Operating (I _{CC})	1
L	H	H	L	Read	D _{OUT}	Operating (I _{CC})	
L	H	H	H	Output disable	High-Z	Operating (I _{CC})	

NOTE:

- X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	1, 2
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTES:

- The maximum applicable voltage on any pin with respect to GND.
- V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{CC}	2.5	3.0	5.5	V	
Input voltage (V _{CC} = 2.5 to 4.5 V)	V _{IH}	V _{CC} - 0.5		V _{CC} + 0.3	V	
	V _{IL}	-0.3		0.2	V	1
Input voltage (V _{CC} = 4.5 to 5.5 V)	V _{IH}	2.2		V _{CC} + 0.3	V	
	V _{IL}	-0.3		0.8	V	

NOTE:

- V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	I _{LI}	V _{IN} = 0 to V _{CC}	-1.0	1.0	μA	
Output leakage current	I _{LO}	CE ₁ = V _{IH} or CE ₂ = V _{IL} or OE = V _{IH} or WE = V _{IL} V _{I/O} = 0 to V _{CC}	-1.0	1.0	μA	
Operating supply current	I _{CC}	CE ₁ = 0.2 V, V _{IN} = 0.2 V or V _{CC} - 0.2 V CE ₂ = V _{CC} - 0.2 V, Output open		20		
		CE ₁ = 0.2 V, V _{IN} = 0.2 V or V _{CC} - 0.2 V CE ₂ = V _{CC} - 0.2 V, Output open		10		mA
		CE ₁ = 0.2 V, V _{IN} = 0.2 V or V _{CC} - 0.2 V CE ₂ = V _{CC} - 0.2 V, Output open, V _{CC} = 3.3 V		8		
Standby current	I _{SB}	CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CC} - 0.2 V		1.0		1
	I _{SB1}	CE ₁ = V _{IH} or CE ₂ = V _{IL}		3.0		
Output Low voltage	V _{OL}	I _{OL} = 500 μA		0.5	V	
Output High voltage	V _{OH}	I _{OH} = -500 μA		V _{CC} - 0.5	V	2

NOTES:

- CE₂ should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V when CE₁ ≥ V_{CC} - 0.2 V.
- V_{OH} is 4.5 V (Min.) at V_{CC} > 5 V.

AC CHARACTERISTICS

(1) READ CYCLE ($T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.5$ to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read cycle time	t_{RC}	500		ns
Address access time	t_{AA}		500	ns
Chip enable access time	(CE ₁)	t_{ACE1}	500	ns
	(CE ₂)	t_{ACE2}	500	ns
Output enable access time	t_{OE}		200	ns
Output hold time	t_{OH}	10		ns
Chip enable to output in Low-Z	(CE ₁)	t_{LZ1}	20	ns
	(CE ₂)	t_{LZ2}	20	ns
Output enable to output in Low-Z	t_{OLZ}	10		ns
Chip enable to output in High-Z	(CE ₁)	t_{HZ1}	0	60
	(CE ₂)	t_{HZ2}	0	60
Output disable to output in High-Z	t_{OHZ}	0	40	ns

(2) WRITE CYCLE ($T_A = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.5$ to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	500		ns
Chip enable to end of write	t_{CW}	250		ns
Address valid to end of write	t_{AW}	250		ns
Address setup time	t_{AS}	100		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	50		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Output active from end of write	t_{OW}	20		ns
WE to output in High-Z	t_{WZ}	0	60	ns
OE to output in High-Z	t_{OHZ}	0	40	ns

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a ± 200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0 to V_{CC}	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	C_L (100 pF)	1

NOTE:

- Includes scope and jig capacitance.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0$ V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{IO} = 0$ V			10	pF

NOTE:

This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V _{CCDR}	CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CCDR} - 0.2 V	2.0	5.5	V	1
Data retention supply current	I _{CCDR}	V _{CCDR} = 3 V, CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CCDR} - 0.2 V		0.2 0.4 0.6	μA	1
Chip disable to data retention	t _{CDR}		0		ns	
Recovery time	t _R		t _{RC}		ns	2

NOTES:

1. CE₂ should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V when CE₁ ≥ V_{CCDR} - 0.2 V.
2. t_{RC} = Read cycle time

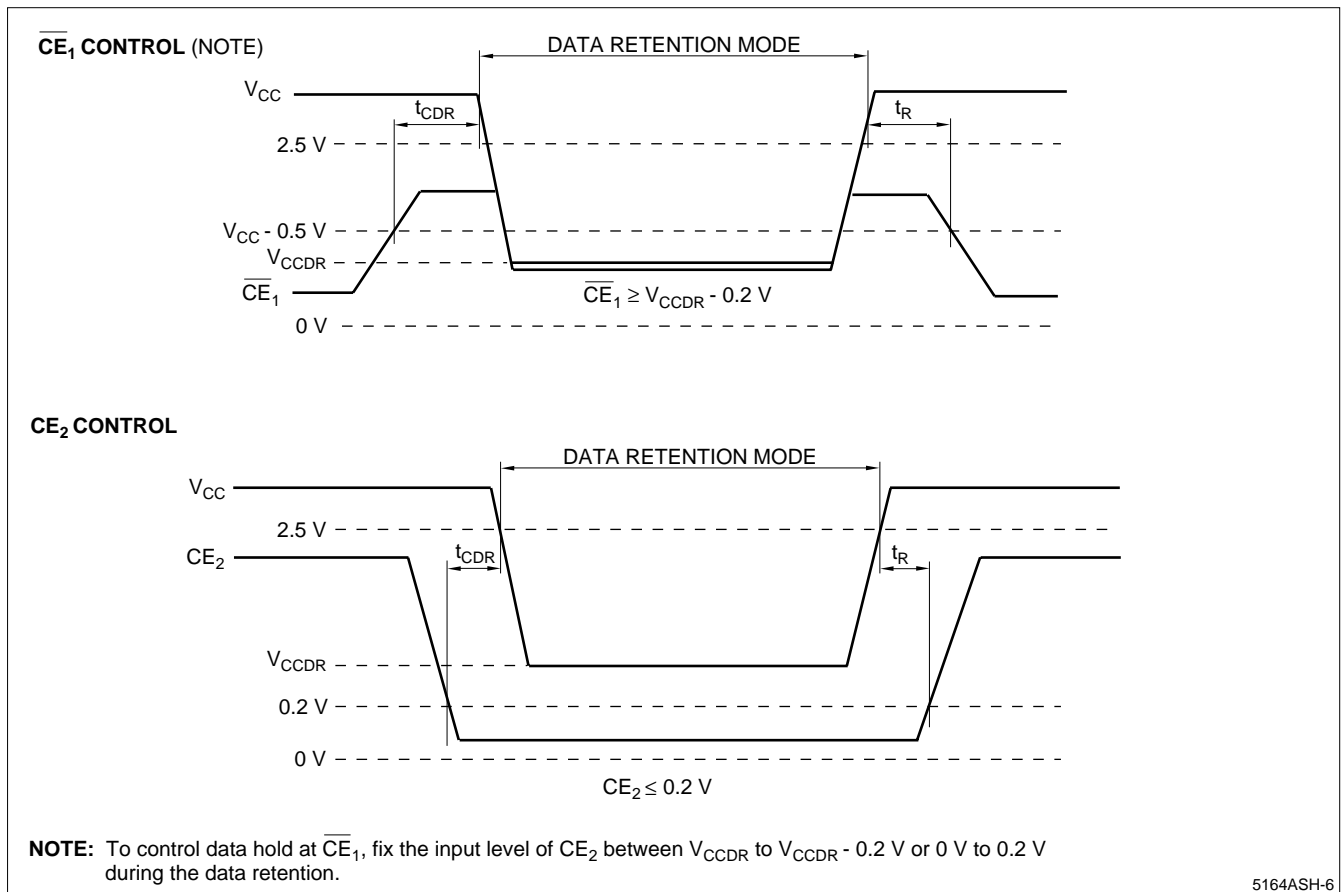


Figure 4. Low Voltage Data Retention

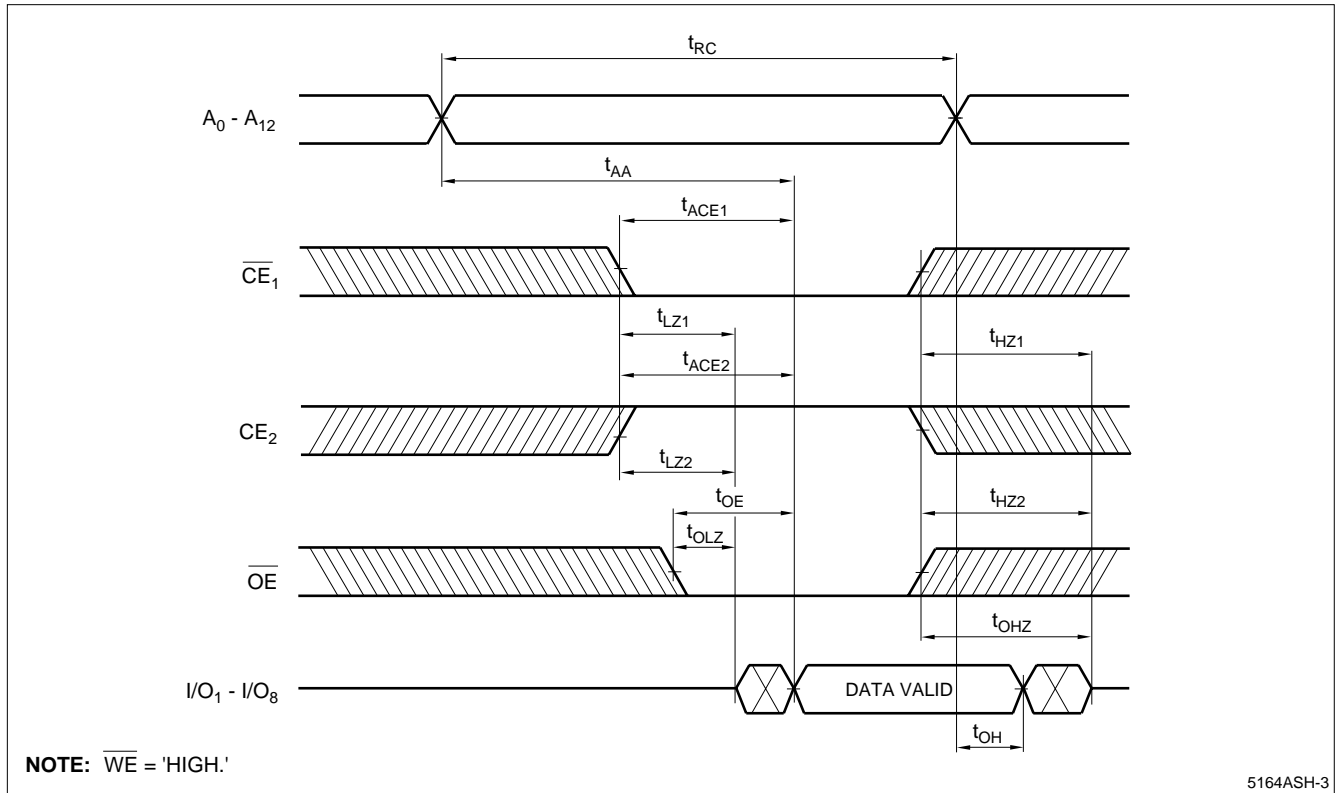
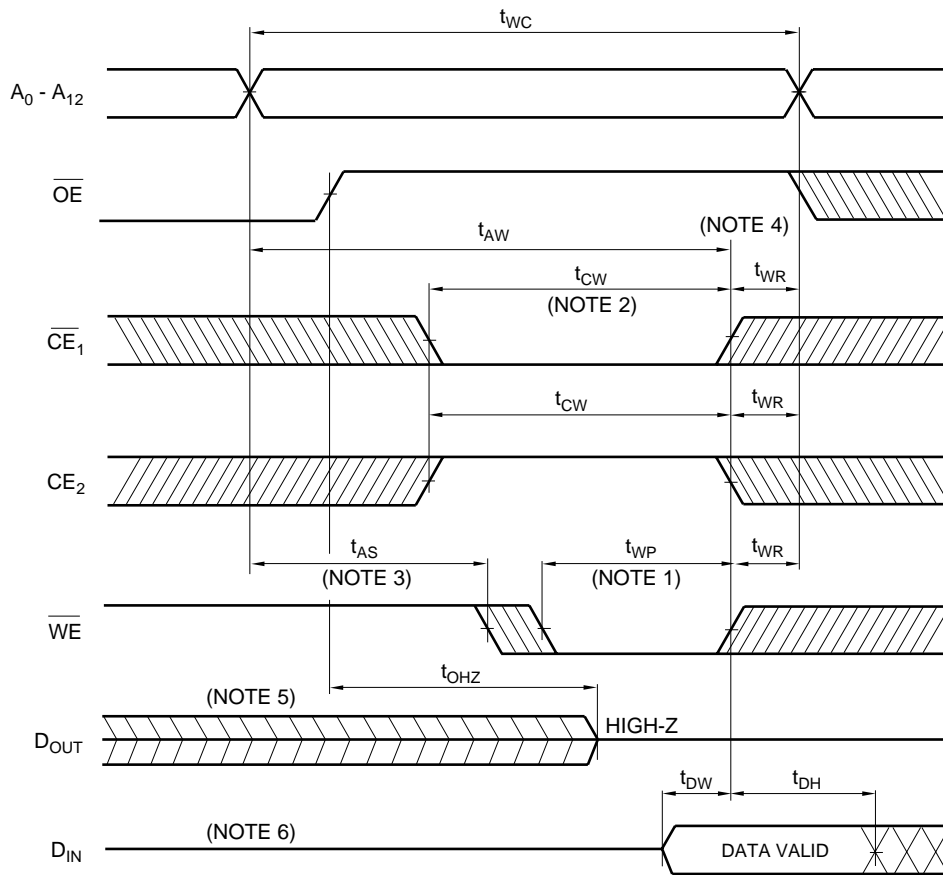


Figure 5. Read Cycle

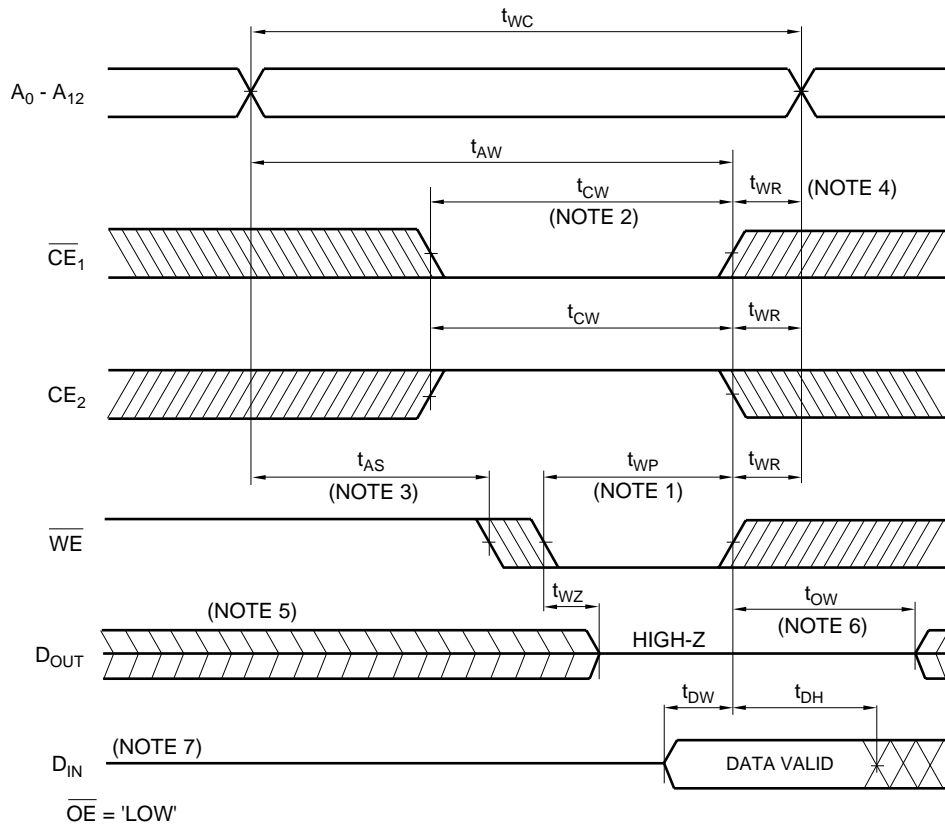


NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}_1 = \text{'LOW'}$, $CE_2 = \text{'HIGH'}$, and $\overline{WE} = \text{'LOW'}$ (t_{WP}).
2. t_{CW} is defined as the time from the last occurring transition, either \overline{CE}_1 LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If \overline{CE}_1 LOW transition or CE_2 HIGH transition occurs at the same time or after \overline{WE} LOW transition, the output will remain high-impedance.
6. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 6. Write Cycle 1 (OE Controlled)

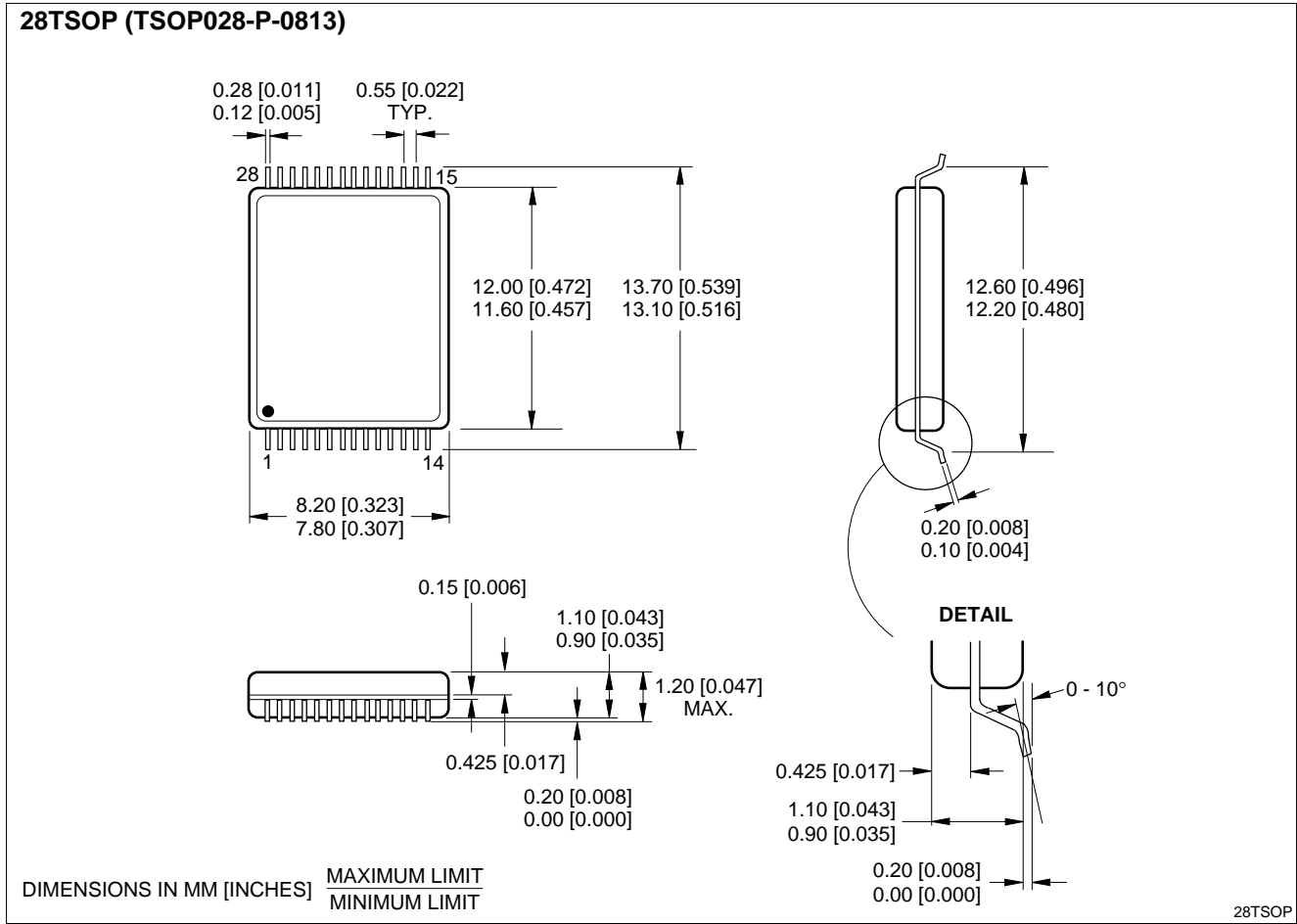


NOTES:

1. The writing occurs during an overlapping of $\overline{CE}_1 = \text{'LOW'}$, $CE_2 = \text{'HIGH'}$, and $\overline{WE} = \text{'LOW'}$ (t_{WP}).
2. t_{CW} is defined as the time from the last occurring transition, either \overline{CE}_1 LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If \overline{CE}_1 LOW transition or CE_2 HIGH transition occurs at the same time or after \overline{WE} LOW transition, the output will remain high-impedance.
6. If \overline{CE}_1 HIGH transition or CE_2 LOW transition occurs at the same time or before \overline{WE} HIGH transition, the output will remain high-impedance.
7. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 7. Write Cycle 2 (OE Low Fixed)



28-pin, 8 × 13 mm² TSOP (Type I)

ORDERING INFORMATION

