

LH5164AV

CMOS 64K (8K × 8) Static RAM

FEATURES

- 8,192 × 8 bit organization
- Access time: 200 ns (MAX.)
- Supply current (MAX.):
 - Operating: 248 mW
 - 55 mW (t_{RC} , $t_{WC} = 1 \mu s$)
 - Standby: 5.5 μW
 - Data retention: 0.6 μW ($V_{CC} = 3 V$, $t_A = 25^\circ C$)
- Wide operating voltage range: 2.7 V to 5.5 V
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Packages:
 - 28-pin, 450-mil SOP
 - 28-pin, 8 × 13 mm² TSOP (Type I)

DESCRIPTION

The LH5164AV is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

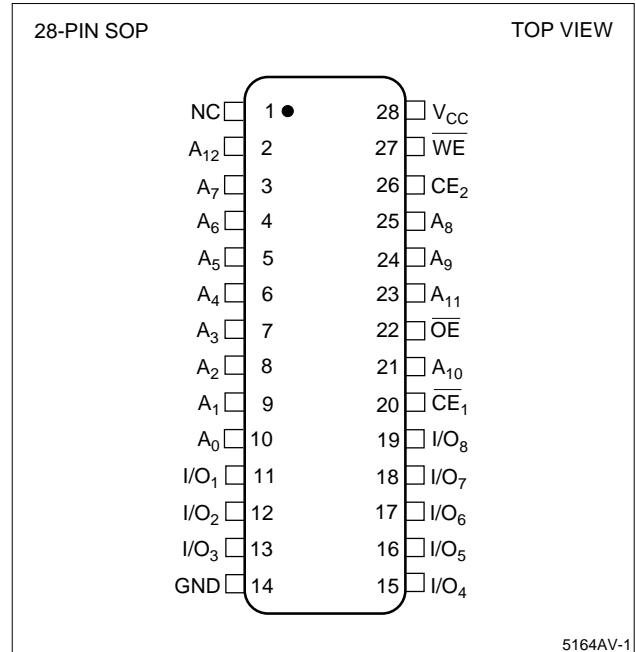


Figure 1. Pin Connections for SOP Package

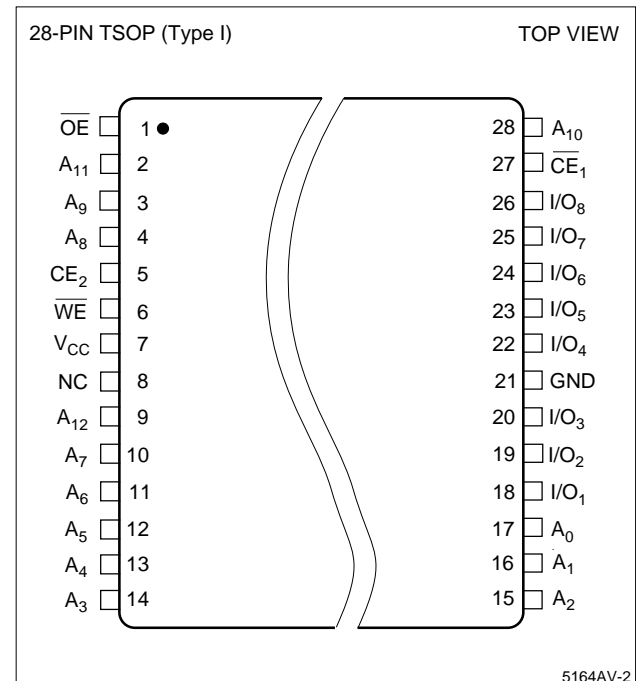


Figure 2. Pin Connections for TSOP Package

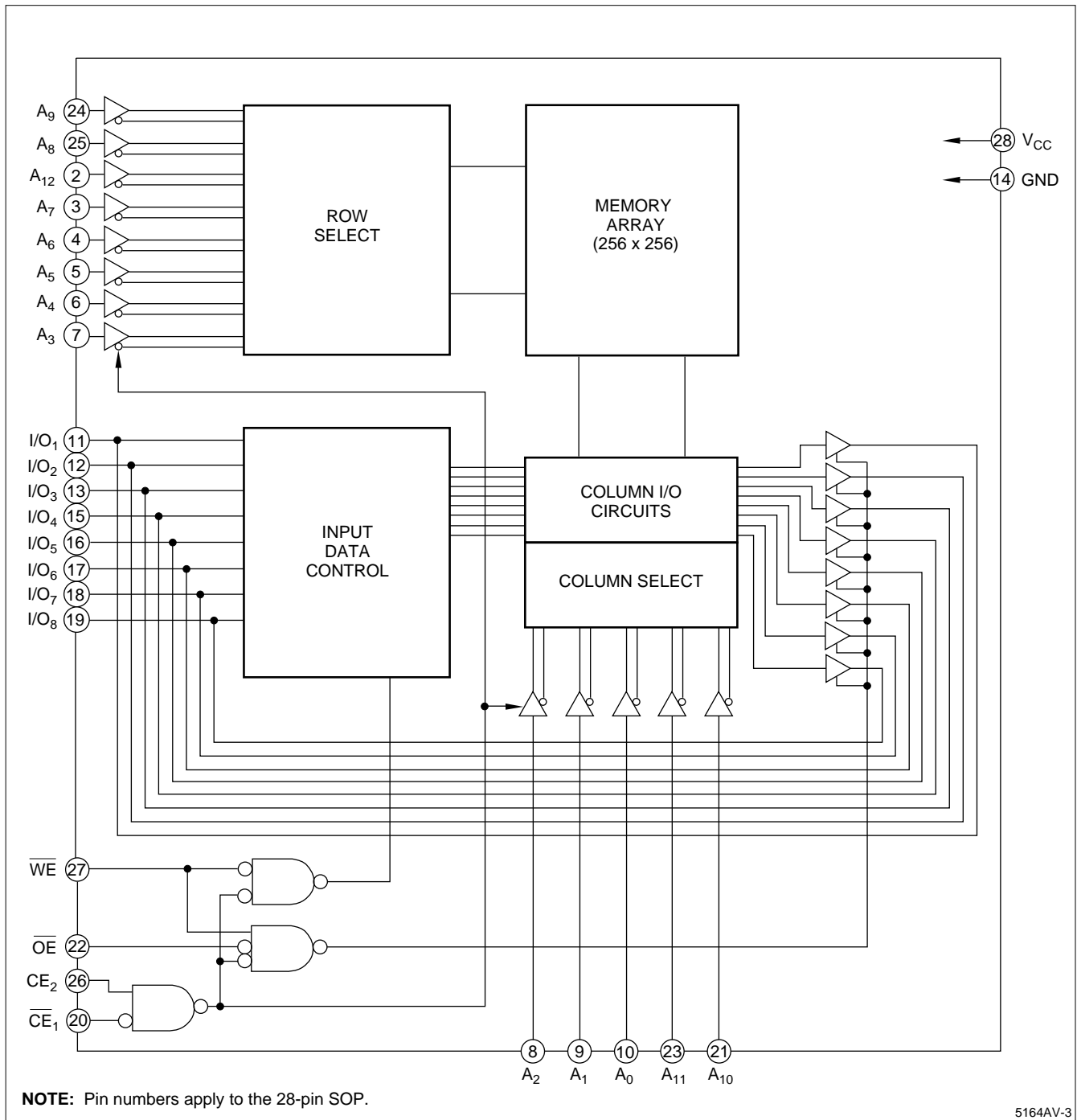


Figure 3. LH5164AV Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₂	Address inputs
CE ₁ /CE ₂	Chip Enable input
WE	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data inputs and outputs
V _{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
H	X	X	X	Standby	High-Z	Standby (I _{SB})	1
X	L	X	X				
L	H	L	X	Write	Data input	Operating (I _{CC})	1
L	H	H	L	Read	Data output	Operating (I _{CC})	
L	H	H	H	Output disable	High-Z	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	1, 2
Operating temperature	T _{opr}	-10 to +70	°C	
Storage temperature	T _{stg}	-65 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -10°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{CC}	2.7		5.5	V	
Input voltage (V _{CC} = 2.7 V to 3.6 V)	V _{IH}	V _{CC} - 0.5		V _{CC} + 0.3	V	
	V _{IL}	-0.3		0.2	V	1
Input voltage (V _{CC} = 4.5 V to 5.5 V)	V _{IH}	2.2		V _{CC} + 0.3	V	
	V _{IL}	-0.3		0.8	V	1

NOTE:

1. V_{IL} (MIN.) = -3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS ¹ ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	$V_{IN} = 0\text{ V}$ to V_{CC}	-1.0	1.0	μA	
Output leakage current	I_{LO}	$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$ $V_{I/O} = 0$ to V_{CC}	-1.0	1.0	μA	
Operating supply current	I_{CC}	$CE_1 = 0.2\text{ V}$, $V_{IN} = 0.2\text{ V}$, or $V_{CC} - 0.2\text{ V}$ $CE_2 = V_{CC} - 0.2\text{ V}$, Outputs open, $V_{CC} = 2.7\text{ V}$ to 3.6 V	$t_{CYCLE} = 200\text{ ns}$	20	mA	
			$t_{CYCLE} = 1.0\text{ }\mu\text{s}$	8		
		$CE_1 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH} $CE_2 = V_{IH}$, Outputs open, $V_{CC} = 4.5\text{ V}$ to 5.5 V	$t_{CYCLE} = 200\text{ ns}$	45		
			$t_{CYCLE} = 1.0\text{ }\mu\text{s}$	10		
Standby current	I_{SB}	$CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CC} - 0.2\text{ V}$	$V_{CC} = 2.7\text{ V}$ to 3.6 V	0.6	μA	1
			$V_{CC} = 4.5\text{ V}$ to 5.5 V	1.0		
Output voltage	V_{OL}	$I_{OL} = 500\text{ }\mu\text{A}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V $I_{OL} = 2.1\text{ mA}$, $V_{CC} = 4.5\text{ V}$ to 5.5 V		0.4	V	
				0.4		
	V_{OH}	$I_{OH} = -500\text{ }\mu\text{A}$, $V_{CC} = 2.7\text{ V}$ to 3.6 V $I_{OH} = -1.0\text{ mA}$, $V_{CC} = 4.5\text{ V}$ to 5.5 V	$V_{CC} - 0.5$		V	
			2.4			
	I_{SB1}	$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$		5	mA	

NOTE:

- CE_2 should be $\geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$ when $CE_1 \geq V_{CC} - 0.2\text{ V}$.

READ CYCLE ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read cycle time	t_{RC}	200		ns
Address access time	t_{AA}		200	ns
CE ₁ access time	t_{ACE1}		200	ns
CE ₂ access time	t_{ACE2}		200	ns
Output enable access time	t_{OE}		150	ns
Output hold time	t_{OH}	10		ns
CE ₁ Low to output in Low-Z	t_{LZ1}	20		ns
CE ₂ High to output in Low-Z	t_{LZ2}	20		ns
OE Low to output in Low-Z	t_{OLZ}	10		ns
CE ₁ High to output in High-Z	t_{HZ1}	0	60	ns
CE ₂ Low to output in High-Z	t_{HZ2}	0	60	ns
OE High to output in High-Z	t_{OHZ}	0	40	ns

WRITE CYCLE ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.7\text{ V}$ to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Write cycle time	t_{WC}	200		ns
CE Low to end of write	t_{CW}	180		ns
Address valid to end of write	t_{AW}	180		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	150		ns
Write recovery time	t_{WR}	0		ns
Input data setup time	t_{DW}	100		ns
Input data hold time	t_{DH}	0		ns
WE High to output in Low-Z	t_{OW}	20		ns
WE Low to output in High-Z	t_{WZ}	0	60	ns
OE High to output in High-Z	t_{OHZ}	0	40	ns

TEST CONDITIONS

PARAMETER	MODE	NOTE
Input pulse level	0.2 V to $V_{CC} - 0.2\text{ V}$	
Input rise/fall time	10 ns	
Input/output timing level	1.5 V	
Output load	C_L (100 pF)	1

NOTE:

- Includes scope and jig capacitance.

CAPACITANCE ¹ ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$			7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$			10	pF

NOTE:

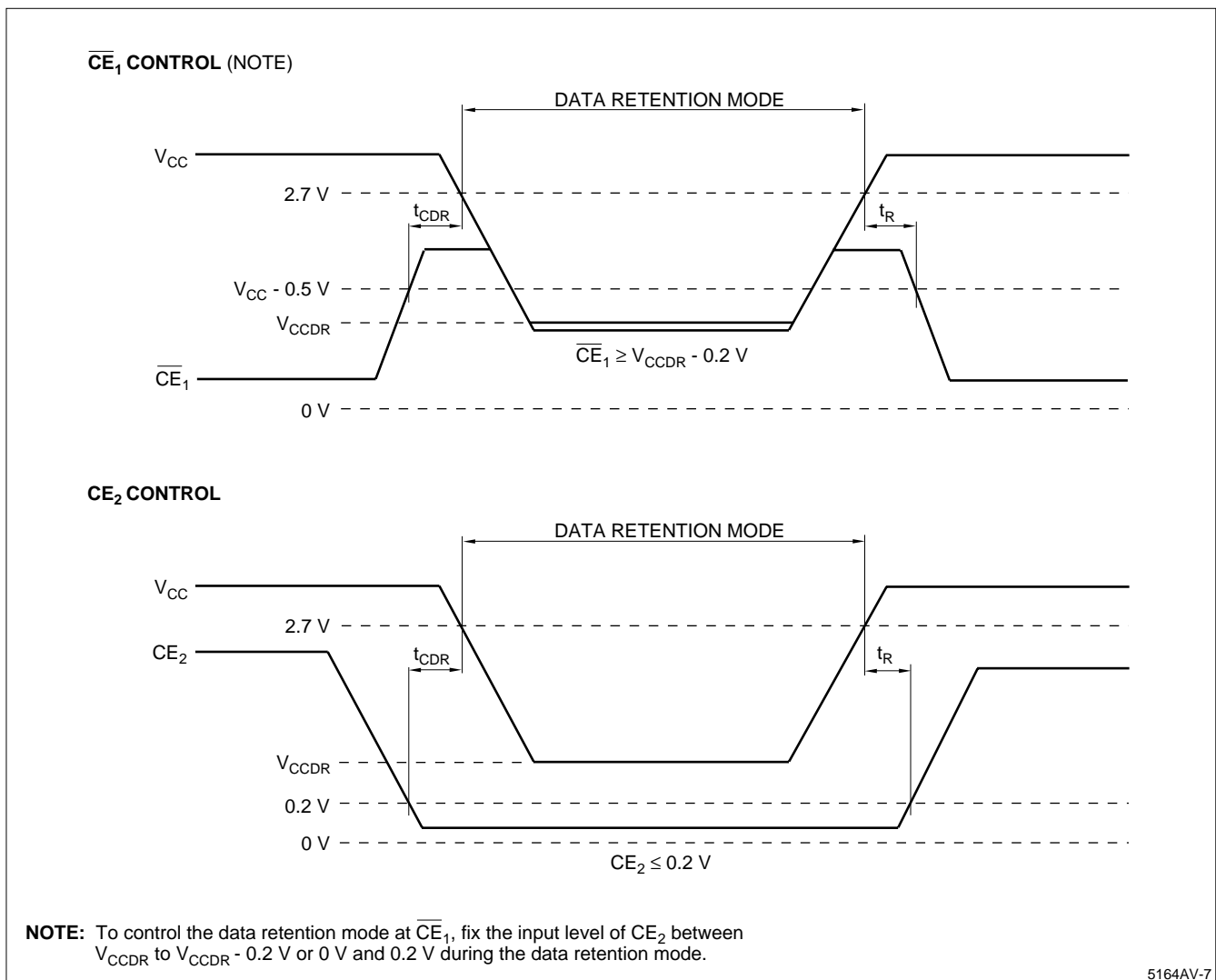
- This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -10°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V _{CCDR}	CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CCDR} - 0.2 V	2.0	5.5	V	1
Data retention supply current	I _{CCDR}	V _{CCDR} = 3 V, CE ₂ ≤ 0.2 V or CE ₁ ≥ V _{CCDR} - 0.2 V		0.2	μA	1
		T _A = 25°C		0.4	μA	
		T _A = 40°C		0.6	μA	
Chip disable to data retention	t _{CDR}		0		ns	
Recovery time	t _R		t _{RC}		ns	2

NOTES:

1. CE₂ should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V when CE₁ ≥ V_{CCDR} - 0.2 V.
2. t_{RC} = Read cycle time.



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Figure 4. Data Retention Characteristics

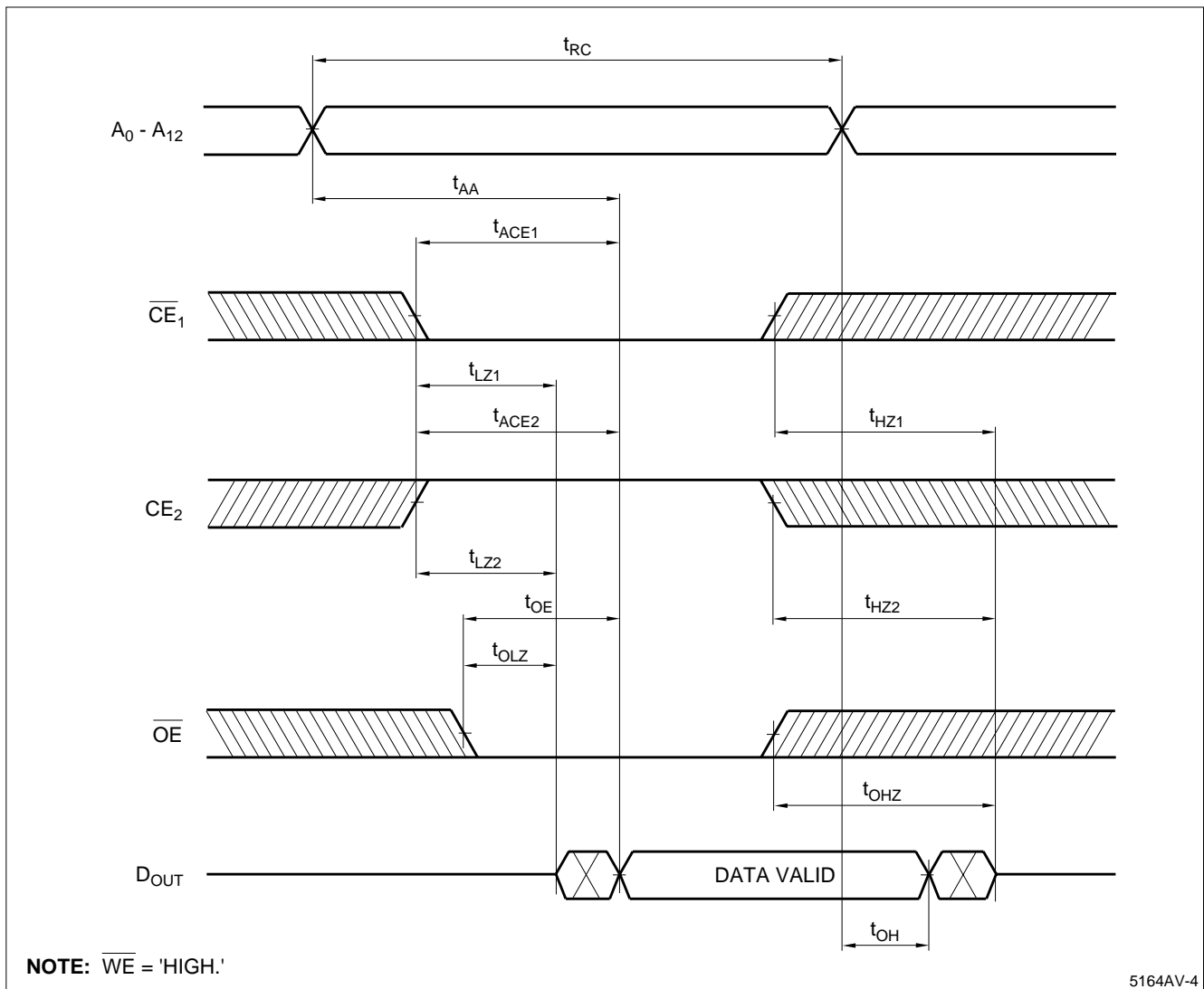
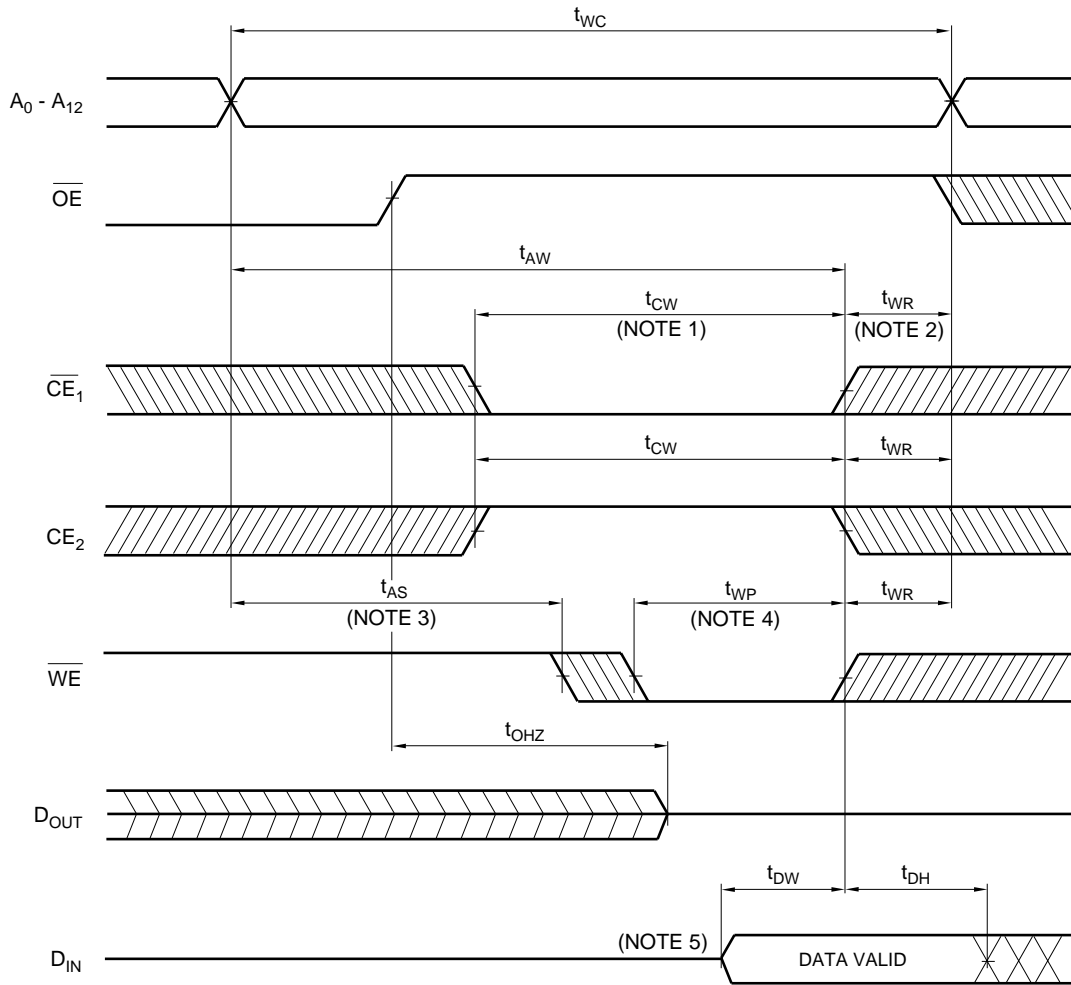


Figure 5. Read Cycle

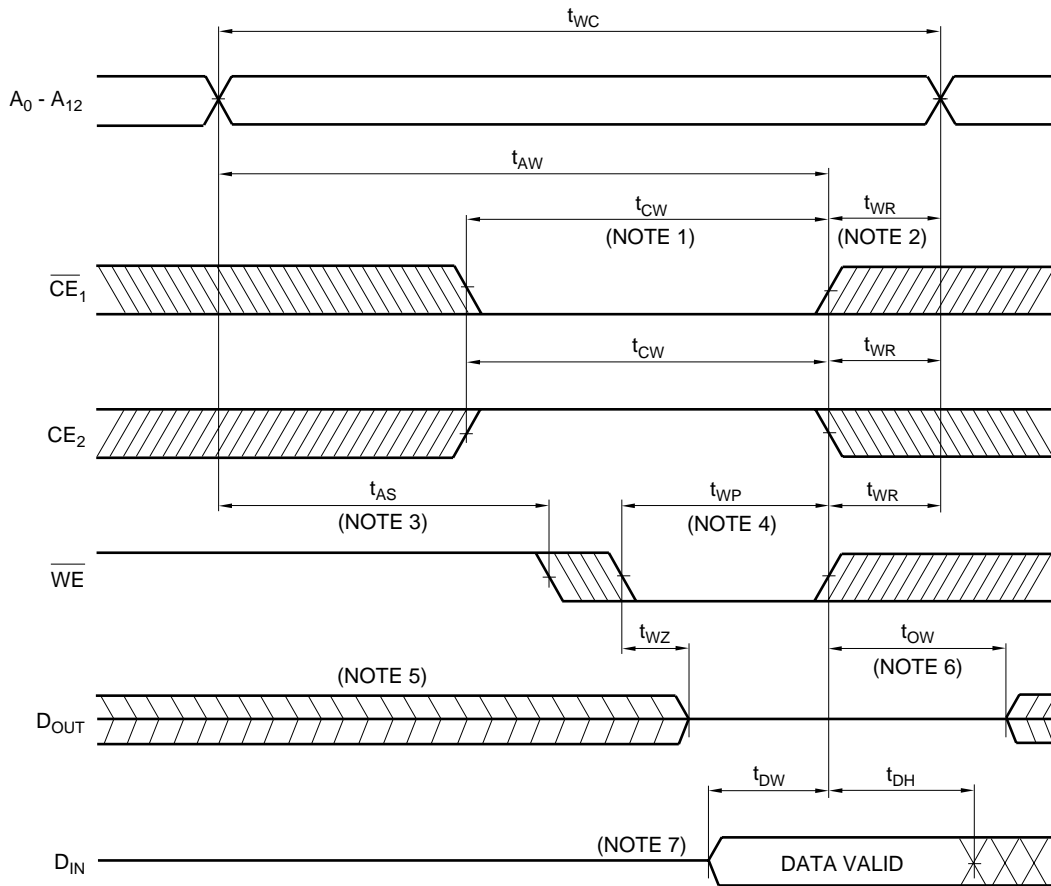


NOTES:

1. t_{CW} is defined as the time from the last occurring transition, either \overline{CE}_1 LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
2. t_{WR} is defined as the time from writing finish to address change.
3. t_{AS} is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of $\overline{CE}_1 = \text{'LOW,'}$ $CE_2 = \text{'HIGH,'}$ and $\overline{WE} = \text{'LOW'}$ (t_{WP}).
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 6. Write Cycle (OE Controlled)



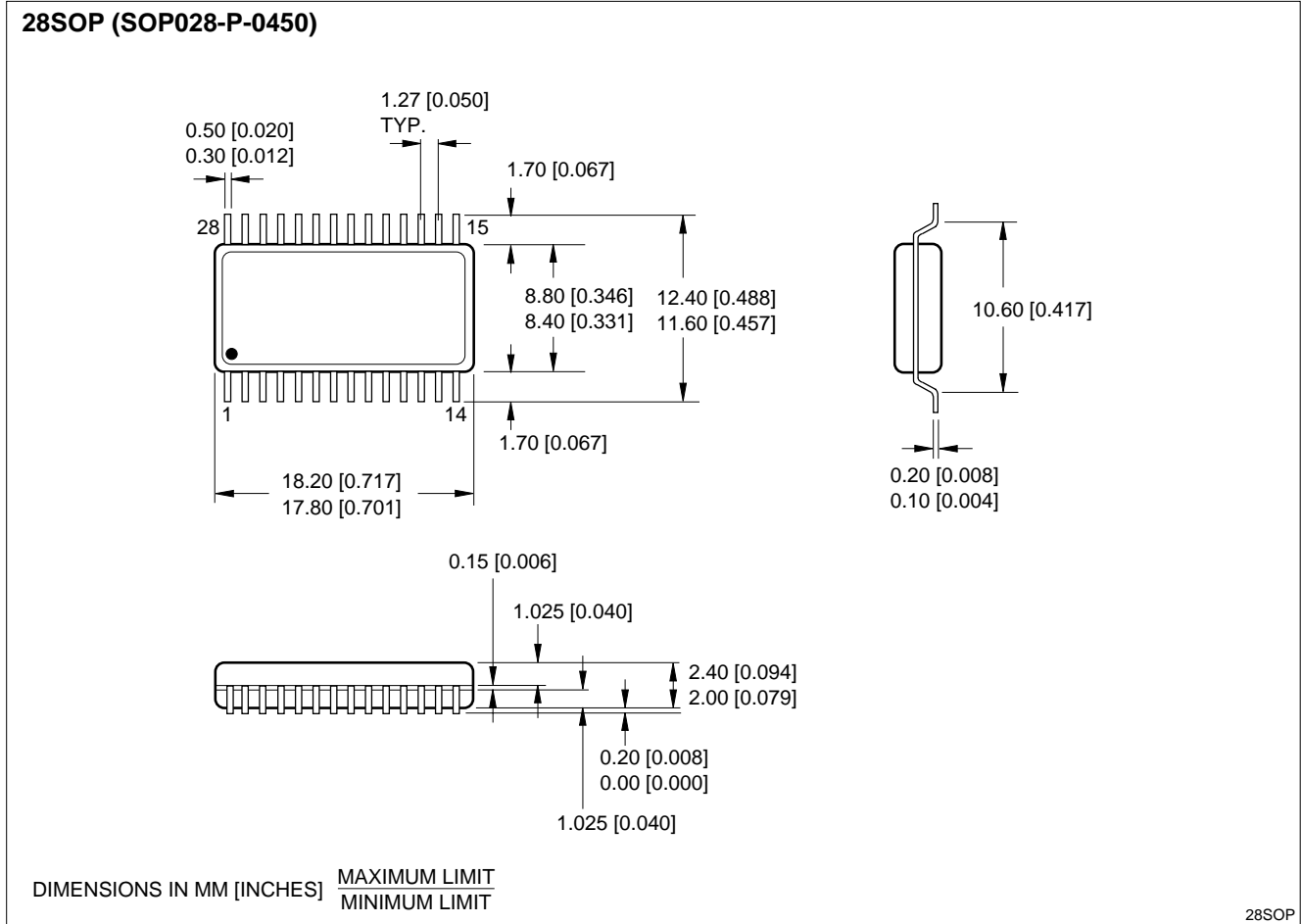
NOTES:

1. t_{CW} is defined as the time from the last occurring transition, either \overline{CE}_1 LOW transition or CE₂ HIGH transition, to the time when the writing is finished.
2. t_{WR} is defined as the time from writing finish to address change.
3. t_{AS} is defined as the time from address change to writing start.
4. The writing occurs during an overlapping period of $\overline{CE}_1 = \text{'LOW'}$, CE₂ = 'HIGH,' and $\overline{WE} = \text{'LOW'}$ (t_{WP}).
5. If \overline{CE}_1 LOW transition or CE₂ HIGH transition occurs at the same time or after \overline{WE} LOW transition, the outputs will remain high-impedance.
6. If \overline{CE}_1 HIGH transition or CE₂ LOW transition occurs at the same time or before \overline{WE} HIGH transition, the outputs will remain high-impedance.
7. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

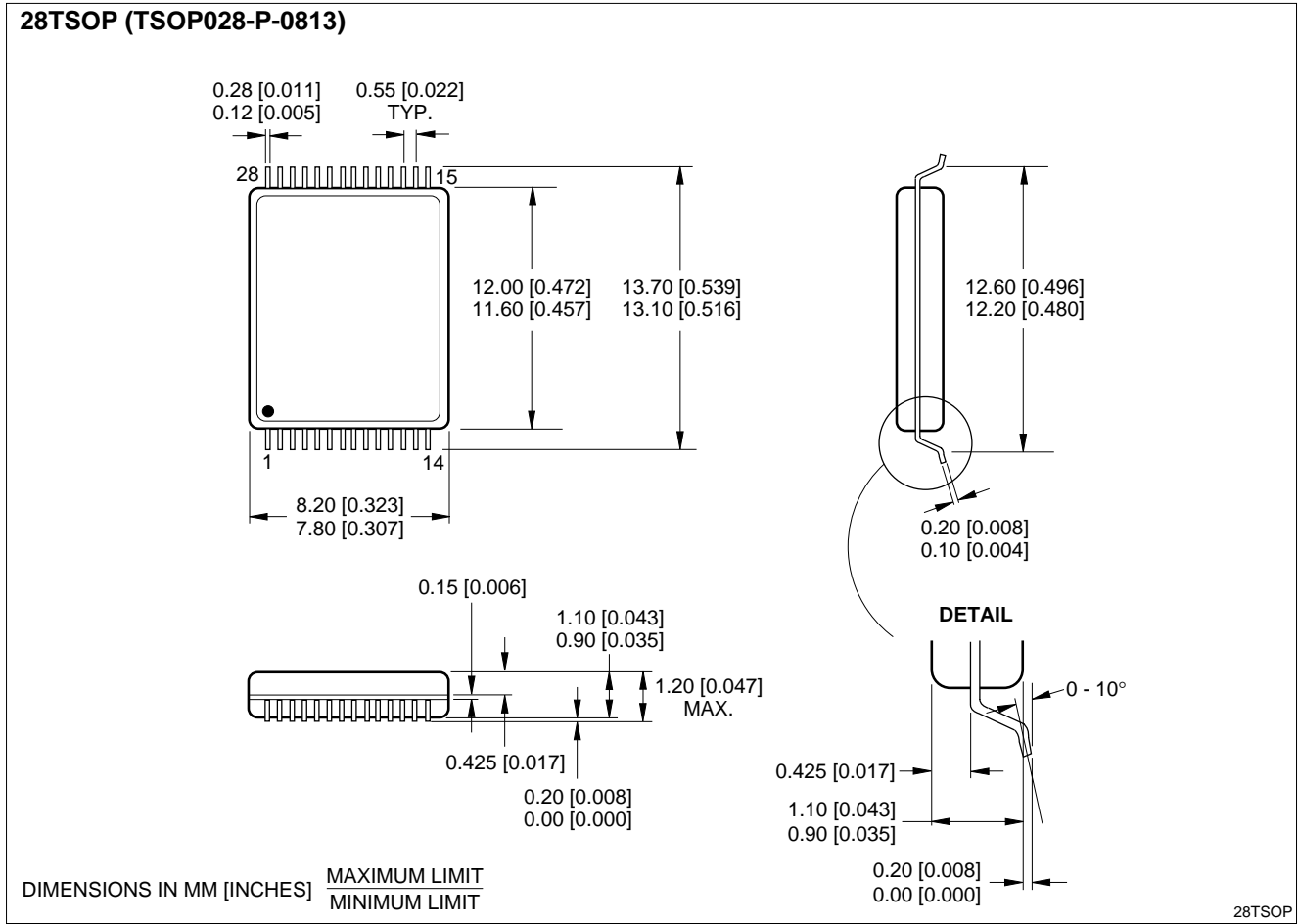
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Figure 7. Write Cycle (OE Low Fixed)

PACKAGE DIAGRAMS



28-pin, 450-mil SOP



28-pin, 8 × 13 mm² TSOP (Type I)

ORDERING INFORMATION

