LH531024

CMOS 1M (64K × 16) MROM

FEATURES

- 65,536 words × 16 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
  Operating: 412.5 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- JEDEC standard EPROM pinout (DIP)
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 650-mil QFJ (PLCC)

DESCRIPTION

The LH531024 is a mask-programmable ROM organized as 65,536 × 16 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

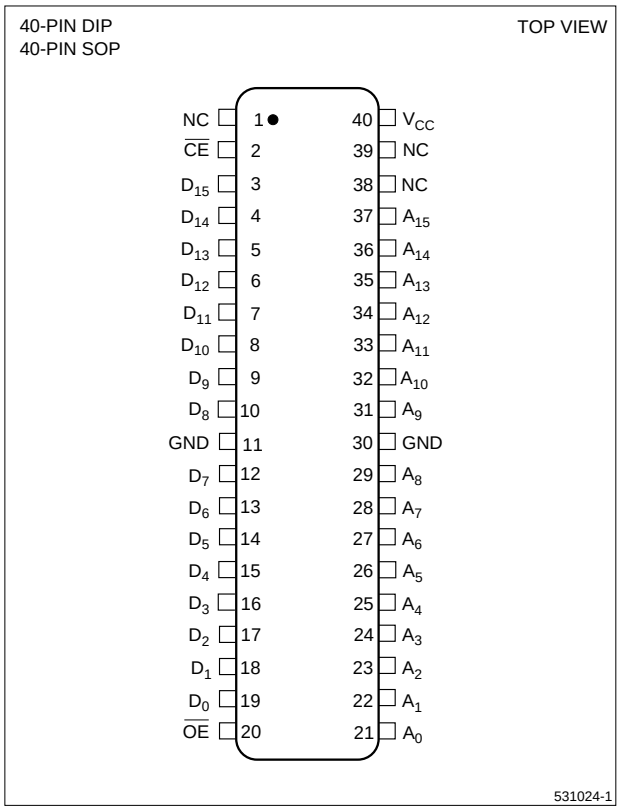


Figure 1. Pin Connections for DIP and SOP Packages

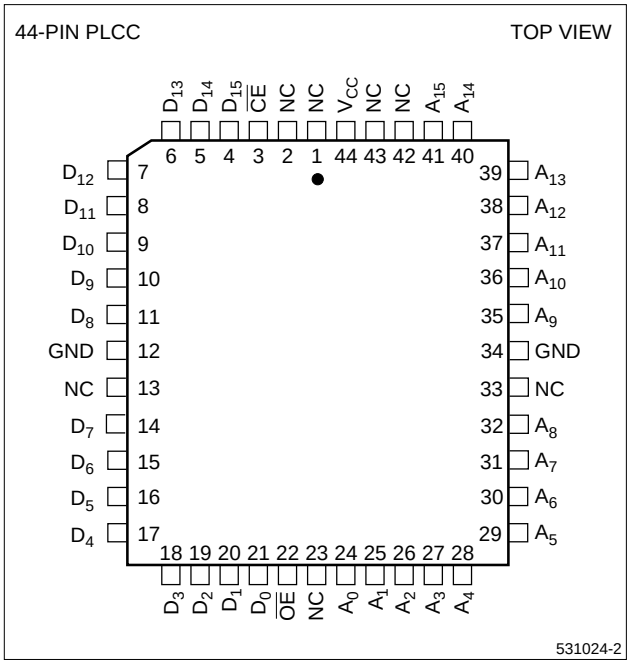


Figure 2. Pin Connections for QFJ (PLCC) Package

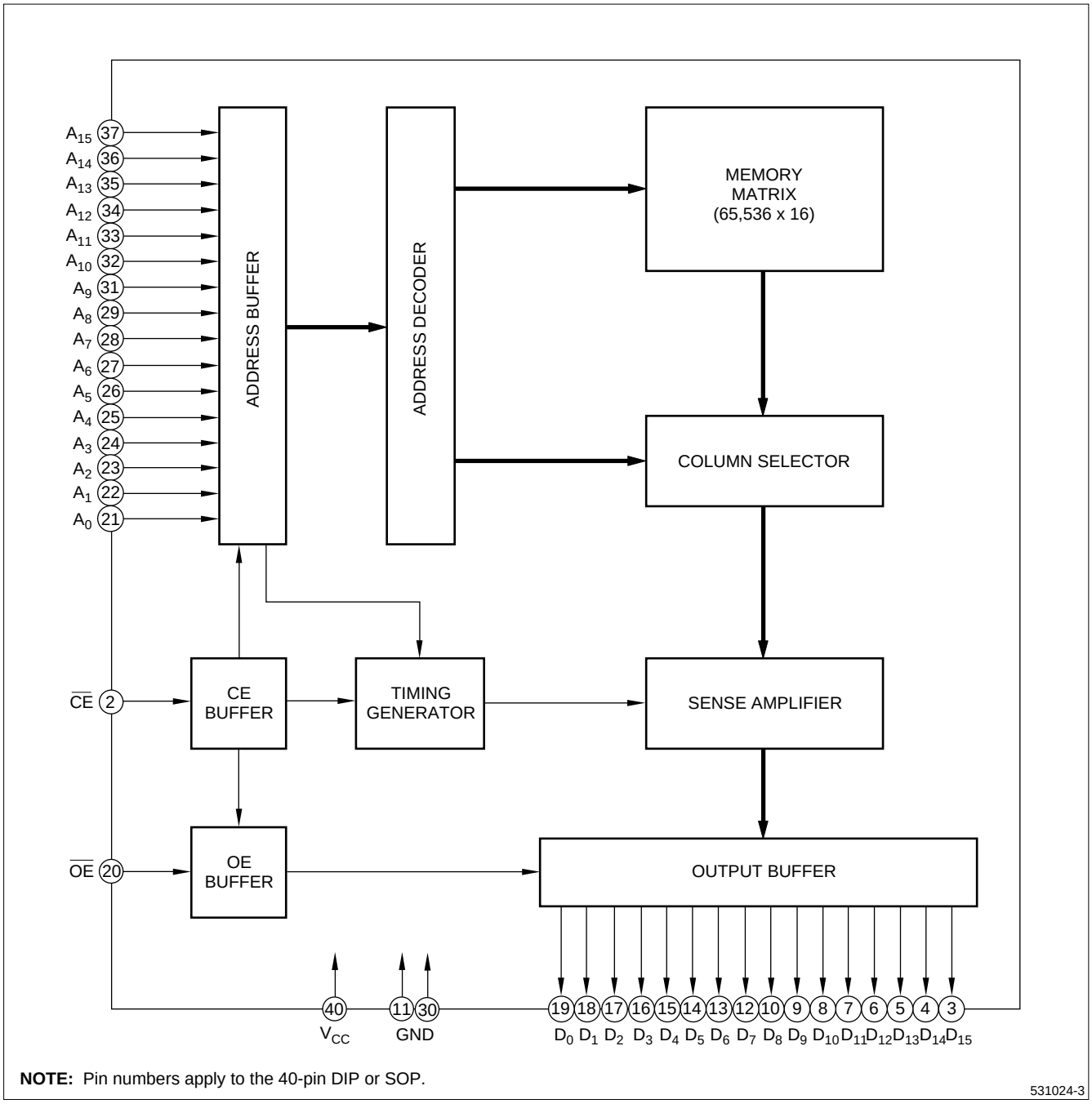


Figure 3. LH531024 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
$A_0 - A_{15}$	Address input
$D_0 - D_{15}$	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+5 V)
GND	Ground

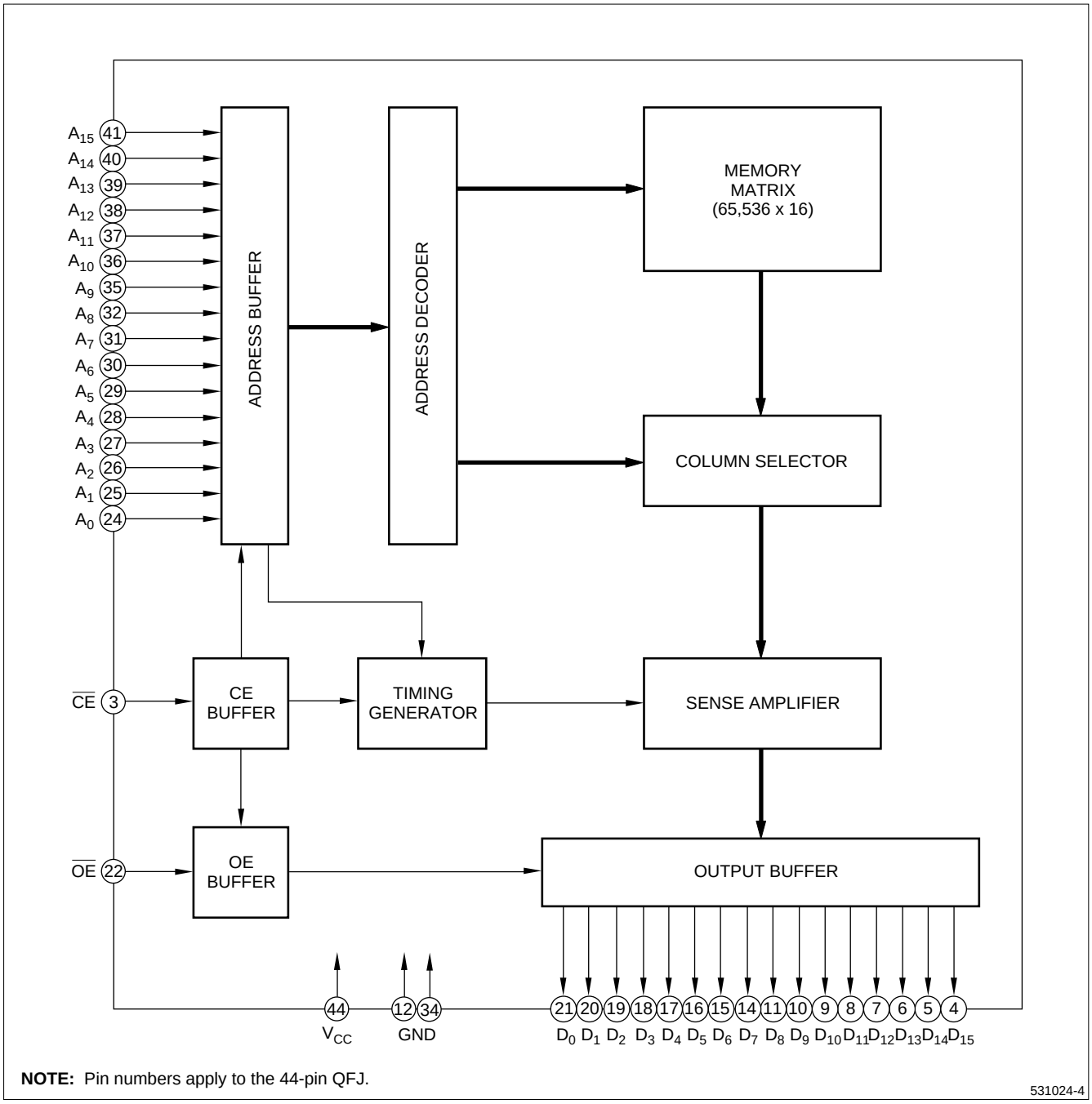


Figure 4. LH531024 Block Diagram

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$D_0 – D_{15}$	SUPPLY CURRENT	NOTE
H	X	High-Z	Standby (I_{SB})	1
L	H		Operating (I_{CC})	
L	L	$D_0 – D_{15}$		

NOTE:
1. X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		–0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns			75	mA	2
	I_{CC2}	t_{RC} = 1 µs			65	mA	
	I_{CC3}	t_{RC} = 100 ns			70	mA	3
	I_{CC4}	t_{RC} = 1 µs			60	mA	
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			50	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			50	ns	1
OE to output in High-Z	t_{OHZ}			50	ns	

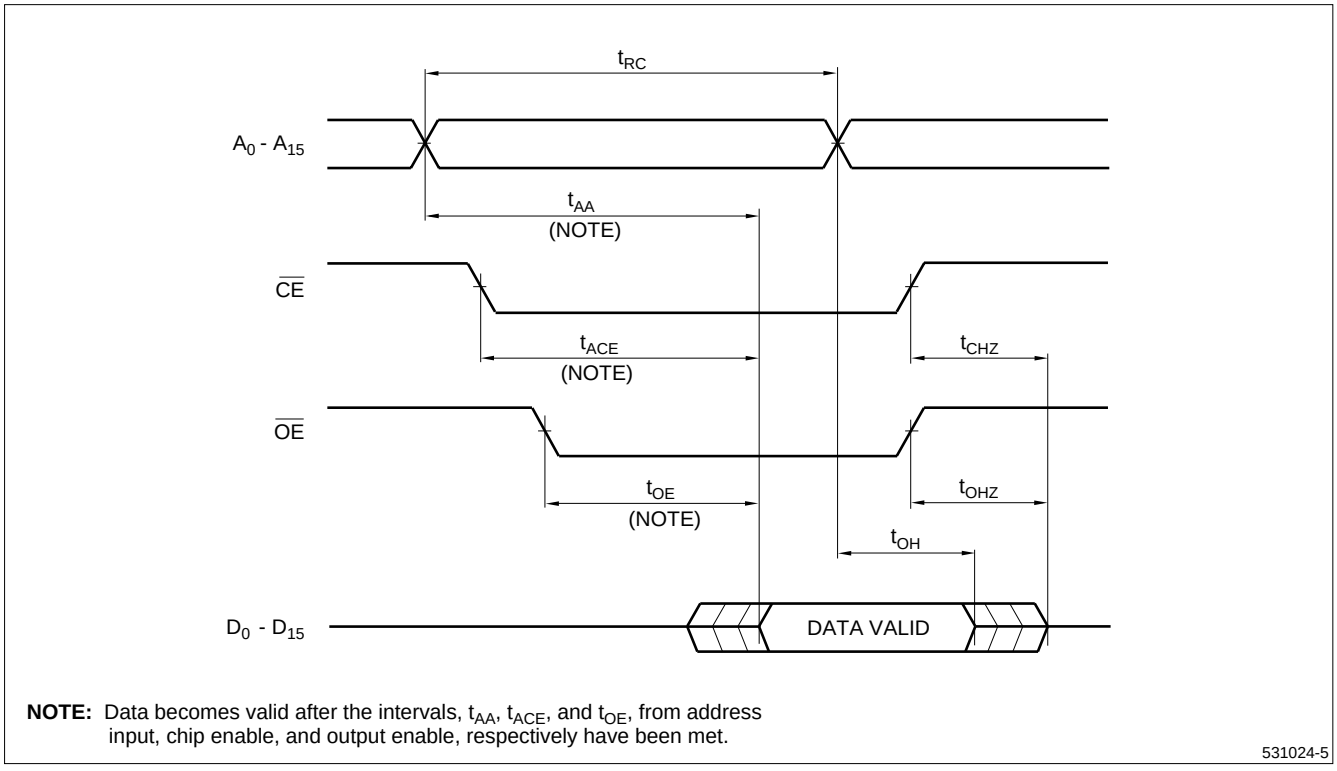
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input signal rise time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL +100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: Data becomes valid after the intervals, t_{AA}, t_{ACE}, and t_{OE}, from address input, chip enable, and output enable, respectively have been met.

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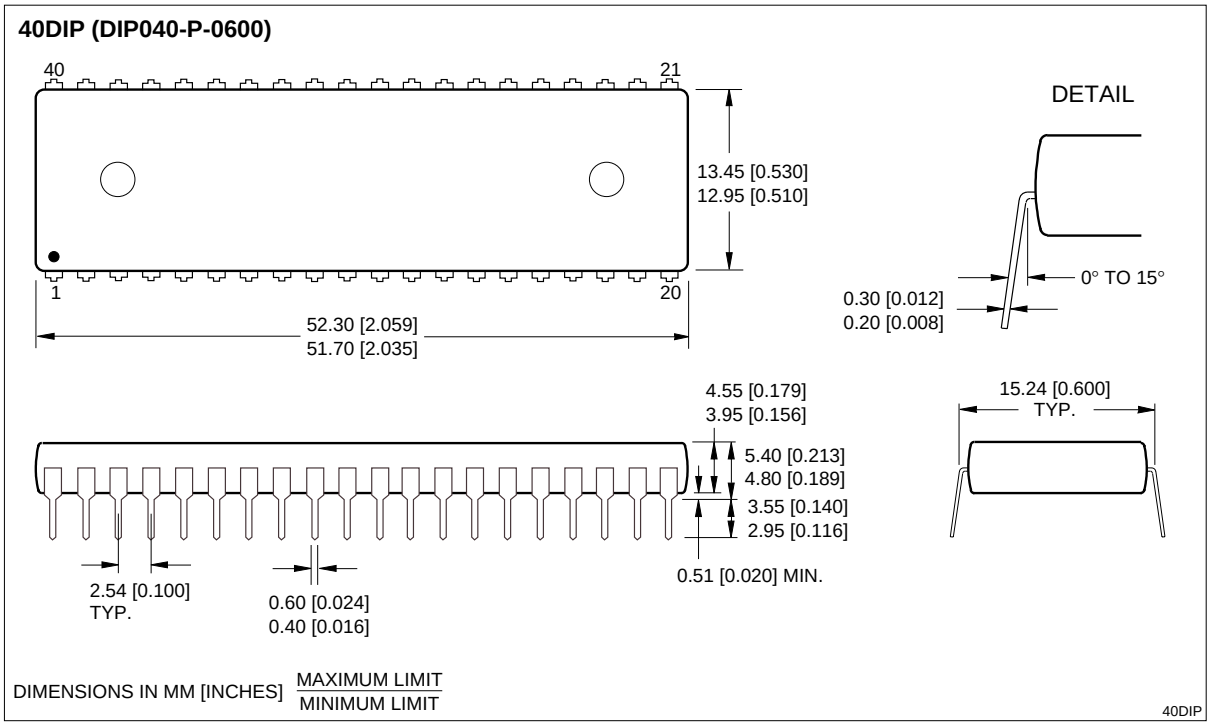
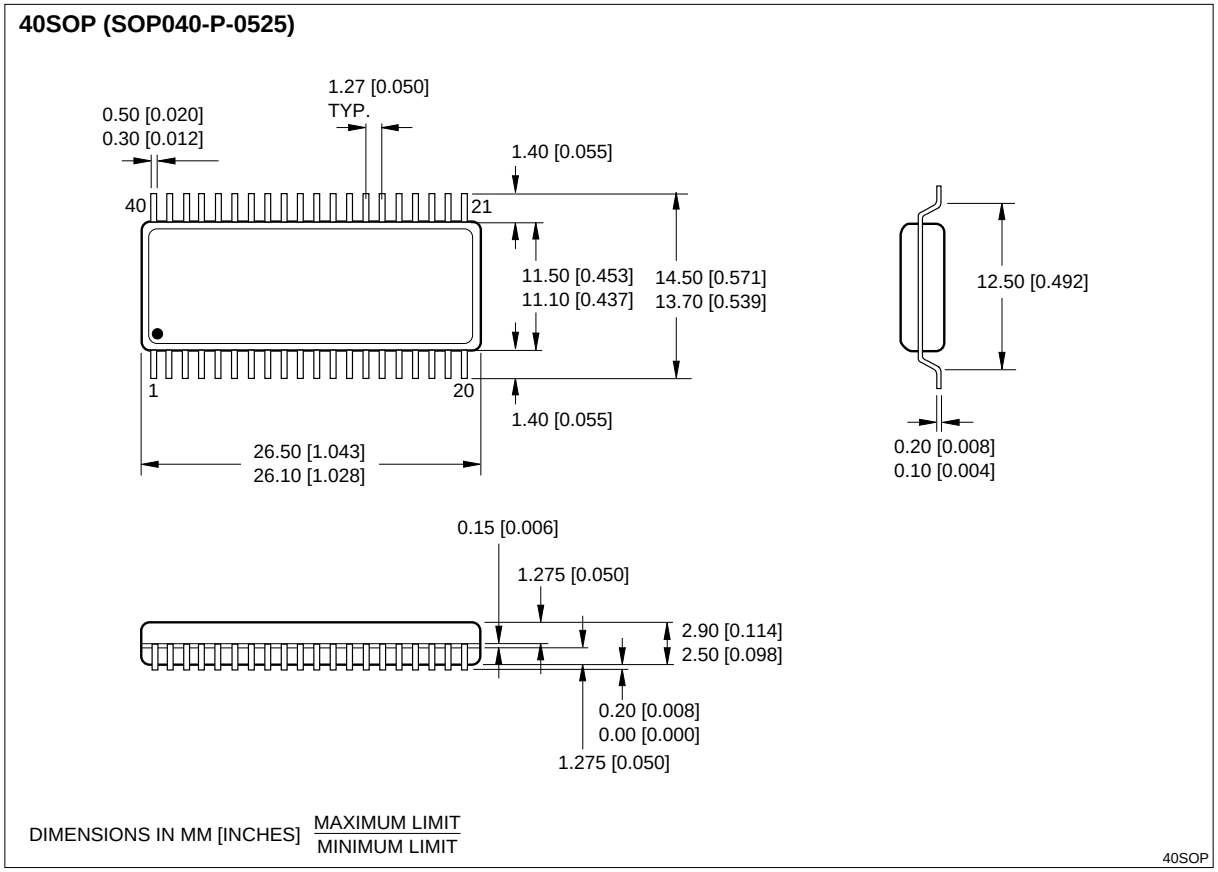
Figure 5. Timing Diagram

PACKAGE DIAGRAMS

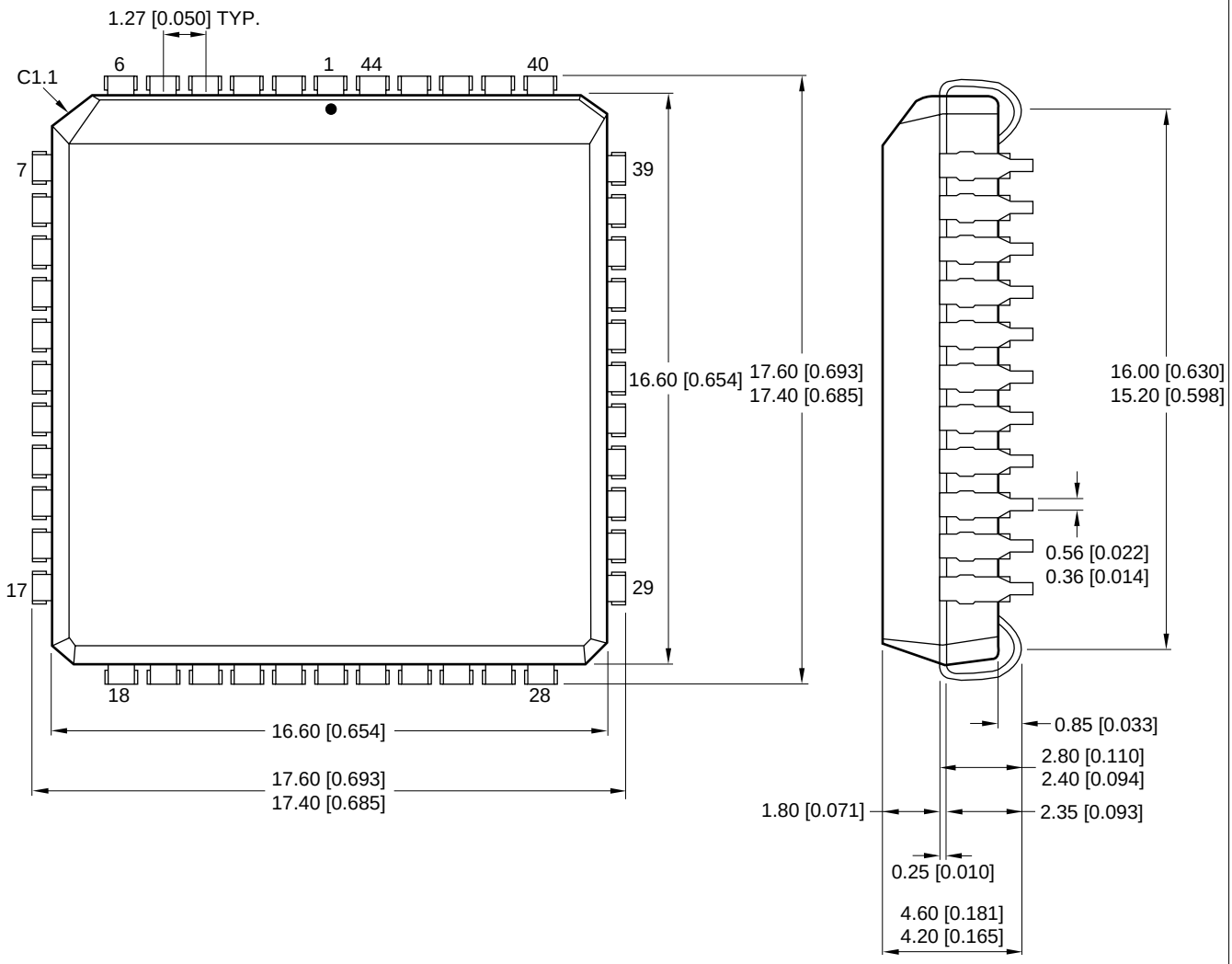


40-pin, 600-mil DIP



40-pin, 525-mil SOP

44QFJ (QFJ044-P-S650)



44-pin, 650-mil QFJ (PLCC)

ORDERING INFORMATION