SHARP

NEW PRODUCT INFORMATION

LH53H4100

High-speed 4M-bit Mask-Programmable ROM

■ Description

The LH53H4100D/N (User's No. : LH5H41XX) is a CMOS 4M-bit mask-programmable ROM organized as 524 288×8 bits. It is fabricated using sillicon-gate CMOS process technology.

■ Features

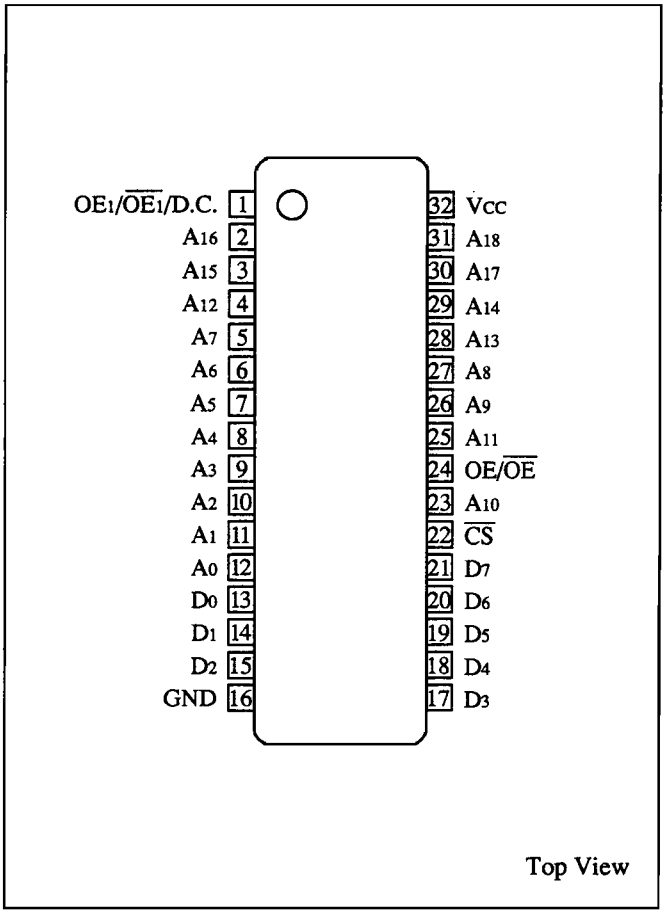
1. 524 288×8 bit organization
2. Maximum access time 80 ns
3. Maximum supply current
   Operating 90 mA
4. Static operation (Internal sync. system)
5. TTL compatible I/O
6. Three-state outputs
7. Supply voltage 5 V±10%
8. Package
   LH53H4100D 32-pin DIP (DIP032-P-0600)
   LH53H4100N 32-pin SOP (SOP032-P-0525)

■ Pin Description

Signal	Pin name	Note
A_0-A_{18}	Address input	
D_0-D_7	Data output	
$\overline{CS}$	Chip select input	
OE/$\overline{OE}$	Output enable input	1
OE_1/$\overline{OE_1}$/D.C.	Output enable input/Don't care connection	
V_{CC}	Power supply	
GND	Ground	

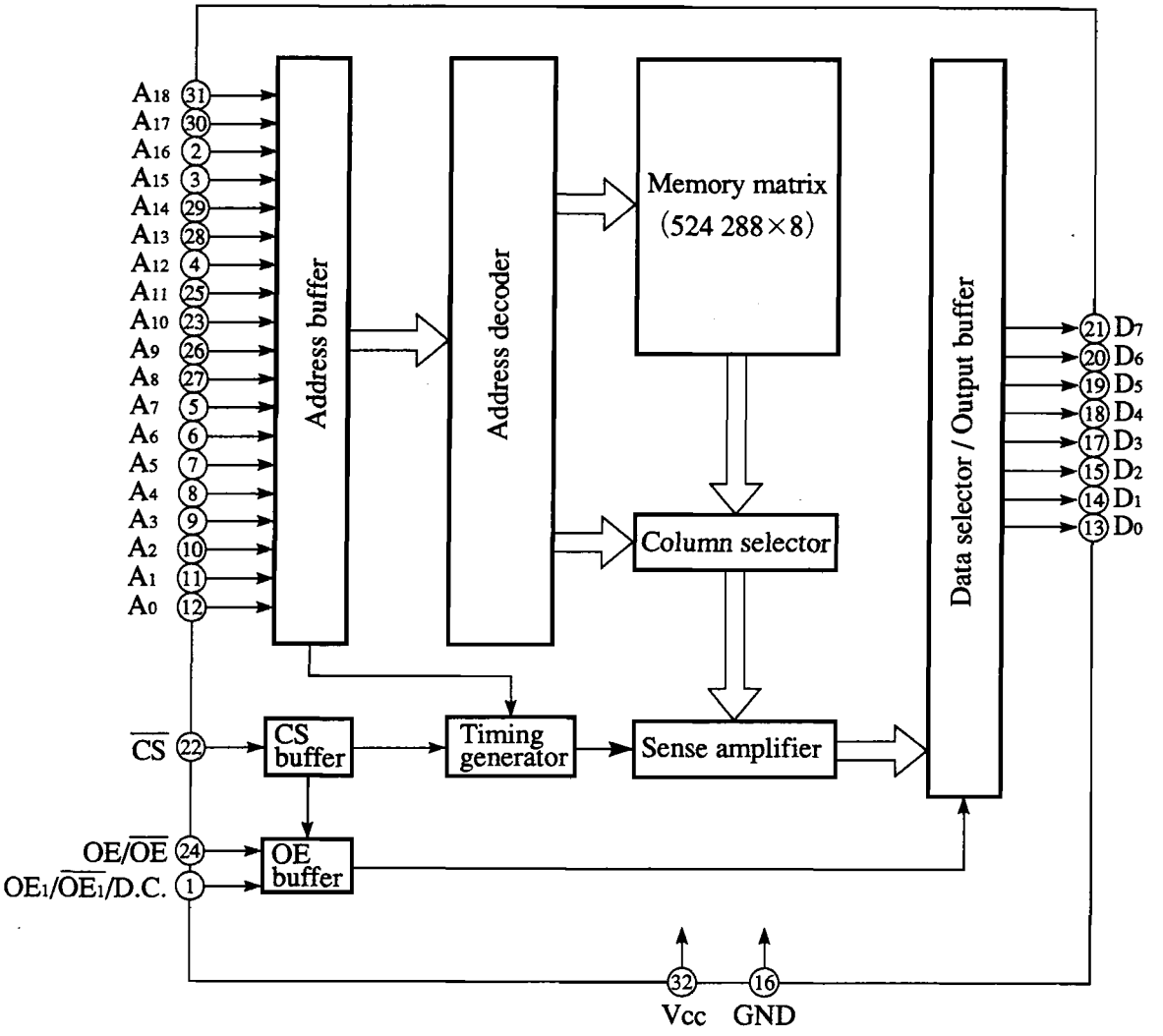
Note 1. Active levels of OE/$\overline{OE}$ and OE_1/$\overline{OE_1}$/D.C. are programmable by mask. When the D.C. is selected out of OE_1/$\overline{OE_1}$/D.C., it is fixed to an active level. (Then it is recommended to apply either "High" or "Low" to the D.C. pin.)

■ Pin Connections



Top View

Block Diagram



Truth Table

$\overline{CS}$	$OE_1/\overline{OE_1}$	$OE/\overline{OE}$	Data output	Supply current
High	X	X	High-impedance	Standby
Low	L/H	X	High-impedance	Operating
Low	X	L/H	High-impedance	Operating
Low	H/L	H/L	D_0-D_7	Operating

X : Don't Care

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−65 to +150	℃

Recommended Operating Conditions

(Ta=0 to 70 ℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V

■ DC Characteristics

(V_{CC}=5 V±10%、Ta=0 to 70 ℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Input "Low" voltage	V_{IL}		−0.3		0.8	V	
Output "High" voltage	V_{OH}	I_{OH}=−400 μA	2.4			V	
Output "Low" voltage	V_{OL}	I_{OL}=2.0 mA			0.4	V	
Input leakage current	$\|I_{LI}\|$	V_{IN}=0 V, V_{CC}			10	μA	
Output leakage current	$\|I_{LO}\|$	V_{OUT}=0 V, V_{CC}			10	μA	2
Supply current (Operating)	I_{CC1}	t_{RC}=80 ns			90	mA	3
	I_{CC2}	t_{RC}=1.0 μs			70	mA	
	I_{CC3}	t_{RC}=80 ns			85	mA	4
	I_{CC4}	t_{RC}=1.0 μs			65	mA	
Supply current (Standby)	I_{SB}	$\overline{CS}$=V_{IH}			40	mA	
Input capacitance	C_{IN}	f=1.0 MHz, Ta=25 ℃			10	pF	
Output capacitance	C_{OUT}				10	pF	

Note 2. $\overline{CS}$=V_{IH}、$\overline{OE}$/OE=V_{IH}/V_{IL}、$\overline{OE_1}$/OE_1=V_{IH}/V_{IL}

Note 3. V_{IN}=V_{IH}/V_{IL}、$\overline{CS}$=V_{IL} (Output is open)

Note 4. V_{IN}=V_{CC}−0.2 V/0.2 V、$\overline{CS}$=0.2 V (Output is open)

■ AC Characteristics

(V_{CC}=5 V±10%、Ta=0 to 70 ℃)

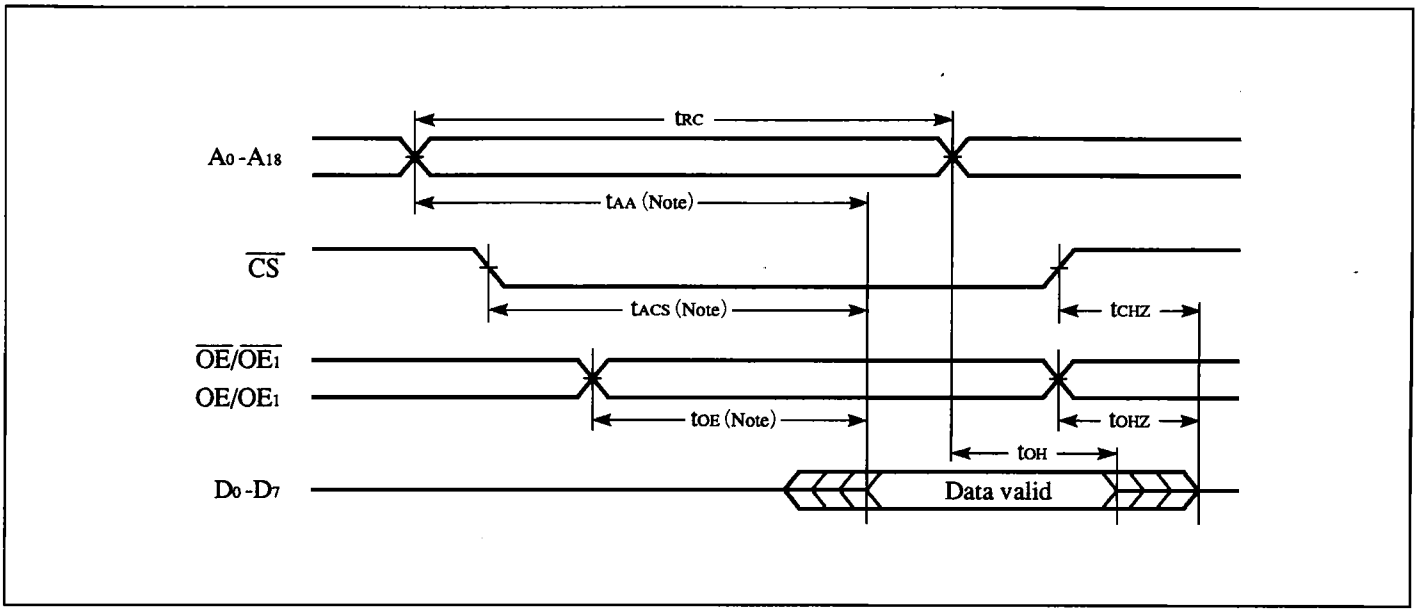
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t_{RC}	80			ns	
Address access time	t_{AA}			80		
Chip select access time	t_{ACS}			80		
Output enable delay time	t_{OE}			50		
Output hold time	t_{OH}	5				
Output floting time	t_{CHZ}			40		5
	t_{OHZ}			40		

Note 5. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC Test Conditions

- Input voltage amplitude : 0.4 to 2.6 V
- Input signal rise / fall time : 10 ns
- Input reference level : 1.5 V
- Output reference level : 1.5 V
- Output load condition : 1TTL+100 pF

Timing Diagram



Note. The output data becomes valid when the last interval t_{AA}, t_{ACE} or t_{OE} have concluded.

■ Sharp's Product Line-up (4M-bit Mask ROM)

★Under development

Configuration (words×bits)	*1 Pinout	Model No.	User's No.	Access time (ns) MAX. Cycle time (ns) MAX.	Supply current (mA) MAX.	Supply voltage (V)	Package
512k× 8	J	LH53H4100D/N	LH5H41XX	80	90	5±10%	32DIP/32SOP
512k× 8	J	LH534700D/N	LH5S47XX	100	75	5±10%	32DIP/32SOP
512k× 8	J	LH534R00AD/AN/AS/ASR	LH5347XX	120	65	5±10%	32DIP/32SOP/32TSOP (II) forward bend/ 32TSOP (II) reverse bend
512k× 8	F	LH534A00T	LH5S4AXX	120	65	5±10%	32TSOP (I) forward bend
512k× 8	F	LH534B00T	LH5S4BXX	120	60	5±10%	40TSOP (I) forward bend
256k×16	J	LH534Y00D/U	LH534YXX	120	65	5±10%	40DIP/44QFJ
512k× 8 256k×16	M	LH53H4000D/N	LH5H40XX	80	90	5±10%	40DIP/40SOP
512k× 8 256k×16	M	LH534600BD/BN/BT/BTR	LH534VXX	100	75	5±10%	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend
512k× 8 256k×16	M	LH534P00AD/AN/AT/ATR	LH5348XX	120	65	5±10%	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend
512k× 8 256k×16	M	LH53B4P00D/N *7	LH5B4PXX	120〔50〕	100	5±10%	40DIP/40SOP
512k× 8 256k×16	M	★LH53V4P00N/T	LH5V4PXX	120	30	2.7 to 3.6	40SOP/48TSOP (I) forward bend
512k× 8 256k×16	M	LH53V4000D/N/T/TR	LH5V40XX	200 (*4) 100 (*2)	30 (*6)	3.0 to 5.5	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend
512k× 8 256k×16	M	LH534000BD/BN/BT/BTR-S	LH534SXX	500 (*3) 200 (*2)	15 (*5)	2.6 to 5.5	40DIP/40SOP/48TSOP (I) forward bend/ 48TSOP (I) reverse bend

*1 J : JEDEC standard EPROM pinout, F : Flash Memory compatible pinout, M : Mask ROM specific pinout
*2 4.5 V≦Vcc≦5.5 V
*3 2.6 V≦Vcc<4.5 V
*4 3.0 V≦Vcc<4.5 V
*5 2.6 V≦Vcc≦3.4 V
*6 3.0 V≦Vcc≦3.6 V
*7 With page mode. Figures in brackets indicate access time during page mode.

MROM 5V LH53H4100 High Speed 4M