

## DUAL DIFFERENTIAL COMPARATORS

The LM393 dual differential comparator is made up of two voltage comparators that operate using the same power supply. The supply voltage can range from 2 to 36 volts.

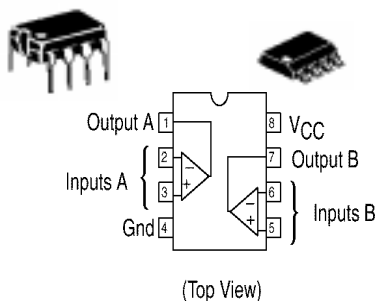
Dual supplies can also be used as long as the difference between them is 2 to 36 volts. The LM393 is designed to operate at a temperature range of 0°C to 70°C.

### FEATURES

- Single or dual supplies
- 2 to 36 V Supply
- Low Input Bias Current
- Low Input Offset Voltage
- Low Input Offset Current
- Low Supply Current Drain
- Output Compatible with TTL, MOS, and CMOS

### PIN ARRANGEMENT

8 DIP LM393CD      8 SOP LM393CS



### ABSOLUTE MAXIMUM RATINGS

| Item  | Symbol                     | Rating           | Unit        |
|---|----------------------------|------------------|-------------|
| Power Supply Voltage                                      | $V_{CC}$                   | +36 or $\pm 18$  | V           |
| Input Differential Voltage Range                          | $V_{IDR}$                  | 36               | V           |
| Input Common Mode Voltage Range                           | $V_{ICR}$                  | -0.3 to +36      | V           |
| Output Short Circuit-to-Ground<br>Output Sink Current (1) | $I_{SC}$<br>$I_{Sink}$     | Continuous<br>20 | mA          |
| Power Dissipation @ 25°C<br>Derate above 25°C             | $P_D$<br>$1/R_{\theta JA}$ | 570<br>5.7       | mW<br>mW/°C |
| Operating Ambient Temperature Range                       | $T_A$                      | 0 to 70          | °C          |
| Operating Junction Temperature                            | $T_J$                      | 125              | °C          |
| Storage Temperature Range                                 | $T_S$                      | -65 to 150       | °C          |

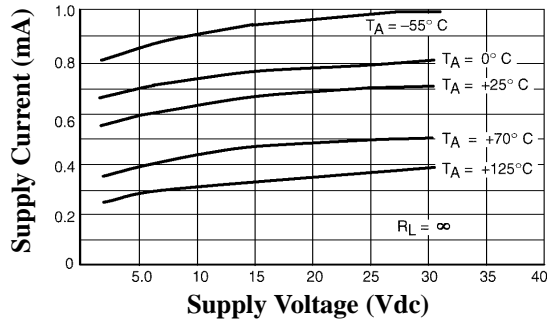
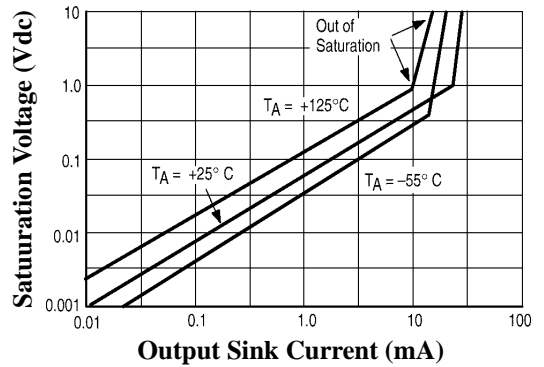
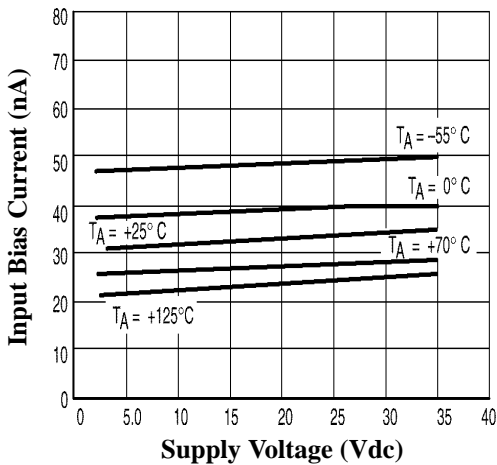
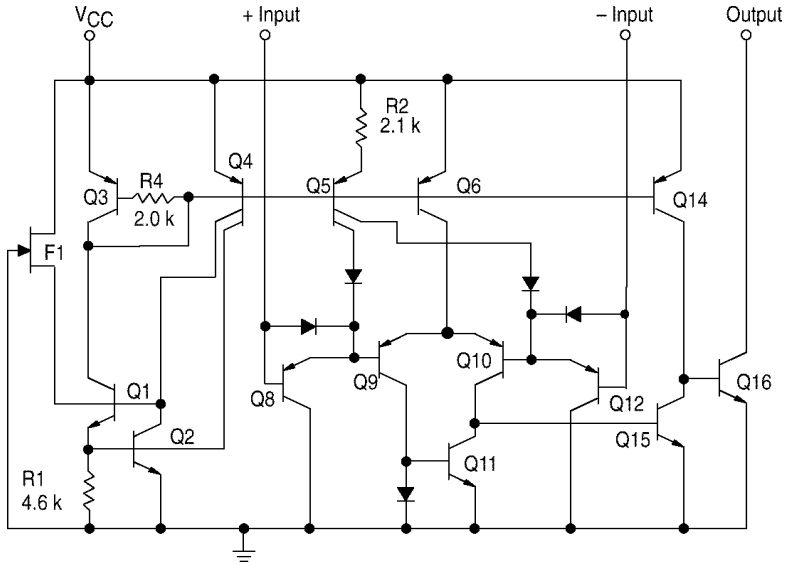
- Notes:
1. The max. output current may be as high as 20 mA, independent of the magnitude of  $V_{CC}$ , output short circuits to  $V_{CC}$  can cause excessive heating and eventual destruction.
  2. At output switch point,  $V_o = 1.4$  Vdc,  $R_s = 0 \Omega$  with  $V_{CC}$  from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0V to  $V_{CC} = -1.5V$ ).
  3. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
  4. Input common mode of either input should not be permitted to go more than 0.3V negative of ground or minus supply. The upper limit of common mode range is  $V_{CC} - 1.5V$ .
  5. Response time is specified with a 100mV step and 5.0mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
  6. The comparator will exhibit proper output state if one of the inputs becomes greater than  $V_{CC}$ , the other input must remain within the common mode range. The low input state must not be less than  $-0.3V$  of ground or minus supply.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0\text{Vdc}$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  (unless otherwise noted)

| Item  | Symbol     | Min    | Typ | Max                          | Unit          |
|---|------------|--------|-----|------------------------------|---------------|
| Input Offset Voltage (2)<br>$T_A = 25^\circ\text{C}$<br>$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  | $V_{IO}$   | ---    | 1.0 | 5.0<br>9.0                   | mV            |
| Input Offset Current<br>$T_A = 25^\circ\text{C}$<br>$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  | $I_{IO}$   | ---    | 5.0 | 50<br>150                    | nA            |
| Input Offset Current (3)<br>$T_A = 25^\circ\text{C}$<br>$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  | $I_{IB}$   | ---    | 25  | 250<br>400                   | nA            |
| Input Common Mode Voltage Range (3)<br>$T_A = 25^\circ\text{C}$<br>$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$   | $V_{ICR}$  | 0<br>0 | --- | $V_{CC}-1.5$<br>$V_{CC}-2.0$ | V             |
| Voltage Gain<br>$R_L \geq 15\text{K}$ , $V_{CC} = 15\text{Vdc}$<br>$T_A = 25^\circ\text{C}$   | $A_{VOL}$  | 50     | 200 | ---                          | V/mV          |
| Large Signal Response Time<br>$V_{in} = \text{TTL Logic Swing}$<br>$V_{ref} = 1.4\text{Vdc}$<br>$V_{RL} = 5.0\text{Vdc}$ , $R_L = 5.1\text{K}$<br>$T_A = 25^\circ\text{C}$  | ---        | ---    | 300 | ---                          | ns            |
| Response Time (5)<br>$V_{RL} = 5.0\text{Vdc}$ , $R_L = 5.1\text{K}$<br>$T_A = 25^\circ\text{C}$   | $t_{TLH}$  | ---    | 13  | ---                          | $\mu\text{s}$ |
| Input Differential Voltage (6)<br>All $V_{in} \geq \text{GND}$ or $V\text{-Supply}$<br>(if used)  | $V_{ID}$   | ---    | --- | $V_{CC}$                     | V             |
| Output Sink Current<br>$V_{in-} \geq 1.0\text{Vdc}$ , $V_{in+} = 0\text{Vdc}$<br>$V_o \leq 1.5\text{Vdc}$ , $T_A = 25^\circ\text{C}$  | $I_{Sink}$ | 6.0    | 16  | ---                          | mA            |
| Output Saturation Voltage<br>$V_{in-} \geq 1.0\text{Vdc}$ , $V_{in+} = 0\text{Vdc}$<br>$I_{Sink} \leq 4.0\text{mA}$ , $T_A = 25^\circ\text{C}$<br>$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$  | $V_{OL}$   | ---    | 150 | 400<br>700                   | mV            |
| Output Leakage Current<br>$V_{in-} = 0\text{Vdc}$ , $V_{in+} \geq 1.0\text{Vdc}$<br>$V_o = 5.0\text{Vdc}$ , $T_A = 25^\circ\text{C}$<br>$V_{in-} = 0\text{Vdc}$ , $V_{in+} \geq 1.0\text{Vdc}$<br>$V_o = 30\text{Vdc}$ , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ | $I_{OL}$   | ---    | 0.1 | ---                          | nA            |
| Supply Current<br>$R_L = \infty$ , $T_A = 25^\circ\text{C}$<br>$R_L = \infty$ , $V_{CC} = 30\text{V}$   | $I_{CC}$   | ---    | 0.4 | 1.0<br>2.5                   | mA            |

## CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



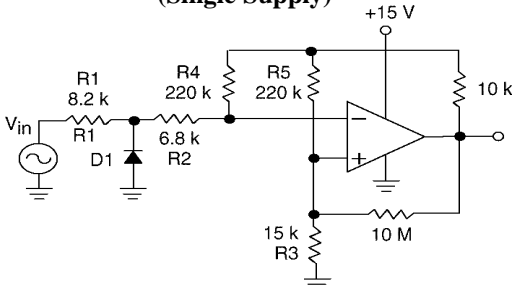
## APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions ( $V_{OL}$  to  $V_{OH}$ ). To alleviate this situation, input resistors  $< 10\text{ k}\Omega$  should be used.

The addition of positive feedback ( $< 10\text{ mV}$ ) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than  $-0.3\text{ V}$  should not be used.

### Zero Crossing Detector (Single Supply)

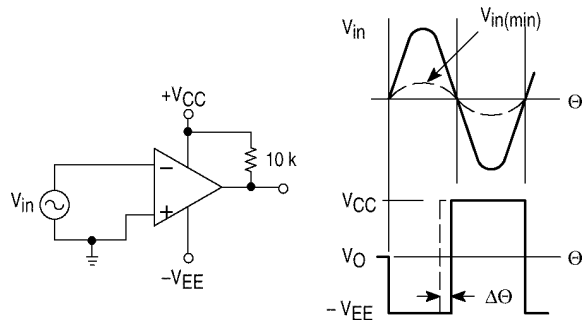


D1 prevents input from going negative by more than  $0.6\text{ V}$ .

$$R1 + R2 = R3$$

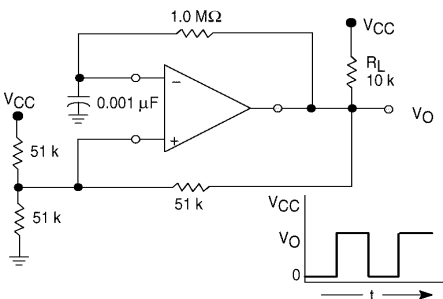
$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing.}$$

### Zero Crossing Detector (Split Supply)

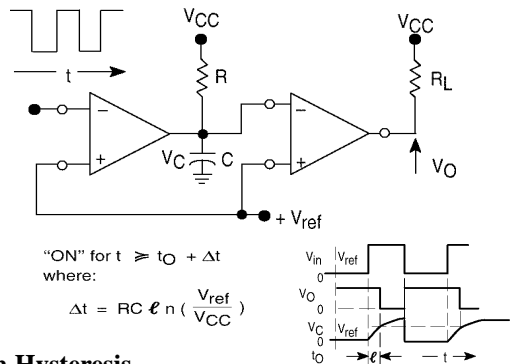


$$V_{in(min)} \approx 0.4\text{ V peak for } 1\% \text{ phase distortion } (\Delta\theta).$$

### Free-Running Square Wave Oscillator



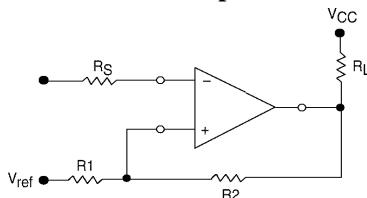
### Time Delay Generator



"ON" for  $t \geq t_O + \Delta t$   
where:

$$\Delta t = RC \ln \left( \frac{V_{ref}}{V_{CC}} \right)$$

### Comparator With Hysteresis



$$R_S = R1 \parallel R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref}) R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O\text{ Low}}) R1}{R1 + R2}$$