LinearDimensions SEMICONDUCTOR

LND TRM34

LOW POWER 300 TO 500 MHz FSK TRANSMITTER

General Description

The LND TRM34 is a low power Frequency Shift Keying (FSK) transmitter designed to operate at transmit frequencies between 300 and 500MHz. It is comprised of a frequency synthesizer and modulator, which accepts a simple CMOS digital data input and generates an FSK modulated output. Output power can be adjusted to a maximum of 2dBm. The LND TRM34 has been optimized for use in battery-powered applications with low current consumption in both transmit and standby modes.

How Does it Work

Simply connect the supply (as low as 2.6V), an external oscillator to RO1 and RO2, and all ground connections. The chip converts logic level inputs to balanced, complimentary, frequency modulated outputs, Out1 and Out 2. Output power can be adjusted using resistor values in Table 5, and can be easily switched with logic input to Standby Mode (extremely low power) when not transmitting. Component selections, network, and antenna options are included in this document.

Applications

- Wireless office and home security systems
- Automotive remote locking/starting
- Consumer remote control units
- Radio data transmission
- Low power telemetry

Features

- Low current consumption in transmit mode
- Low standby current (typically a few nA)
- Conforms to requirements of ETSI-300-220, PT1340 and FCC Part 15
- Easy to use with low external component count and cost
- No discrete external inductors required
- Adjustable output power level

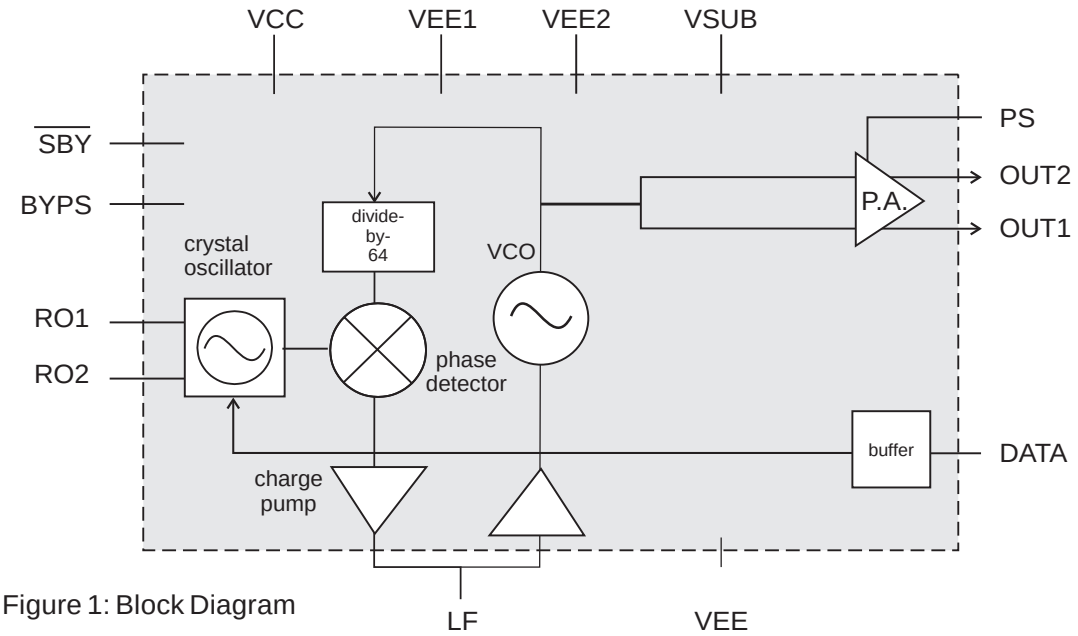


Figure 1: Block Diagram

Theory of operation

The LND TRM34 comprises three main elements:

1 Input buffer and modulator

2 Frequency synthesizer for generation of the RF output carrier from a low frequency external crystal

3 Power amplifier for driving an external antenna

The IC accepts a digital CMOS input, and modulates a fixed amplitude RF carrier in frequency according to the digital input level. The RF carrier is generated by the on-chip phase locked loop (PLL) frequency synthesizer. This contains a fixed divider which ensures that the RF output frequency is 64 times the crystal reference frequency. The power amplifier provides a variable output level of up to 2 dBm of output power depending upon the value of an external resistor RI.

The PA has balanced outputs OUT1 and OUT2 which are in open collector configuration. A balanced output is used since it provides a high degree of suppression of even-order harmonics of the fundamental. Odd order harmonic suppression is achieved using on-chip cancellation techniques.

Electrical characteristics

Table 1: Absolute maximum ratings

Parameter	Conditions	Symbol	Min	Max	Unit
Supply voltage		VCC	-0.3	+7.0	V
Input voltage - Logic Inputs	DATA & $\overline{SBY}$ pins		-0.3 V	VCC + 0.3V	
Input Current - Logic Inputs	DATA & $\overline{SBY}$ pins		-1.0	+1.0	mA
Storage temperature			-40	150	°C
Junction temperature			-40	150	°C

Table 2: Operating conditions
@ 434 MHz; @ 318 MHz

Parameter	Symbol	Min	Max	Unit
Supply voltage	VCC	2.6	4.8	V
Ambient temperature	Ta	-40	65	°C

Note:
All specification parameters guaranteed only with the following components
(please refer to figure 2 for application circuit):

RF transformer	Mini-Circuits TC4-14
Crystal	Euroquartz B537 6.78-MHz crystal (Cicad = 10 pF)
	R1 = 3.9 k R2 = 3.3 k C7 = 1 nF C8 = 47 pF C1 = C2 = 22 pF

Table 3: DC Characteristics at 3.0V VCC and 23ºC ambient temperature
all parameters 100% production tested under these conditions unless otherwise stated

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Standby Current	SBY = low	Iccstb		0.1	1	µA
Supply Current	including open-collector output currents	Icclow			25	mA
DATA logic high level	guaranteed by design	Vhigh	0.7*VCC		VCC+0.3	
DATA logic low level	guaranteed by design	Vlow	-0.3V		0.3*VCC	
DATA input current	guaranteed by design -0.3 < Vin < VCC+0.3	Idata	-10		+10	µA
Bias voltage on pin PS	guaranteed by design I(PS) = 100 µA	V(PS)		0.4		V

Electrical characteristics (continued)

Table 4: AC Characteristics at 3.0V VCC and 23ºC ambient temperature, fc = 433.92 MHz, unless otherwise stated
all parameters 100 % production tested under these conditions unless otherwise stated

Parameter	Conditions	Symbo	Min	Typ	Max	Unit
Maximum Carrier Frequency		fcmax	440			MHz
Minimum Carrier Frequency		fcmin			290	MHz
Maximum Data Rate	received BER<1% with receiver pre-detection bandwidth matched to data rate	Rmfsk		200		kbits/s
Frequency Deviation (TH7106 in SOP)	static peak-to peak value: crystal and system dependent	Δ f		20		kHz
Frequency Deviation (TH7106 in SSOP)	static peak-to peak value: crystal and system dependent	Δ f		22		kHz
Reference Frequency	guaranteed by design, external crystal	fref	4.5		7.0	MHz
Output Power	with R1=3.9 kOhms	Δ Po		0.5		dBm
2nd Harmonic		Δ P2		-34	-29	dBc
3rd Harmonic		Δ P3		-35	-28	dBc
Reference Spurious	at fc + (fref to 3fref)	Pref		-45	-40	dBc
Phase Noise	guaranteed by design, at 10 kHz offset	PN		-75		dBc/Hz
VCO gain	guaranteed by design	KVCO		125		MHz/V
Phase detector gain	guaranteed by design	KPD		16		µA/rad

Matching network and antenna options

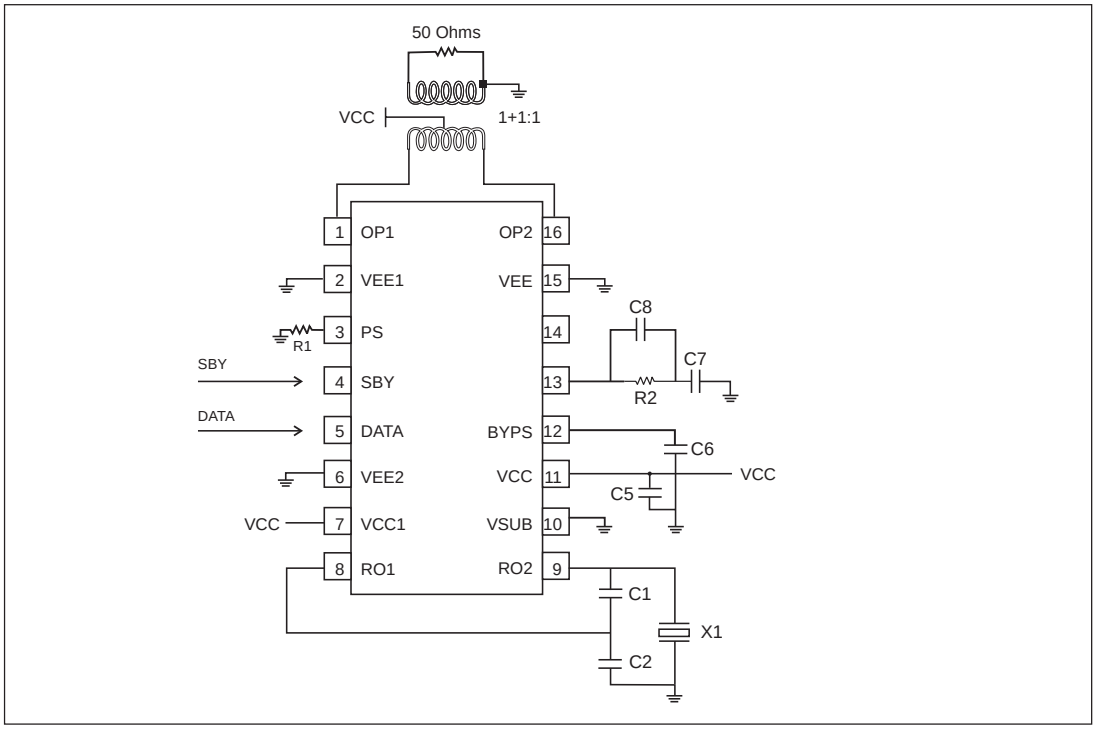


Figure 2: Application Diagram

Matching network and antenna options (continued)

Figure 2 shows a typical application diagram. In order to minimise second harmonic distortion, a differential output configuration is recommended. The LND TRM34 needs the following:

1) a dc bias reference to VCC (preferrably through direct connection of a loop antenna connected to VCC at its centre, or use of printed bias inductors with a connection to VCC). Linear's TRM3x series of evaluation boards provide large and small loop antenna solutions for customers to copy. These boards require a minimum number of external components, and importantly no discrete inductors are required. For driving an external single-ended antenna, a high efficiency printed balun is also available.

   For optimum operation, the following points are highlighted:

1) The IC can provide 7.5mA of current into the load
2) for maximum output power, it is recommended that the antenna load be transformed to an impedance of 200Ohms (RPS is set at 3.9kOhms)

Table 5: Output Power Settings		
R (kOhms)	Output power (dBm)	Current cons. (mA)
2.8	2	25
3.8	0	22
5.2	-2	20
6.7	-4	19
8.5	-6	18
9.7	-8	17
10.3	-10	16
10.7	-12	16

3) the PLL synthesizer is designed to operate with an external second order loop as shown in figure 2, with component values as shown in Table 7. These values determine the loop bandwidth and dynamics and operation of the loop is not guaranteed for any other values
4) The bias current for the power amplifier directly controls the output current and hence the O/P power. This bias current is set by an external resistor connected between PS and ground. Output power versus RI values is shown in Table 5, for a differential load impedance of 200Ω.

Frequency deviation

The amount of frequency deviation depends upon the type of external crystal used. An on-chip capacitor of 3pF is switched in parallel with the crystal to shift its frequency of operation. For instance, on the TRM3x series of evaluation boards, the peak-to-peak frequency deviation possible with the supplied crystal is over 15kHz in SOP packaged parts and 25 kHz for SSOP packaged parts. The crystal parameters are specified as shown aside:

For smaller frequency deviations, then a less pullable crystal can be specified (eg 20 pF or 30 pF load crystals are less pullable). If peak-to-peak frequency deviations of much greater than 15kHz are required, then please consult Linear Dimensions for information on how to achieve this.

Table 6 - Crystal specifications	
Supplier/part number	Euroquartz: B537 Tel.: 0044146076477
Frequency	6.78 MHz
Package	HC49/U
Operating mode	AT
Calibration tolerance	+/-10 ppm
Temperature stability	+/-10 ppm
Operating temp range	-10 to + 60°C
Circuit loading	10 pF
Maximum ESR, R1	50 Ohms
Static capacitance (typical), Co	5 pF
Motional capacitance (typical), C1	20 fF
Pullability	40 ppm/pF

External components

Table 7: Recommended External Components				
Component	Function	Value	Tolerance	Units
C1	Crystal Oscillator	22 pF	± 5%	pF
C2	Crystal Oscillator	22 pF	± 5%	pF
C5	Supply Decoupling	100	± 20%	nF
C6	Regulator Decoupling	100	± 20%	nF
C7	PLL Loop Filter	1	± 5%	nF
C8	PLL Loop Filter	47	± 5%	pF
R1	O/P power set	3.9	± 5%	kOhms
R2	PLL Loop Filter	3.3	± 5%	kOhms
X1	Crystal	6.78	< 20ppm	MHz

I/O interfacing

Table 8: I/O interfacing

No.	Signal	Description
1	OP1	PA Output
2	VEE1	Ground (0V)
3	PS	Power Set
4	SBY	Standby (complete power down)
5	DATA	Data
6	VEE2	Ground (0V)
8	RO1	Reference Oscillator (emitter)
9	RO2	Reference Oscillator (base)
10	VSUB	Substrate Connection (0V)
11	VCC	Supply (Battery)
12	BYPS	Power supply decoupling to ground
13	LF	Low Pass Filter
15	VEE	Ground (0V)
16	OP2	PA Output (complement)

Input and output interface diagrams

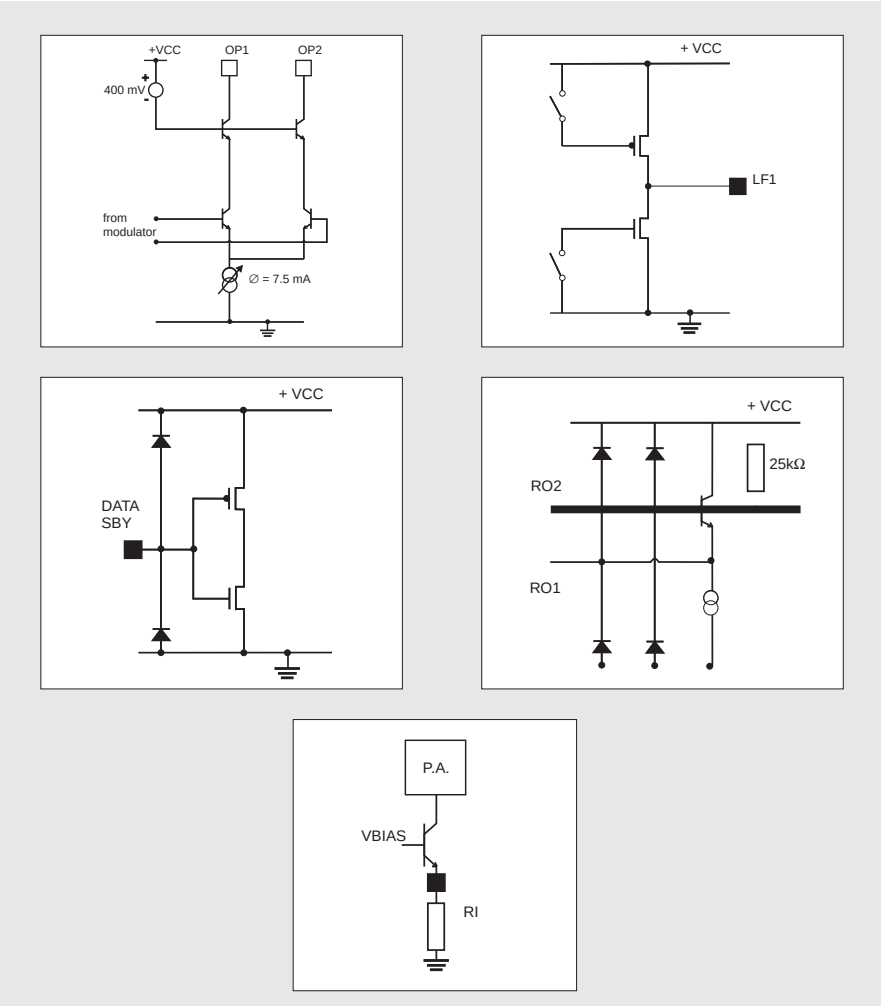
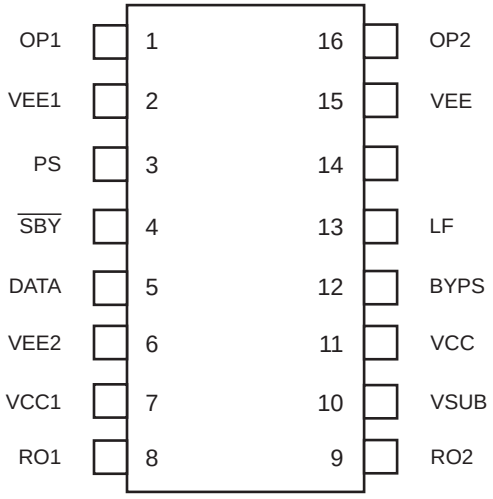


Figure 3: Input and output interface diagrams

Pinout Information



SOP 16 / SSOP 16

Package Information