

**AMIC**

**LP62S1024B-I Series**

**128K X 8 BIT LOW VOLTAGE CMOS SRAM**

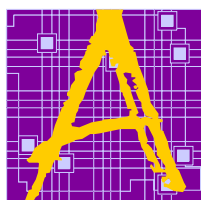
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**Document Title**

**128K X 8 BIT LOW VOLTAGE CMOS SRAM**

**Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	May 30, 2002	Preliminary
0.1	Add 32L Pb-Free TSSOP package type	October 2, 2002	
1.0	Final version release	July 18, 2003	Final
1.1	Change $I_{CCDR1}$ , $I_{CCDR2}$ (max.) from $3\mu A$ to $1\mu A$	June 29, 2004	
1.2	Add Pb-Free package type for all parts	August 9, 2004	
1.3	Change Data Retention Spec. from 2V to 1.5V	January 23, 2007	
1.4	Add access time 45ns grade	December 26, 2008	



**AMIC**

## LP62S1024B-I Series

### 128K X 8 BIT LOW VOLTAGE CMOS SRAM

#### Features

- Power supply range: 2.7V to 3.6V
- Access times: 45/55/70 ns (max.)
- Current:
  - Very low power version: Operating: 30mA(max.)
  - Standby: 5uA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 1.5V (min.)
- Available in 32-pin SOP, TSOP, TSSOP (8 X 13.4mm) forward type and 36-pin CSP packages
- All Pb-free (Lead-free) products are RoHS compliant

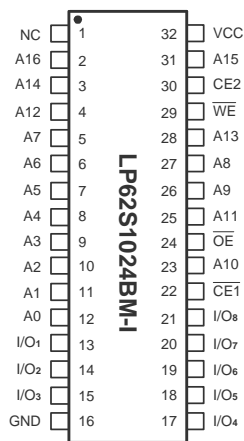
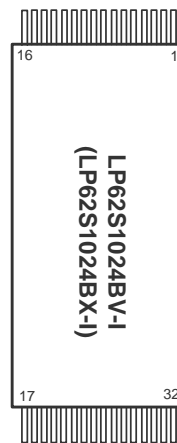
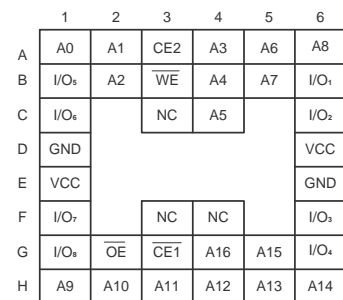
#### General Description

The LP62S1024B-I is a low operating current 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a low power voltage: 2.7V to 3.6V. It is built using AMIC's high performance CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. Two chip enable inputs are provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing. Data retention is guaranteed at a power supply voltage as low as 1.5V.

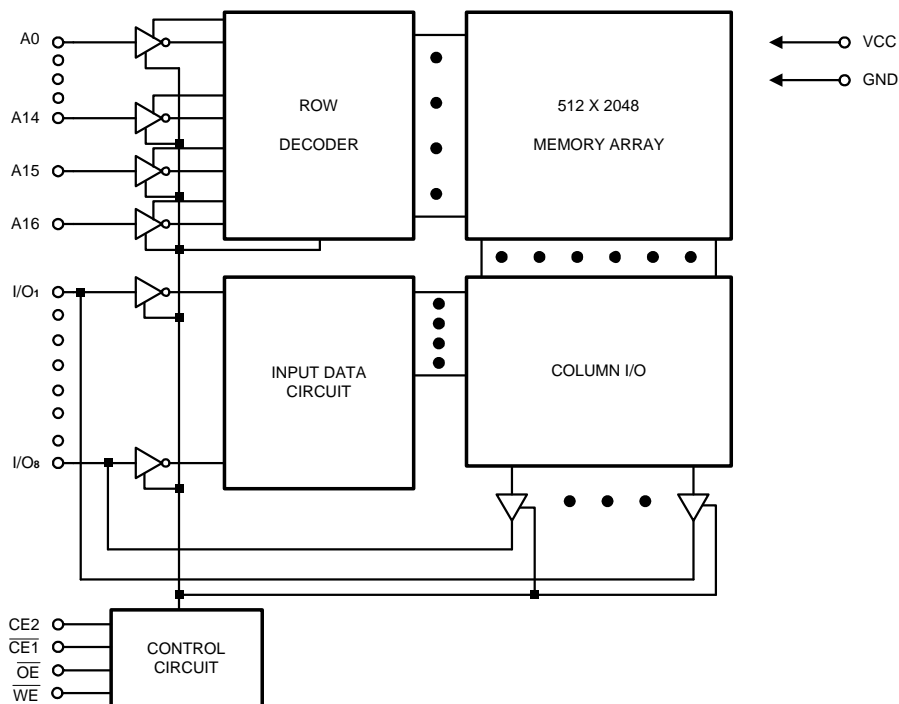
#### Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I <sub>CCDR</sub> , Typ.)	Standby (I <sub>SB1</sub> , Typ.)	Operating (I <sub>CC2</sub> , Typ.)	
LP62S1024B	-40°C ~ +85°C	2.7V~3.6V	45ns/55ns/70ns	0.05μA	0.08μA	1.5mA	32L SOP 32L TSOP 32L TSSOP 36B μBGA

1. Typical values are measured at VCC = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.
2. Data retention current VCC = 1.5V.

**Pin Configurations**
**■ SOP**

**■ TSOP/TSSOP**

**■ CSP (Chip Size Package)**
**36-pin Top View**


Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A11	A9	A8	A13	WE	CE2	A15	VCC	NC	A16	A14	A12	A7	A6	A5	A4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A3	A2	A1	A0	I/O <sub>1</sub>	I/O <sub>2</sub>	I/O <sub>3</sub>	GND	I/O <sub>4</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>	I/O <sub>7</sub>	I/O <sub>8</sub>	CE1	A10	OE

**Block Diagram**


**Pin Descriptions - SOP**

Pin No.	Symbol	Description
1	NC	No Connection
2 - 12, 23, 25 - 28, 31	A0 - A16	Address Inputs
13 - 15, 17 - 21	I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Outputs
16	GND	Ground
22	$\overline{CE1}$	Chip Enable
24	$\overline{OE}$	Output Enable
29	$\overline{WE}$	Write Enable
30	CE2	Chip Enable
32	VCC	Power Supply

**Pin Description – TSOP/TSSOP**

Pin No.	Symbol	Description
1 - 4, 7, 10 - 20, 31	A0 - A16	Address Inputs
5	$\overline{WE}$	Write Enable
6	CE2	Chip Enable
8	VCC	Power Supply
9	NC	No Connection
21 - 23, 25 - 29	I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Outputs
24	GND	Ground
30	$\overline{CE1}$	Chip Enable
32	$\overline{OE}$	Output Enable

**Pin Description - CSP**

Symbol	Description	Symbol	Description
A0 - A16	Address Inputs	NC	No Connection
$\overline{WE}$	Write Enable	I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Output
$\overline{OE}$	Output Enable	VCC	Power Supply
$\overline{CE1}$	Chip Enable	GND	Ground
CE2	Chip Enable	--	--

**Recommended DC Operating Conditions**

 (T<sub>A</sub> = -40°C to +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.6	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	VCC + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	+0.6	V
C <sub>L</sub>	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

**Absolute Maximum Ratings\***

VCC to GND .....-0.5V to +4.6V  
 IN, IN/OUT Volt to GND ..... -0.5V to VCC +0.5V  
 Operating Temperature, T<sub>opr</sub> ..... -40°C to +85°C  
 Storage Temperature, T<sub>stg</sub> ..... -55°C to +125°C  
 Temperature Under Bias, T<sub>bias</sub> ..... -40°C to +85°C  
 Power Dissipation, P<sub>r</sub> ..... 0.7W

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = -40°C to +85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S1024B-45LLI/55LLI/70LLI		Unit	Conditions
		Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	-	1	μA	V <sub>IN</sub> = GND to VCC
I <sub>LO</sub>	Output Leakage Current	-	1	μA	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to VCC
I <sub>CC</sub>	Active Power Supply Current	-	3	mA	$\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub> I <sub>I/O</sub> = 0mA
I <sub>CC1</sub>	Dynamic Operating Current	-	30	mA	Min. Cycle, Duty = 100% $\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub> I <sub>I/O</sub> = 0mA
I <sub>CC2</sub>		-	3	mA	$\overline{CE1} = V_{IL}$ , CE2 = V <sub>IH</sub> V <sub>IH</sub> = VCC, V <sub>IL</sub> = 0V f = 1 MHz, I <sub>I/O</sub> = 0mA
I <sub>SB</sub>	Standby Power Supply Current	-	0.5	mA	VCC ≤ 3.3V, $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub>
I <sub>SB1</sub>		-	5	μA	VCC ≤ 3.3V, $\overline{CE1} \geq VCC - 0.2V$ or CE2 ≤ 0.2V, V <sub>IN</sub> ≥ 0V
V <sub>OL</sub>	Output Low Voltage	-	0.4	V	I <sub>OL</sub> = 2.1mA
V <sub>OH</sub>	Output High Voltage	2.2	-	V	I <sub>OH</sub> = -1.0mA

**Truth Table**

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	$I_{SB}, I_{SB1}$
	X	L	X	X	High Z	$I_{SB}, I_{SB1}$
Output Disable	L	H	H	H	High Z	$I_{CC}, I_{CC1}, I_{CC2}$
Read	L	H	L	H	D <sub>OUT</sub>	$I_{CC}, I_{CC1}, I_{CC2}$
Write	L	H	X	L	D <sub>IN</sub>	$I_{CC}, I_{CC1}, I_{CC2}$

Note: X = H or L

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

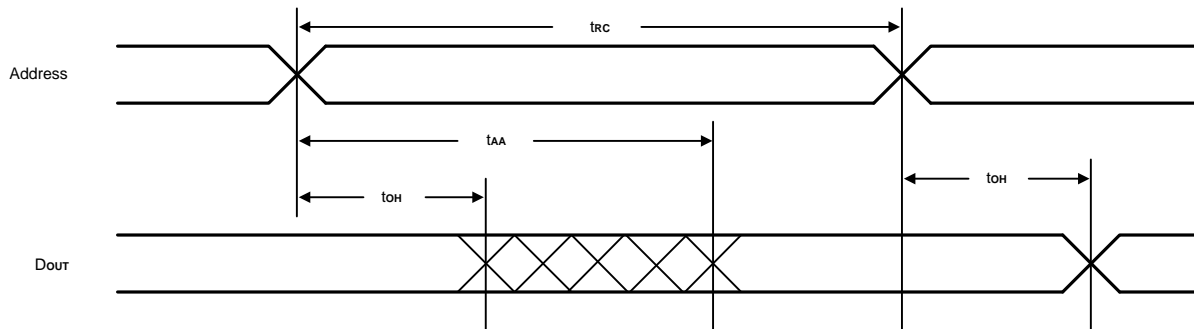
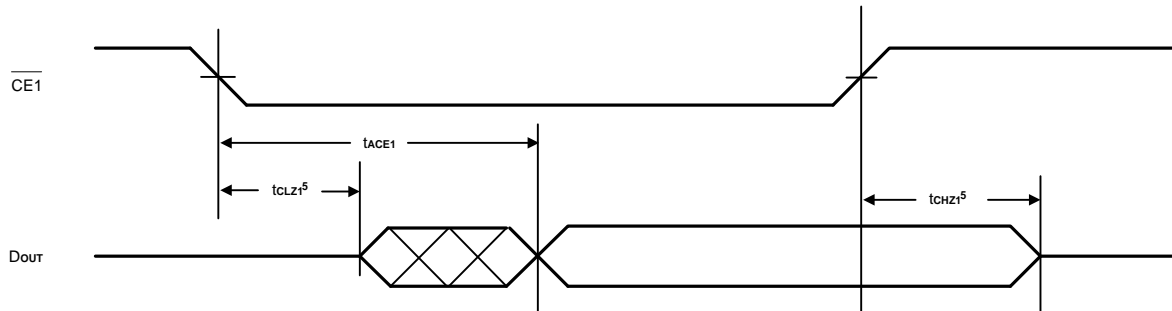
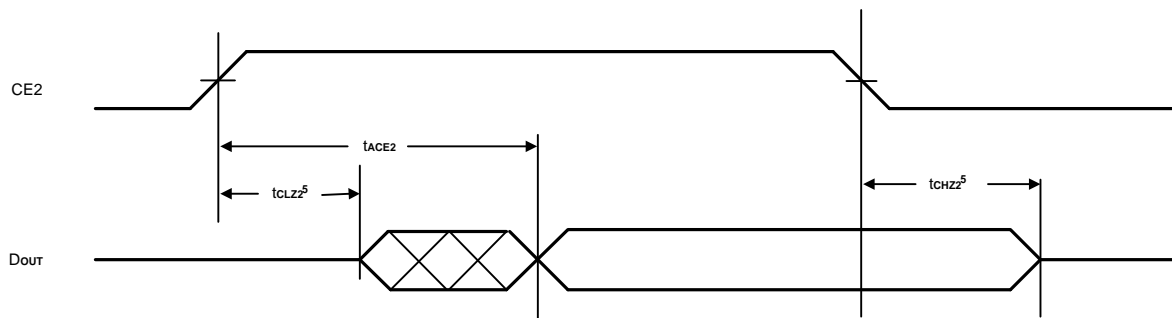
Symbol	Parameter	Min.	Max.	Unit	Conditions
$C_{IN}^*$	Input Capacitance		6	pF	$V_{IN} = 0V$
$C_{IO}^*$	Input/Output Capacitance		8	pF	$V_{IO} = 0V$

\* These parameters are sampled and not 100% tested.

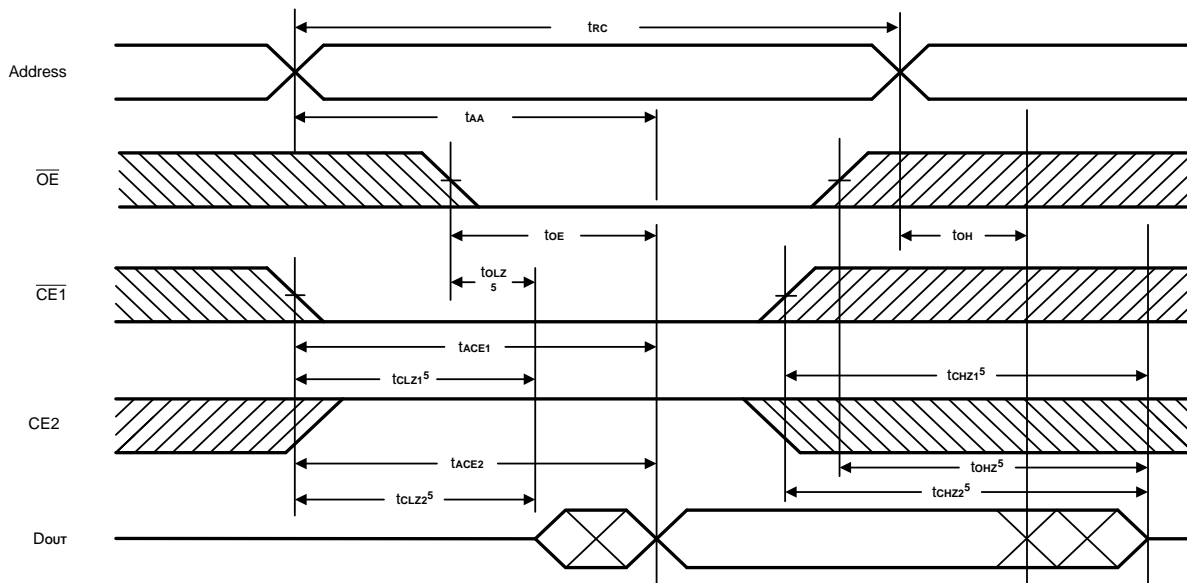
**AC Characteristics** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

Symbol	Parameter	LP62S1024B-45LLI		LP62S1024B-55LLI		LP62S1024B-70LLI		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle									
t <sub>RC</sub>	Read Cycle Time	45	-	55	-	70	-	ns	
t <sub>AA</sub>	Address Access Time	-	45	-	55	-	70	ns	
t <sub>ACE1</sub>	Chip Enable Access Time	$\overline{\text{CE1}}$	-	45	-	55	-	70	ns
t <sub>ACE2</sub>		CE2	-	45	-	55	-	70	ns
t <sub>OE</sub>	Output Enable to Output Valid	-	20	-	30	-	35	ns	
t <sub>CLZ1</sub>	Chip Enable to Output in Low Z	$\overline{\text{CE1}}$	5	-	10	-	10	-	ns
t <sub>CLZ2</sub>		CE2	5	-	10	-	10	-	ns
t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	5	-	ns	
t <sub>CHZ1</sub>	Chip Disable to Output in High Z	$\overline{\text{CE1}}$	0	15	0	20	0	25	ns
t <sub>CHZ2</sub>		CE2	0	15	0	20	0	25	ns
t <sub>OHZ</sub>	Output Disable to Output in High Z	0	15	0	20	0	25	ns	
t <sub>OH</sub>	Output Hold from Address Change	5	-	5	-	10	-	ns	
Write Cycle									
t <sub>WC</sub>	Write Cycle Time	45	-	55	-	70	-	ns	
t <sub>CW</sub>	Chip Enable to End of Write	35	-	50	-	60	-	ns	
t <sub>AS</sub>	Address Setup Time	0	-	0	-	0	-	ns	
t <sub>AW</sub>	Address Valid to End of Write	35	-	50	-	60	-	ns	
t <sub>WP</sub>	Write Pulse Width	35	-	40	-	50	-	ns	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns	
t <sub>WHZ</sub>	Write to Output in High Z	0	20	0	25	0	25	ns	
t <sub>DW</sub>	Data to Write Time Overlap	20	-	25	-	30	-	ns	
t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns	
t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	5	-	ns	

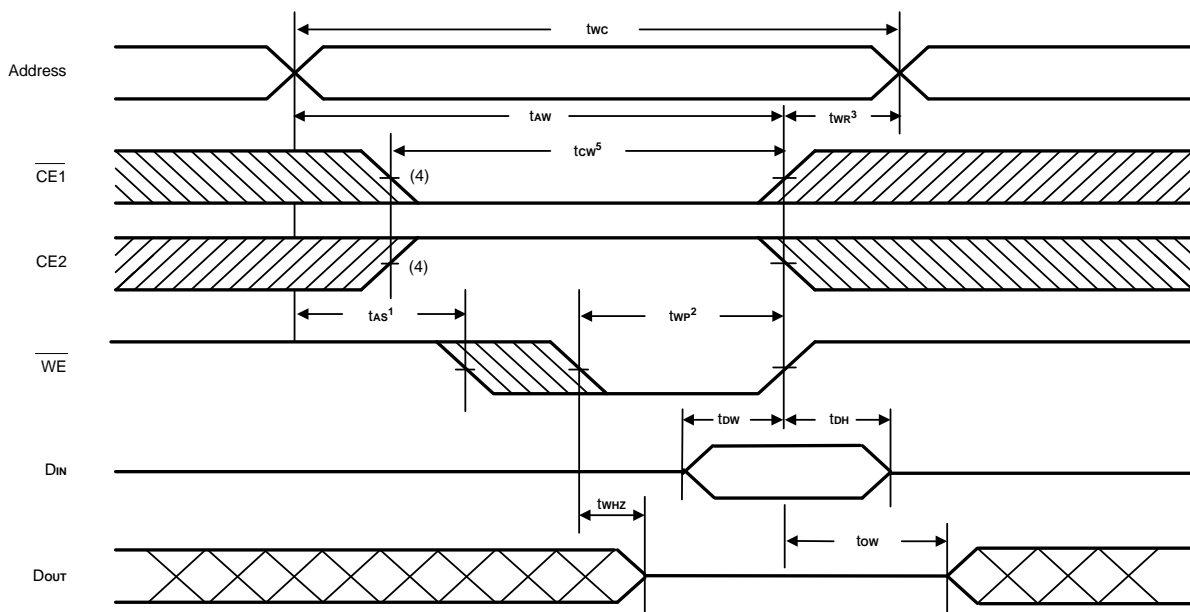
Notes: t<sub>CHZ1</sub>, t<sub>CHZ2</sub>, t<sub>OHZ</sub>, and t<sub>WHZ</sub> are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

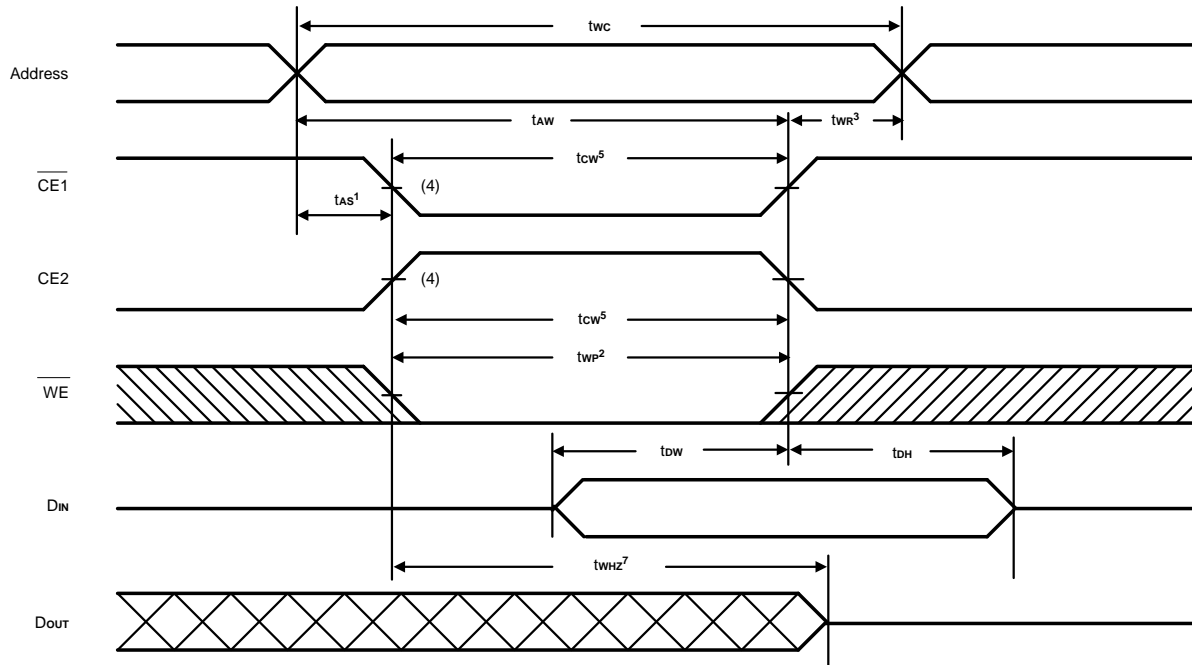
**Timing Waveforms**
**Read Cycle 1 (1, 2, 4)**

**Read Cycle 2 (1, 3, 4, 6)**

**Read Cycle 3 (1, 4, 7, 8)**




**Timing Waveforms (continued)**
**Read Cycle 4 <sup>(1)</sup>**


- Notes:
1.  $\overline{WE}$  is high for Read Cycle.
  2. Device is continuously enabled  $\overline{CE1} = V_{IL}$  and  $CE2 = V_{IH}$ .
  3. Address valid prior to or coincident with  $\overline{CE1}$  transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.
  6.  $\overline{CE2}$  is high.
  7.  $\overline{CE1}$  is low.
  8. Address valid prior to or coincident with  $CE2$  transition high.

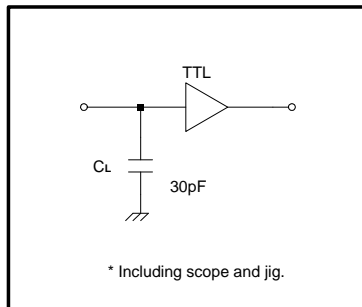
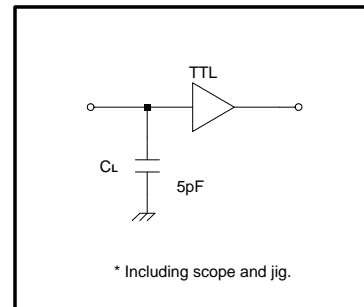
**Write Cycle 1 <sup>(6)</sup>**
**(Write Enable Controlled)**


**Timing Waveforms (continued)**
**Write Cycle 2  
(Chip Enable Controlled)**


- Notes:
1.  $t_{as}$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{wp}$ ) of a low  $\overline{CE1}$ , a high CE2 and a low  $\overline{WE}$ .
  3.  $t_{wr}$  is measured from the earliest of  $\overline{CE1}$  or  $\overline{WE}$  going high or CE2 going low to the end of the Write cycle.
  4. If the  $\overline{CE1}$  low transition or the CE2 high transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  5.  $t_{cw}$  is measured from the later of  $\overline{CE1}$  going low or CE2 going high to the end of Write.
  6.  $\overline{OE}$  is continuously low. ( $\overline{OE} = V_{IL}$ )
  7. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

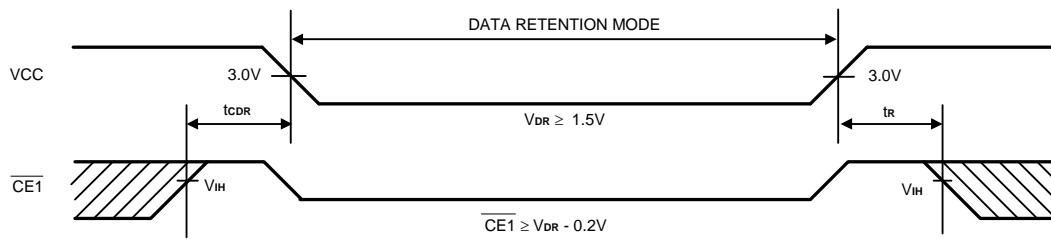
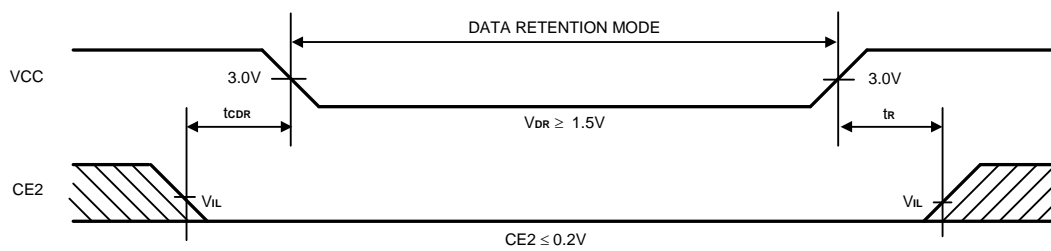
**AC Test Conditions**

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2


**Figure 1. Output Load**

**Figure 2. Output Load for  $t_{CL1}$ ,  $t_{CL2}$ ,  $t_{OHZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 
**Data Retention Characteristics** ( $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ )

Symbol	Parameter	Min.	Max.	Unit	Conditions
$V_{DR1}$	VCC for Data Retention	1.5	3.6	V	$\overline{CE1} \geq VCC - 0.2V$
$V_{DR2}$		1.5	3.6	V	$CE2 \leq 0.2V$ ,
$I_{CCDR1}$	Data Retention Current	-	1*	$\mu\text{A}$	$VCC = 1.5V$ , $\overline{CE1} \geq VCC - 0.2V$ , $V_{IN} \geq 0V$
$I_{CCDR2}$		-	1*	$\mu\text{A}$	$VCC = 1.5V$ , $CE2 \leq 0.2V$ , $V_{IN} \geq 0V$
$t_{CDR}$	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
$t_R$	Operation Recovery Time	5	-	ms	

\* LP62S1024B-45LLI/55LLI/70LLI  $I_{CCDR}$ : max.  $1\mu\text{A}$  at  $T_A = 0^\circ\text{C}$  to  $+40^\circ\text{C}$

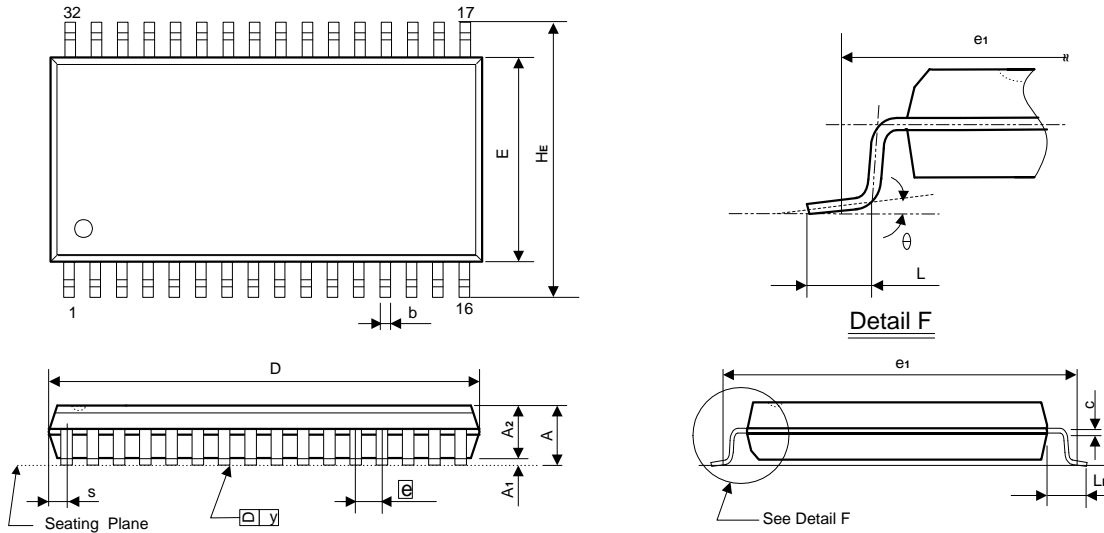
**Low VCC Data Retention Waveform (1) ( $\overline{\text{CE1}}$  Controlled)**

**Low VCC Data Retention Waveform (2) (CE2 Controlled)**


**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. ( $\mu$ A)	Package
LP62S1024BM-45LLIF	45	30	5	32L Pb-Free SOP
LP62S1024BV-45LLIF				32L Pb-Free TSOP
LP62S1024BX-45LLIF				32L Pb-Free TSSOP
LP62S1024BU-45LLIF				36L Pb-Free CSP
LP62S1024BM-55LLI	55	30	5	32L SOP
LP62S1024BM-55LLIF				32L Pb-Free SOP
LP62S1024BV-55LLI				32L TSOP
LP62S1024BV-55LLIF				32L Pb-Free TSOP
LP62S1024BX-55LLI				32L TSSOP
LP62S1024BX-55LLIF				32L Pb-Free TSSOP
LP62S1024BU-55LLI				36L CSP
LP62S1024BU-55LLIF				36L Pb-Free CSP
LP62S1024BM-70LLI	70	30	5	32L SOP
LP62S1024BM-70LLIF				32L Pb-Free SOP
LP62S1024BV-70LLI				32L TSOP
LP62S1024BV-70LLIF				32L Pb-Free TSOP
LP62S1024BX-70LLI				32L TSSOP
LP62S1024BX-70LLIF				32L Pb-Free TSSOP
LP62S1024BU-70LLI				36L CSP
LP62S1024BU-70LLIF				36L Pb-Free CSP

**Package Information**
**SOP (W.B.) 32L Outline Dimensions**

unit: inches/mm



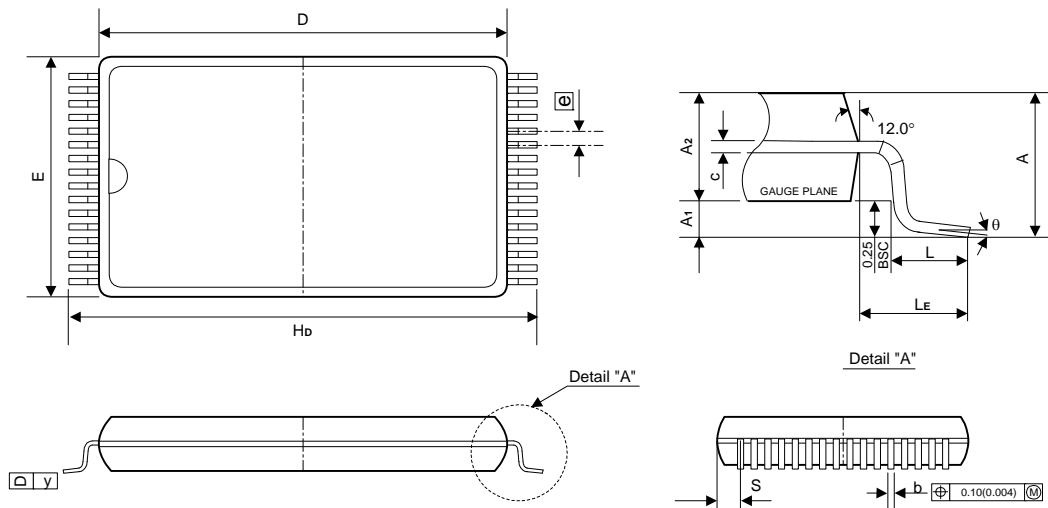
Symbol	Dimensions in inches	Dimensions in mm
A	0.118 Max.	3.00 Max.
A1	0.004 Min.	0.10 Min.
A2	0.106±0.005	2.69±0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.008 +0.004 -0.002	0.20 +0.10 -0.05
D	0.805 Typ. (0.820 Max.)	20.45 Typ. (20.83 Max.)
E	0.445±0.010	11.30±0.25
$\overline{e}$	0.050 ±0.006	1.27±0.15
e <sub>1</sub>	0.525 NOM.	13.34 NOM.
HE	0.556±0.010	14.12±0.25
L	0.031±0.008	0.79±0.20
LE	0.055±0.008	1.40±0.20
S	0.044 Max.	1.12 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e<sub>1</sub> is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

**Package Information**
**TSOP 32L TYPE I (8 X 20mm) Outline Dimensions**

unit: inches/mm



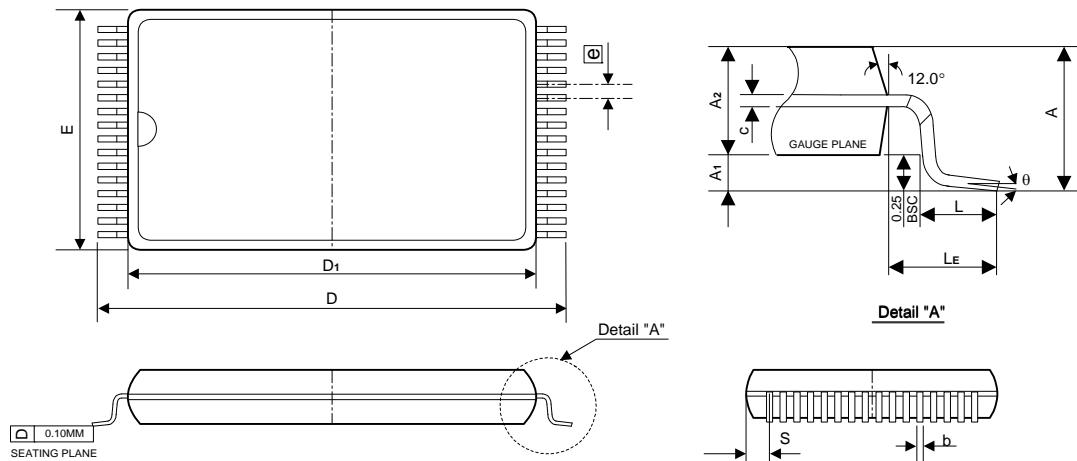
Symbol	Dimensions in inches	Dimensions in mm
A	0.047 Max.	1.20 Max.
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.001	0.15±0.02
D	0.724±0.004	18.40±0.10
E	0.315±0.004	8.00±0.10
e <sub>1</sub>	0.020 TYP.	0.50 TYP.
Hb	0.787±0.007	20.00±0.20
L	0.020±0.004	0.50±0.10
LE	0.031 TYP.	0.80 TYP.
S	0.0167 TYP.	0.425 TYP.
Y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e<sub>1</sub> is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

**Package Information**
**TSSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.049 Max.	1.25 Max.
A1	0.002 Min.	0.05 Min.
A2	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.0003	0.15±0.008
E	0.315±0.004	8.00±0.10
e	0.020 TYP.	0.50 TYP.
D	0.528±0.008	13.40±0.20
D1	0.465±0.004	11.80±0.10
L	0.02±0.008	0.50±0.20
LE	0.0266 Min.	0.675 Min.
S	0.0109 TYP.	0.278 TYP.
y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

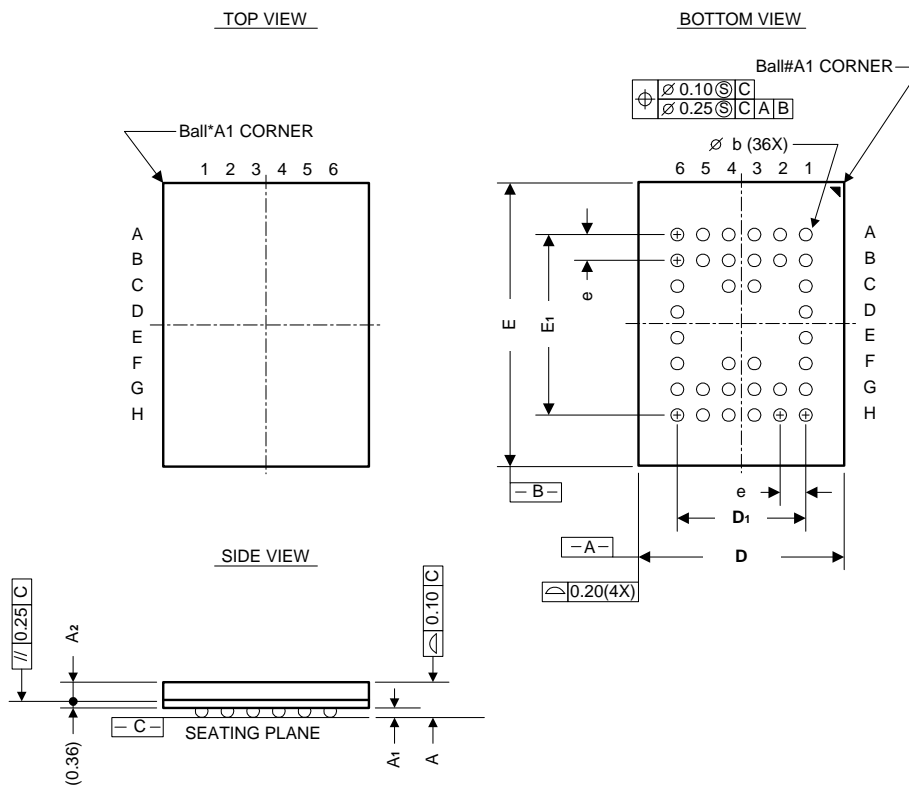
**Notes:**

1. The maximum value of dimension D includes end flash.
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4. Dimension S includes end flash.



**Package Information**
**36LD CSP (6 x 8 mm) Outline Dimensions**

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A <sub>1</sub>	0.16	0.21	0.26
A <sub>2</sub>	0.48	0.53	0.58
D	5.80	6.00	6.20
E	7.80	8.00	8.20
D <sub>1</sub>	---	3.75	---
E <sub>1</sub>	---	5.25	---
e	---	0.75	---
b	0.25	0.30	0.35

**Note:**

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.