

## High Input Voltage SMPS Start-up

### Features

- ▶ Accepts inputs from 35V to 450V
- ▶ Output current limiting
- ▶ For PWM ICs with start-up threshold voltage of 13.9 - 18.0V
- ▶ Very low power consumption after start-up

### Applications

- ▶ Notebook and laptop computers
- ▶ Telecommunication power supplies
- ▶ Battery chargers
- ▶ Motor controllers

### General Description

The Supertex LR745 is a high input voltage SMPS start-up circuit. The LR745 is ideally suited for use with industry standard low voltage PWM ICs having start thresholds of 13.9 - 18.0V. It allows the PWM ICs to be operated from rectified 120 or 240VAC lines, and eliminates the use of power resistors often used for this purpose.

The internal circuitry of the LR745 allows the PWM ICs to operate at a  $V_{CC}$  voltage below their start threshold voltage after start-up. The auxiliary voltage can be less than the start threshold voltage, which allows for improved efficiency. Current from the high voltage line is drawn only during the start-up period. After start-up, the internal high voltage line is disconnected from the IC, thereby reducing the continuous power dissipation to a minimum.

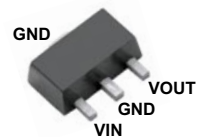
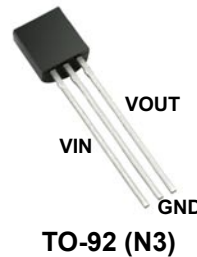
### Ordering Information

Device	Package Options	
	TO-92	TO-243AA (SOT-89)
LR745	LR745N3-G	LR745N8-G

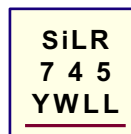
-G indicates package is RoHS compliant ('Green')



### Pin Configurations



### Package Markings



Y = Last Digit of Year Sealed  
 W = Code for Week Sealed  
 L = Lot Number  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

**TO-92 (N3)**



W = Code for Week Sealed  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

**TO-243AA (SOT-89) (N8)**

### Absolute Maximum Ratings

Parameter	Value
Input voltage	450V
Output voltage	25V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

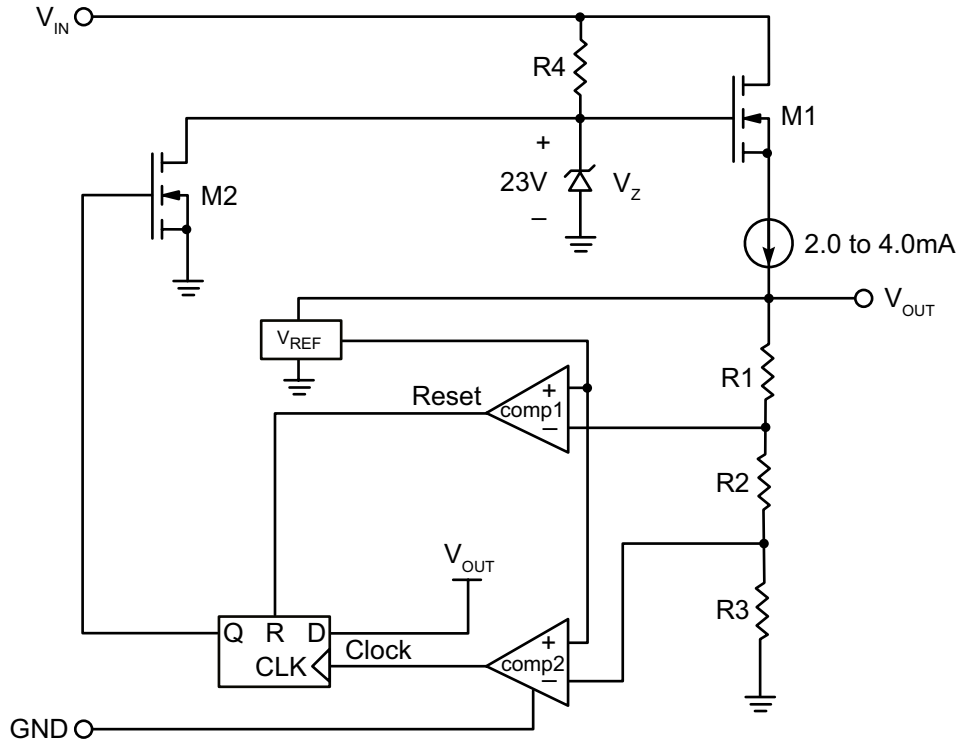
\* Distance of 1.6mm from case for 10 seconds.

**Electrical Characteristics**

(Test conditions unless otherwise specified:  $T_A = 25^{\circ}\text{C}$ ;  $V_{IN} = 450\text{V}$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{OUT}$	Output voltage	18.0	-	24	V	$I_{OUT} = 0$
	$V_{OUT}$ over temperature	17.7	-	24.3	V	$I_{OUT} = 0$ , $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
$I_{OUT}$	Output current limiting	2.0	3.0	4.0	mA	---
$V_{IN}$	Operating input voltage range	35	-	450	V	---
$I_{INQ}$	Input quiescent current	-	-	500	$\mu\text{A}$	$V_{IN} = 400\text{V}$ , $I_{OUT} = 0$
$V_{OFF}$	Output turn off voltage	12.6	13.25	13.9	V	---
	$V_{OFF}$ over temperature	12.3	13.25	14.2	V	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
$V_{RESET}$	Output reset voltage	6.3	7.0	7.7	V	---
	$V_{RESET}$ over temperature	6.0	7.0	8.0	V	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
$I_{OFF}$	$V_{IN}$ off-state leakage current	-	-	75	$\mu\text{A}$	$V_{IN} = 400\text{V}$
$V_{AUX}$	External voltage applied to $V_{OUT}$	-	-	22	V	---
$I_{AUX}$	Input current applied to $V_{OUT}$	-	-	500	$\mu\text{A}$	$V_{AUX} = 22\text{V}$

**Block Diagram**



## Block Diagram Detailed Description

The Supertex LR745 is a high voltage, switch-mode power supply start-up circuit which has 3 terminals:  $V_{IN}$ , GND, and  $V_{OUT}$ . An input voltage range of 35 - 450VDC can be applied directly at the input  $V_{IN}$  pin. The output voltage,  $V_{OUT}$ , is monitored by the 2 comparators, COMP1 and COMP2. An internal reference,  $V_{REF}$ , and resistor divider R1, R2, and R3 set the nominal  $V_{OUT}$  trip points of 7.0V for COMP1 and 13.25V for COMP2.

When a voltage is applied on  $V_{IN}$ ,  $V_{OUT}$  will start to ramp up from 0V. When  $V_{OUT}$  is less than 7.0V, the output of COMP1 will be at a logic high state, keeping the D flip flop in a reset state. The output of the D flip flop, Q, will be at logic low keeping transistor M2 off. The data input for the D flip flop, D, is internally connected to a logic high. As  $V_{OUT}$  becomes greater than 7.0V, COMP1 will change to a logic low state.  $V_{OUT}$  will continue to increase, and the constant current source of typically 3.0mA output will charge an external storage capacitor. As  $V_{OUT}$  reaches above 13.25V, the output of COMP2 will then switch from a logic high to a logic low state. The D flip flop's output does not change state since its clock input is designed to trigger only on a rising edge, logic low to logic high transition. When there is no load connected to the output, the output voltage will continue to increase until it reaches 21.5V, which is the zener voltage minus the threshold voltage of transistor M1. The zener voltage is typically 23V, and the threshold voltage of M1 is typically 1.5V. The zener diode is biased by resistor R4.

$V_{OUT}$  will start to decrease when it is connected to an external load greater than the internal constant current source, which is the case when the PWM IC starts up. When  $V_{OUT}$  falls below 13.25V, the output of COMP2 will switch from a logic low to a logic high. The output of COMP2 will clock in a logic 1 into the D flip flop, causing the D flip flop's output, Q, to switch from a logic low to a logic high. Transistor M2 will then be turned on pulling the gate of transistor M1 to ground, thereby turning transistor M1 off. Transistor M1 will remain off as long as  $V_{OUT}$  is greater than 7.0V. Once  $V_{OUT}$  decreases below 7.0V, COMP1 will reset the D flip flop, thereby turning transistor M2 off and transistor M1 back on.

## Typical Application

Figure 1 shows a simplified typical configuration of a switch-mode power supply, SMPS, using the Supertex LR745 in the start-up circuit.

The LR745's  $V_{OUT}$  terminal is connected to the  $V_{CC}$  line of a PWM IC, Unitrode part #UC3844. An auxiliary winding on the transformer is used to generate a  $V_{CC}$  voltage to power the PWM IC after start-up. The LR745 is used to supply power for the PWM IC only during start-up. After start-up, the LR745 turns off and the auxiliary winding is used to supply power for the PWM IC. Figure 2 shows the typical current and voltage waveforms at various stages from power up to operation powered by the auxiliary winding.

### Stage I

Once a voltage is applied on  $V_{IN}$ , the LR745 will start to charge the  $V_{CC}$  capacitor, C1. The  $V_{CC}$  voltage will start to increase at a rate limited by the internal current limiter of 3.0mA. The PWM IC is in its start-up condition and will typically draw 0.5mA from the  $V_{CC}$  line. The  $V_{CC}$  voltage will continue to increase until it reaches the PWM IC's start threshold voltage of typically 16V.

### Stage II

Once  $V_{CC}$  reaches 16V, the PWM IC is in its operating condition and will draw typically 20mA, depending on the operating frequency and size of the switching MOSFET. The output of the LR745,  $V_{OUT}$ , is internally current limited to 3.0mA. The remaining 17mA will be supplied by C1 causing the  $V_{CC}$  voltage decrease. When  $V_{CC}$  decreases to 13.25V, the LR745 will turn off its output, thereby reducing its input current from 3.0mA to 10s of microamperes. At this point, all 20mA will be supplied by C1. The PWM IC can now operate to a minimum  $V_{CC}$  voltage of typically 10V.

Once the switching MOSFET starts operating, the energy in the primary winding is transferred to the secondary outputs and the auxiliary winding, thereby building up  $V_{AUX}$ . It is necessary to size the  $V_{CC}$  storage capacitor, C1, such that  $V_{AUX}$  increases to a voltage greater than 10V before  $V_{CC}$  decreases to 10V. This allows  $V_{AUX}$  to supply the required operating current for the PWM IC.

If for some reason the auxiliary voltage does not reach 10V,  $V_{CC}$  will continue to decrease. Once  $V_{CC}$  goes below 10V, the PWM IC will return to its start-up condition. The PWM IC will now only draw 0.5mA.  $V_{CC}$  will continue to decrease but at a much slower rate. Once  $V_{CC}$  decreases below 7.0V, the LR745 will turn the output,  $V_{OUT}$ , back on.  $V_{OUT}$  will start charging C1 as described in Stage I.

Figure 1: Simplified SMPS Using LR745

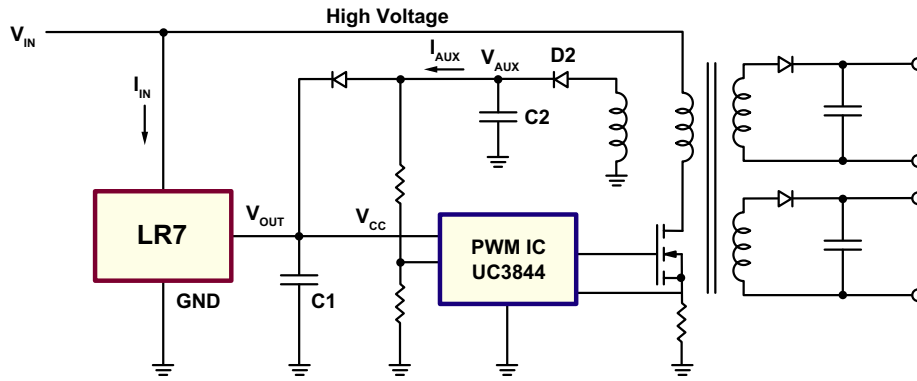
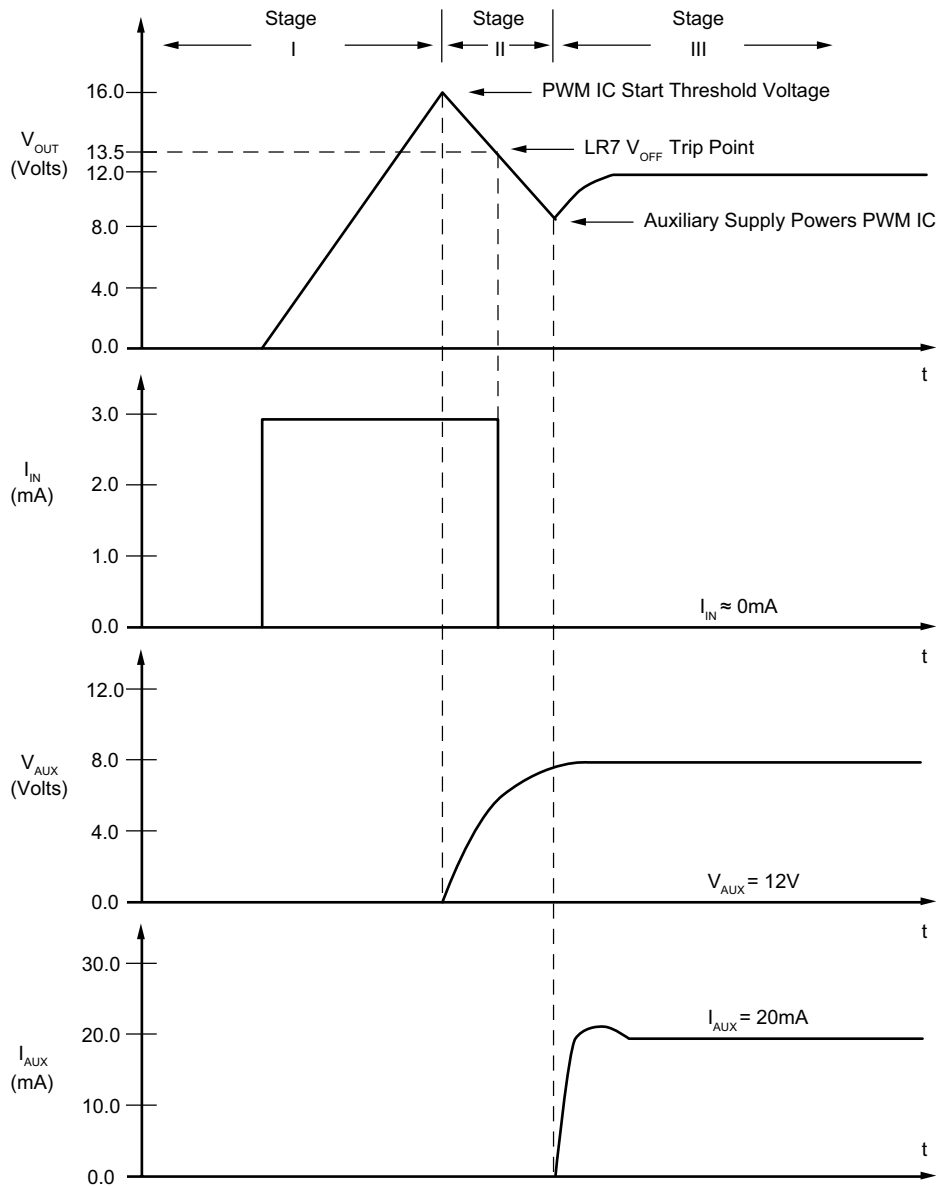


Figure 1: LR745 Start-up Waveforms



**Stage III**

At this stage the LR745's output is turned off and the PWM IC is operating from the  $V_{AUX}$  supply. The auxiliary voltage,  $V_{AUX}$ , can be designed to vary anywhere between the minimum operating  $V_{CC}$  voltage of the PWM IC (10V) to the maximum auxiliary voltage rating of the LR745 (22V).

**Design Considerations**

**I. Calculating the value for C1**

Sizing the  $V_{CC}$  capacitor, C1, is an important factor. Making C1 too large will cause the SMPS to power up too slowly. However, if too small, C1 will not allow the SMPS to power up due to insufficient charge in the capacitor to power the IC and MOSFET until the auxiliary supply is available. The value of C1 can be approximated by the following equation:

$$C1 = \frac{\left[ \frac{1}{f} \right] \times (N) \times (I)}{(V_{START} - V_{MIN})}$$

where,

- f = switching frequency
- N = number of clock cycles required to charge  $V_{AUX}$  to  $V_{MIN}$  value
- I = PWM operating current
- $V_{START}$  = PWM IC start threshold rating
- $V_{MIN}$  = PWM IC minimum  $V_{CC}$  operating voltage

Consider for example, a PWM IC with a switching frequency of 100KHz, operating current of 20mA, start threshold of 16V, and a minimum operating voltage of 10V. If 100 clock cycles are required to charge the auxiliary voltage to 10V, the minimum value of C1 is calculated as follows:

$$C1 = \frac{\left[ \frac{1}{100KHz} \right] \times (100) \times (20mA)}{(16V - 10V)}$$

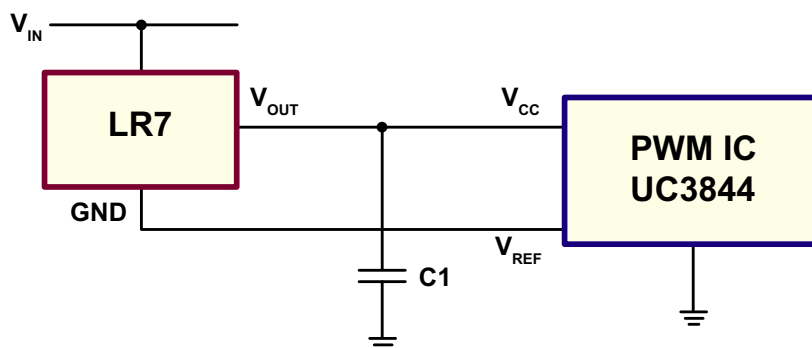
$$C1 = 3.3\mu F$$

**II. SMPS with wide minimum to maximum load**

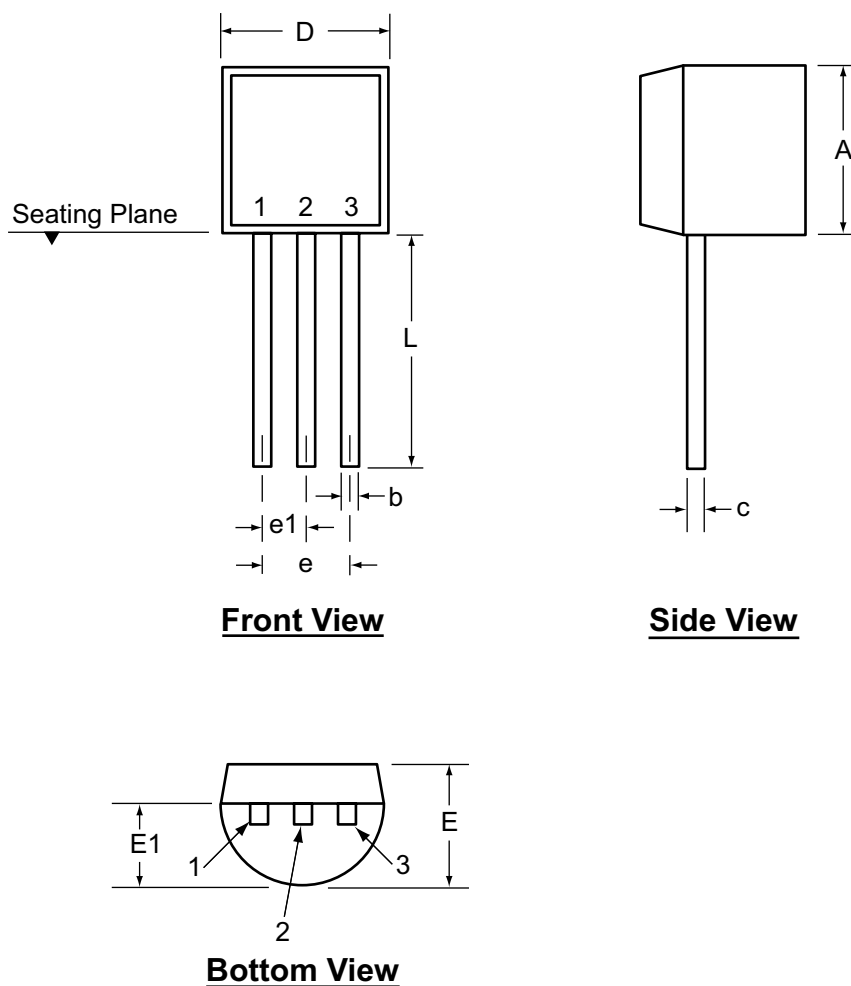
An important point is that the LR745's output voltage,  $V_{OUT}$ , must discharge to below the nominal  $V_{OFF}$  trip point of 13.25V in order for its output to turn off. If the SMPS requires a wide minimum to maximum output load variation, it will be difficult to guarantee that  $V_{CC}$  will fall below 13.25V under minimum load conditions. Consider an SMPS that is required to power small as well as large loads and is also required to power up quickly. Such a SMPS may power up too fast with a small load, not allowing the  $V_{CC}$  voltage to fall below 13.25V. For such conditions, the circuit in Figure 3 is recommended.

In Figure 3, the  $V_{REF}$  pin of the UC3844 is used to bias the ground pin of the LR745. The  $V_{REF}$  pin on the UC3844 is a 5.0V reference, which stays at 0V until the  $V_{CC}$  voltage reaches the start threshold voltage. Once  $V_{CC}$  reaches the start threshold voltage,  $V_{REF}$  will switch digitally from 0V to 5.0V. During start-up, the LR745 will be on, and  $V_{CC}$  will start to increase up to 16V. Once  $V_{CC}$  reaches 16V, the UC3844 will start to operate and  $V_{REF}$  will increase from 0V to 5.0V. The LR745 will see an effective  $V_{OUT}$  voltage of 11V (16V minus 5.0V) because the ground of the LR745 is now at 5.0V. The LR745 will immediately turn off its output,  $V_{OUT}$ , without having to wait for the  $V_{CC}$  voltage to decrease. The  $V_{REF}$  switching from 0 to 5.0V during start is a common feature in most PWM ICs.

**Figure 3: Using  $V_{REF}$  for the LR745 Ground Voltage**



### 3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

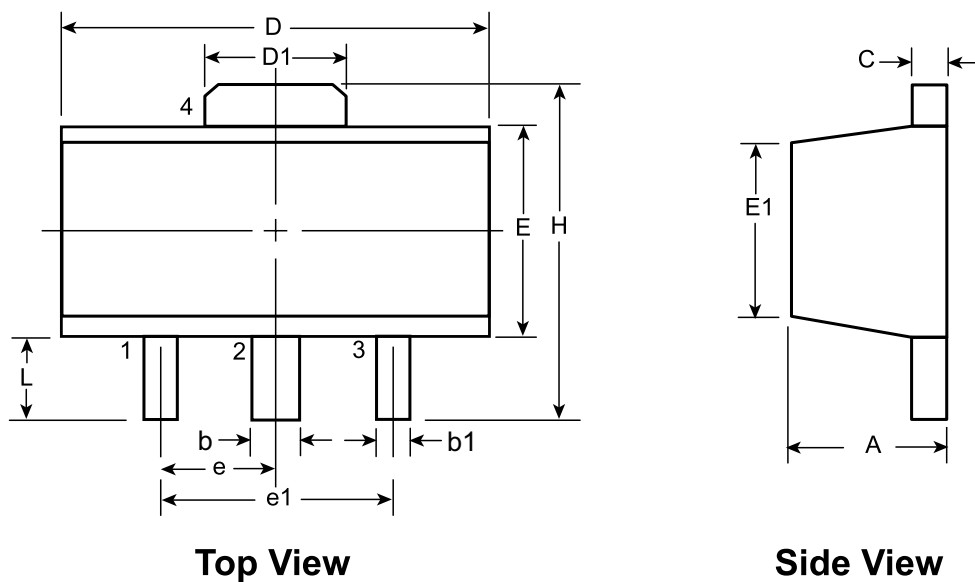
\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

### 3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version D070908.

(The package drawings in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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