

## 24-BIT QUADRATURE COUNTER

### FEATURES:

- Programmable modes are: Up/Down, Binary, BCD, 24 Hour Clock, Divide-by-N, x1 or x2 or x4 Quadrature and Single-Cycle.
- DC to 25MHz Count Frequency.
- 8-Bit I/O Bus for uP Communication and Control.
- 24-Bit comparator for pre-set count comparison.
- Readable status register.
- Input/Output TTL and CMOS compatible.
- 3V to 5.5V operation (VDD - VSS).
- LS7166 (DIP); LS7166-S (SOIC); LS7166-TS24 (24-Pin TSSOP) - **See Figure 1** -

### GENERAL DESCRIPTION:

The LS7166 is a CMOS, 24-bit counter that can be programmed to operate in several different modes. The operating mode is set up by writing control words into internal control registers (see Figure 8). There are three 6-bit and one 2-bit control registers for setting up the circuit functional characteristics. In addition to the control registers, there is a 5-bit output status register (OSR) that indicates the current counter status. The IC communicates with external circuits through an 8-bit three state I/O bus. Control and data words are written into the LS7166 through the bus. In addition to the I/O bus, there are a number of discrete inputs and outputs to facilitate instantaneous hardware based control functions and instantaneous status indication.

### REGISTER DESCRIPTION:

Internal hardware registers are accessible through the I/O bus (D0 - D7) for READ or WRITE when CS = 0. The C/D input selects between the control registers (C/D = 1) and the data registers (C/D = 0) during a READ or WRITE operation. (See Table 1)

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

### PIN ASSIGNMENTS - Top View

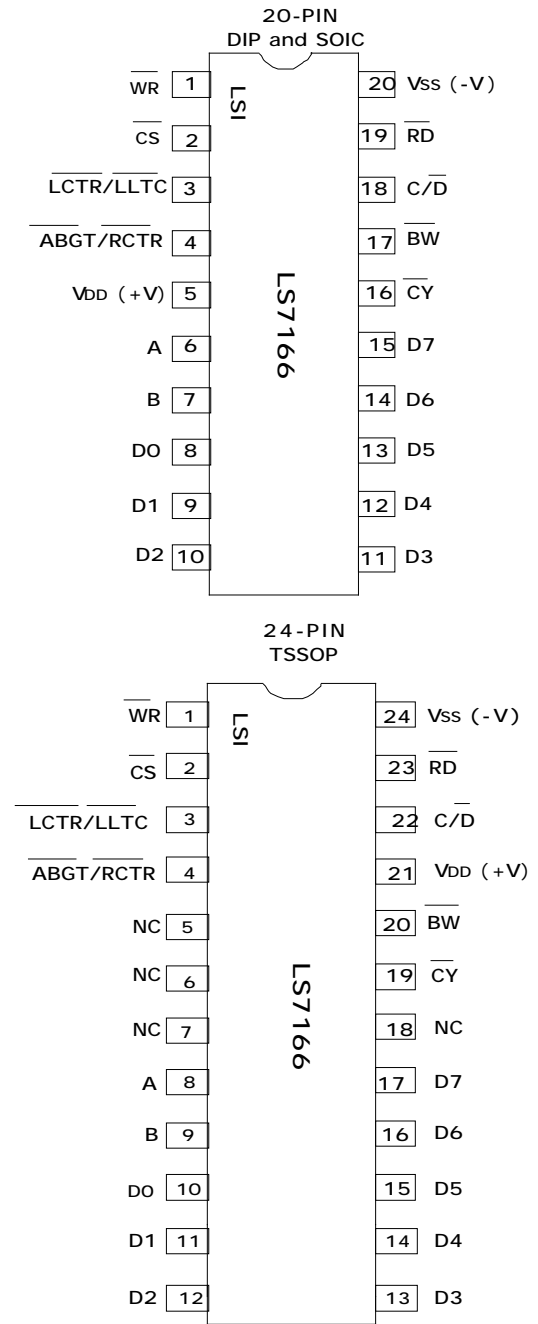
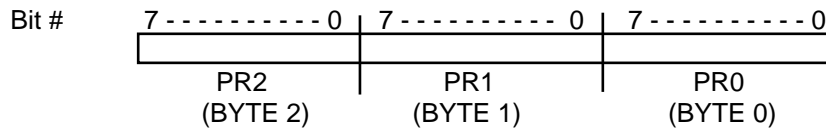


FIGURE 1

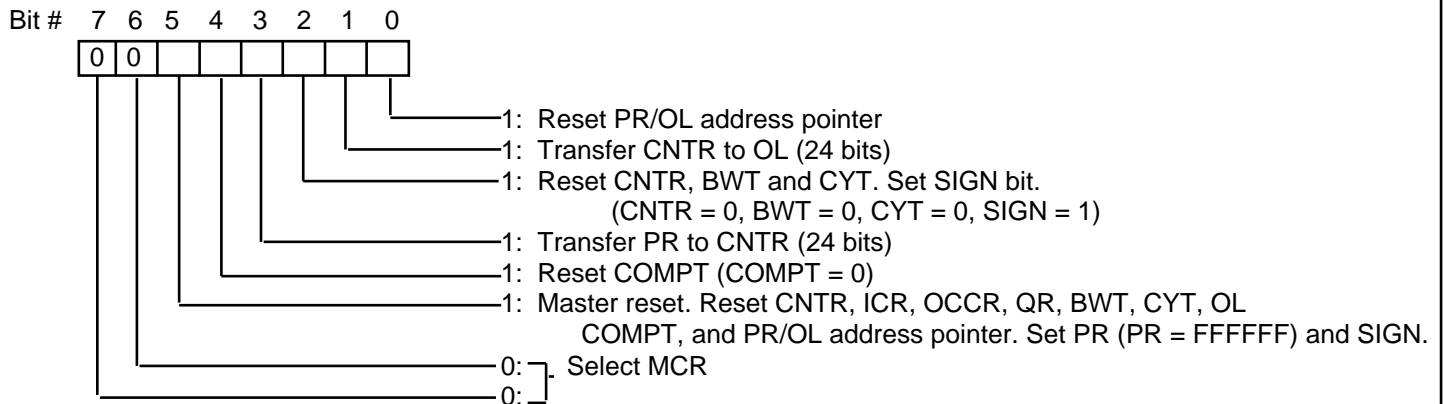
**PR (Preset register).** The PR is the input port for the CNTR. The CNTR is loaded with a 24 bit data via the PR. The data is first written into the PR in 3 WRITE cycle sequence of Byte 0 (PR0), Byte 1 (PR1) and Byte 2 (PR2). The address pointer for PR0/PR1/PR2 is automatically incremented with each write cycle. Accessed by: WRITE when  $C/\bar{D} = 0$ ,  $\bar{CS} = 0$ .



Standard Sequence for Loading PR and Reading CNTR:

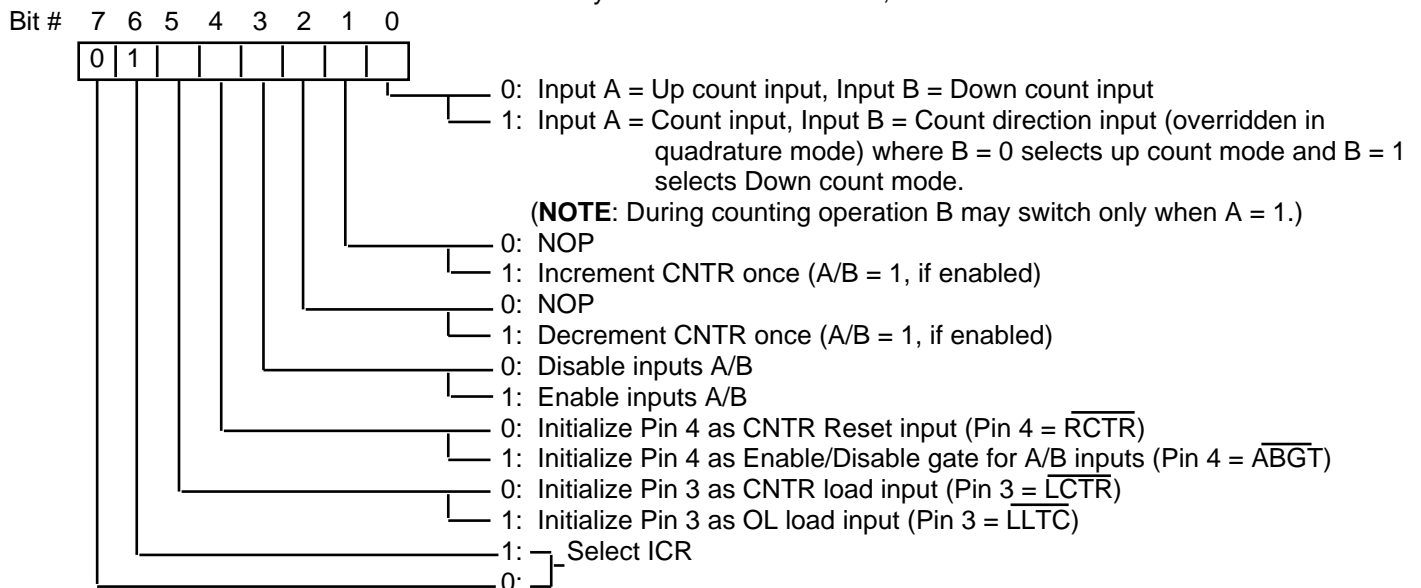
- 1 → MCR ; Reset PR address pointer
- WRITE PR ; Load Byte 0 and into PR0 increment address
- WRITE PR ; Load Byte 1 and into PR1 increment address
- WRITE PR ; Load Byte 2 and into PR3 increment address
- 8 → MCR ; Transfer PR to CNTR

**MCR (Master Control Register).** Performs register reset and load operations. Writing a "non-zero" word to MCR does not require a follow-up write of an "all-zero" word to terminate a designated operation. Accessed by: WRITE when  $C/\bar{D} = 1$ ,  $\bar{CS} = 0$ .



**NOTE:** Control functions may be combined.

**ICR (Input Control Register).** Initializes counter input operating modes. Accessed by: WRITE when  $C/\bar{D} = 1$ ,  $\bar{CS} = 0$ .



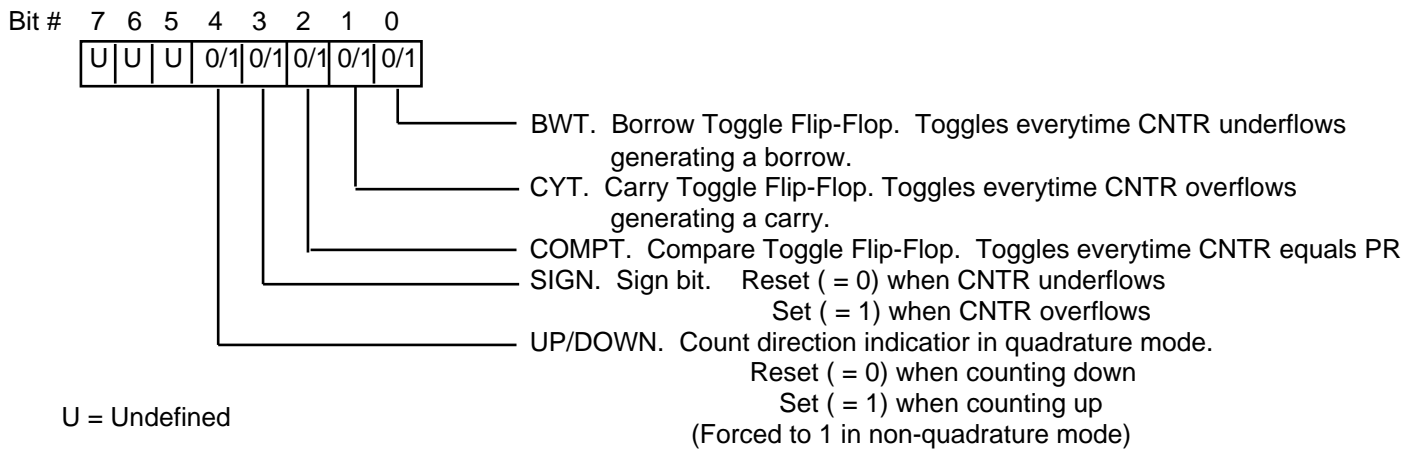
**NOTE:** Control functions may be combined.

**TABLE 1 - Register Addressing Modes**

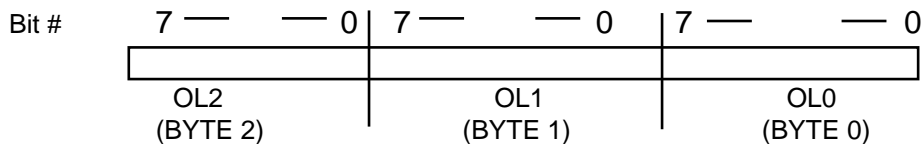
D7	D6	C/D	R $\bar{D}$	$\bar{W}R$	$\bar{C}S$	COMMENT
X	X	X	X	X	1	Disable Chip for READ/WRITE
0	0	1	1	$\bar{1}$	0	Write to Master Control Register (MCR)
0	1	1	1	$\bar{1}$	0	Write to input control register (ICR)
1	0	1	1	$\bar{1}$	0	Write to output/counter control register (OCCR)
1	1	1	1	$\bar{1}$	0	Write to quadrature register (QR)
X	X	0	1	$\bar{1}$	0	Write to preset register (PR) and increment register address counter.
X	X	0	$\bar{1}$	1	0	Read output latch (OL) and increment register address counter
X	X	1	$\bar{1}$	1	0	Read output status register (OSR).

X = Don't Care

**OSR (Output Status Register).** Indicates CNTR status: Accessed by: READ when  $C/\bar{D} = 1, \bar{C}S = 0$ .



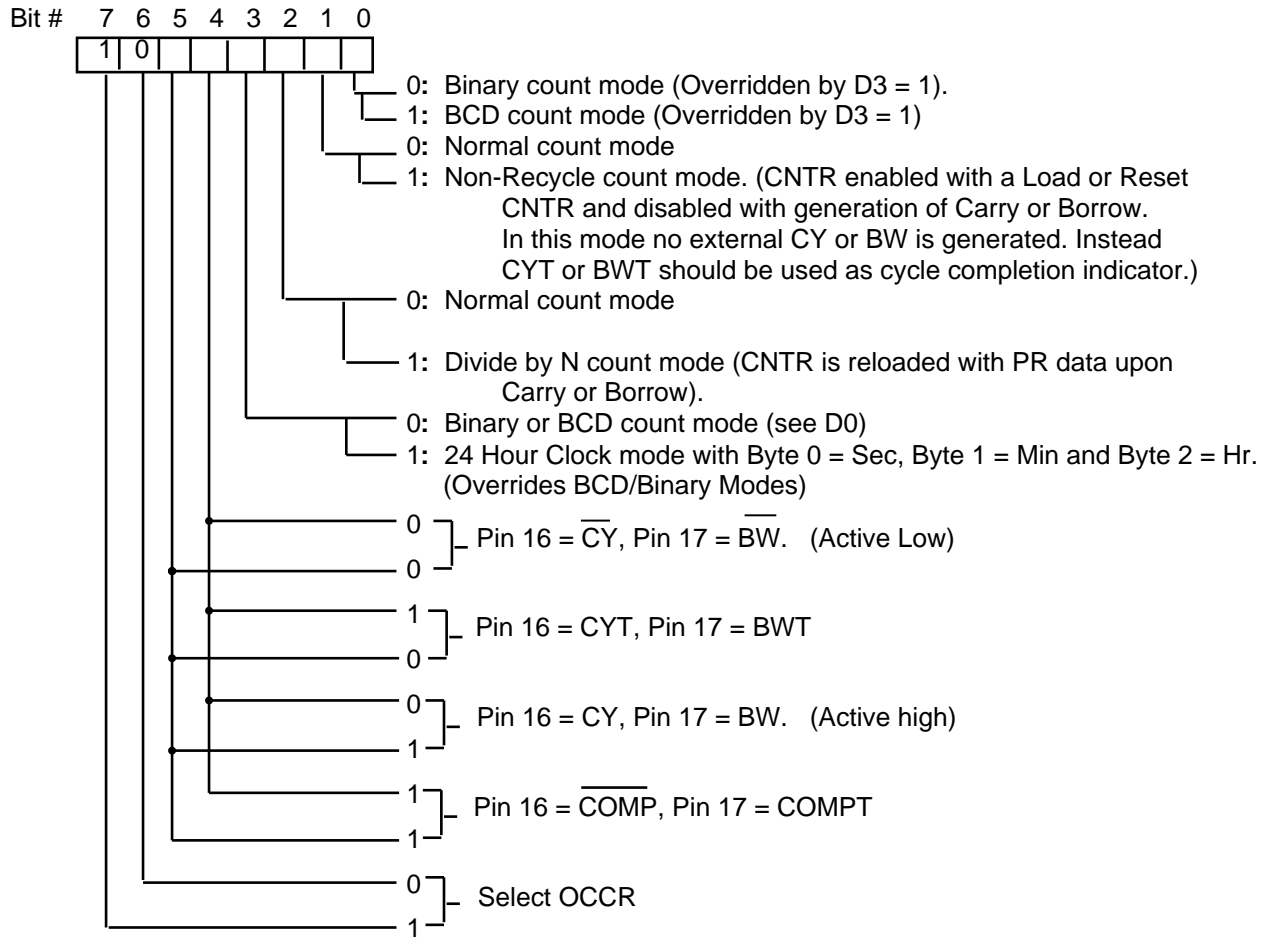
**OL(Output latch).** The OL is the output port for the CNTR. The 24 bit CNTR Value at any instant can be accessed by performing a CNTR to OL transfer and then reading the OL in 3 READ cycle sequence of Byte 0 (OL0), Byte 1 (OL1) and Byte 2 (OL2). The address pointer for OL0/OL1/OL2 is automatically incremented with each READ cycle. Accessed by: READ when  $C/\bar{D} = 0, \bar{C}S = 0$ .



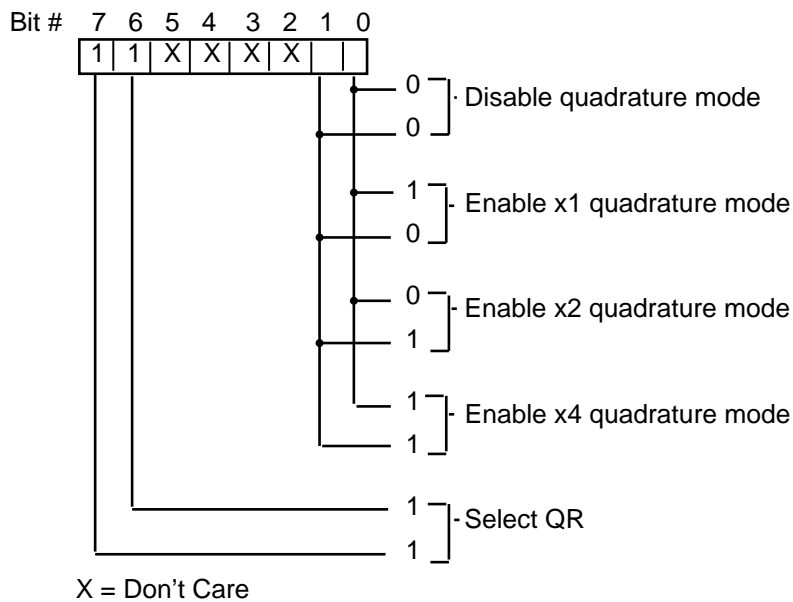
Standard Sequence for Loading and Reading OL:

- 3  $\rightarrow$  MCR ; Reset OL address pointer and Transfer CNTR to OL
- READ OL ; Read Byte 0 and increment address
- READ OL ; Read Byte 1 and increment address
- READ OL ; Read Byte 2 and increment address

**OCCR (Output Control Register)** Initializes CNTR and output operating modes.  
 Accessed by: WRITE when  $C/\bar{D} = 1$ ,  $\bar{CS} = 0$ .



**QR (Quadrature Register).** Selects quadrature count mode (See Fig. 7)  
 Accessed by: WRITE when  $C/\bar{D} = 1$ ,  $\bar{CS} = 0$ .



**I/O DESCRIPTION:****(See REGISTER DESCRIPTION for I/O Prgramming.)**

**Data-Bus (D0 - D7)** (Pin 8 - Pin 15). The 8-line data bus is a three-state I/O bus for interfacing with the system bus.

**$\overline{CS}$  (Chip Select Input)** (Pin 2). A logical "0" at this input enables the chip for Read and Write.

**$\overline{RD}$  (Read Input)** (Pin 19). A logical "0" at this input enables the OSR and the OL to be read on the data bus.

**$\overline{WR}$  (Write Input)** (Pin 1). A logical "0" at this input enables the data bus to be written into the control and data registers.

**$C/\overline{D}$  (Control/Data Input)** (Pin 18). A logical "1" at this input enables a control word to be written into one of the four control registers or the OSR to be read on the I/O bus. A logical "0" enables a data word to be written into the PR, or the OL to be read on the I/O bus.

**A** (Pin 6). Input A is a programmable count input capable of functioning in three different modes, such as up count input, down count input and quadrature input. In non-quadrature mode, the counter advances on the rising edge of Input A.

**B** (Pin 7). Input B is also a programmable count input that can be programmed to function either as down count input, or count direction control gate for input A, or quadrature input. In non-quadrature mode, and when programmed as the Down Count input, the counter advances on the rising edge of Input B. When B is programmed as the count direction control gate, B = 0 enables A as the Up Count input and B = 1 enables A as the Down Count input. When programmed as the direction input, B can switch state only when A is high.

**$\overline{ABGT}/\overline{RCTR}$**  (Pin 4). This input can be programmed to function as either inputs A and B enable gate or as external counter reset input. A logical "0" is the active level on this input. In non-quadrature mode, if Pin 4 is programmed as A and B enable gate input, it may switch state only when A is high (if A is clock and B is direction) or when both A and B are high (if A and B are clocks). In quadrature mode, if Pin 4 is programmed as A and B enable gate, it may switch state only when either A or B switches.

**$\overline{LCTR}/\overline{LLTC}$**  (Pin 3) This input can be programmed to function as the external load command input for either the CNTR or the OL. When programmed as counter load input, the counter is loaded with the data contained in the PR. When programmed as the OL load input, the OL is loaded with data contained in the CNTR. A logical "0" is the active level on this input.

**$\overline{CY}$**  (Pin 16) This output can be programmed to serve as one of the following:

- A.  $\overline{CY}$ . Complemented Carry out (active "0").
- B. CY. True Carry out (active "1").
- C. CYT. Carry Toggle flip-flop out.
- D.  $\overline{COMP}$ . Comparator out (active "0")

**$\overline{BW}$**  (Pin 17) This output can be programmed to serve as one of the following:

- A.  $\overline{BW}$ . Complemented Borrow out (active "0").
- B. BW. True Borrow out (active "1").
- C. BWT. Borrow Toggle flip-flop out.
- D. COMPT. Comparator Toggle output.

**VDD** (Pin 5) Supply voltage positive terminal.

**VSS** (Pin 20) Supply voltage negative terminal.

**Absolute Maximum Ratings:**

Parameter	Symbol	Values	Unit
Voltage at any input	V <sub>IN</sub>	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V
Operating Temperature	T <sub>A</sub>	-40 to +125	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Supply Voltage	V <sub>DD</sub> - V <sub>SS</sub>	+7.0	V

**DC Electrical Characteristics.** (All voltages referenced to V<sub>SS</sub>.)

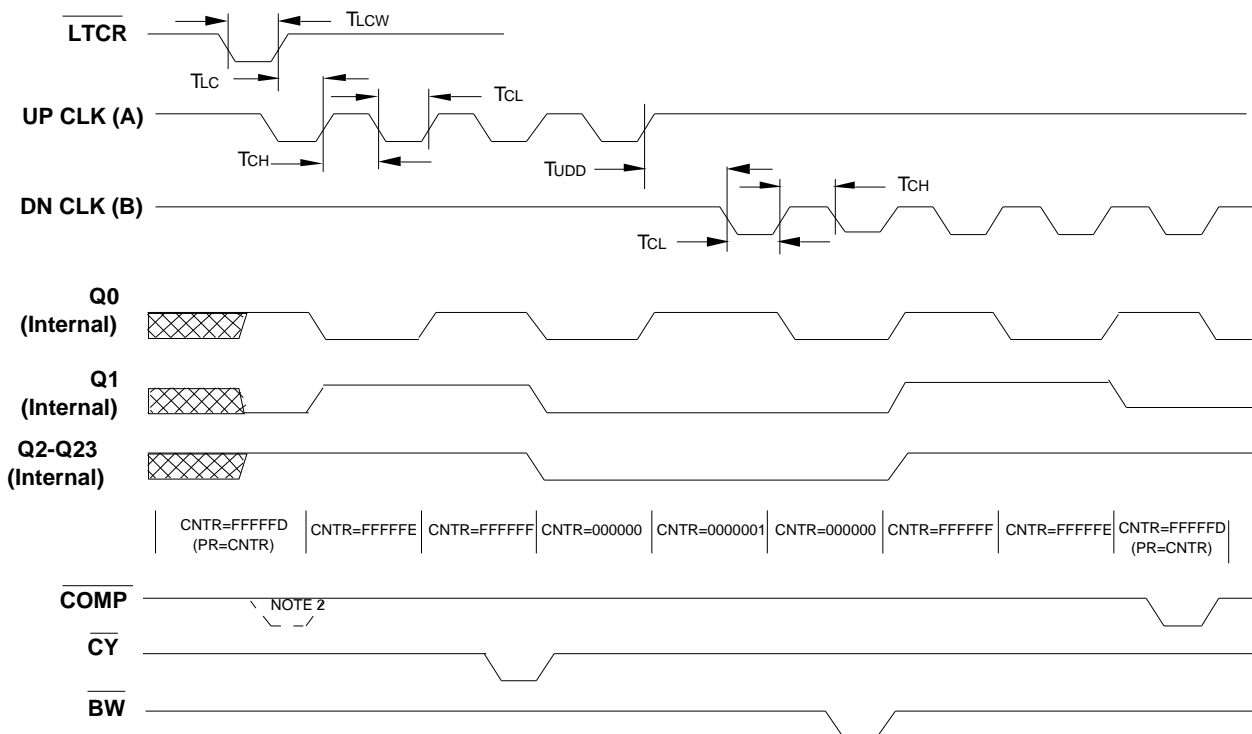
T<sub>A</sub> = 0° to 85°C, V<sub>DD</sub> = 3V to 5.5V, f<sub>c</sub> = 0, unless otherwise specified)

Parameter	Symbol	Min. Value	Max. Value	Unit	Remarks
Supply Voltage	V <sub>DD</sub>	3.0	5.5	V	-
Supply Current	I <sub>DD</sub>	-	350	µA	Outputs open
Input Low Voltage	V <sub>IL</sub>	0	0.8	V	-
Input High Voltage	V <sub>IH</sub>	2.0	V <sub>DD</sub>	V	-
Output Low Voltage	V <sub>OL</sub>	-	0.4	V	4mA Sink, V <sub>DD</sub> = 5V
Output High Voltage	V <sub>OH</sub>	2.5	-	V	200µA Source, V <sub>DD</sub> = 5V
Input Current	-	-	15	nA	Leakage Current
Output Source Current	I <sub>SRC</sub>	200	-	µA	V <sub>OH</sub> = 2.5V, V <sub>DD</sub> = 5V
Output Sink Current	I <sub>SINK</sub>	4	-	mA	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 5V
Data Bus Off-State Leakage Current	-	-	15	nA	-

**TRANSIENT CHARACTERISTICS** (See Timing Diagrams in Fig. 2 thru Fig. 7,  
VDD = 3V to 5.5V, TA = 0° to 85°C, unless otherwise specified)

Parameter	Symbol	Min.Value	Max.Value	Unit
Clock A/B "Low"	TCL	18	No Limit	ns
Clock A/B "High"	TCH	22	No Limit	ns
Clock A/B Frequency (See NOTE 1)	fc	0	25	MHz
Clock UP/DN Reversal Delay	TUDD	100	-	ns
LCTR Positive edge to the next A/B positive or negative edge delay	TLC	100	-	ns
Clock A/B to CY/BW/COMP "low" propagation delay	TCBL	-	65	ns
Clock A/B to CY/BW/COMP "high" propagation delay	TCBH	-	85	ns
LCTR and LLTC pulse width	TLCW	60	-	ns
Clock A/B to CYT, BWT and COMPT "high" propagation delay	TTFH	-	100	ns
Clock A/B to CYT, BWT and COMPT "low" propagation delay	TTFL	-	100	ns
WR pulse width	TWR	60	-	ns
RD to data out delay (CL=20pF)	TR	-	110	ns
CS, RD Terminate to Data-Bus Tri-State	TRT	-	30	ns
Data-Bus set-up time for WR	TDS	30	-	ns
Data-Bus hold time for WR	TDH	30	-	ns
CS set-up time for RD	TSRS	0	-	ns
CS hold time for RD	TSRH	0	-	ns
Back to Back RD delay	TRR	60	-	ns
RD to WR delay	-	60	-	ns
C/D set-up time for RD	TCRS	0	-	ns
C/D hold time for RD	TCRH	30	-	ns
C/D set-up time for WR	TCWS	30	-	ns
C/D hold time for WR	TCWH	30	-	ns
CS set-up time for WR	TSWS	60	-	ns
CS hold time for WR	TSWH	0	-	ns
Back to Back WR delay	Tww	60	-	ns
WR to RD delay	-	60	-	ns
<b>Quadrature Mode:</b>				
Clock A/B Validation delay (See NOTE 1)	Tcqv	-	160	ns
A and B phase delay	TPH	208	-	ns
Clock A/B frequency	fcq	-	1.2	MHz
CY, BW, COMP pulse width	TCBW	85	200	ns

**NOTE 1:** In quadrature mode A/B inputs are filtered and required to be stable for at least Tcqv length to be valid.

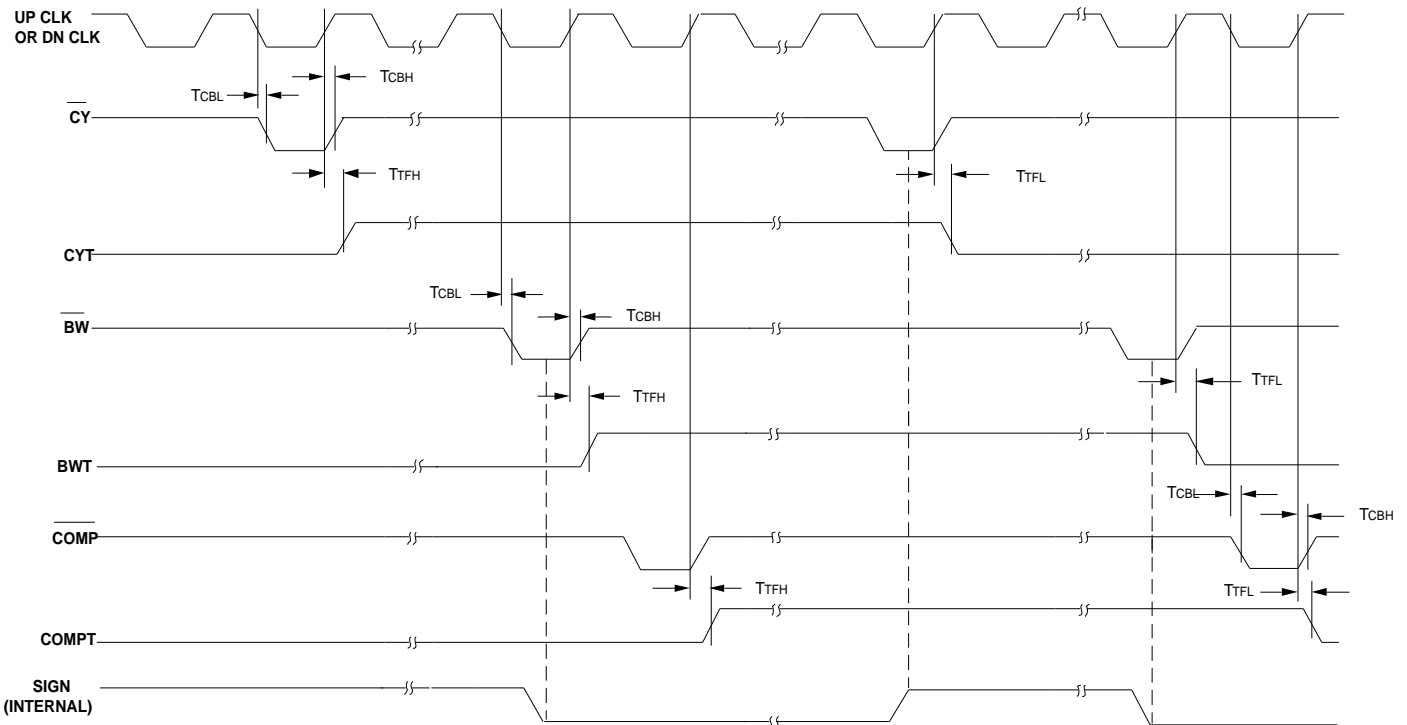


**FIGURE 2 . LOAD COUNTER, UP CLOCK, DOWN CLOCK, COMPARE OUT, CARRY, BORROW**

**NOTE 1:** The counter in this example is assumed to be operating in the binary mode.

**NOTE 2:** No COMP output is generated here, although PR = CNTR. COMP output is disabled with a counter load command and enabled with the rising edge of the next clock, thus eliminating invalid COMP outputs whenever the CNTR is loaded from the PR.

**NOTE 3:** When UP Clock is active, the DN Clock should be held "HIGH" and vice versa.



**FIGURE 3. CLOCK TO  $\overline{CY}/\overline{BW}$  OUTPUT PROPAGATION DELAYS**

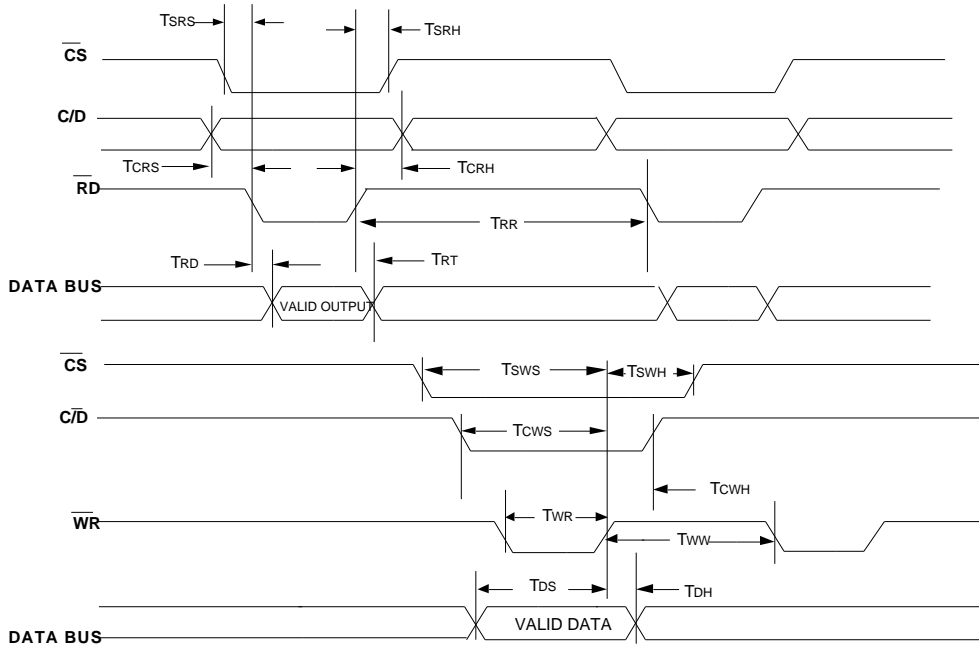
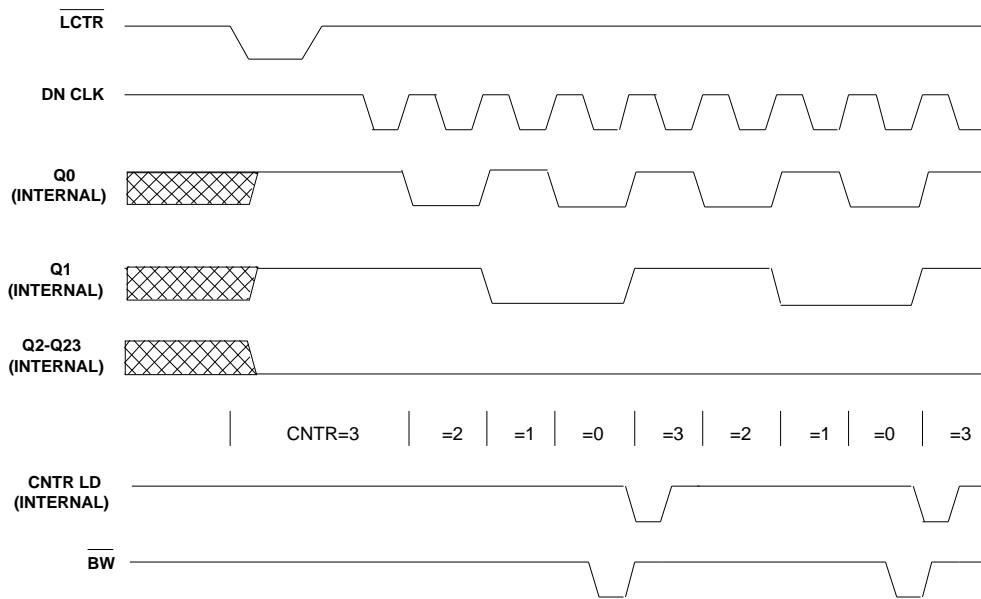


FIGURE 4. READ/WRITE CYCLES



NOTE: EXAMPLE OF DIVIDE BY 4 IN DOWN COUNT MODE

FIGURE 5. DIVIDE BY N MODE

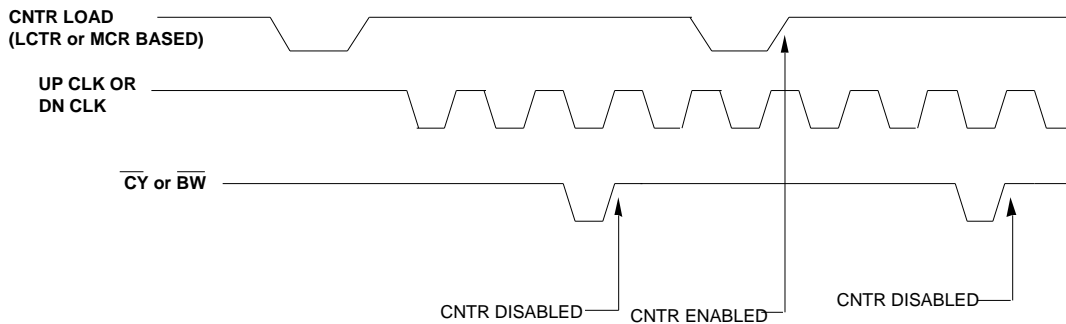
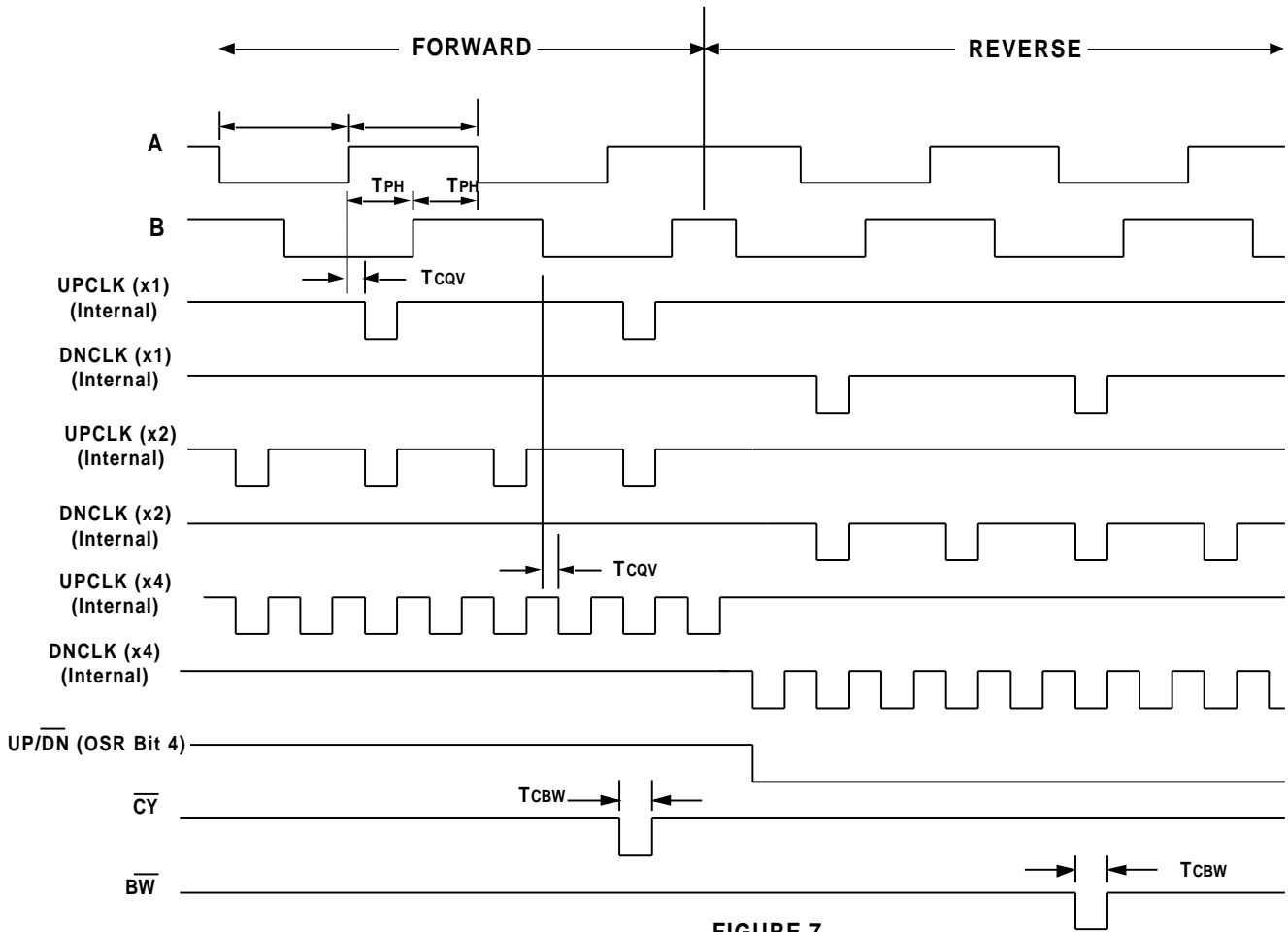
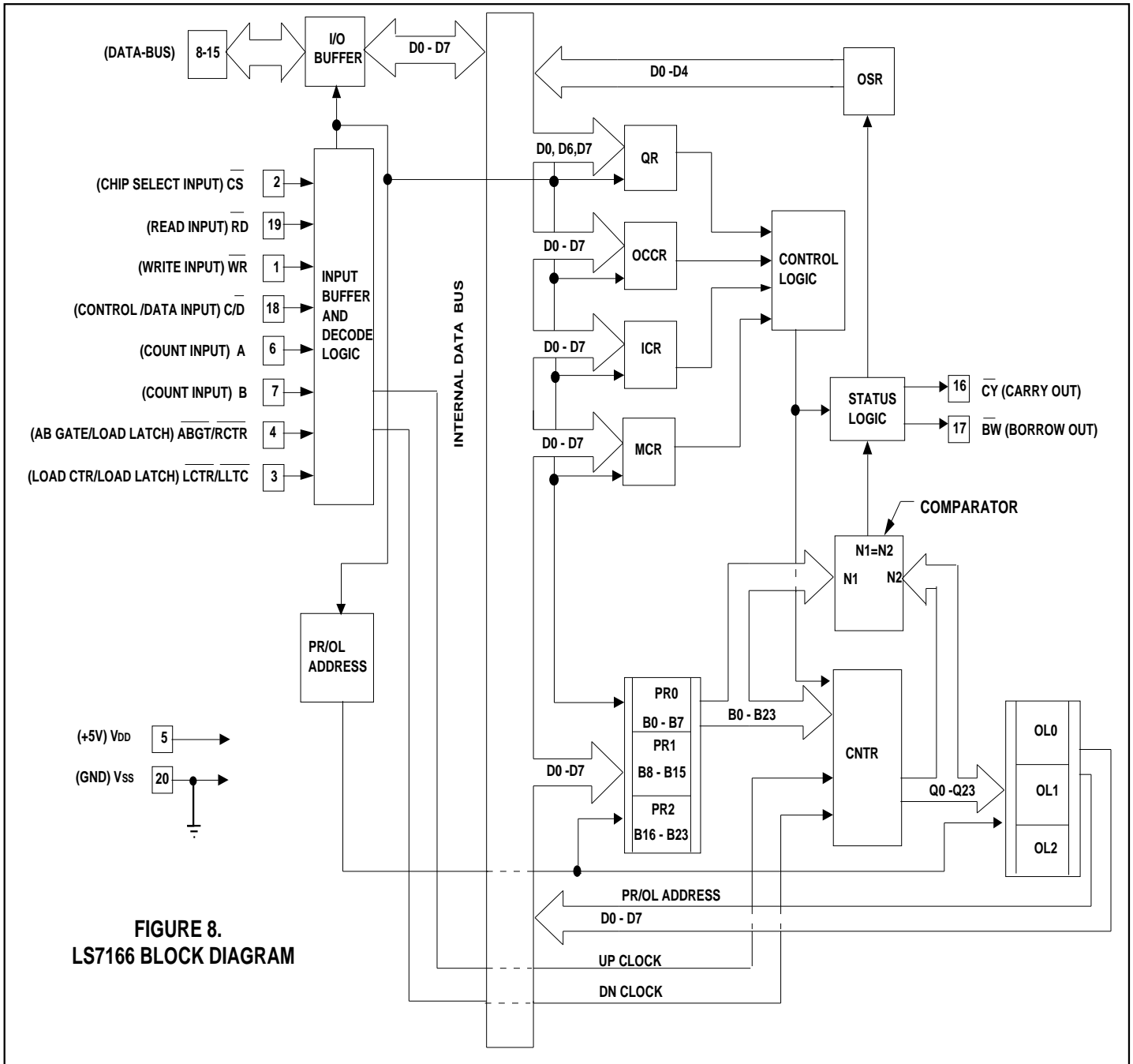


FIGURE 6. CYCLE ONCE MODE





**FIGURE 7.**  
**QUADRATURE MODE INTERNAL CLOCKS**



**FIGURE 8.**  
**LS7166 BLOCK DIAGRAM**



FIGURE 10. 8751 INTERFACE TO LS7166 IN I/O MODE

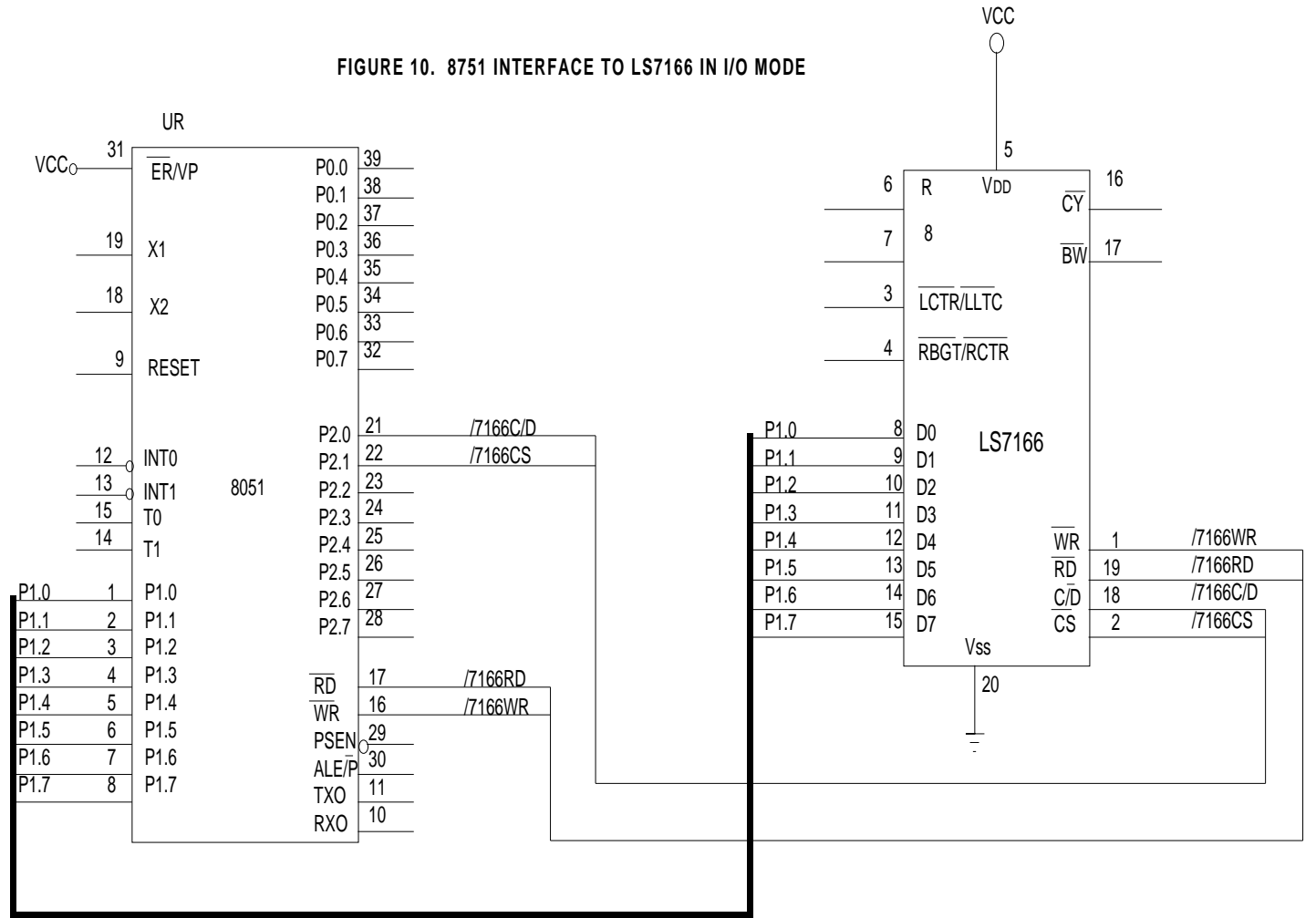
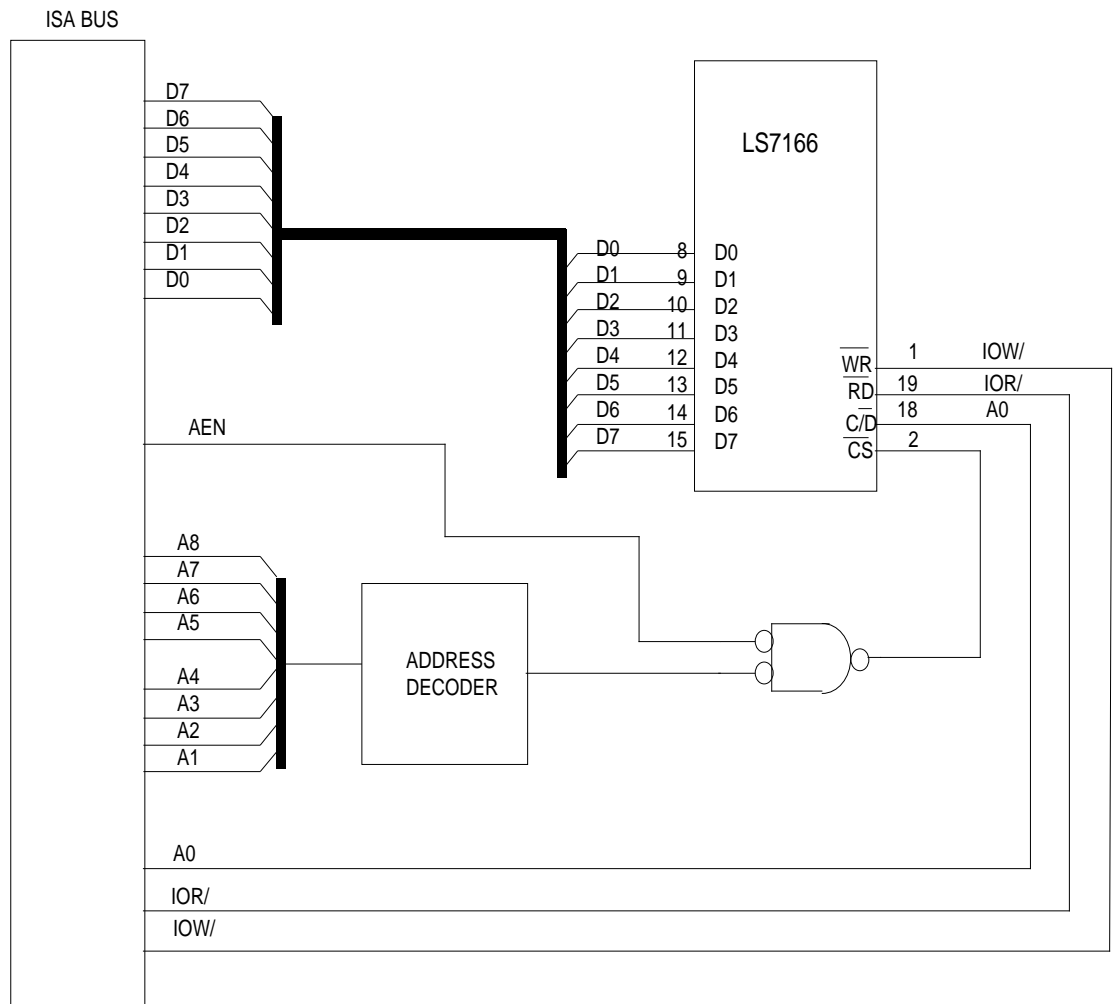




FIGURE 12. LS7166 INTERFACE EXAMPLE



**FIGURE 13. 68000 INTERFACE TO LS7166**

