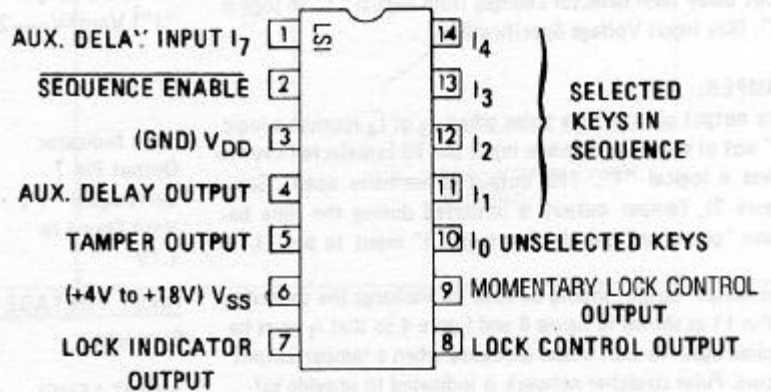


DIGITAL LOCK CIRCUIT with Tamper Output

FEATURES:

- Stand Alone Lock Logic
- 5040, 4 Digit Combination with a 10 number Key Board
- Out of Sequence Detection
- Tamper Output, Sequence Enable Input
- Direct LED and Lock Relay Drive
- Externally Controlled Combination Delay
- Internal Pull Down Resistors on all Inputs
- High Noise Immunity
- Low Current Consumption (40 μ A max @ 12 VDC)
- Single Power Supply Operation (+4V to +18V)
- Momentary or Static Lock Control Output
- Auxiliary Delay Circuitry Included



TOP VIEW
STANDARD 14 PIN DIP
Figure 1

DESCRIPTION:

The LS7225 is a monolithic, ion implanted MOS 4 Key Keyless lock. The circuit includes sequential logic for interpretation of correct key closure; a momentary and Static Lock Control output, out of sequence detection circuitry and a tamper output.

DESCRIPTION OF OPERATION:

SELECTED KEYS AND COMBINATION DELAY:

A sequence of logical "1" 's at the inputs I_1 , I_2 , I_3 , and I_4 (in correct sequence) sets the "SEQUENTIAL MEMORY", causing the LOCK CONTROL output to go high, the MOMENTARY LOCK CONTROL OUTPUT to go high, (See MOMENTARY LOCK CONTROL), and the lock indicator to open. An external capacitor at input I_1 (Pin 11) determines the amount of time allowed to enter the SELECTED KEYS inputs in proper sequence. The delay is a function of the external capacitance and the supply voltage (See figure 2)

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

UNSELECTED KEYS:

A logical "1" at this input resets the "SEQUENTIAL DETECTOR" for the SELECTED KEYS inputs and causes the TAMPER output to transmit a pulse. This input should be wired to all the keys that are not part of the input sequence.

LOCK CONTROL:

This toggle output will change state (logical "1" or open) when the "SEQUENTIAL MEMORY" is set. (See SELECTED KEYS).

*See figure 7

DC ELECTRICAL CHARACTERISTICS:

($V_{DD} = 0V$, $V_{SS} = +4$ to $+18V$, $-25^{\circ}C \leq T_A \leq +70^{\circ}C$ unless otherwise specified).

	VSS	MIN	TYP	MAX	UNITS
Lock Control and Momentary Lock Control Output Pin 8 and 9 On (Logic "1") $V_{out} = V_{SS} - 2$	5Vdc 9Vdc 12Vdc 15Vdc 18Vdc	1.50 3.00 5.00 8.00 9.00	3.00 5.50 7.50 10.00 11.00	4.50 8.00 9.50 12.50 13.50	mA
Tamper Output Pin 5 On (Logical "1") $V_{out} = V_{SS} - 2$	5Vdc 9Vdc 12Vdc 15Vdc 18Vdc	0.05 0.50 0.70 0.90 1.50	0.10 0.80 1.00 1.50 2.10	0.30 1.20 1.60 2.00 2.60	mA
Aux Delay output Pin 4 On (Logic "1") $V_{out} = V_{SS} - 2$	5Vdc 9Vdc 12Vdc 15Vdc 18Vdc	0.40 1.24 1.84 2.44 3.04	0.62 1.62 2.37 3.12 3.87	0.84 2.04 3.00 3.84 4.74	mA
Lock Indicator Output Pin 7 On (Logical "1") V_{out} Clamp to 1.7V	5Vdc 9Vdc 12Vdc 15Vdc 18Vdc	0.30 2.00 5.00 7.00 8.00	0.60 3.00 6.00 8.00 10.00	1.00 4.50 7.00 10.00 13.00	mA

LOCK INDICATOR:

This output is the complement of the LOCK CONTROL output (it drives an LED directly.)

MOMENTARY LOCK CONTROL:

This output goes on (Logical "1") when the "SEQUENTIAL MEMORY" is set. It goes open when input I_1 (pin 11) to the input delay level detector changes from logical "1" to logical "0". (See Input Voltage Specification)

TAMPER:

This output gives a 15 μ s pulse when I_3 or I_4 receives a logic "1" out of sequence or when input pin 10 (unselected key) receives a logical "1". This output is normally open. (See Figure 3) Tamper output is inhibited during the time between "power on" and the first logic "1" input to pin 11.

The tamper output should be used to discharge the capacitor at Pin 11 as shown in figure 8 and figure 4 so that I_1 must be applied again to start a new sequence when a tamper output occurs. Pulse stretcher network is indicated to provide sufficient discharge time.

SEQUENCE ENABLE:

A Logical "1" at this input disables the "SEQUENTIAL DETECTOR" thereby disallowing any sequential input. This input is intended to be used in conjunction with the TAMPER output (See Application Note 2).

POWER-ON-RESET:

A Power-On-Reset circuit resets the device to a "lock" condition upon application of power.

POWER SUPPLIES:

The circuit will operate over the range of +4 to +18 volts.

AUXILIARY DELAY NETWORK (pins 1 & 4)

This retriggerable one shot is provided for any convenient delay generation.

MAXIMUM RATINGS: (Voltages Referenced to V_{DD})

Rating	Symbol	Value	Units
DC Supply Voltage	V_{SS}	+4 to +18	Vdc
Operating Temperature Range	TA	-25 to +70	$^{\circ}C$
Storage Temperature Range	TSTG	-65 to +150	$^{\circ}C$

INPUT VOLTAGE SPECIFICATIONS:

Parameter	Symbol	V_{SS} Vdc	MIN	MAX	UNITS
INPUT LEVEL DETECTORS Pins 1 and 11					
Input Logic "0"	V_{iL}	5.0 9 12 15 18	0 0 0 0 0	$V_{SS}-3$ $V_{SS}-6$ $V_{SS}-8$ $V_{SS}-9$ $V_{SS}-9.5$	Vdc
Input Logic "1"	V_{iH}	5.0 9 12 15 18	$V_{SS}-1.0$ $V_{SS}-2.5$ $V_{SS}-4.5$ $V_{SS}-5.0$ $V_{SS}-5.5$	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	Vdc
All Other Inputs					
Input Logic "0"	V_{iL}	V_{SS}	0	$V_{SS}-3$	Vdc
Input Logic "1"	V_{iH}	V_{SS}	$V_{SS}-1$	V_{SS}	Vdc

All Other Inputs

Input Logic "0" V_{iL} V_{SS} 0 $V_{SS}-3$ Vdc
Input Logic "1" V_{iH} V_{SS} $V_{SS}-1$ V_{SS} Vdc

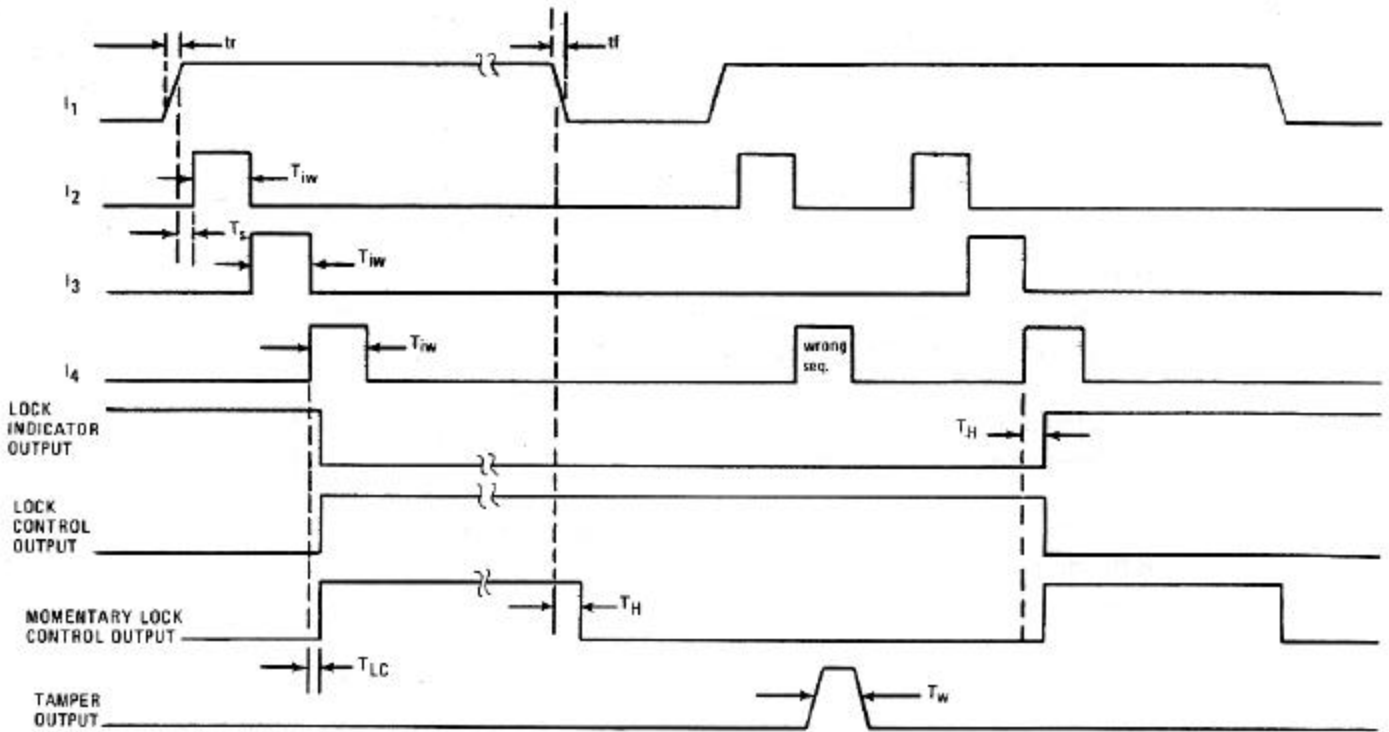
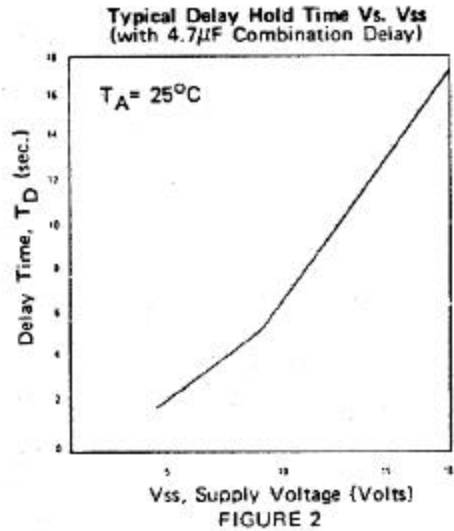
NOTE: Typical input load current is 6 μ A with input @ V_{DD} , V_{SS} @ +12V.

INPUT CAPACITANCE: 10 PF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Convenience Delay					
Set-Up Time	T_S	6	8	10	μ sec
Hold Time	T_H	14	16	20	μ sec
Input Lock Control					
Output Delay	T_{LC}	10	13	15	μ sec
Input Pulse Width	T_{iw}	100			μ sec
Tamper Output					
Tamper Output					
Pulse Width	T_W			15	μ s
Combination Delay					
Rise Time	tr	C+70ns			
Fall Time	tf	C+60ns			

QUIESCENT SUPPLY CURRENT: (All inputs and outputs open)

Symbol	V _{SS}	MAX	UNITS
I _{DD}	5Vdc	20	μA
	9Vdc	30	
	12Vdc	40	
	15Vdc	50	
	18Vdc	70	



Timing Diagram
Figure 3

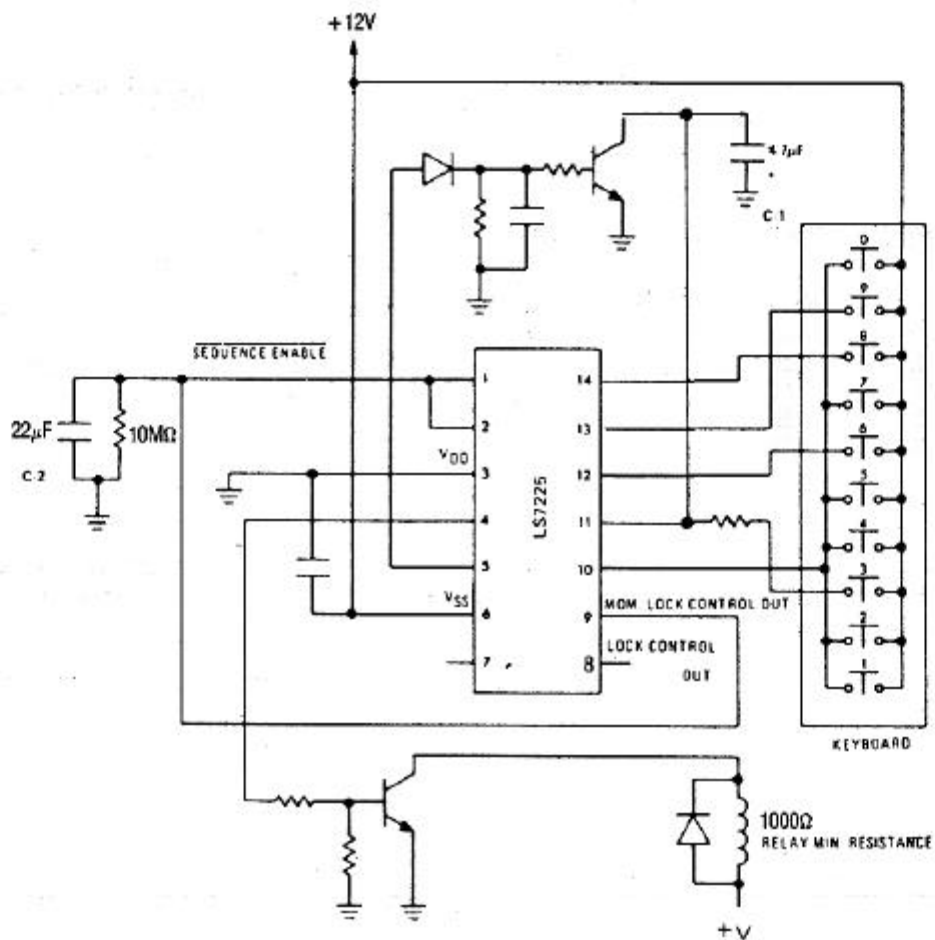
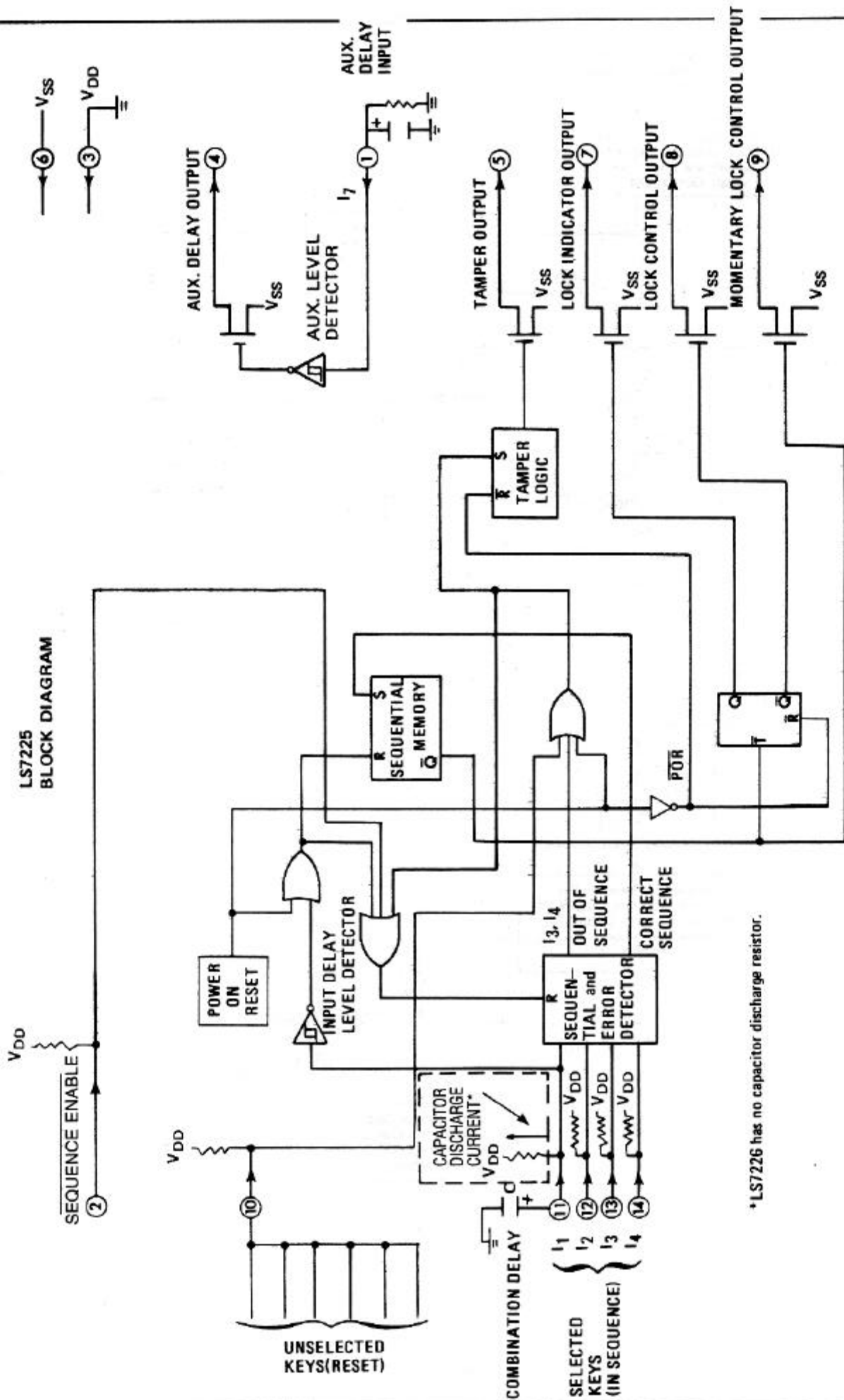


Figure 8
 Typical application for independent control of combination
 (input) time and "UNLOCK" time.

C-1 determines input time.
 C-2 determines "UNLOCK" time.

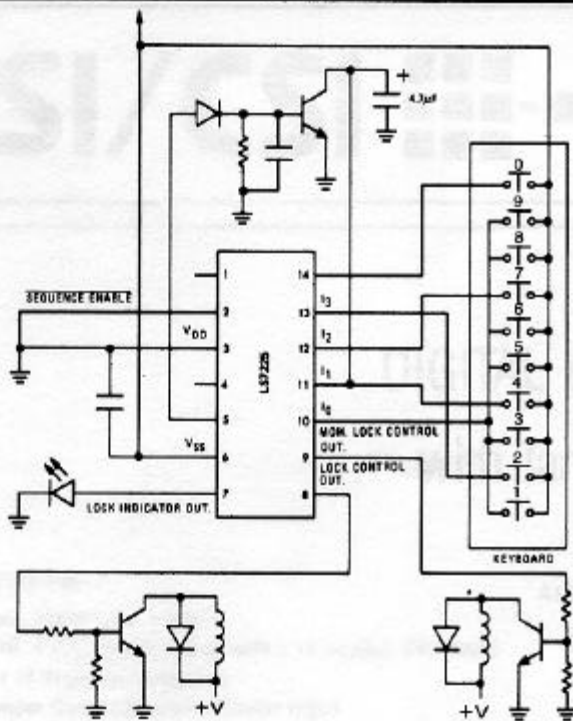
Note: With this configuration one tamper pulse is transmitted
 at the start of "UNLOCK" time.

LS7225
BLOCK DIAGRAM



*LS7226 has no capacitor discharge resistor.

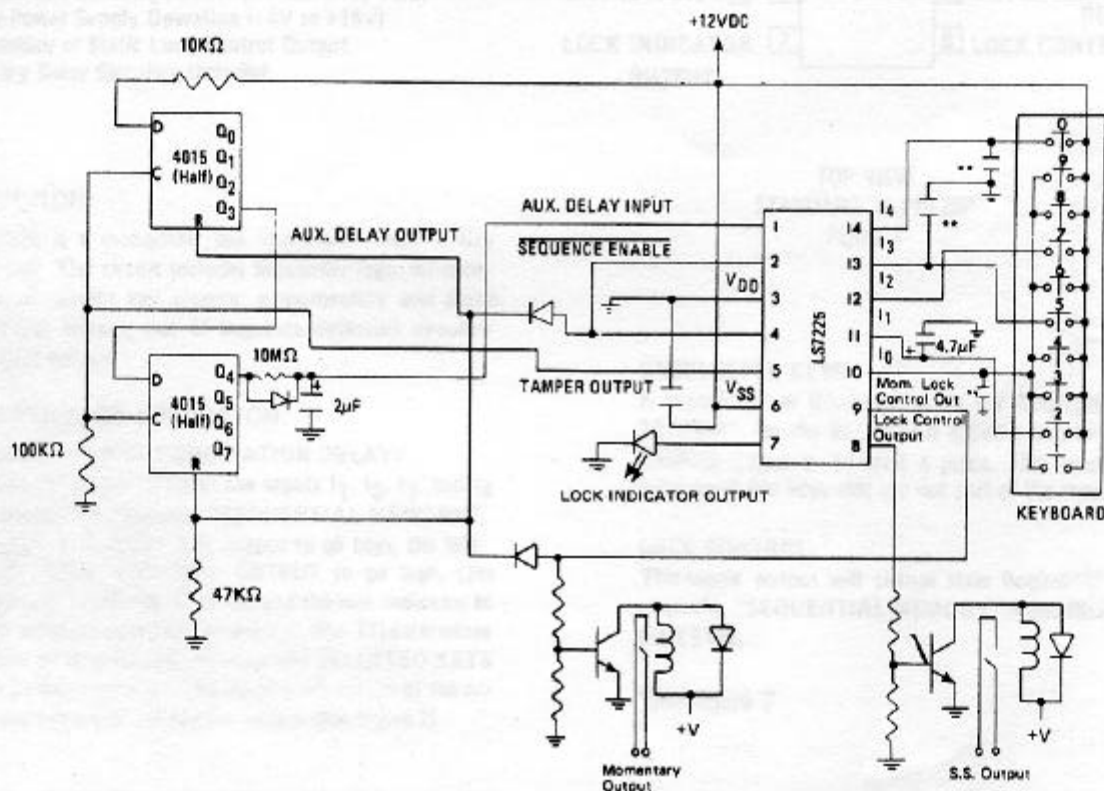
Figure 7



A typical circuit is shown in the schematic diagram. When input I₁ (pin 11) goes high, the circuit is ready to accept the unlocking input sequence at I₂, I₃ and I₄ (pins 12, 13, and 14 respectively). If the Keys associated with these inputs are depressed exactly in sequence of I₁, I₂, I₃ and I₄, the lock control output (pin 8) will become ON, the momentary lock control output (pin 9) will be ON until input I₁ (pin 11) becomes low. The state ON of the lock control will be indicated by the OFF Condition of the lock indicator output (pin 7) which will render the LED OFF (an indication of unlock condition). If the Keys are depressed in any sequence other than as described above, the internal "SEQUENTIAL DETECTOR" will be reset and the entire sequence must be repeated. The lock control output is turned OFF by repeating the input sequence. The Momentary Lock Control output goes high each time the correct sequence is entered. The specific code shown is 4720.

TYPICAL APPLICATION OF LS7225 IN MACHINE OR AREA ACCESS

Figure 4



TYPICAL TAMPER LOCK DISABLE APPLICATION

Figure 5

A System with 12 seconds reset after 5 TAMPER outputs and support circuitry is shown. The specific code is 2750. If the Keys associated with the given code are not depressed exactly in sequence or if any Key associated with the unselected Keys (Reset) is depressed, the pulse from the Tamper output will clock the 4015 Dual 4-bit shift register which transmits a logical "1" from input D to output Q4 after five clock pulses. A logical "1" in Q4 will charge up the 2µF capacitor, turn on the AUX. DELAY OUTPUT for 12 seconds and keep the LS7225 in the RESET Mode vis SEQUENCE ENABLE (pin 2). After the 2µF capacitor discharges, pin 2 of LS7225 becomes a logical "0" and the keyless lock integrated circuit is ready to accept key inputs.

**NOTE: Due to mechanical keyboard bounce it may be necessary to include these (750pf) capacitors.