LSI/CSI

LS7260
LS7262

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (631) 271-0400 FAX (631) 271-0405

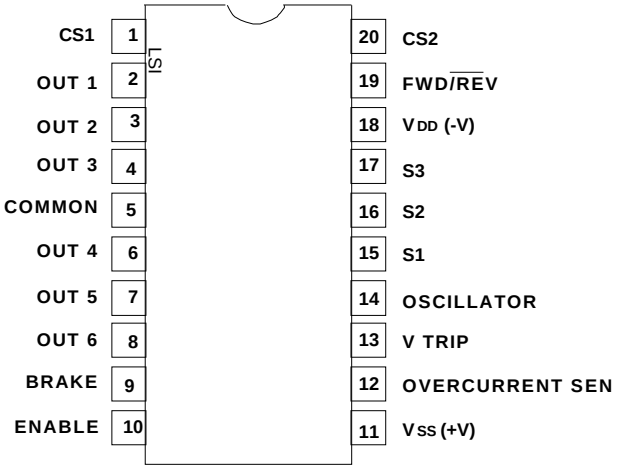
BRUSHLESS DC MOTOR COMMUTATOR/CONTROLLER

November 1997

FEATURES:

- Direct drive of P-Channel and N-Channel FETs (LS7260)
- Direct drive of PNP and NPN transistors (LS7262)
- Six outputs drive power switching bridge directly
- Open or closed loop motor speed control.
- +5V to +28V operation (Vss - V_{DD}).
- Externally selectable input to output code for 60°, 120°, 240°, or 300° electrical sensor spacing.
- Three or four phase operation
- Analog Speed control
- Direction control
- Output Enable control
- Positive Static Braking
- Overcurrent Sensing
- LS7260, LS7262 (DIP); LS7260-S, LS7262-S (SOIC) LS7260-TS, LS7262-TS (TSSOP) - See Connection Diag.

CONNECTION DIAGRAM - TOP VIEW



DESCRIPTION:

The LS7260/LS7262 are monolithic, MOS integrated circuits designed to generate the signals necessary to control a three phase or four phase brushless DC motor. They are the basic building blocks of a brushless DC motor controller. The circuits respond to changes at the SENSE inputs, originating at the motor position sensors, to provide electronic commutation of the motor windings. Pulse Width Modulation of outputs for motor speed control is accomplished through either the ENABLE input or through the Analog input (VTRIP) in conjunction with the OSCILLATOR input. Overcurrent circuitry is provided to protect the windings, associated drivers and power supply. The overcurrent circuitry causes the external output drivers to switch off immediately upon sensing the overcurrent condition and on again only when the overcurrent condition disappears and the positive edge of either the ENABLE input or the sawtooth OSCILLATOR occurs. This limits the overcurrent sense cycling to the chopping rate of the ENABLE input or the sawtooth OSCILLATOR.

A positive braking feature is provided to effect rapid deceleration. While the LS7262 is designed for driving NPN and PNP transistors (See Fig. 2), the LS7260 is designed to drive both NMOS and PMOS Power FETs and develops a full 12V drive for both the N-Channel and P-Channel devices (See Fig. 1) when using a 12V power supply.

INPUT/OUTPUT DESCRIPTION:

COMMUTATION SELECTS (Pins 1, 20)

These inputs are used to select the proper sequence of outputs based on the electrical separation of the motor position sensors. See Table 3. Note that in all cases the external output drivers are disabled for invalid SENSE input codes. Internal pull down resistors are provided at Pins 1 and 20 causing a logic zero when these pins are left open.

FORWARD/$\overline{\text{REVERSE}}$ (Pin 19)

This input is used to select the proper sequence of Outputs for the desired direction of rotation for the Motor (See Table 3). An internal pull-up resistor holds the input high when left open.

SENSE INPUTS (Pins 15, 16, 17)

These inputs provide control of the output commutation sequence as shown in Table 3. S1, S2, S3 originate in the position sensors of the motor and must sequence in cycle code order. Hall Switch pull-up resistors are provided at Pins 15, 16 and 17. The positive supply of the Hall devices should be common to the chip Vss.

BRAKE (Pin 9)

For the LS7262, a high level at this input unconditionally turns OFF Outputs 1, 2 and 3 and turns ON Outputs 4, 5 and 6 (See Fig. 2). For the LS7260, a high level at this input turns ON Outputs 1, 2 and 3 and Outputs 4, 5 and 6 (See Fig. 1). In both cases, transistors Q101, Q102 and Q103 cut off and transistors Q104, Q105 and Q106 turn on, shorting the windings together, The BRAKE has priority over all other inputs.

BRAKE (Pin 9) (Cont'd)
An internal pull-down resistor holds the input low when left open. (Center- tapped motor configuration requires a power supply disconnect transistor controlled by the BRAKE signal - See Figure 2A).

ENABLE (Pin 10)
A high level at this input permits the output to sequence as in Table 3, while a low disables all external output drivers. An internal pull-up resistor holds the input high when left open. Positive edges at this input will reset the overcurrent flip-flop.

OVERCURRENT SENSE (Pin 12)
This input provides the user a way of protecting the motor winding, drivers and power supply from an overload condition. The user provides a fractional-ohm resistor between the negative supply and the common emitters of the NPN drivers or common sources of N-Channel FET drivers. This point is connected to one end of a potentiometer (e.g. 100K ohms), the other end of which is connected to the positive supply. The wiper pickoff is adjusted so that all outputs are disabled for currents greater than the limit. The action of the input is to disable all external output drivers. When BRAKE exists, OVERCURRENT SENSE will be overridden. The overcurrent circuitry latches the overcurrent condition. The latch may be reset by the positive edge of either the sawtooth OSCILLATOR or the ENABLE input. When using the ENABLE input as a chopped input, the OSC input should be held at V_{SS}. When the ENABLE input is held high, the OSC- must be used to reset the overcurrent latch.

VTRIP (Pin 13)
This input is used in conjunction with the sawtooth OSC input. When the voltage level applied to VTRIP is more negative than the waveform at the OSC input, the Outputs will be enabled as shown in Table 3. When VTRIP is more positive than the sawtooth OSCILLATOR waveform the external output drivers are disabled.

The sawtooth waveform at the OSC input typically varies from .4 Vss to Vss-2V. The purpose of the VTRIP input in conjunction with the OSCILLATOR is to provide variable speed adjustment for the motor by means of PWM.

OSCILLATOR (Pin 14)
An R and C connected to this input (See Figure 6) provide the timing components for a sawtooth OSCILLATOR. The signal generated is used in conjunction with VTRIP to provide PWM for variable speed applications and to reset the overcurrent condition.

OUTPUTS 1, 2, 3 (Pins 2, 3, 4)
For the LS7262, these open drain Outputs are enabled as shown in Table 2 and provide base current to PNP transistors or gate drive to P-Channel FET drivers when COMMON is floating. If COMMON is held at Vss, these Outputs can provide drive to NPN transistors or N-Channel FET drivers. For the LS7260, these Outputs provide drive to P-Channel FET drivers if COMMON is held at V_{SS}.

OUTPUTS 4, 5, 6 (Pins 6, 7, 8)
These open drain Outputs are enabled as in Table 2 and provide base current to NPN transistors or gate drive to N-Channel FET drivers.

COMMON (Pin 5)
The COMMON may be connected to Vss when using a center-tapped motor configuration or when using all NPN or N-Channel drivers. For the LS7260, the COMMON is tied to V_{SS}.

Vss (Pin 11)
Supply voltage positive terminal.

V_{DD} (Pin 18)
Supply voltage negative terminal (ground).

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Temperature	T_A	-25 to +85	°C
	T_A **(1)**	-40 to +125	°C
Voltage (any pin to Vss)	V_{MAX}	-30 to +.5	V

(1) Available on special order. Contact factory for details.

DC ELECTRICAL CHARACTERISTICS:
(All Voltages Referenced to V_{DD}, T_A = 25°C unless otherwise specified)

	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{SS}	5	-	28	V
Supply Current (Outputs not loaded)	I_{DD}	-	4.5	6	mA
Input Specifications:					
BRAKE, ENABLE, CS1, CS2	R_{IN}	-	150	-	KΩ
S1, S2, S3, FWD/REV					
Voltage (Logic "1")	V_{IH}	V_{SS}-1.5	-	V_{SS}	V
(Logic "0")	V_{IL}	0	-	V_{SS}-4.0	V
OVERCURRENT SENSE (See Note)					
Threshold Voltage	V_{TH}	(V_{SS}/2)-.25	-	(V_{SS}/2)+.25	V

Oscillator:

Frequency Range	Fosc	0	1/RC	100	kHz
External Resistor Range	Rosc	22	-	1000	kΩ

NOTE: Theoretical switching point of the OVERCURRENT SENSE input is one half of the power supply determined by an internal bias network in manufacturing. Tolerances cause the switching point to vary plus or minus .25V. After manufacture, the switching point remains fixed within 10mV over time and temperature. The input switching sensivity is a maximum of 50mV. There is no hysteresis on the OVERCURRENT SENSE input.

TYPICAL CIRCUIT OPERATION:

The oscillator is used for motor speed control as explained under VTRIP. Both upper and lower motor drive transistors are pulse width modulated (See Fig. 1 or 2) during speed control.

For the LS7262, the outputs turn on in pairs (See Table 3). For example (See dotted line, Fig. 2): Q8 and Q4 are on, thus enabling a path from the positive supply through the emitter-base junction of Q101, Q8, Q4, R5, the base emitter junction of Q105 and the fractional-ohm resistor to ground. The current in the above described path is determined by the power supply voltage, the voltage drops across the base-emitter junctions of Q101 and Q105 (1.4V for single transistor or 2.8V for Darlington pairs), the impedance of Q8 and Q4 and the value of R5. Table 1 provides the recommended value for R5. R4 and R6 are the same value.

For the LS7260, (See Fig. 1) the external drivers also turn on in pairs. Internal operation is somewhat different than the LS7262. For example, external transistors Q101 and Q105 will turn on when internal transistor Q8 turns off and Q4 turns on enabling full power supply drive on Q101 and Q105. Since Pin 5 is tied to VSS, the gate of P-channel Driver Q101 is brought to ground by R1 and the Gate of N-Channel driver Q105 is brought to VSS by Q4. Other external output pairs turn on similarly and the commutation sequence is identical to that of the LS7262 (Table 3). Table 2 indicates the minimum value of R1 (=R2=R3=R4=R5=R6) needed as a function of output drive voltage for Fig. 1.

TABLE 1
OUTPUT CURRENT LIMITING RESISTOR SELECTION TABLE

POWER SUPPLY (VOLTS)	OUTPUT CURRENT 20	15	10	7.5	5	2.5	mA
6	**	**	**	**	**	.24	
9	**	**	**	.43	.86	2.2	
12	.20	.33	.62	.91	1.5	3.3	
15	.36	.56	.91	1.3	2.2	4.3	Resistance
18	*	.75	1.2	1.6	2.7	5.1	(kΩ)
21	*	*	1.5	2.0	3.3	6.2	
24	*	*	1.8	2.3	3.6	7.5	
28	*	*	*	2.7	4.3	9.1	

*causes excessive power dissipation
**exceeds max current possible for this voltage

TABLE 2
For Power Supply 5V-28V

R1 (k ohms)	Output Voltage
10	Vss -0.5
4.0	Vss -1.0
1.5	Vss -2.0

TABLE 3. OUTPUT COMMUTATION SEQUENCE FOR THREE PHASE OPERATION

SEQUENCE SELECT	CS1 CS2	CS1 CS2	CS1 CS2	CS1 CS2	FWD/$\overline{REV}$=1				FWD/$\overline{REV}$=0			
	0 0	0 1	1 0	1 1								
ELECTRICAL SEPARATION	(-60°-)	(-120°-)	(-240°-)	(-300°-)	OUTPUTS *	DRIVERS *			OUTPUTS *	DRIVERS *		
SENSE INPUTS	S1 S2 S3	S1 S2 S3	S1 S2 S3	S1 S2 S3	ENABLED	A	B	C	ENABLED	A	B	C
	0 0 0	0 0 1	0 1 0	0 1 1	O1, O5	+	-	Off	O2, O4	-	+	Off
	1 0 0	1 0 1	1 1 0	1 1 1	O3, O5	Off	-	+	O2, O6	Off	+	-
	1 1 0	1 0 0	1 0 0	1 1 0	O3, O4	-	Off	+	O1, O6	+	Off	-
	1 1 1	1 1 0	1 0 1	1 0 0	O2, O4	-	+	Off	O1, O5	+	-	Off
	0 1 1	0 1 0	0 0 1	0 0 0	O2, O6	Off	+	-	O3, O5	Off	-	+
	0 0 1	0 1 1	0 1 1	0 0 1	O1, O6	+	Off	-	O3, O4	-	Off	+
	0 1 0	0 0 0	0 0 0	0 1 0	ALL DISABLED				ALL DISABLED			
	1 0 1	1 1 1	1 1 1	1 0 1	ALL DISABLED				ALL DISABLED			

* See Figures 1 and 2. For the LS7260, Outputs O1,O2,O3 are the logical inversions of the corresponding Outputs of the LS7262.

The OVERCURRENT input (BRAKE low) enables external output drivers in normal sequence when more negative than Vss/2 and disables all external output drivers when more positive than Vss/2. The OVERCURRENT is sensed continuously, and sets a flip flop which is reset by the rising edge of the ENABLE input or the sawtooth OSCILLATOR. (See description under OVERCURRENT SENSE.)

The VTRIP Input (BRAKE low) enables the outputs in normal sequence when more negative than the OSC input and disables all outputs when more positive than the OSC input. The VTRIP input may be disabled by connecting it to VDD and the OSC input to VSS. (See description under VTRIP)

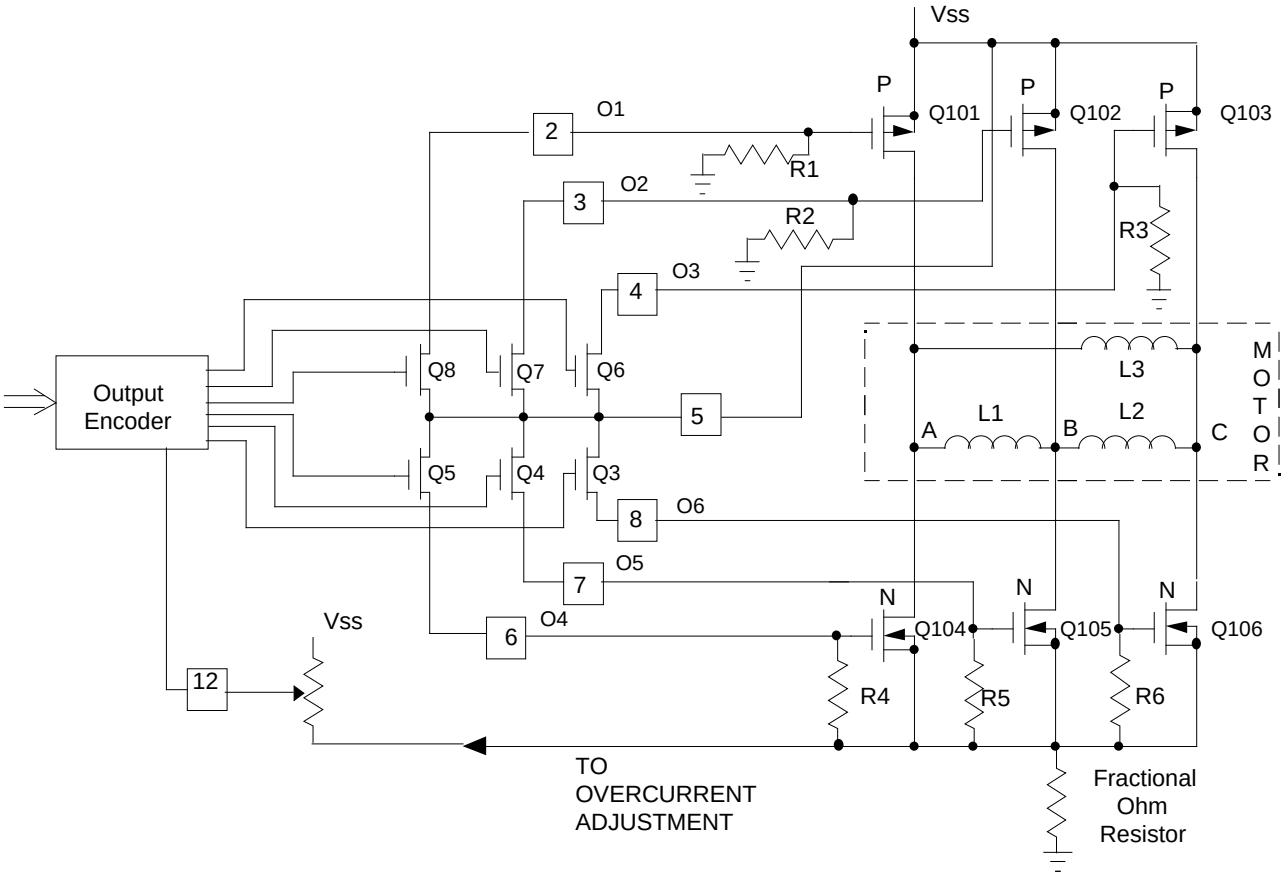


FIGURE 1. LS7260 THREE PHASE OUTPUT DRIVER CIRCUITRY

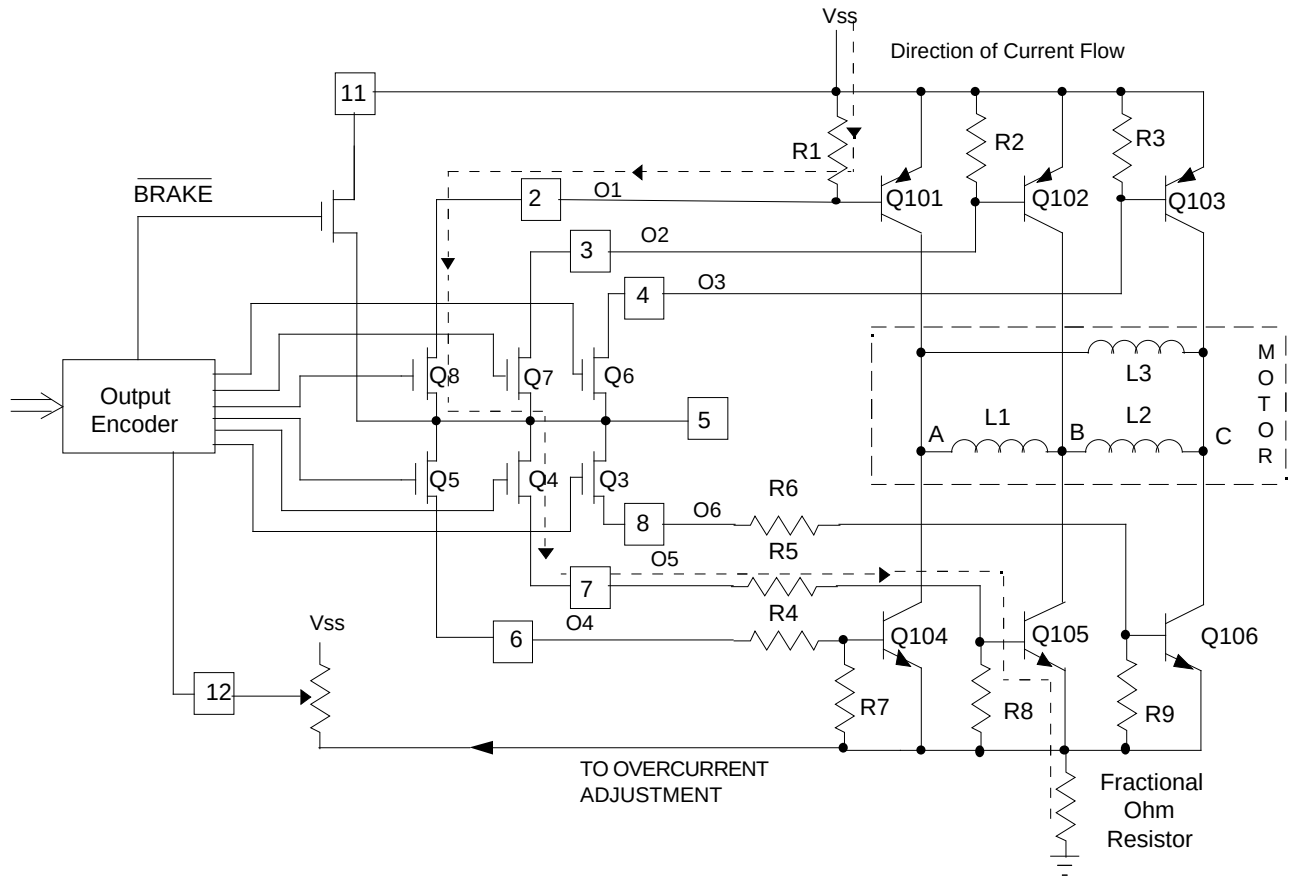


FIGURE 2. LS7262 THREE PHASE OUTPUT DRIVER CIRCUITRY

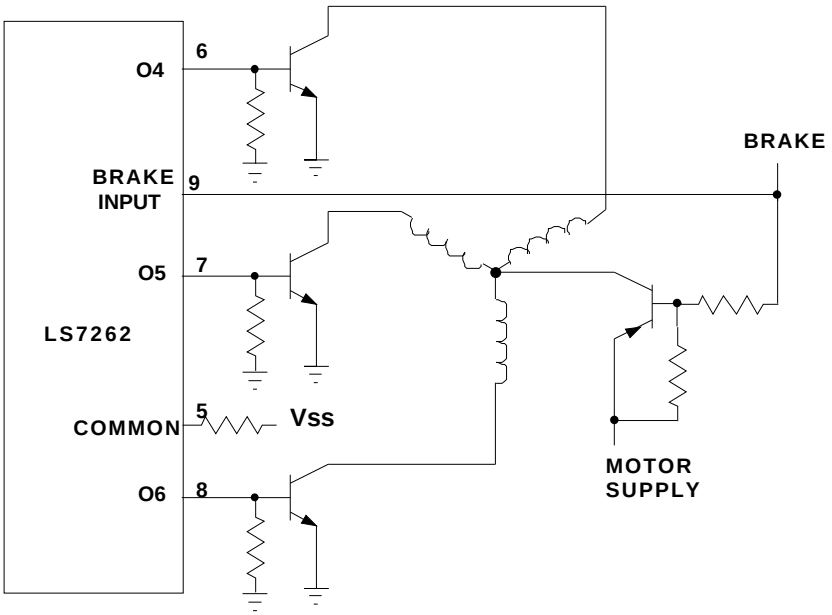


FIGURE 2A. SINGLE-ENDED DRIVER CIRCUIT

This configuration requires only one base current limiting resistor connected from the COMMON pin to Vss.

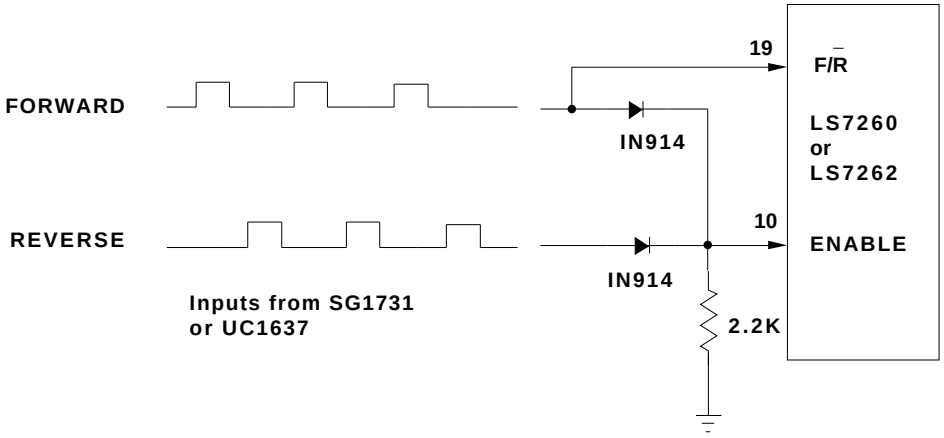


FIGURE 3. PRECISION CONTROL BRUSHLESS DC MOTOR DRIVE

For controlled acceleration and deceleration of motors in the forward or reverse directions, a motor control pulse width modulator circuit such as the SG1731 or UC1637 can be interfaced with the LS7260 or LS7262.

The logical OR gate made up of the resistor-diode network permits the LS7260 or LS7262 to be enabled when either the forward or reverse input is high. By applying the forward input directly to Pin 19, the motor can only operate in the forward direction when the forward input is high and only in the reverse direction when the reverse input is high. Motor direction is determined by relative pulse widths of the forward and reverse inputs while acceleration or deceleration is determined by variations of these widths.

TABLE 4. OUTPUT COMMUTATION SEQUENCE FOR FOUR PHASE OPERATION
CS1=CS2=0 OUTPUTS ENABLED

S1	S2,S3	FWD/$\overline{\text{REV}}$ = 1	FWD/$\overline{\text{REV}}$ = 0
0	0	O1	O4
1	0	O3	O6
1	1	O4	O1
0	1	O6	O3

For four phase commutation (See Fig. 4), the COMMUTATION SELECT inputs must both be tied low. The S1 input is driven from one motor position sensor while the S2 and S3 inputs are connected together and driven by the second position sensor. The COMMON input must be connected to Vss. The sensors have an electrical separation of 90°. Figure 4A indicates the use of Bipolar Transistors. Figure 4B indicates the use of FETs. In both cases, the LS7262 is used.

FIGURE 4. FOUR PHASE OUTPUT DRIVER CIRCUITRY

FIGURE 4A

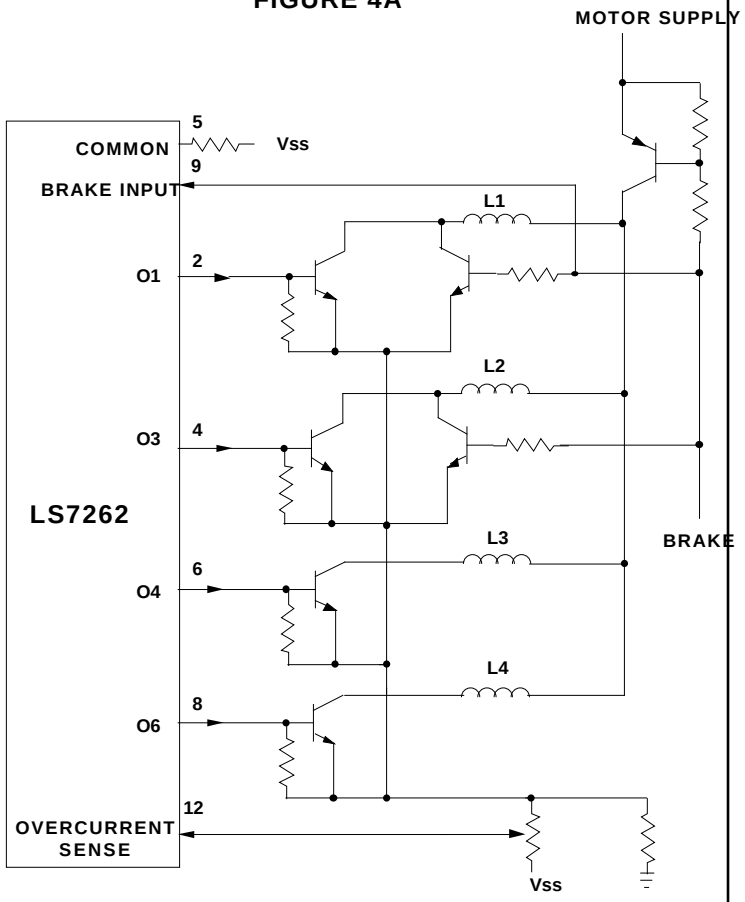
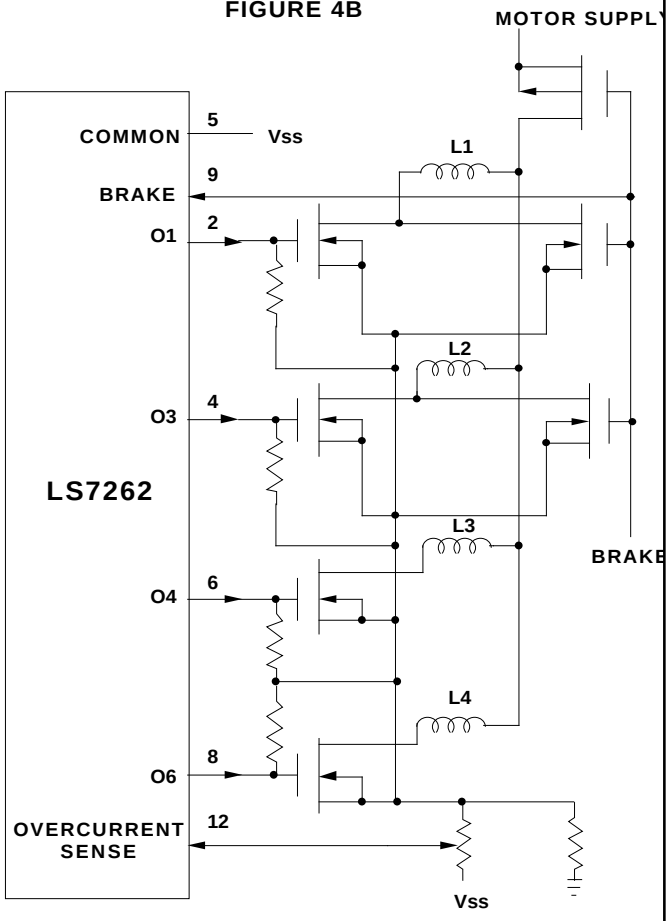


FIGURE 4B



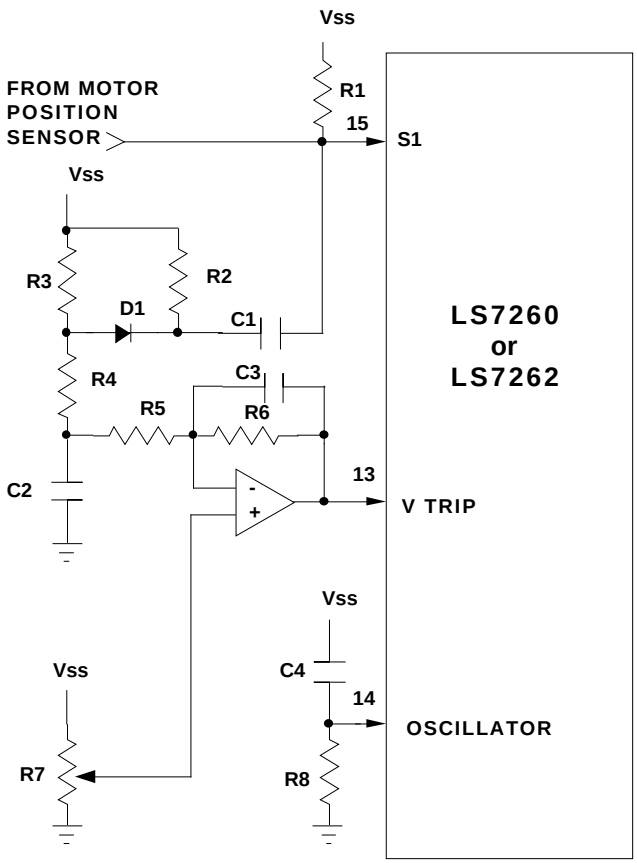
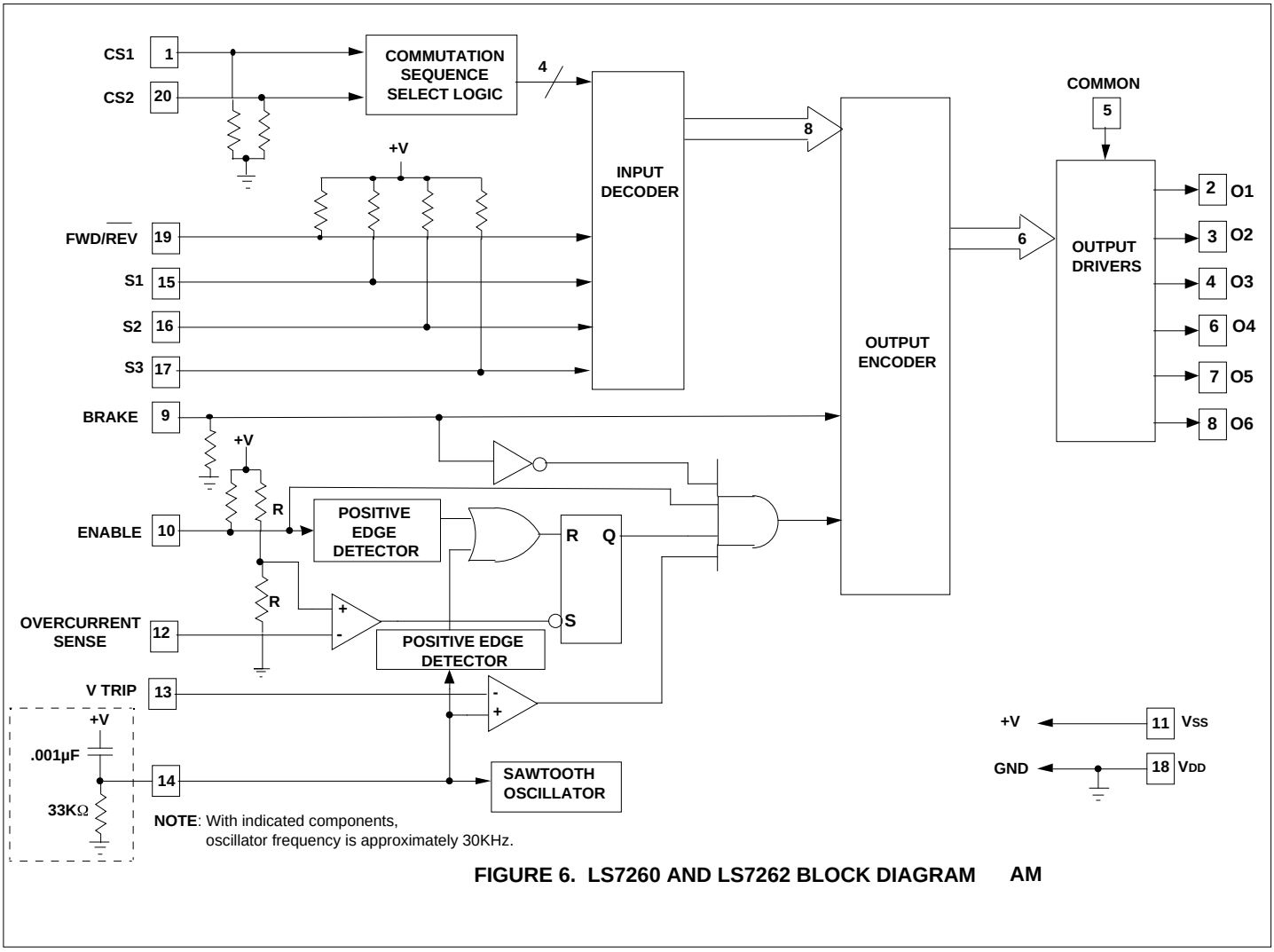


FIGURE 5
CLOSED-LOOP SPEED CONTROLLER

A closed loop system can be configured by differentiating one of the motor position sense inputs and integrating only the negative pulses to form a DC voltage that is applied to the inverting input of an op-amp. The non-inverting input voltage is adjusted with a potentiometer until the resultant voltage at VTRIP causes the motor to run at desired speed. The R2-C1 differentiator, the R3-D1 negative pulse transmitter and the R4-C2 integrator form a frequency to voltage converter. An increase in motor speed above the desired speed causes VTRIP to increase which lowers the PWM and the resultant motor speed. A decrease in speed lowers VTRIP and raises the PWM and the resultant motor speed. For proper operation, both R5 and R6 should be greater than R4, and R4 in turn should be greater than both R2 and R3. Also, the R4-C2 time constant should be greater than the R2-C1 time constant. C3 may be added across R6 for additional VTRIP smoothing.



NOTE: With indicated components, oscillator frequency is approximately 30KHz.

FIGURE 6. LS7260 AND LS7262 BLOCK DIAGRAM AM