LINEAR SYSTEMS

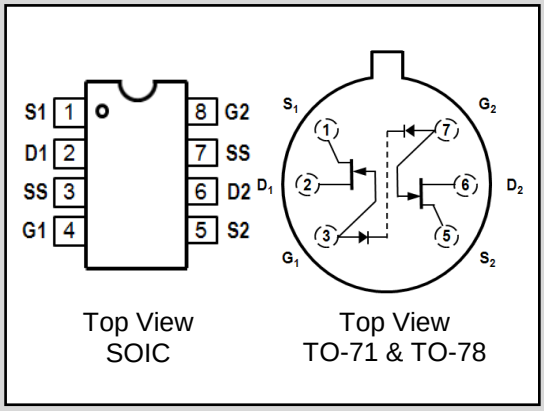
Twenty-Five Years Of Quality Through Innovation

LS830 LS831 LS832 LS833

ULTRA LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW DRIFT	$\lvert \Delta V_{GS1-2}/\Delta T \rvert$ = 5µV/ºC max.
ULTRA LOW NOISE	I_G=80fA TYP.
LOW NOISE	e_n=70nV/√Hz TYP.
LOW CAPACITANCE	C_{ISS}=3pf max.

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10µA
Maximum Power Dissipation @ TA = 25ºC		
Continuous Power Dissipation (Total)		500mW



Top View SOIC

Top View TO-71 & TO-78

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0 I_G= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_G= ±1µA I_D= 0 I_S = 0
	TRANSCONDUCTANCE					
g_{fss}	Full Conduction	70	300	500	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
g_{fs}	Typical Operation	50	100	200	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
$\lvert g_{fs1-2}/g_{fs} \rvert$	Differential	--	1	5	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	400	1000	µA	V_{DG}= 10V V_{GS}= 0
$\lvert I_{DSS1-2}/I_{DSS} \rvert$	Differential at Full Conduction	--	2	5	%	

ELECTRICAL CHARACTERISTICS TA = 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS830	LS831	LS832	LS833	UNITS	CONDITIONS
$\lvert \Delta V_{GS1-2}/\Delta T \rvert$ max.	Drift vs. Temperature	5	10	20	75	µV/ºC	V_{DG} = 10V I_D = 30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2} \rvert$ max.	Offset Voltage	25	25	25	25	mV	V_{DG} = 10V I_D = 30µA
$-I_G$ typical	Operating	0.1	0.1	0.1	0.5	pA	
$-I_G$ typical	High Temperature	0.1	0.1	0.1	0.5	nA	TA= +125ºC
I_{GSS} typical	At Full Conduction	0.2	0.2	0.2	1.0	pA	V_{GS} = 20V, V_{GS} = 0V
I_{GSS} typical	High Temperature	0.5	0.5	0.5	1.0	nA	V_{GS} = 0 V_{GS} = 20V TA= +125ºC

Linear Integrated Systems

• 4042 Clipper Court • Fremont, CA 94538 • Tel: 510 490-9160 • Fax: 510 353-0261

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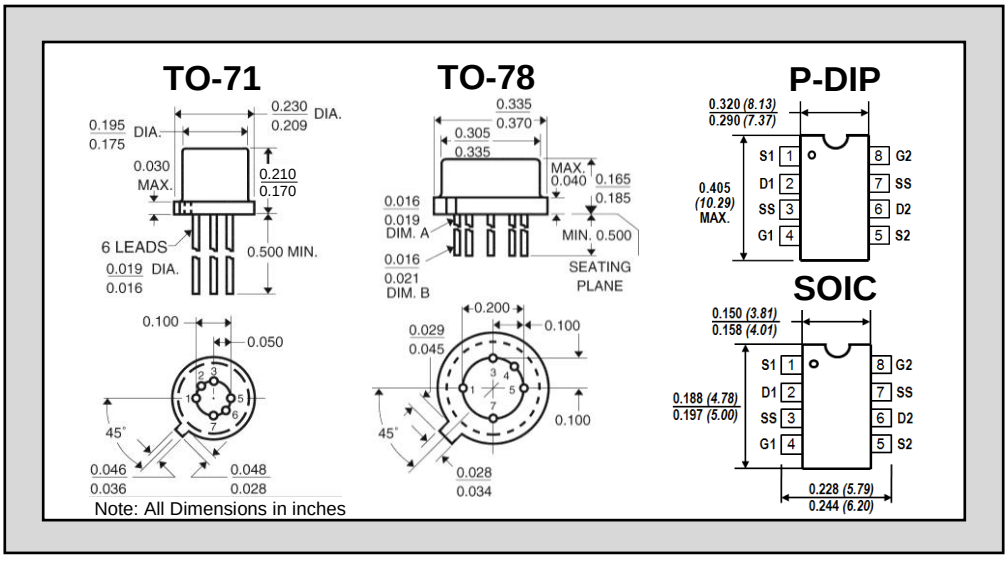
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
	GATE-SOURCE							
$V_{GS}(off)$	Cutoff Voltage	-0.6	-2	-4.5	V	V_{DS}= 10V	I_D= 1nA	
V_{GS}	Operating Range	--	--	-4	V	V_{DG}= 10V	I_D= 30µA	
	GATE CURRENT							
I_{GGO}	Gate-to-Gate Leakage	--	1	--	pA	V_{GG}= ±20V	$I_D = I_S$ = 0A	
	OUTPUT CONDUCTANCE							
g_{OSS}	Full Conduction	--	--	5	µS	V_{DG}= 10V	V_{GS}= 0	
g_{OS}	Operating	--	--	0.5	µS	V_{DG}= 10V	I_D= 30µA	
$\lvert g_{OS\ 1\text{-}2} \rvert$	Differential	--	--	0.1	µS			
	COMMON MODE REJECTION							
CMRR	-20 log $\lvert \Delta V_{GS1\text{-}2} / \Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V		I_D=30µA
CMRR	-20 log $\lvert \Delta V_{GS1\text{-}2} / \Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V		I_D=30µA
	NOISE							
NF	Figure	--	--	1	dB	V_{DS}= 10V f= 100Hz	V_{GS}= 0 NBW= 6Hz	R_G=10MΩ
e_n	Voltage	--	20	70	nV/√Hz	V_{DG}= 10V NBW= 1Hz	I_D= 30µA	f= 10Hz
	CAPACITANCE							
C_{ISS}	Input	--	--	3	pF	V_{DS}= 10V	V_{GS}= 0	f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V	V_{GS}= 0	f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DG}= 10V	I_D= 30µA	



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.

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