

**LV1100****Digital Surround Audio Signal-Processing IC****Overview**

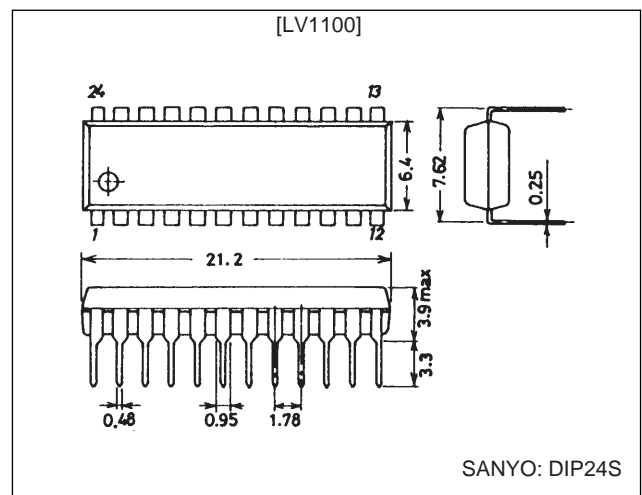
The LV1100 is an audio signal-processing Bi-CMOS LSI that integrates input and output filters, a delay line (built-in memory), and a delay/reverb function with a maximum delay of 120 ms on a single chip. It also provides built-in fixed matrix (L+R, L-R) and front mixing (with level and phase switching) functions. A full complement of surround modes can be easily implemented by combining these functions.

**Functions and Features**

- Input switching (L+R, L-R, IN-A)
- On-chip memory (12K SRAM)
- Front adder (+3 dB, 0 dB, -3 dB, -∞)
- Input and output filters
- Input filter -7 kHz low-pass filter
- Output filter -5 kHz low-pass filter: switchable with a 3 kHz low-pass filter
- On-chip  $V_{DD}$  circuit
- Input and output muting function
- A simulated surround system can be easily implemented with only one chip.
- ADM A/D and D/A converters
- Variable delay times
  - Short mode; Maximum delay: 60 ms. Delay time selectable from six delay times in 10-ms steps.
  - Long mode; Maximum delay: 120 ms. Delay time selectable from six delay times in 20-ms steps.

**Package Dimensions**

unit: mm

**3067-DIP24S****Specifications****Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$** 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$		12	V
Allowable power dissipation	$P_d \text{ max}$	$T_a \leq 70^\circ\text{C}$	420	mW
Operating temperature	$T_{opr}$		-25 to +70	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

**Allowable Operating Ranges at  $T_a = 25^\circ\text{C}$** 

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}$		9	V
Operating supply voltage range	$V_{CC \text{ opg}}$		8 to 10	V

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## LV1100

**Electrical Characteristics at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 9\text{ V}$ ,  $R_L = 20\text{ k}\Omega$ ,  $V_{IN} = 300\text{ mV}$  and  $f = 1\text{ kHz}$  unless otherwise specified.**

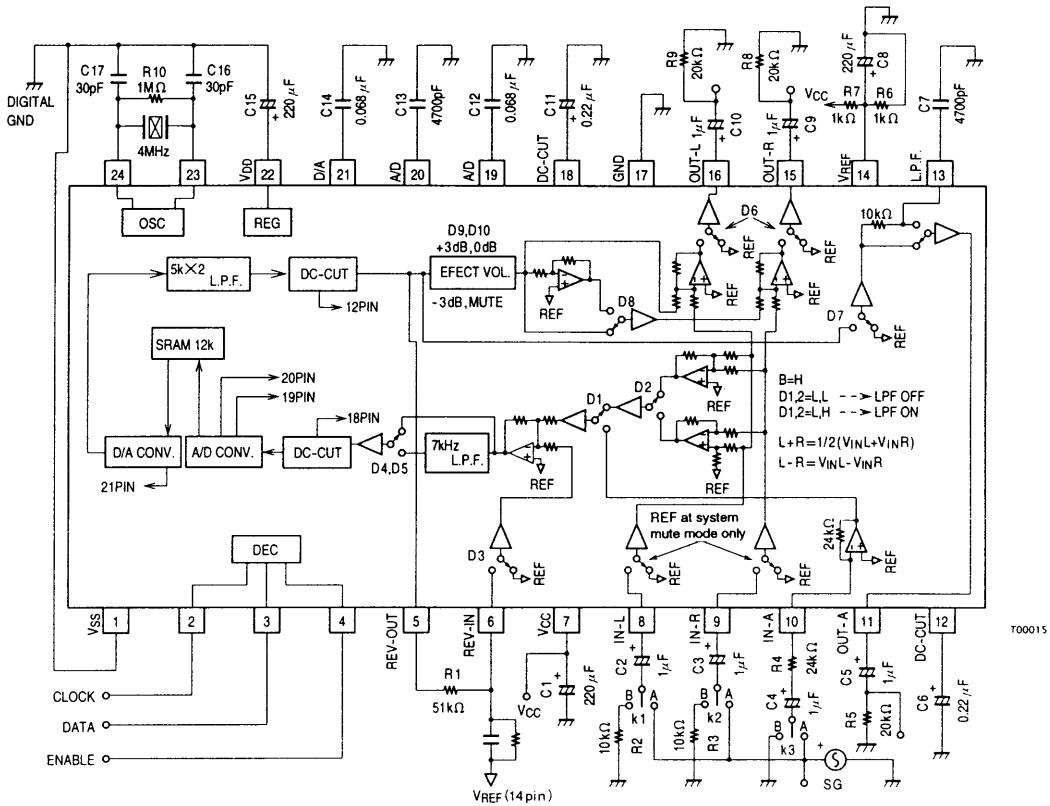
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	$I_{CCO}$		15	28	42	mA
Maximum output voltage	$V_{O\text{ maxA}}$	OUT-A, CLOCK FAST, THD = 10% $V_{CC} = 8\text{ V}$	0.7	1.0		V
	$V_{O\text{ maxL}}$	OUT-L, THD = 1% (effect off), $V_{CC} = 8\text{ V}$	1.6			V
	$V_{O\text{ maxR}}$	OUT-R, THD = 1% (effect off), $V_{CC} = 8\text{ V}$	1.6			V
Output noise voltage	$V_{NOAF}$	OUT-A, CLOCK FAST (5 kHz L.P.F) JIS A, $R_g = 10\text{ k}\Omega$		-89	-80	dBV
	$V_{NOAS}$	OUT-A, CLOCK SLOW (3 kHz L.P.F) JIS A, $R_g = 10\text{ k}\Omega$		-84	-75	dBV
	$V_{NOL}$	OUT-L (effect off), JIS A, $R_g = 10\text{ k}\Omega$		-103	-95	dBV
	$V_{NOR}$	OUT-R (effect off), JIS A, $R_g = 10\text{ k}\Omega$		-103	-95	dBV
	$V_{NOLE}$	OUT-L (effect -3 dB), JIS A, $R_g = 10\text{ k}\Omega$		-88	-80	dBV
	$V_{NORE}$	OUT-R (effect -3 dB), JIS A, $R_g = 10\text{ k}\Omega$		-88	-80	dBV
Output level deviation	VGA	OUT-A, CLOCK FAST	-4	0	4	dB
	VGL	OUT-L (effect off)	-2	0	2	dB
	VGR	OUT-R (effect off)	-2	0	2	dB
Total harmonic distortion	THDAF	OUT-A, CLOCK FAST (5 kHz L.P.F): 400 to 30 kHz BPF		0.3	1.0	%
	THDAS	OUT-A, CLOCK SLOW (3 kHz L.P.F): 400 to 30 kHz BPF		0.6	1.5	%
	THDL	OUT-L (effect off): 400 to 30 kHz B.P.F		0.01	0.03	%
	THDR	OUT-R (effect off): 400 to 30 kHz B.P.F		0.01	0.03	%

### Control Data

Parameter	Symbol	Conditions	Ratings	Unit
Control data Input low-level voltage	$V_{IL}$		0 to 1.5	V
Control data Input high-level voltage	$V_{IH}$		3.5 to 5.5	V

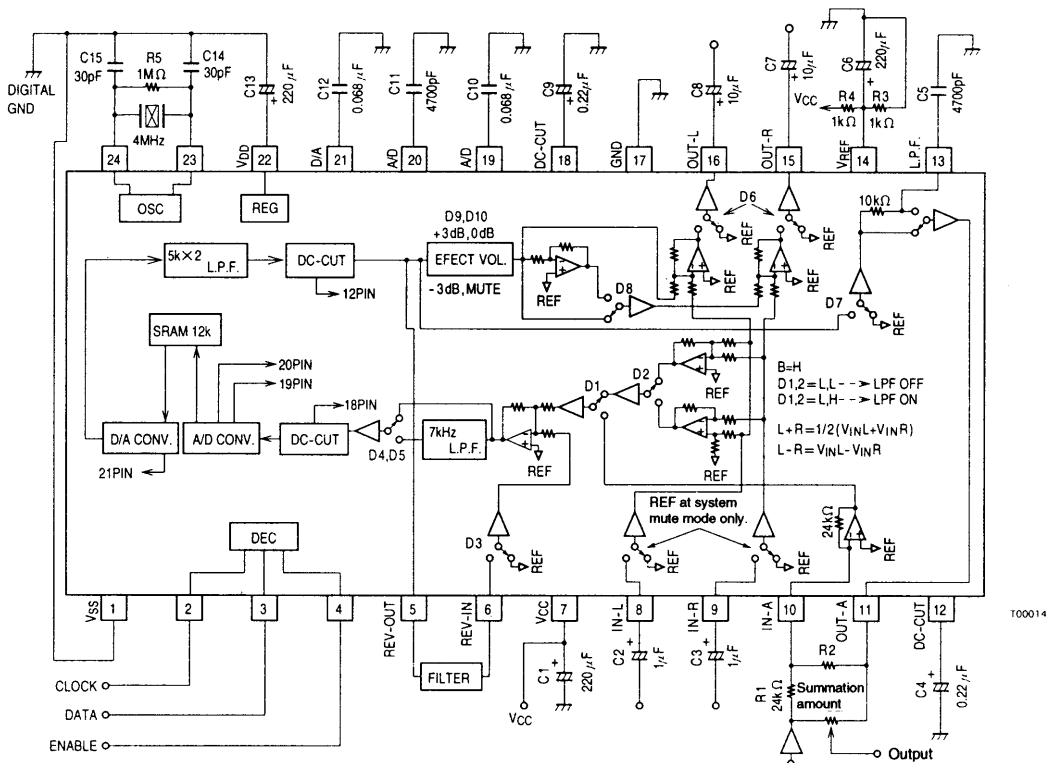
# LV1100

## Test Circuit



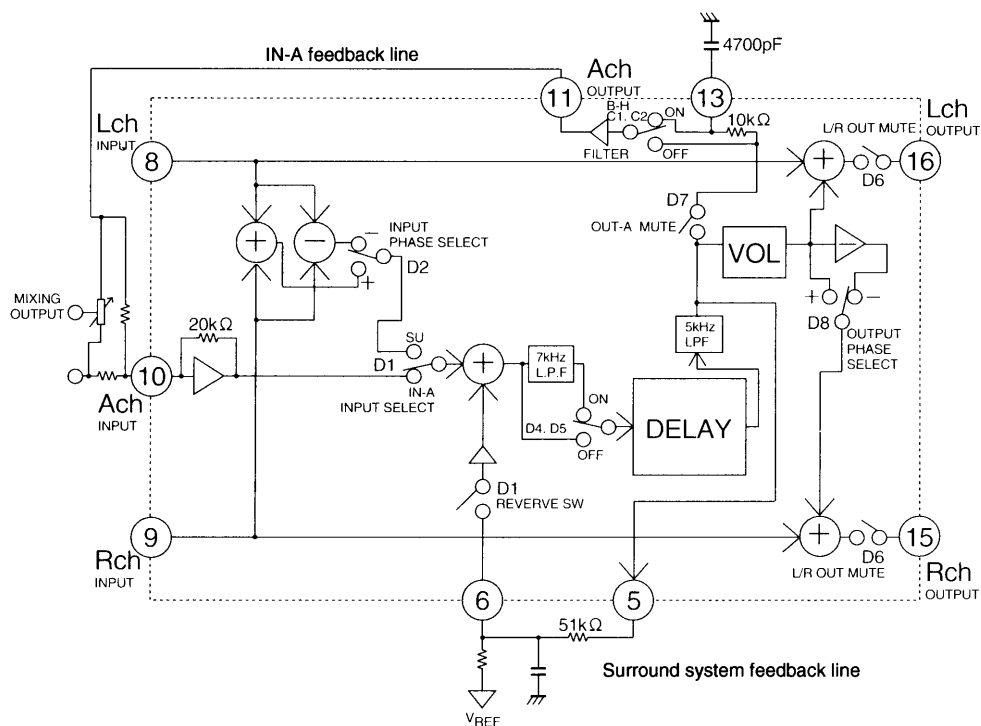
- Notes:
1. The items D1 through D10 in the figure indicate points that are switched by the serial data.
  2. Use capacitors with good high-frequency characteristics for the capacitors on pins 7, 14, and 22. Also, connect 0.1-μF ceramic capacitors in parallel.

## Application Circuit Example



Note: The items D1 through D10 in the figure indicate points that are switched by the serial data.

## Block Diagram



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## Functional Description

## 1.INPUT PHASE SELECT

Selects either the input summation signal (L+R) or the input difference signal (L-R). When set to low, L+R is selected, and when set to high, L-R is selected.

## 2.INPUT SELECT

Selects either the IN-L and IN-R input signals, or the IN-A input signal.

## 3.INPUT FILTER

Selects whether the signal input from either IN-L and IN-R or IN-A is passed through a 7-kHz low-pass filter, or whether it is directly input to the delay block.

## 4.DELAY

In clock fast mode, creates one of six delayed signals with delays of 10 to 60 ms in 10-ms steps.

In clock slow mode, creates one of six delayed signals with delays of 20 to 120 ms in 20-ms steps.

## 5.VOL (effect volume)

Selects the amount of the front L and R signals added to the delayed signal. Possible settings are +3 dB, 0 dB, -3 dB, and  $-\infty$ .

## 6.OUTPUT PHASE SELECT

Selects in-phase (+ setting) or out-of-phase (- setting) with respect to the left channel for the right channel of the VOL output signal.

## 7.REVERVE SW

Set this switch to the on position to specify that the surround system output signal be fed back.

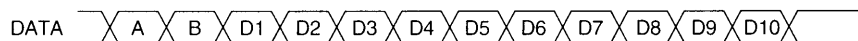
## 8.IN-A OUTPUT FILTER

Allows the signal to be output after passing through a 3-kHz low-pass filter.

## LV1100

### Command List

LV1100 Control Format



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A = L ... Selects the LV1100.

B = L ... When B is low, the mode settings listed below can be made.

	L	H
D1	IN-A DELAY	L+R, L-R DELAY
D2	L+R	L-R
D3	DELAY OUT ON; Turns on surround system feedback	DELAY OUT OFF; Turns off surround system feedback
7 kHz L.P.F ON/OFF		
D4, D5		
LL	THROUGH	
LH	NOT USE	
HL	FILTER	
HH	A/D INPUT MUTE	
	L	H
D6	OUT-L, -R MUTE ON	OUT-L, -R MUTE OFF
D7	OUT-A MUTE ON	OUT-A MUTE OFF
D8	FRONT ADD INPHASE (In-phase addition)	FRONT ADD INVERTED PHASE (Out-of-phase addition)
FRONT ADD EFFECT VOL (Addition to the front left and right channels)		
D9, D10		
LL	+3 dB	
LH	0 dB	
HL	-3 dB	
HH	MUTE	

B = H ... When B is high, the mode settings listed below can be made.

D1	D2	IN-A output filter
L	L	3 kHz L.P.F-OFF
L	H	3 kHz L.P.F-ON

D3	D4	D5
*	*	*

\* = don't care

## LV1100

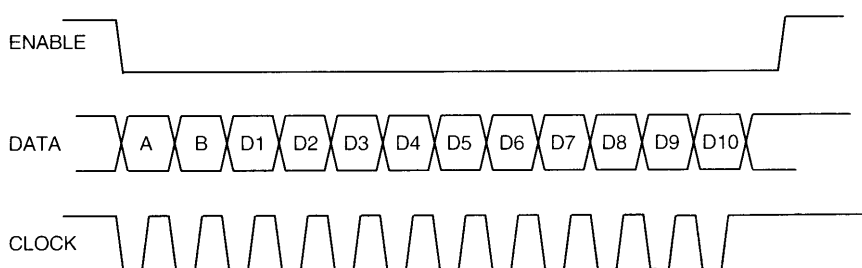
### Delay Time Data (D6 to D8)

D6	D7	D8	CLK FAST	CLK SLOW
L	L	L	10 ms	20 ms
L	L	H	20 ms	40 ms
L	H	L	30 ms	60 ms
L	H	H	40 ms	80 ms
H	L	L	50 ms	100 ms
H	L	H	60 ms	120 ms

Note: D6, D7, and D8 must not be used for any purposes other than the above commands.

	L	H
D9	SYSTEM MUTE ON	SYSTEM MUTE OFF
D10	CLK FAST	CLK SLOW

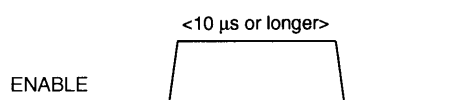
### Control Data Format



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- Data is read in on the rising edge of the clock.
- The control data consists of 12 bits.
- The input data is latched on the rising edge of the enable signal.
- The clock and enable signals must be held high when not being used to control the LV1100.
- Command interval time

The timing of intervals between enable signals must meet the conditions shown in the figure.



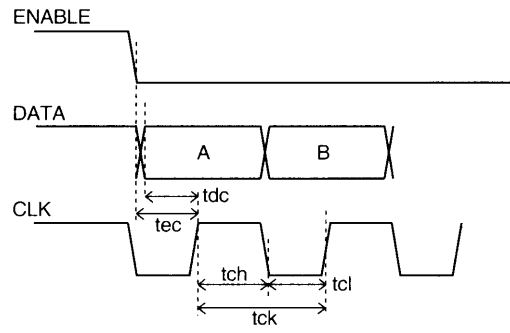
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### Notes on Mode Control (System Mute Usage)

- 1 When power is first applied, after the IC is fully operating (about 2 seconds after power is applied) applications must send commands that turn the system muting off and then on again.
- 2 Applications must perform system muting on/off operations when switching the delay time or clock fast/slow settings. After sending a system muting on command along with the new data, send the new data again, this time with a system muting off command.

Note: By performing the operations described in items 1 and 2 here, the memory contents are initialized, thus preventing incorrect operation.

Data Timing


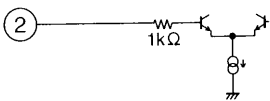
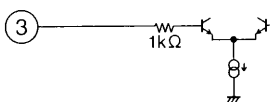
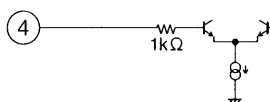
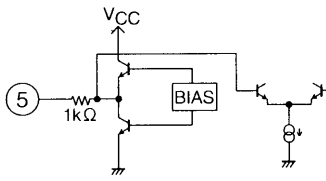
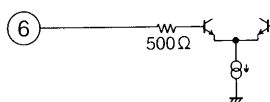
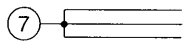
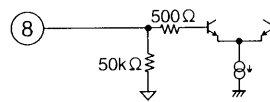
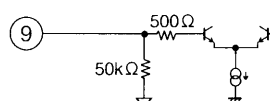
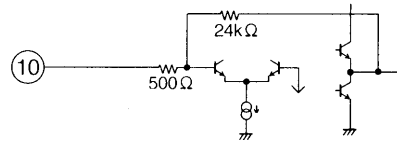
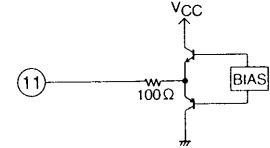
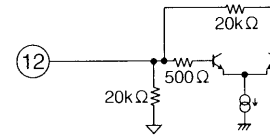


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Timing Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Enable clock delay time	$t_{ec}$		5			$\mu\text{s}$
Data clock delay time	$t_{dc}$		5			$\mu\text{s}$
Clock high-level hold time	$t_{ch}$		5			$\mu\text{s}$
Clock low-level hold time	$t_{cl}$		5			$\mu\text{s}$
Clock cycle time	$t_{ck}$		10			$\mu\text{s}$

Pin Functions

Pin no.	Pin	Pin voltage	Internal equivalent circuit
1	DIGITAL-GND	0 V	 A05990
2	CLK	Control voltage Apply a voltage of 0 or 5 V.	 A05991
3	DATA	Control voltage Apply a voltage of 0 or 5 V.	 A05992
4	ENABLE	Control voltage Apply a voltage of 0 or 5 V.	 A05993
5	REV-OUT	$1/2 V_{CC}$	 A05994
6	REV-IN	$1/2 V_{CC}$ Apply the voltage output by pin 5 through an external resistor.	 A05995
7	$V_{CC}$	$V_{CC}$ (Power-supply voltage)	 A05996
8	IN-L	$1/2 V_{CC}$	 A05997
9	IN-R	$1/2 V_{CC}$	 A05998
10	IN-AUX	$1/2 V_{CC}$	 A05999
11	OUT-AUX	$1/2 V_{CC}$	 A06000
12	DC-CUT	$1/2 V_{CC}$	 A06001

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Pin no.	Pin	Pin voltage	Internal equivalent circuit
13	L.P.F	$1/2 V_{CC}$	<p style="text-align: right;">A06002</p>
14	$V_{REF}$	$1/2 V_{CC}$	<p style="text-align: right;">A06003</p>
15	OUT-R	$1/2 V_{CC}$	<p style="text-align: right;">A06004</p>
16	OUT-L	$1/2 V_{CC}$	<p style="text-align: right;">A06005</p>
17	ANALOG-GND	0 V	<p style="text-align: right;">A06006</p>
18	DC-CUT	$1/2 V_{CC}$	<p style="text-align: right;">A06007</p>
19	A/D integrator	$1/2 V_{CC}$	<p style="text-align: right;">A06008</p>
20	A/D noise shaper	$1/2 V_{CC}$	<p style="text-align: right;">A06009</p>
21	D/A integrator	$1/2 V_{CC}$	<p style="text-align: right;">A06009</p>
22	$V_{DD}$	5 V	<p style="text-align: right;">A06011</p>
23 24	OSC	Charged by 0 or 5 V.	<p style="text-align: right;">A06012</p>

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