



SANYO Semiconductors

DATA SHEET

LV4901H — Bi-CMOS LSI Built-in 80mW Headphone amplifier BTL 10W×2ch Class-D Audio Power Amplifier

Overview

The LV4901H is a 10W per channel stereo digital power amplifier that takes analog inputs. The LV4901H uses unique SANYO-developed feedback technology to achieve excellent audio quality despite being a class D amplifier and can be used to implement high quality flat display panel (FDP) based systems.

Features

- Supports circuit designs that do not require output LC filters
- BTL output, class D amplifier system
- Unique SANYO-developed feedback technology achieves superb audio quality
- High-efficiency class D amplifier, Low EMI
- Soft muting function reduces impulse noise at power on/off
- Full complement of built-in protection circuits : overcurrent protection, thermal protection, and low power supply voltage protection circuits
- Built in boot strap diode
- Built in Headphone amplifier

Functions

- 10W output ($V_D = 12V$, $R_L = 8\Omega$, $THD + N = 10\%$)
- Efficiency : $\eta > 85\%$ ($V_D = 12V$, $R_L = 8\Omega$, $f_{in} = 1kHz$, $P_O = 10W$)
- 80mW Stereo Headphone amplifier ($V_D = 12V$, $R_L = 16\Omega$, $THD + N = 10\%$)
- Package HSOP-36

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SANYO Semiconductor Co., Ltd.

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LV4901H

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VD	Externally applied voltage	14	V
Maximum output current	$I_{O \text{ peak}}$		3.5	A/ch
Allowable power dissipation	$P_d \text{ max}$	Independent package	886	mW
Operating temperature	T_{opr}		-25 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-50 to +150	$^\circ\text{C}$

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage range	VD	Externally applied voltage	10	12	13.5	V
Recommended load resistance	$R_L \text{ (SP)}$	Speaker load	4	8		Ω
	$R_L \text{ (HP)}$	Headphone		16		Ω

Electrical Characteristics at $T_a = 25^\circ\text{C}$

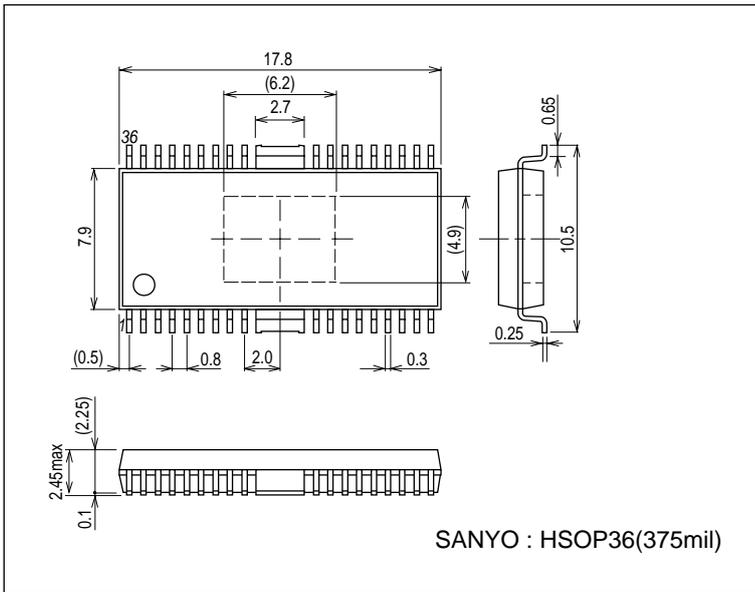
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Digital amplifier block : VD = 12V, $R_L = 8\Omega$, L = 22 μH , C = 0.33 μF , $C_L = 1\mu\text{F}$						
Standby current	I_{st}	$\overline{\text{STBY}} = \text{L}$, $\overline{\text{MUTE}} = \text{L}$		13	25	μA
Mute current	I_{mute}	$\overline{\text{STBY}} = \text{H}$, $\overline{\text{MUTE}} = \text{L}$		13	20	mA
Quiescent current	I_{CCO}	$\overline{\text{STBY}} = \text{H}$, $\overline{\text{MUTE}} = \text{H}$		60	70	mA
Voltage gain	VG	$f_{in} = 1\text{kHz}$, $V_O = 0\text{dBm}$	27	29	31	dB
Output offset voltage	V_{offset}	$R_g = 0$	-150		150	mV
Total harmonic distortion	THD@1W	$P_O = 1\text{W}$, $f_{in} = 1\text{kHz}$, AES17		0.2	0.8	%
Maximum output	$P_{O1@10\%}$	THD+N = 10%, AES17	8	10		W
Channel separation	CH sep.	$f_{in} = 1\text{kHz}$, $V_O = 0\text{dBm}$, $R_g = 0$, DIN AUDIO	55	70		dB
Ripple rejection ratio	SVRR	$f_r = 100\text{Hz}$, $V_r = 0\text{dBm}$, $R_g = 0$, A-weight	35	50		dB
Noise	V_{NO}	$R_g = 0$, A-weight		200	500	μVrms
High-level input voltage	V_{IH}	$\overline{\text{STBY}}$ pin and $\overline{\text{MUTE}}$ pin	3			V
Low-level input voltage	V_{IL}	$\overline{\text{STBY}}$ pin and $\overline{\text{MUTE}}$ pin			1	V
Power supply voltage drop protection circuit upper limit value	UV_UPPER	VD pin voltage monitor		8.0		V
Power supply voltage drop protection circuit lower limit value	UV_LOWER	VD pin voltage monitor		7.0		V
Headphone amplifier block : VD = 12V, $R_L = 16\Omega$, $f_{in} = 1\text{kHz}$						
Quiescent current	I_{CCO}^{hp}	$\overline{\text{HP_STBY}} = \text{H}$		5.5	9.5	mA
Voltage gain	VG	$V_O = -10\text{dBm}$	10	12	14	dB
Total harmonic distortion	THD	$P_O = 1\text{mW}$, DIN AUDIO		0.25	0.8	%
Maximum output	P_O	THD = 10%, DIN AUDIO	60	80		mW
Channel separation	CH sep.	$f_{in} = 1\text{kHz}$, $V_r = 0\text{dBm}$, $R_g = 0$, DIN AUDIO	35	45		dB
Ripple rejection ratio	SVRR	$f_r = 100\text{Hz}$, $V_r = 0\text{dBm}$, $R_g = 0$, DIN AUDIO	55	70		dB
High-level input voltage	V_{IH}	$\overline{\text{HP_STBY}}$ pin	3			V
Low-level input voltage	V_{IL}	$\overline{\text{HP_STBY}}$ pin			1	V
Noise	V_{NO}	$R_g = 0\Omega$, DIN AUDIO		50	200	μVrms

Note : The values of these characteristics were measured in the SANYO test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

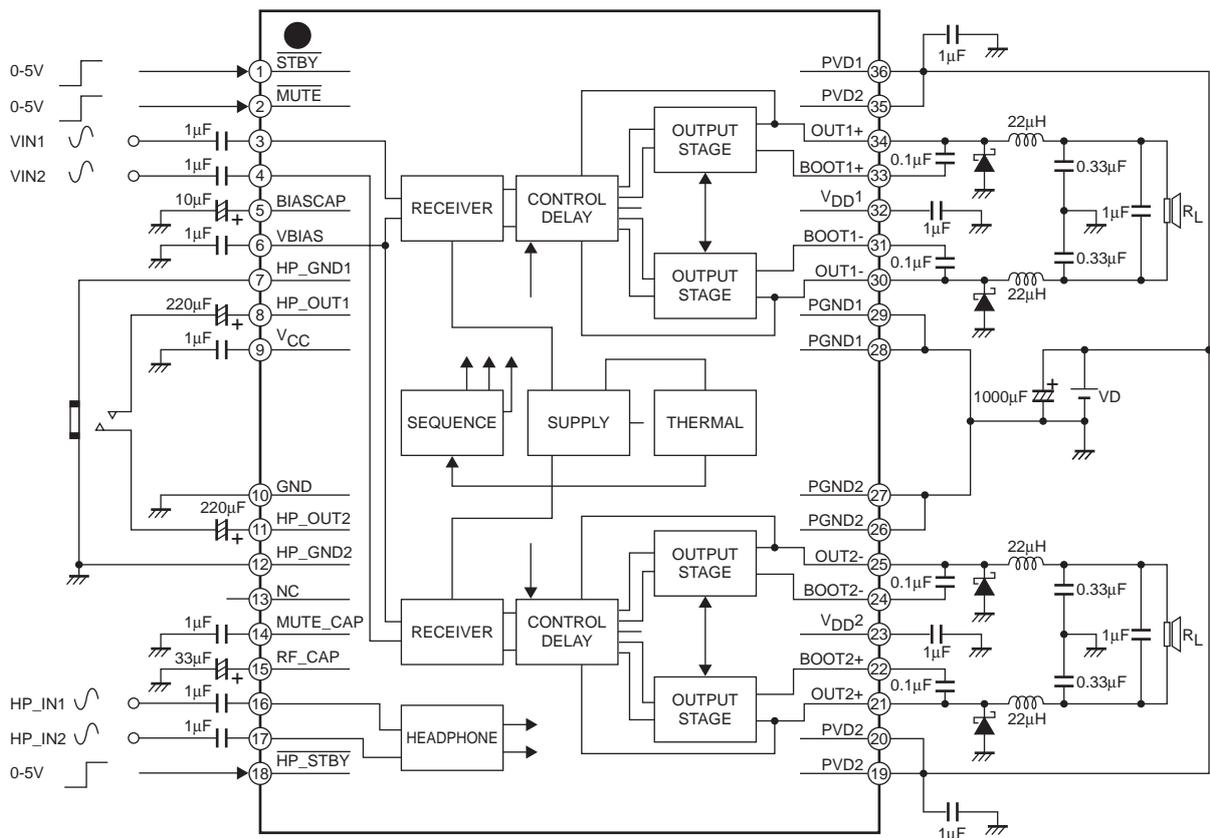
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Package Dimensions

unit : mm (typ)
3235A



Block Diagram ($R_L = 8\Omega$)



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Pin Equivalent Circuit

Pin No.	Pin name	I/O	Description	Equivalent Circuit
1	$\overline{\text{STBY}}$	I	Standby mode control	
2	$\overline{\text{MUTE}}$	I	Muting control	
3	$V_{\text{IN}1}$	I	Channel 1 input	
4	$V_{\text{IN}2}$	I	Channel 2 input	
5	BIASCAP	O	Internal regulator decoupling capacitor connection	

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Pin No.	Pin name	I/O	Description	Equivalent Circuit
6	VBIAS	O	Internal regulator decoupling capacitor connection	
7	HP_GND1		Headphone ground of channel 1	
8	HP_OUT1	O	Headphone channel 1 output	
9	VCC	O	Internal power supply decoupling capacitor connection	
10	GND		Analog system ground	
11	HP_OUT2	O	Headphone channel 2 output	
12	HP_GND2		Headphone ground of channel 2	
13	NC		NC	
14	MUTE_CAP	O	Muting system capacitor connection	

*VD2 : 9V line of Headphone Amp block

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Pin No.	Pin name	I/O	Description	Equivalent Circuit
15	RF_CAP	O	Headphone Ripple filter	
16	HP_IN1	I	Headphone channel 1 input	
17	HP_IN2	I	Headphone channel 2 input	
18	HP_STBY	I	Headphone standby mode control	
19	PVD2		Channel 2 power system power supply	
20	PVD2		Channel 2 power system power supply	
21	OUT2+	O	Channel 2 high side output	
22	BOOT2+	I/O	Boot strap terminal, Channe 2 positive supply of high side	

*PREVD : 6V line of Headphone Amp block

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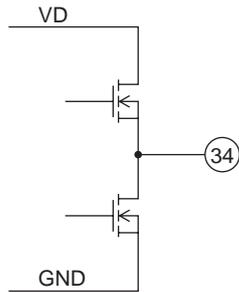
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Pin No.	Pin name	I/O	Description	Equivalent Circuit
23	V _{DD2}	O	Channel 2 internal regulator decoupling capacitor connection	
24	BOOT2-	I/O	Boot strap terminal, Channel 2 positive supply of high side	
25	OUT2-	O	Channel 2 low side output	
26	PGND2		Channel 2 power system ground	
27	PGND2		Channel 2 power system ground	
28	PGND1		Channel 1 power system ground	
29	PGND1		Channel 1 power system ground	
30	OUT1-	O	Channel 1 low side output	
31	BOOT1-	I/O	Boot strap terminal, Channel 1 positive supply of high side	
32	V _{DD1}	O	Channel 1 internal regulator decoupling capacitor connection	
33	BOOT1+	I/O	Boot strap terminal, Channel 1 positive supply of high side	

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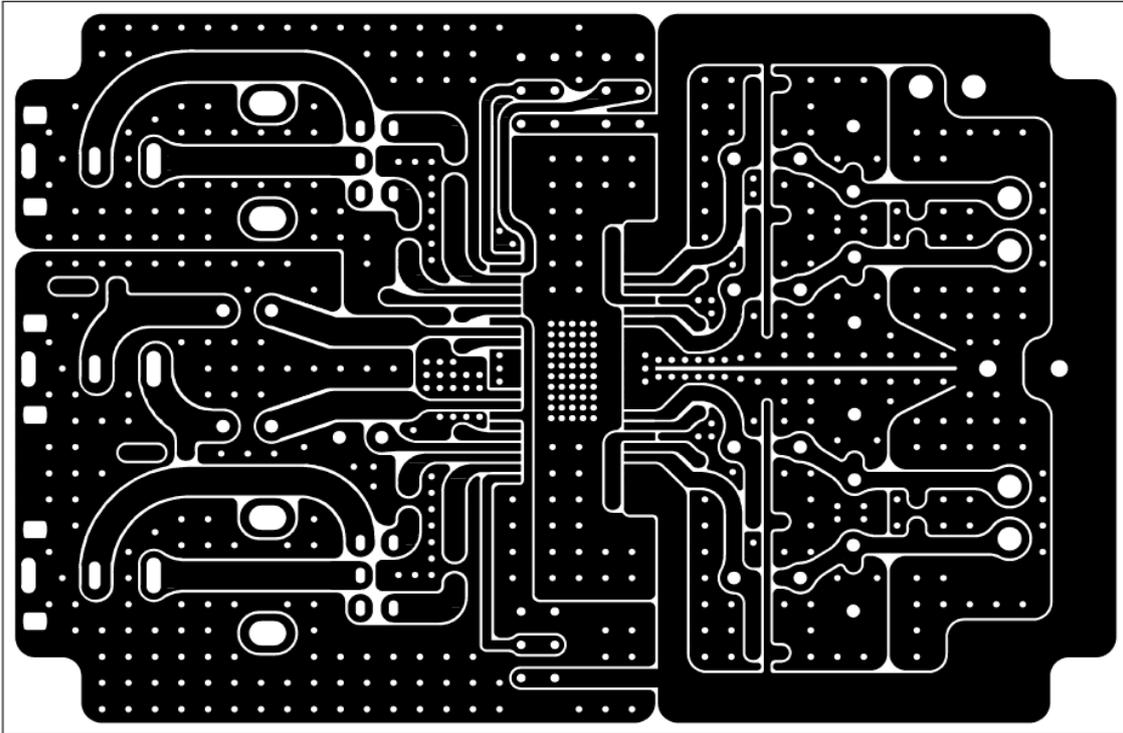
Pin No.	Pin name	I/O	Description	Equivalent Circuit
34	OUT1+	O	Channel 1 high side output	
35	PVD1		Channel 1 power system power supply	
36	PVD1		Channel 1 power system power supply	

Note : Smoothing capacitors must be connected to each power supply pin.

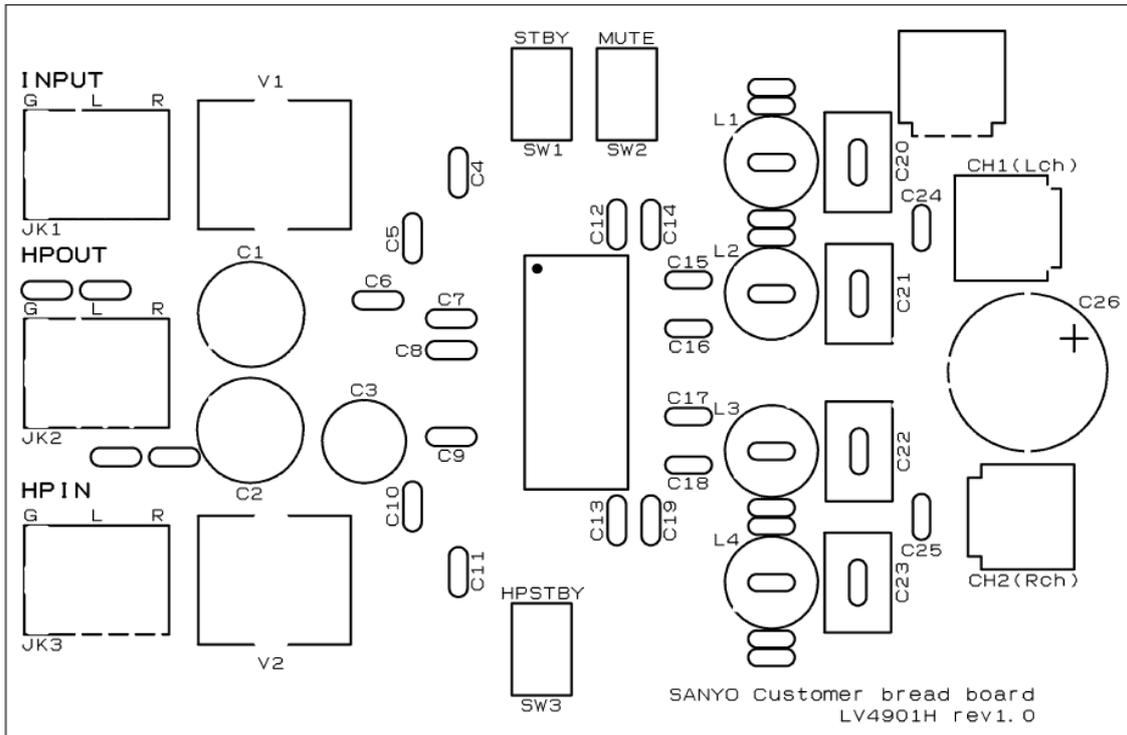
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LV4901H Customer bread board rev.1.0

Pattern



Silk



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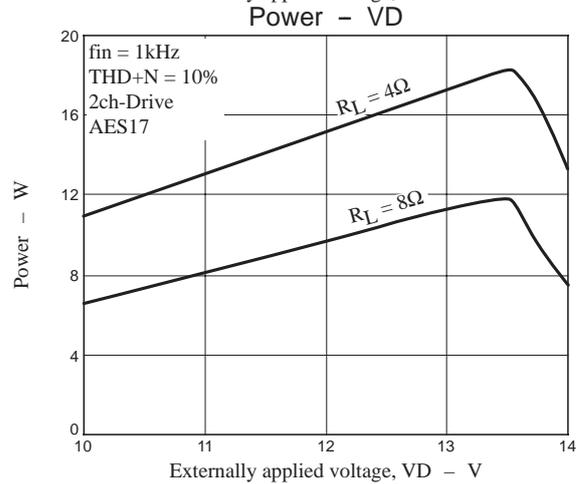
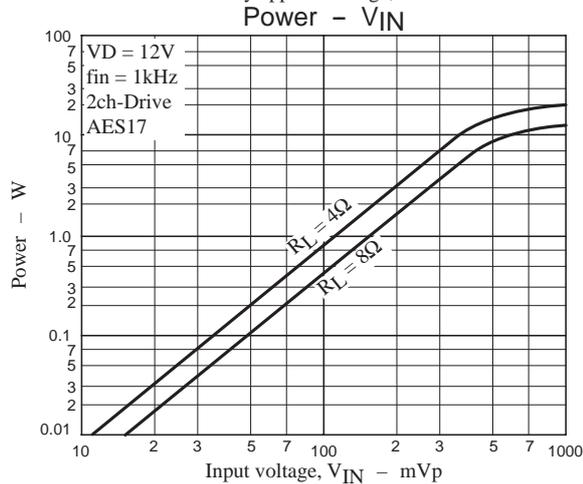
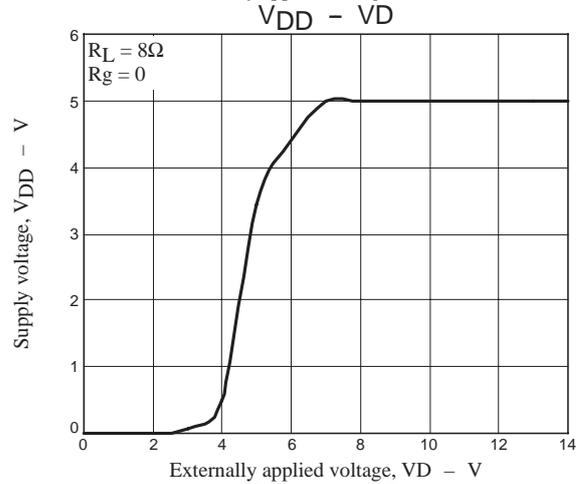
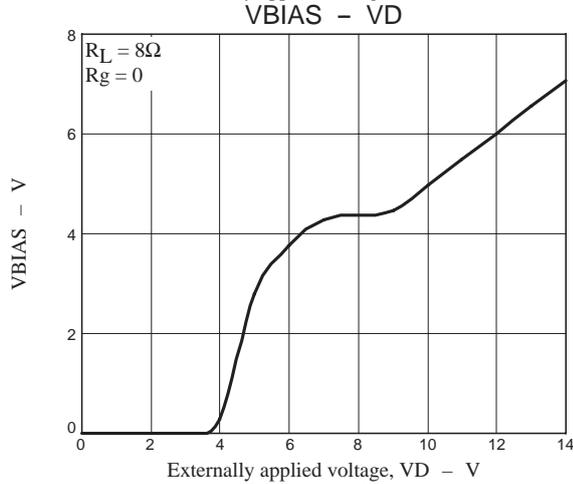
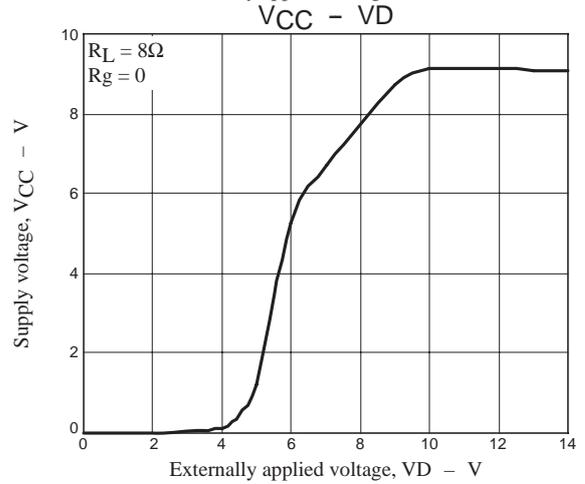
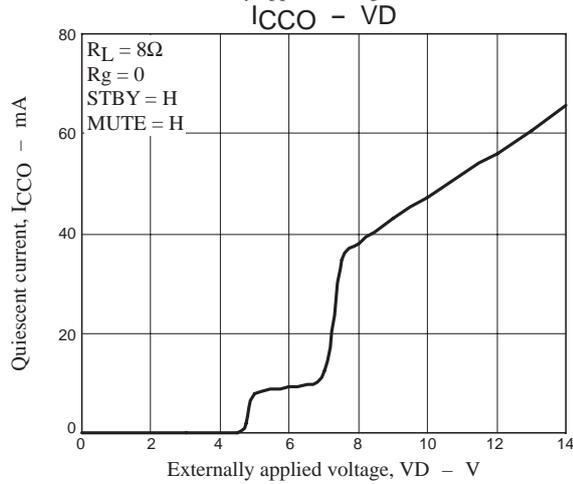
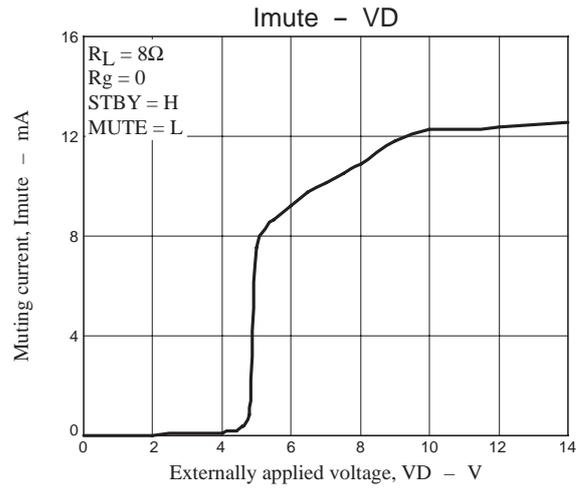
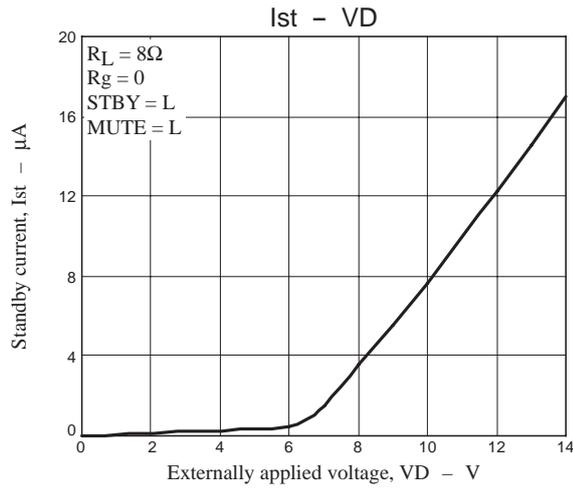
Components

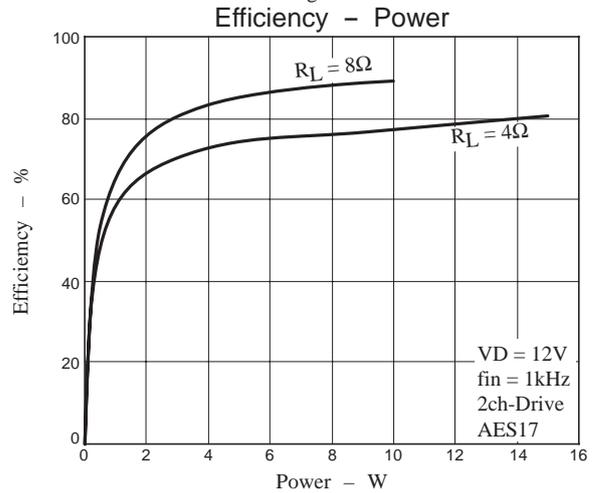
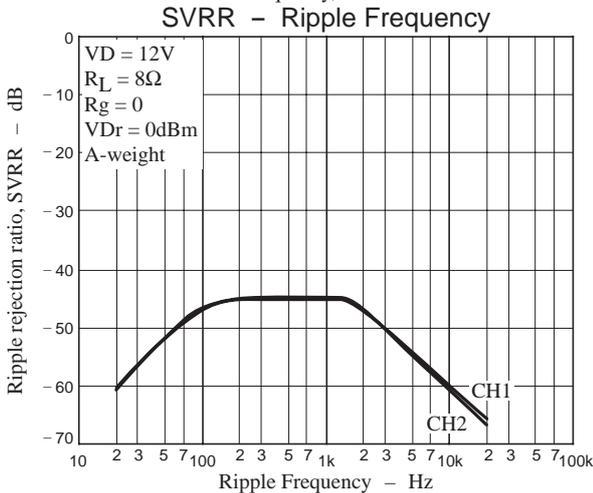
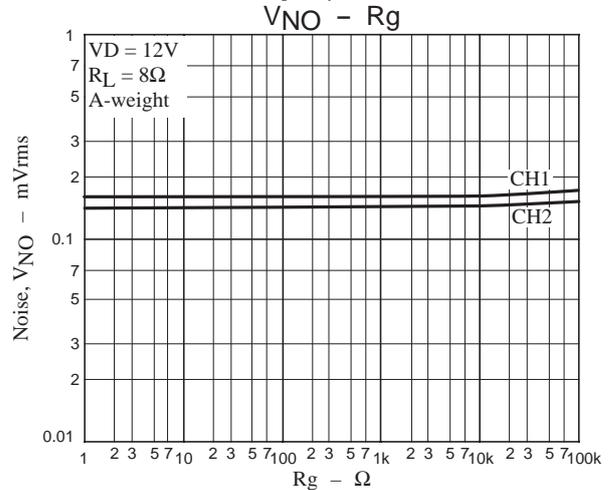
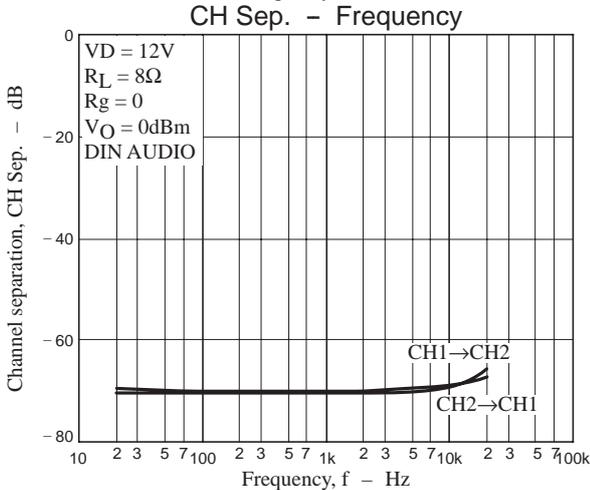
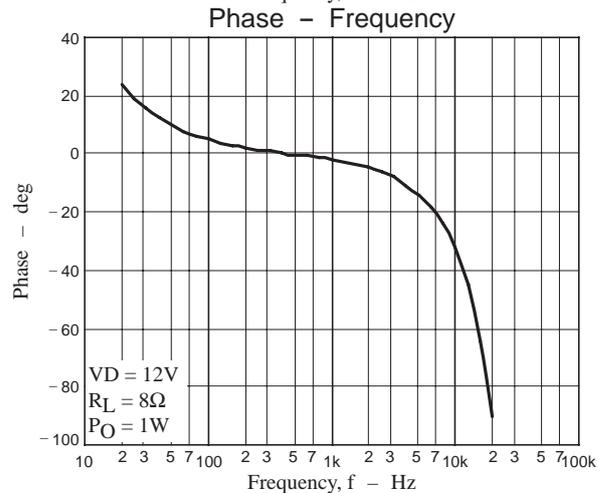
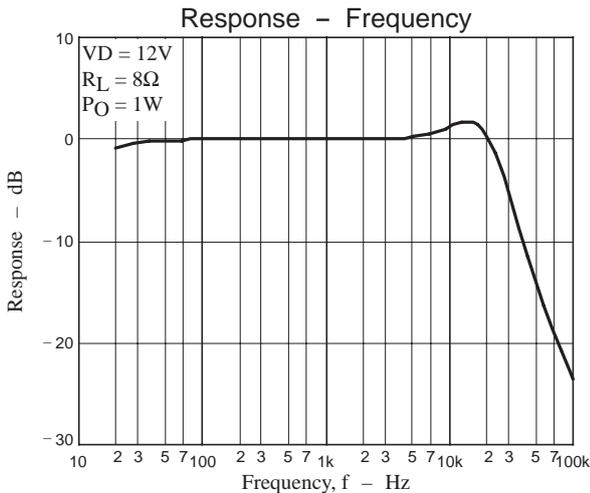
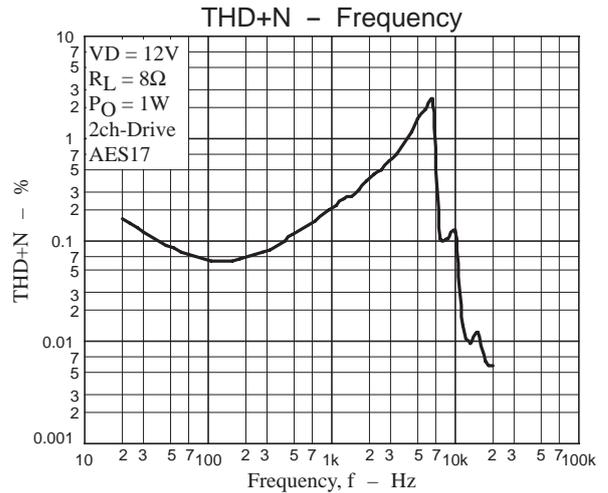
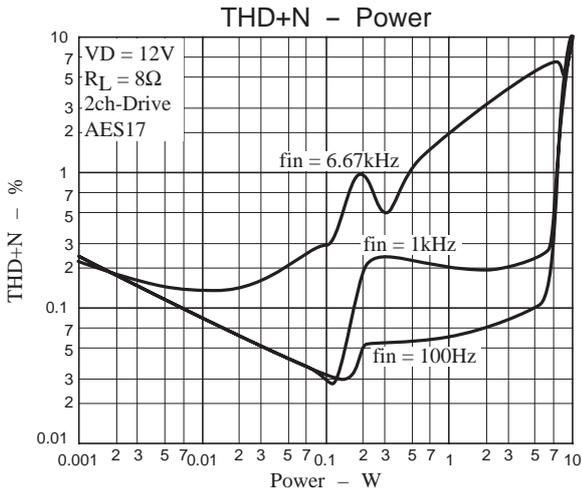
Symbol	Part No.	Function
-----	JK1	Jack for D-Amp input.
-----	JK2	Jack for HP output.
-----	JK3	Jack for HP input.
-----	SW1	STBY switch. Lower position : standby state.
-----	SW2	MUTE switch. Lower position : mute state.
-----	SW3	HP stanby switch. Lower position : standby state.
CHPO	C1, C2	HP output coupling capacitors.
CRFCAP	C3	HP_Mute capacitor for soft mute.
CIN	C4, C5, C10, C11	Input coupling capacitors.
CBIASCAP	C6	Internal regulator (VBIAS) input decoupling capacitor.
CVBIAS	C7	Internal regulator (VBIAS) output decoupling capacitor.
CVCC	C8	Internal regulator (VCC) output decoupling capacitor.
CMUTE	C9	Soft muting time constant adjustment capacitor.
* CVDD	C12, C13	internal regulator (VDD) output decoupling capacitors.
* CVD	C14, C15	VD high-frequency attenuation capacitors.
* CBOOT	C16, C17, C18, C19	Boot strap capacitors.
L	L1, L2, L3, L4	Output low-pass filter coils : $f_c = 1 / (2\pi\sqrt{LC})$
C	C20, C21, C22, C23	Output low-pass filter capacitors.
CL	C24, C25	Capacitor between outputs.
CPVD	C26	VD power supply capacitor.

* CVDD, CVD and CBOOT, Each capacitor is arranged in the neighborhood of IC as much as possible

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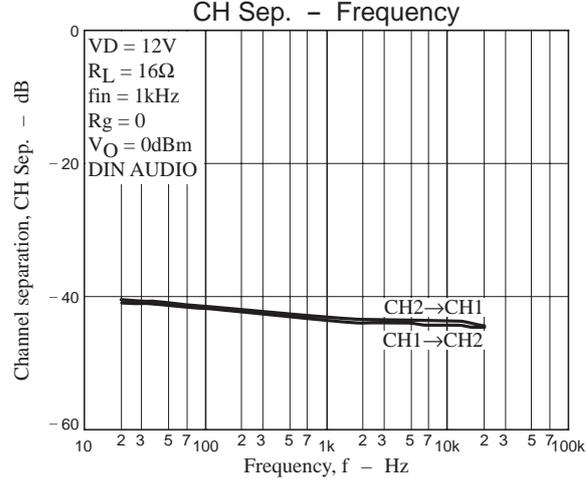
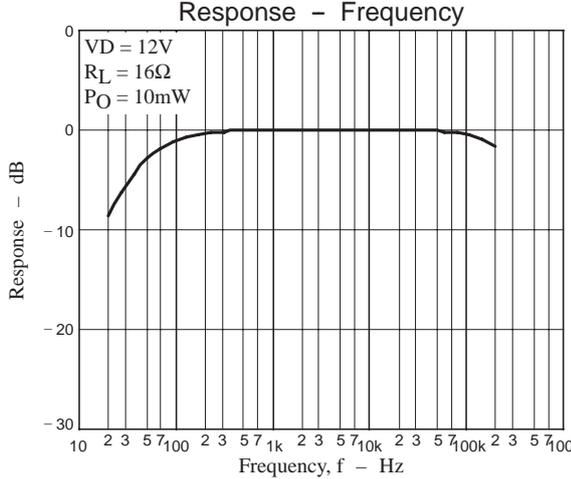
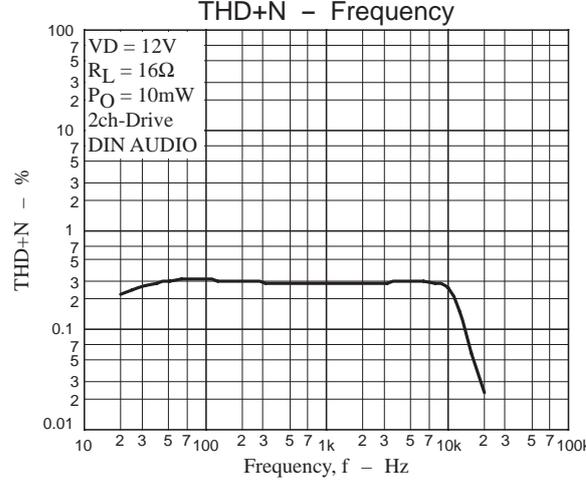
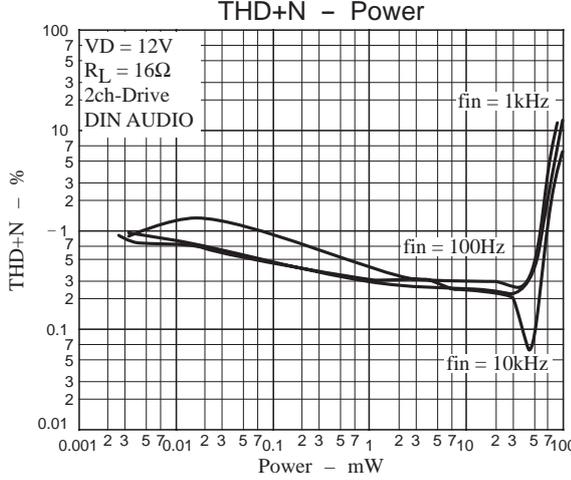
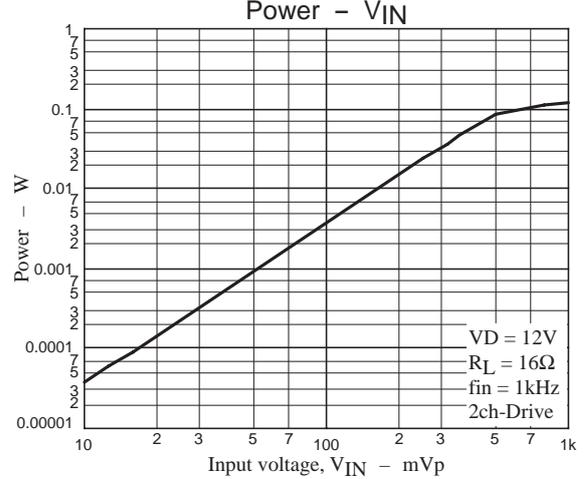
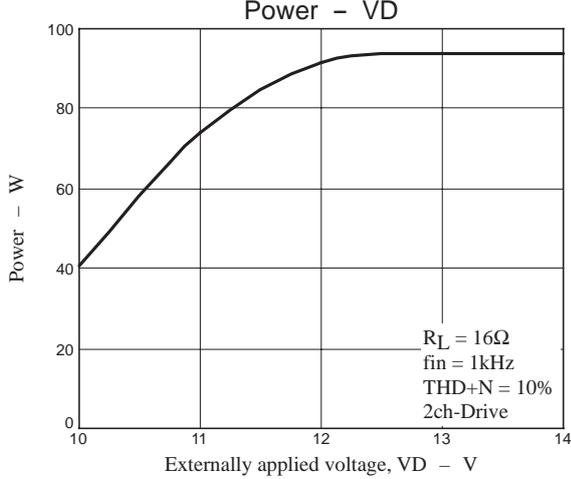
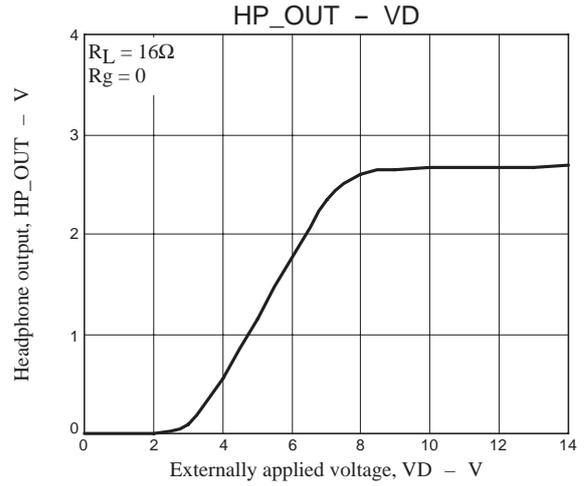
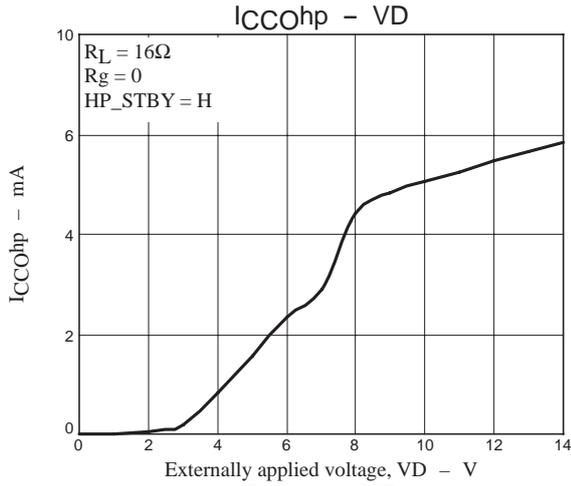
Digital amplifier block characteristics

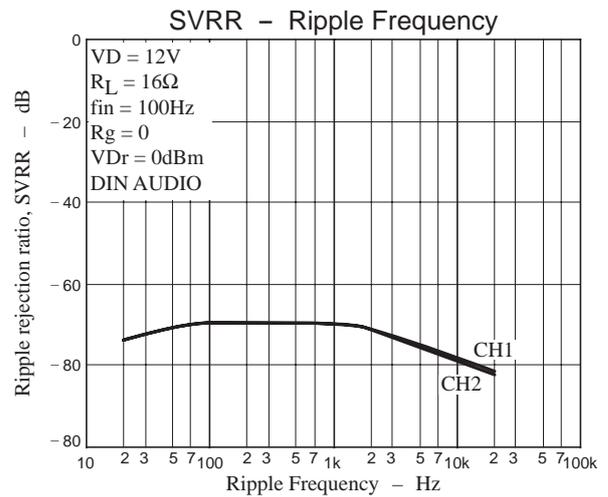
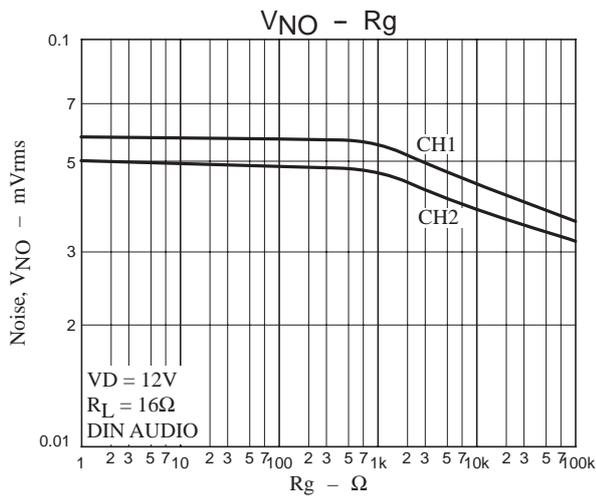




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Headphone amplifier block characteristics





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