



SANYO Semiconductors

DATA SHEET

LV49157V

Bi-CMOS LSI

**Class-D Audio Power Amplifier with built-in
Headphone Amplifier**

BTL 15W × 2ch

Overview

The LV49157V is a 15W per channel stereo digital power amplifier that takes analog inputs. The LV49157V uses unique SANYO-developed feedback technology to achieve excellent audio quality despite being a class D amplifier and can be used to implement high quality flat display panel (FDP) based systems.

Features

- BTL output, class D amplifier system
- Unique SANYO-developed feedback technology achieves superb audio quality
- High-efficiency class D amplifier
- Soft muting function reduces impulse noise at power on/off
- Full complement of built-in protection circuits : over current protection, thermal protection, and low power supply voltage protection circuits
- Built in Power limiter
- Built in Headphone Amplifier

Functions

- Power : 15W × 2ch output (VD = 15V, R_L = 8Ω, fin = 1kHz, AES17, THD + N = 10%)
- Efficiency : 93% (VD = 15V, R_L = 8Ω, fin = 1kHz, P_O = 15W)
- THD + N : 0.08% (VD = 15V, R_L = 8Ω, fin = 1kHz, P_O = 1W, Filter : AES17)
- Noise : 90μVrms (Filter : A-weight)
- 60mW Stereo headphone Amplifier (VD = 15V, R_L = 16Ω, THD + N = 10%)
- Package SSOP44J (275mil)

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Specifications

Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------------|--------|-------------------------|-------------|------|
| Maximum supply voltage | VD | Supply voltage | 20 | V |
| Allowable power dissipation | Pd max | Our PCB, Soldered * | 5 | W |
| Package thermal resistance | θjc | Our PCB, Soldered * | 2.1 | °C/W |
| | | Our PCB, Not soldered * | 3.6 | °C/W |
| Maximum junction temperature | Tj max | | 150 | °C |
| Operating temperature | Topr | | -25 to +75 | °C |
| Storage temperature | Tstg | | -50 to +150 | °C |

* : Mounted on a specified board 110.0mm x 100.0mm x 1.5mm, glass epoxy (two-layer)

Recommended Operating Range at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------|--------|----------------|---------|-----|-----|------|
| | | | min | typ | max | |
| Supply voltage range | VD | Supply voltage | 9 | 15 | 18 | V |
| Load impedance range | RL | Speaker load | 4 | 8 | | Ω |
| | RL(HP) | Headphone | | 16 | | Ω |

Electrical Characteristics at Ta = 25°C, VD = 15V

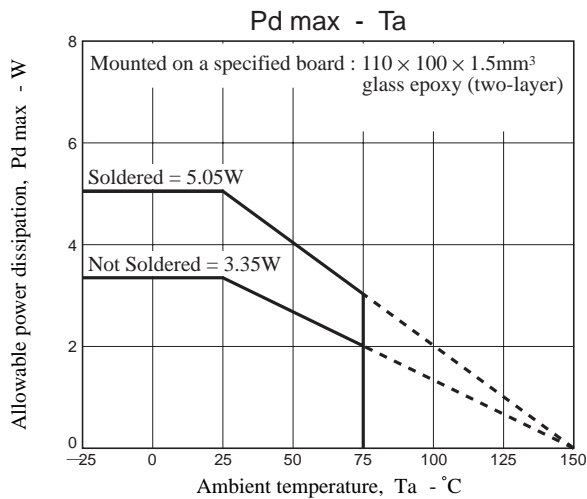
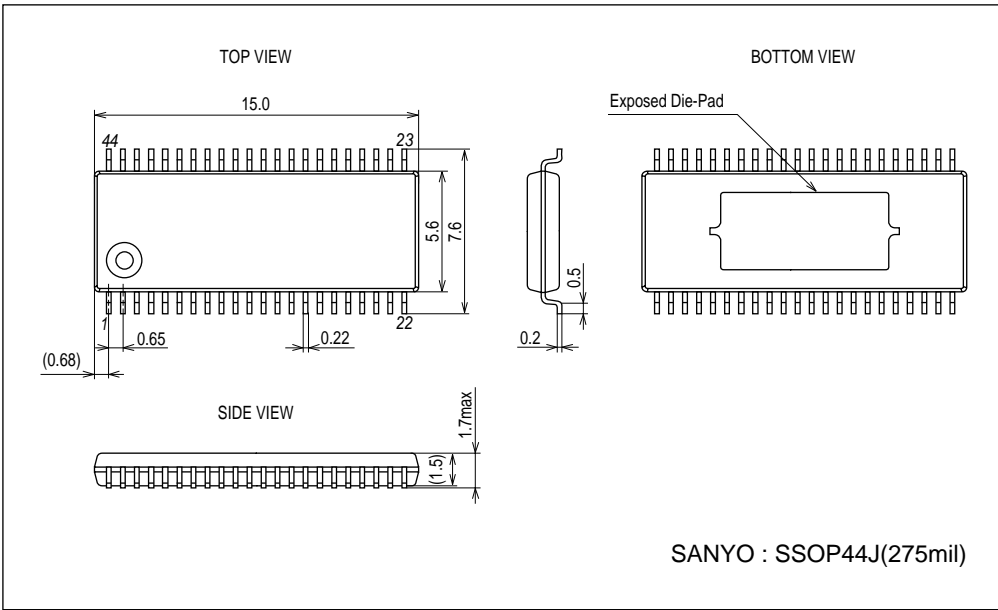
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|----------|--|---------|------|------|-------|
| | | | min | typ | max | |
| Main Amplifier (RL = 8Ω, L = 33μH (TOKO : A7502BY-330M), C = 0.1μF, CL=0.47μF) | | | | | | |
| Standby current | Ist | STBY = L, MUTE = L | | 1 | 10 | μA |
| Mute current | Imute | STBY = H, MUTE = L | 14 | 20 | 26 | mA |
| Quiescent current | ICCO | STBY = H, MUTE = H | 35 | 45 | 55 | mA |
| Voltage gain | VG | fin = 1kHz, VO = 0dBm | 28 | 30 | 32 | dB |
| Offset voltage | Voffset | Rg = 0 | -150 | | 150 | mV |
| Total harmonic distortion | THD+N | PO = 1W, fin = 1kHz, AES17 | | 0.08 | 0.4 | % |
| Output power | PO | THD+N = 10%, AES17 | 13 | 15 | | W |
| Channel separation | CH sep. | Rg = 0, VO = 0dBm, DIN AUDIO | 55 | 70 | | dB |
| Ripple rejection ratio | SVRR | fr = 100Hz, Vr = 0dBm, Rg = 0, DIN AUDIO | 50 | 60 | | dB |
| Noise | VNO | Rg = 0, A-weight | | 90 | 300 | μVrms |
| High-level input voltage | VIH | STBY and MUTE pin | 3 | | VD | V |
| Low-level input voltage | VIL | STBY and MUTE pin | 0 | | 1 | V |
| Under voltage protection UPPER | UV_UPPER | VD voltage measure | | 8.0 | | V |
| Under voltage protection LOWER | UV_LOWER | VD voltage measure | | 7.0 | | V |
| Headphone Amplifier (RL = 16Ω, fin=1kHz) | | | | | | |
| Quiescent current | ICCO | HP_STBY = H | | 8 | 12 | mA |
| Voltage gain | VG | VO = -10dBm | 9.5 | 11.5 | 13.5 | dB |
| Total harmonic distortion | THD+N | PO = 10mW, DIN AUDIO | | 0.05 | 0.3 | % |
| Output power | PO | THD+N = 10%, DIN AUDIO | 48 | 60 | 72 | W |
| Channel separation | CH sep. | fin=1kHz, Rg = 0, VO = -10dBm, DIN AUDIO | 55 | 70 | | dB |
| Ripple rejection ratio | SVRR | fr = 100Hz, Vr = 0dBm, Rg = 0, DIN AUDIO | 55 | 70 | | dB |
| Noise | VNO | Rg = 0, A-weight | | 12 | 60 | μVrms |
| High-level input voltage | VIH | HP_STBY pin | 3 | | VD | V |
| Low-level input voltage | VIL | HP_STBY pin | 0 | | 1 | V |

Note : The values of these characteristics were measured in the SANYO test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

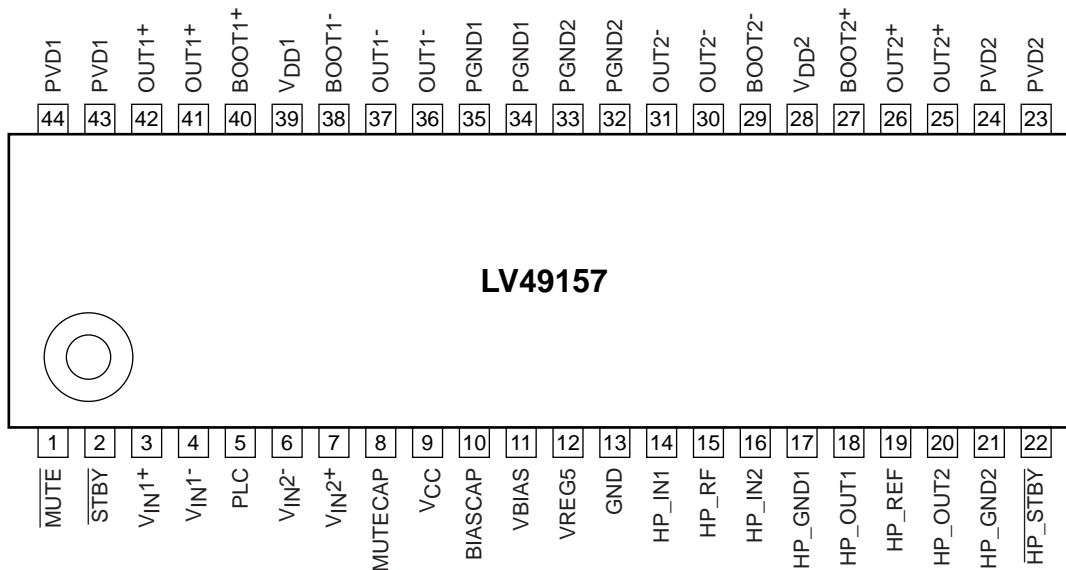
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Package Dimensions

unit : mm (typ)
3285



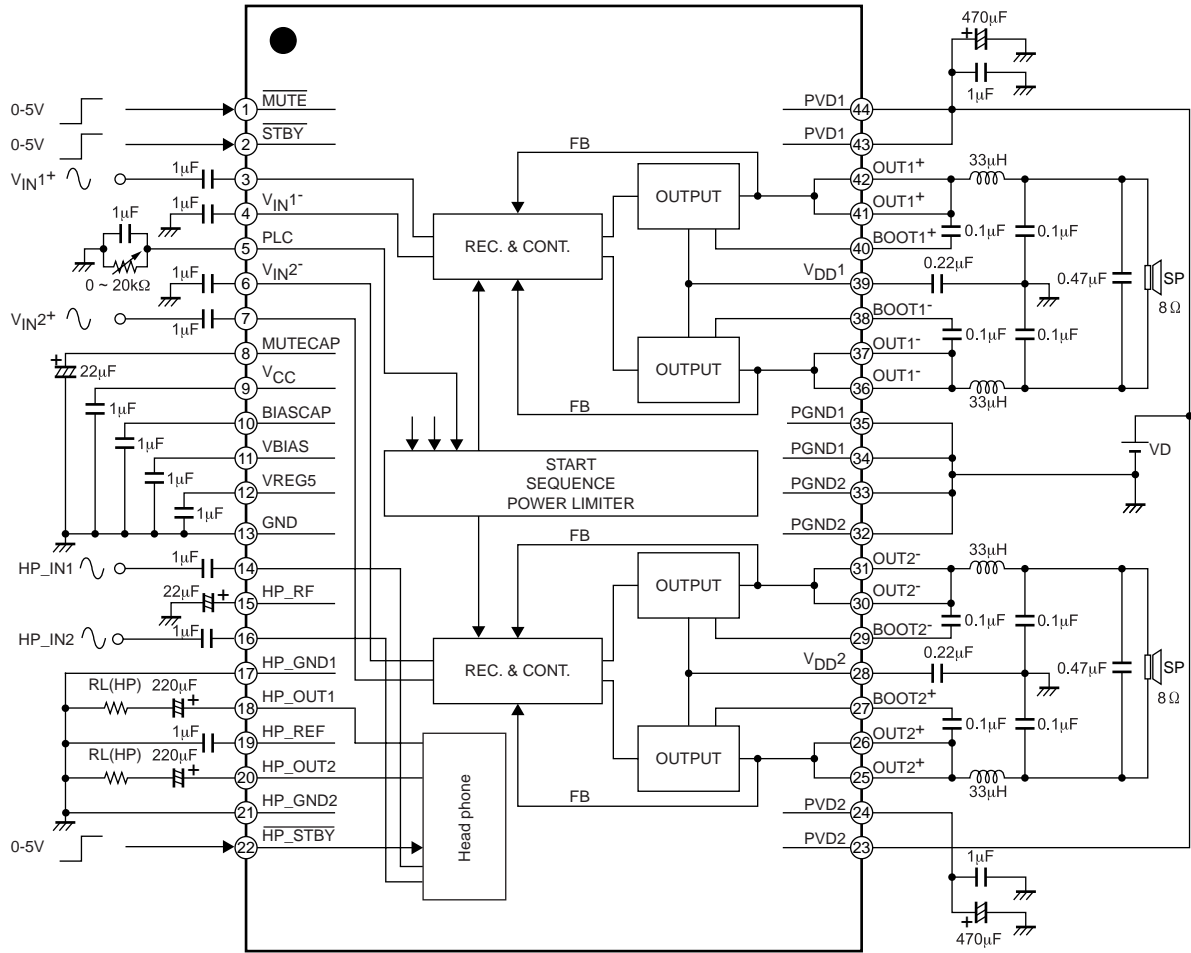
Pin Assignment



Top view

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Block Diagram and Application Circuit



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Pin Equivalent Circuit

| Pin No. | Pin name | I/O | Description | Equivalent Circuit |
|---------|-------------------------------|-----|-------------------------|--------------------|
| 1 | MUTE | I | Mute control pin | |
| 2 | STBY | I | Standby control pin | |
| 3 | V _{IN1} ⁺ | I | Input pin, CH1 plus | |
| 4 | V _{IN1} ⁻ | I | Input pin, CH1 minus | |
| 5 | PLC | I | Power level control pin | |

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| Pin No. | Pin name | I/O | Description | Equivalent Circuit |
|---------|-------------|-----|--|--------------------|
| 6 | V_{IN2^-} | I | Input pin, CH2 minus | |
| 7 | V_{IN2^+} | I | Input pin, CH2 plus | |
| 8 | MUTECAP | O | Muteing sysytem capcitor connection | |
| 9 | V_{CC} | O | Internal power supply decupling capacitor connection | |
| 10 | BIASCAP | O | Internal regulator decupling capacitor connection | |

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| Pin No. | Pin name | I/O | Description | Equivalent Circuit |
|---------|----------|-----|--|--------------------|
| 11 | VBIAS | O | Internal regulator decoupling capacitor connection | |
| 12 | VREG5 | O | Internal regulator decoupling capacitor connection | |
| 13 | GND | | Analog Ground | |
| 14 | HP_IN1 | I | Headphone CH1 input | |
| 15 | HP_RF | O | Internal regulator decoupling capacitor connection | |
| 16 | HP_IN2 | I | Headphone CH2 input | |

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Continued from preceding page.

| Pin No. | Pin name | I/O | Description | Equivalent Circuit |
|---------|----------|-----|--|--------------------|
| 17 | HP_GND1 | | Headphone Ground | |
| 18 | HP_OUT1 | O | Headphone CH1 output | |
| 19 | HP_REF | O | Internal regulator decoupling capacitor connection | |
| 20 | HP_OUT2 | O | Headphone CH2 output | |
| 21 | HP_GND2 | | Headphone Ground | |
| 22 | HP_STBY | I | Headphone Amplifier standby control pin | |
| 23 | PVD2 | | CH2 power supply | |
| 24 | PVD2 | | CH2 power supply | |
| 25 | OUT2+ | O | Output pin, CH2 plus | |

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Continued from preceding page.

| Pin No. | Pin name | I/O | Description | Equivalent Circuit |
|---------|------------------|-----|--|--------------------|
| 26 | OUT2+ | O | Output pin, CH2 plus | |
| 27 | BOOT2+ | I/O | Boot strap pin, CH2 plus | |
| 28 | V _{DD2} | O | CH2 internal regulator decoupling capacitor connection | |
| 29 | BOOT2- | I/O | Boot strap pin, CH2 minus | |
| 30 | OUT2- | O | Output pin, CH2 minus | |
| 31 | OUT2- | O | Output pin, CH2 minus | |
| 32 | PGND2 | | CH2 Power Ground | |
| 33 | PGND2 | | CH2 Power Ground | |
| 34 | PGND1 | | CH1 Power Ground | |
| 35 | PGND1 | | CH1 Power Ground | |
| 36 | OUT1- | O | Output pin, CH1 minus | |
| 37 | OUT1- | O | Output pin, CH1 minus | |
| 38 | BOOT1- | I/O | Boot strap pin, CH1 minus | |
| 39 | V _{DD1} | O | CH1 internal regulator decoupling capacitor connection | |
| 40 | BOOT1+ | I/O | Boot strap pin, CH1 plus | |

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Continued from preceding page.

| Pin No. | Pin name | I/O | Description | Equivalent Circuit |
|---------|----------|-----|----------------------|--------------------|
| 41 | OUT1+ | O | Output pin, CH1 plus | |
| 42 | OUT1+ | O | Output pin, CH1 plus | |
| 43 | PVD1 | | CH1 power supply | |
| 44 | PVD1 | | CH1 power supply | |

Operation Mode Summary

STBY mode ($\overline{\text{STBY}} = \text{L}$, $\overline{\text{MUTE}} = \text{L}$ and $\overline{\text{HP_STBY}} = \text{L}$)

Each bias becomes off state when the regulator in IC has been turned off.

The most of circuits becomes off state.

The supply current : 1 μA (typical).

MUTE mode ($\overline{\text{STBY}} = \text{H}$ and $\overline{\text{MUTE}} = \text{L}$)

Each bias becomes on state when the regulator in IC has been turned on.

When more than half of the circuits are active, the amplifier in the output stages become off.

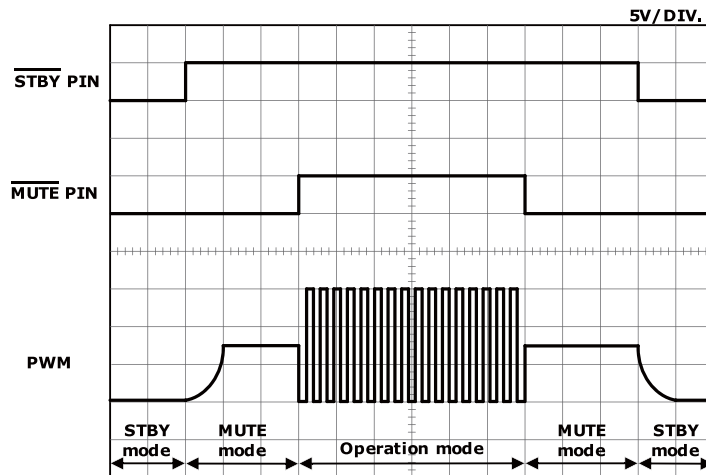
The supply current : 20mA (typical).

Operation mode ($\overline{\text{STBY}} = \text{H}$, $\overline{\text{MUTE}} = \text{H}$ and $\overline{\text{HP_STBY}} = \text{H}$)

The LV49157V operates as D-class amplifier and Headphone amplifier.

The output signal is synchronized with the input signal.

The current of the main amplifier is 45mA (typical) in our recommendation condition, and the current of the headphone amplifier is 8mA (typical) at $R_G=0$.



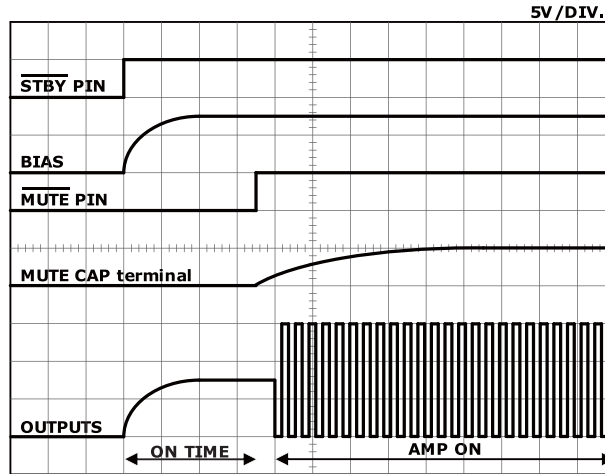
Main amplifier function image

ON TIME/OFF TIME

Secure and control ON TIME and OFF TIME about the control of the terminal $\overline{\text{STBY}}$ and the terminal $\overline{\text{MUTE}}$ for the Pop noise decrease. The following, ON TIME, and OFF TIME are the recommendation and set time in our recommendation constant.

ON TIME

Please secure ON TIME of 350msec or more for reducing Pop noise.

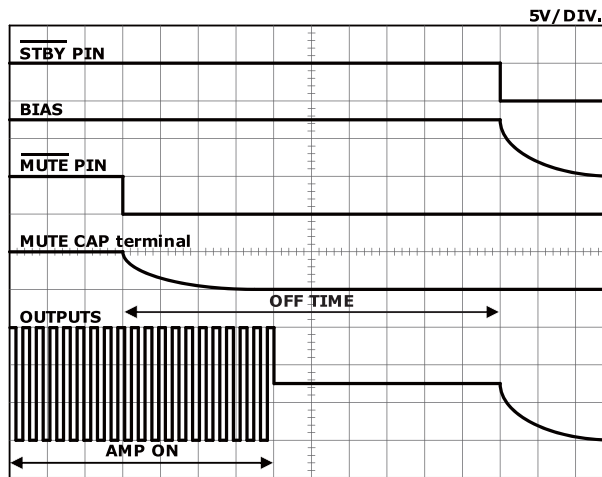


Function image

ON TIME ••• the time until the $\overline{\text{MUTE}}$ pin is set to high level after the $\overline{\text{STBY}}$ pin is set to high level

OFF TIME

Please secure OFF TIME of 1000msec or more for reducing Pop noise.



Function image

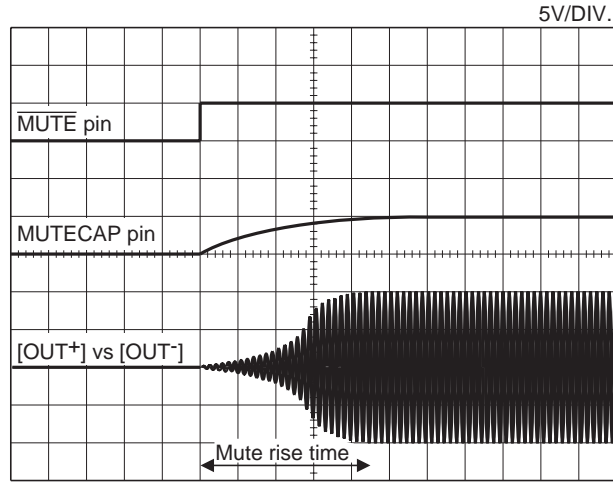
OFF TIME ••• the time until the $\overline{\text{STBY}}$ pin is set to low level after the $\overline{\text{MUTE}}$ pin is set to low level

SOFT MUTE

The soft mute circuit is able to use fade in/fade out function, and the main amplifier can set Rise time and fall time by the time constant of the MUTE_{CAP} capacitor.

Main amplifier FADE IN

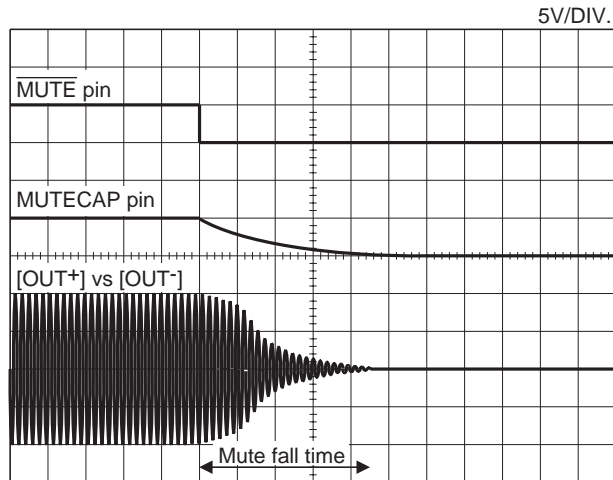
Mute rise time is Applpx.450msec in our recommended external components.



Main amplifier FADE IN function image

Main amplifier FADE OUT

Mute fall time is Applpx.450msec in our recommended external components.



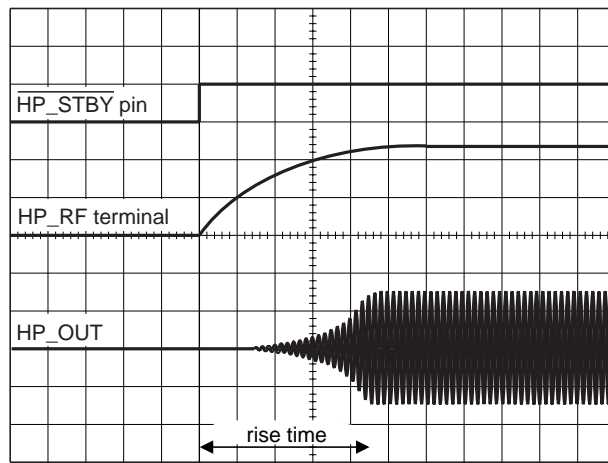
Main amplifier FADE OUT function image

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The headphone amplifier can set Rise time and fall time by the time constant of the $\overline{\text{HP_RF}}$ capacitor.

Headphone amplifier FADE IN

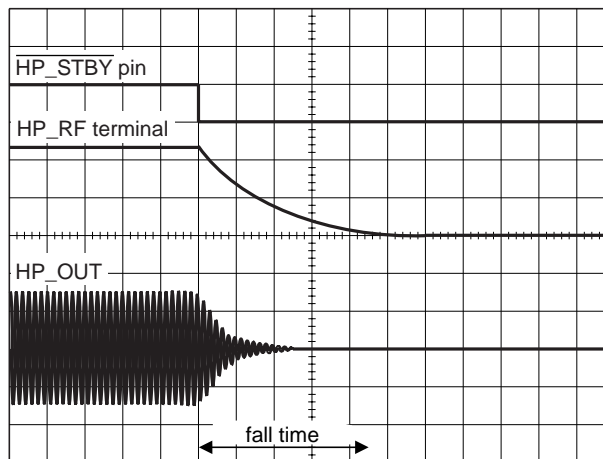
Rise time is Applpx.900msec in our recommended external components.



Headphone amplifier FADE IN function image

Headphone amplifier FADE OUT

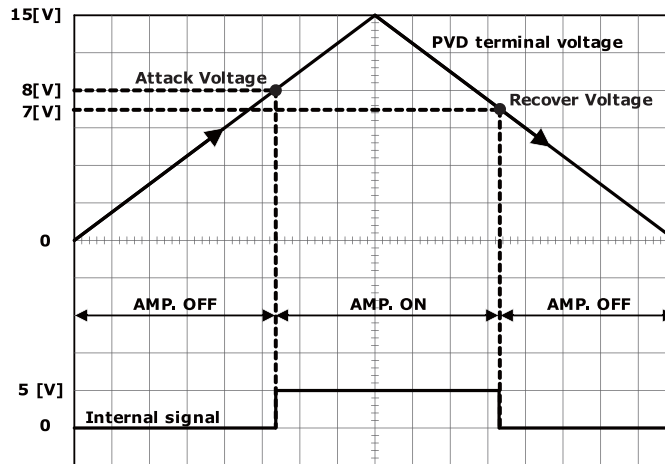
Fall time is Applpx.900msec in our recommended external components.



Headphone amplifier FADE OUT function image

Power supply lowering protection circuit

Since the instable operation in the low voltage is prevented by using this circuit, after the voltage of the PVD pin is monitored and the voltage below the Attack voltage (PVD = 8V typ.), AMP is turned off. Also, to prevent the instable operation when the voltage of the PVD pin is decreased by any cause during operations, the Attack voltage (PVD = 7V typ.) is set. The voltage of Attack and Recover has hysteresis (About 1V) to prevent ON/OFF continuous action of the power supply lowering protection circuit.

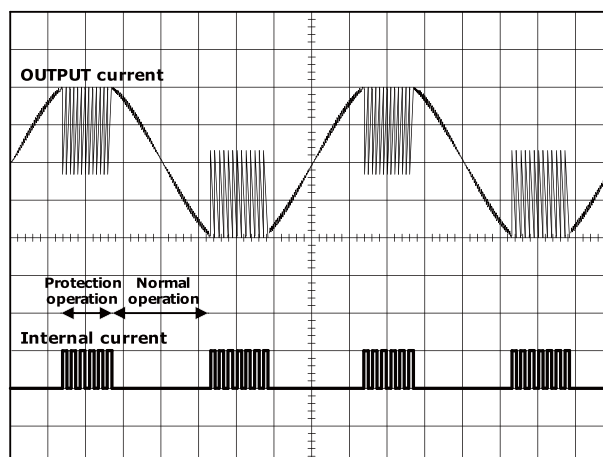


Function image

Also, this IC is designed to turn off AMP in the same sequence that the MUTE is on as a pop noise measures when the plug of products are put off.

Over current protection circuit

The over current protection circuit is a protection circuit * to protect the output DMOS from the over current and corresponds to any mode of the power supply, GND and a load short. The protection operation is performed when the current reaches the detection current value set out in IC and the output DMOS is compulsorily turned off for about 20μsec. After compulsorily tuning off the output DMOS, when the Amplifier is automatically reset in usual operation and the over current flows continuously, the protection operation is performed again.



Function image

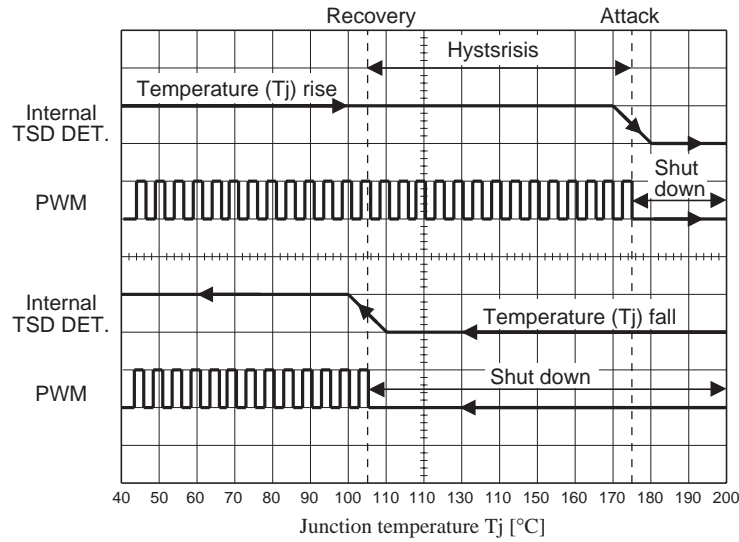
* The over current protection circuit is a function to avoid the abnormal state like the output short-circuit temporarily. Unfortunately, we cannot guarantee that IC is not destroyed.

Thermal protection circuit

The LV49157V includes a thermal protection circuit to prevent damage to or destruction of the IC should abnormal internal heat generation occur.

This means that should the IC junction temperature (T_j) rise above about 175°C due to inadequate heat dissipation or other reason, the thermal protection circuit will operate to stop IC operation should the temperature rise further.

If the temperature is reduced by lowering the input level or other means, the thermal protection circuit will recover automatically (about 105°C).



Function image

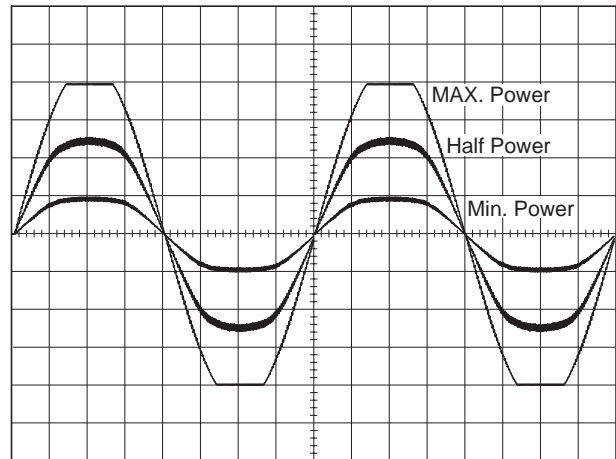
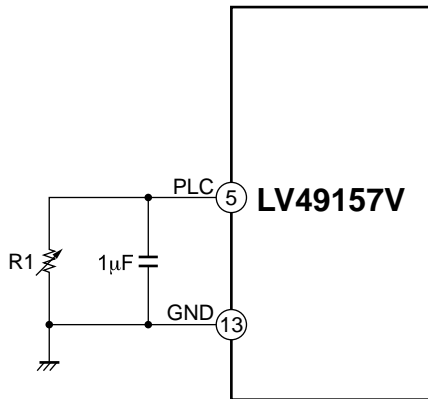
* The thermal protection circuit is a function to avoid the abnormal state temporarily. Unfortunately, we cannot guarantee that IC is not destroyed.

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PLC

The PLC (power level control) function is able to control the maximum index modulation by setting a value of external PLC resistance R1 voluntarily, and prevent a PWM signal from becoming the over modulation mode. In addition, this circuit can be used as an output power limit circuit because the PLC function can set the maximum index modulation voluntarily, and variable from 2W to 15W with output power linearly in the state that made the power supply voltage and load resistance fixation. Because the PLC function can set the suitable rated output with the same power supply voltage/speaker regardless of screen size in flat screen televisions by this, set can plan the commonization of the board.

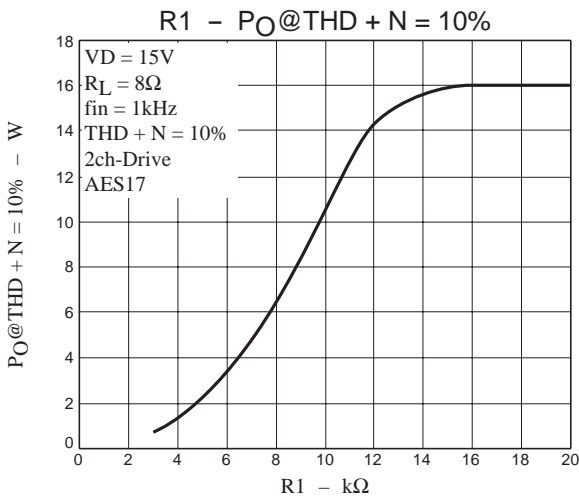
Furthermore, The PLC function can reduce abnormal noise in the hard clip so that output wave pattern becomes the soft clip when it limited output power.



Function image

Measuring condition

VD = 15V, R_L = 8Ω, L = 33μH (TOKO : A7502BY-330M), C = 0.1μF, C_L = 0.47μF, T_a = 25°C

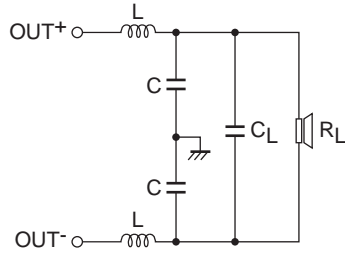


| R1 [kΩ] | Po@10% [W] |
|---------|------------|
| 3.0 | 0.694 |
| 3.6 | 1.073 |
| 4.7 | 1.982 |
| 6.2 | 3.642 |
| 7.5 | 5.562 |
| 8.2 | 6.855 |
| 9.1 | 8.591 |
| 10 | 10.64 |
| 13 | 15.32 |
| 15 | 15.94 |
| 20 | 16.01 |

Setting example of the output power limit value

- * When it is used this function as output power limit, please use the high-precision resistance such as the metal film resistor when precision of the electricity value is necessary.
- * The value of external PLC resistance R1 please connects more than 3kΩ.
- * When it is changed a value of external PLC resistance R1, please turn off an amplifier.

Cut-off frequency calculation method and the output LC filter setting



The cut off frequency f_c of the output LC filter is calculated by the following formula.

$$f_c = \frac{1}{2\pi\sqrt{2LC_L}}$$

Also, by setting the cut off frequency f_c , the value of C_L and L is calculated by using the following formula.

$$C_L = \frac{1}{2\sqrt{2} \times \pi R_L f_c}$$

$$L = \frac{\sqrt{2} \times R_L}{4\pi f_c}$$

In general, the value from 20% to 30% of C_L is set to C .

In case of $f_c = 30\text{kHz}$

| R_L [Ω] | L [μH] | C_L [μF] | C [μF] | Q |
|--------------------|-----------------------|-------------------------|-----------------------|-------|
| 4 | 15 | 1 | 0.22 | 0.650 |
| 6 | 22 | 0.68 | 0.15 | 0.636 |
| 8 | 33 | 0.47 | 0.1 | 0.704 |
| 16 | 68 | 0.22 | 0.047 | 0.739 |

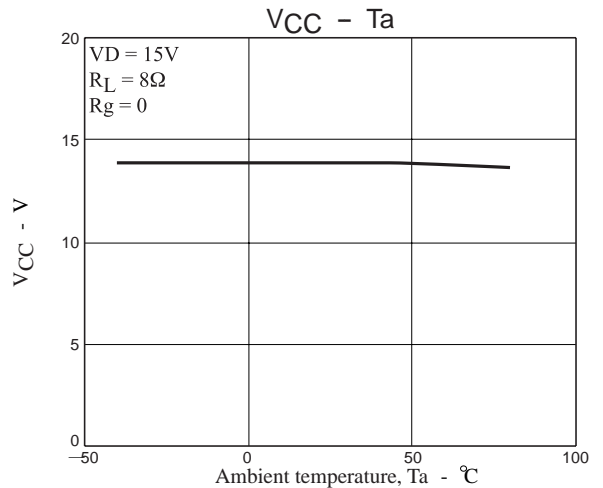
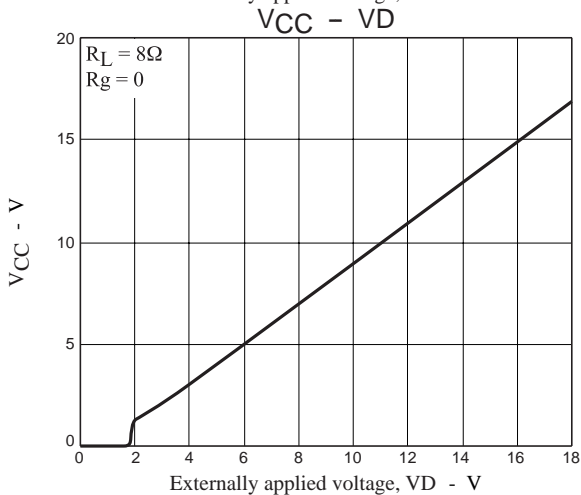
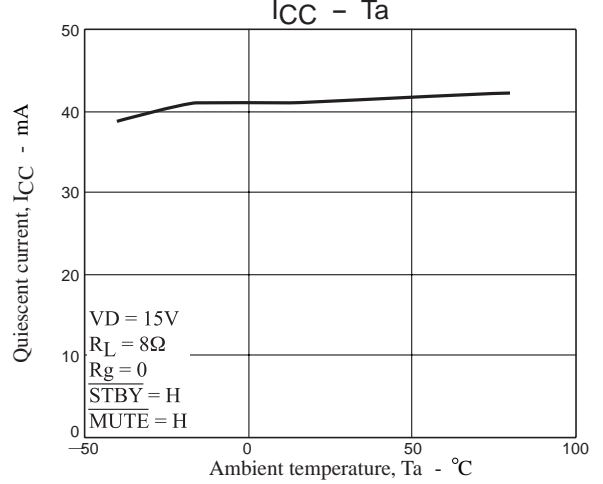
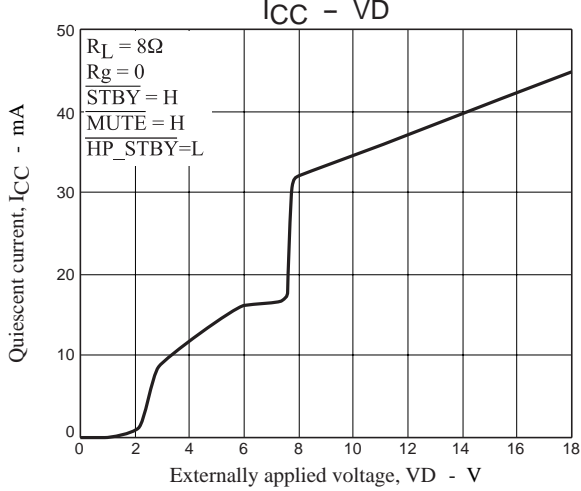
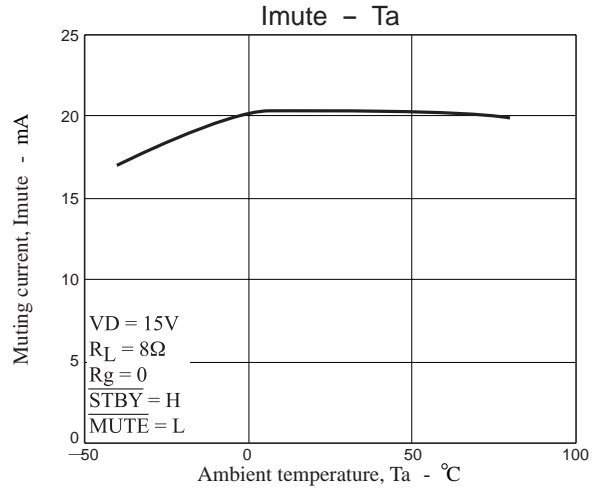
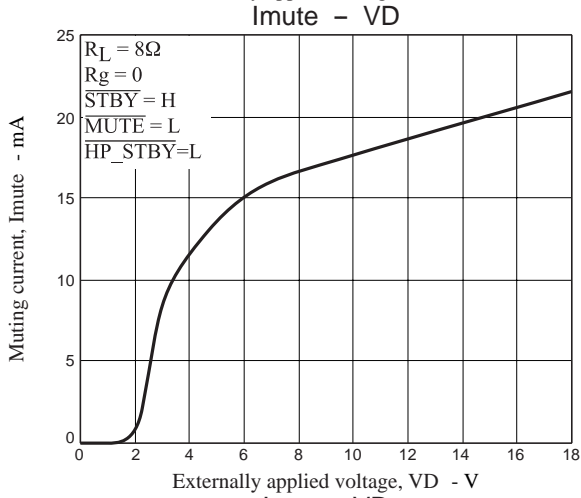
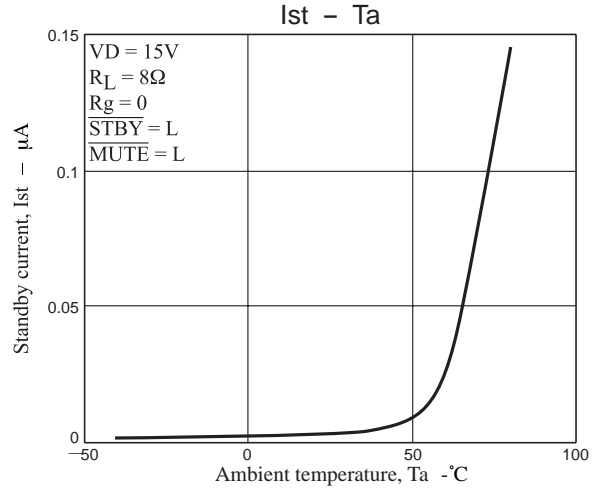
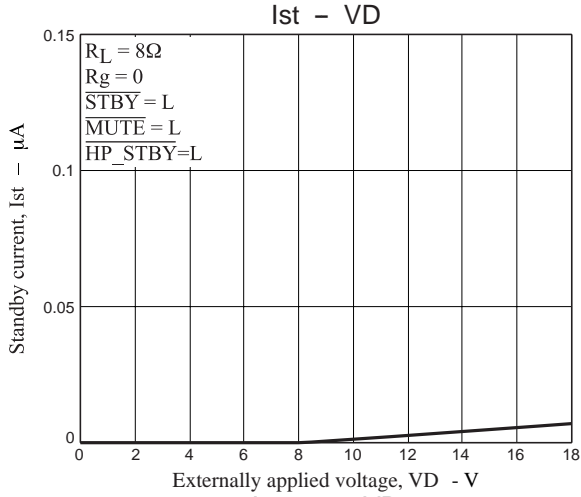
Above formula is common calculation method and is a measure of constant setting.

In fact, it is necessary to set with each set that considers the speaker characteristics.

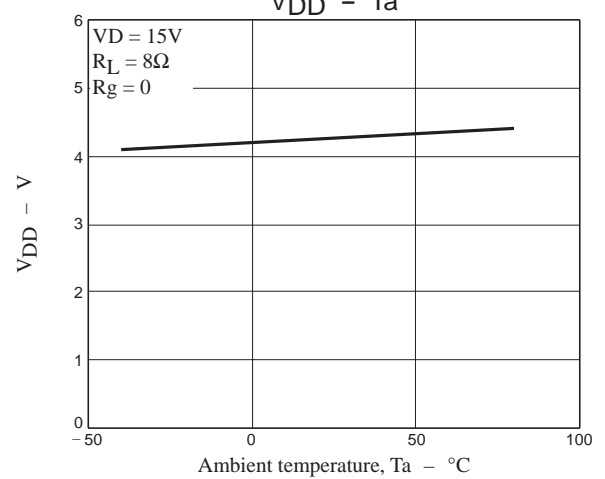
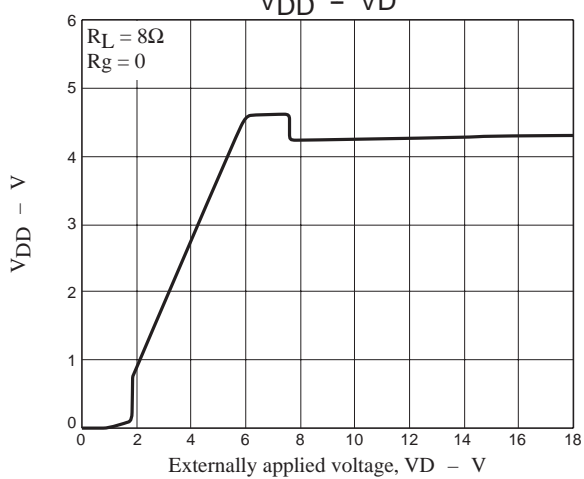
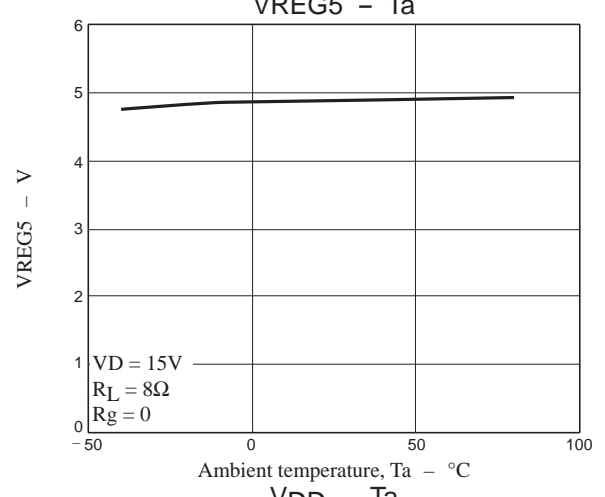
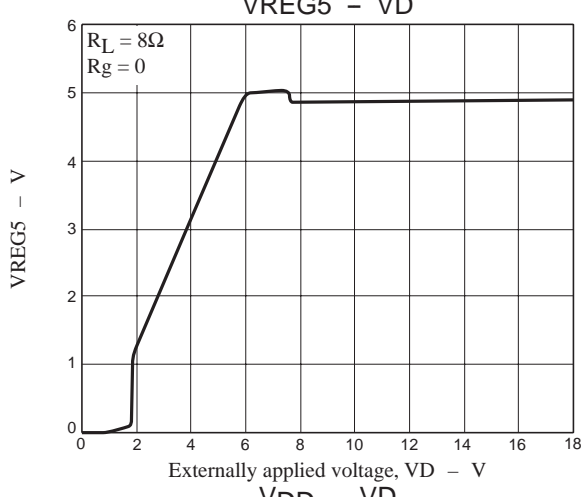
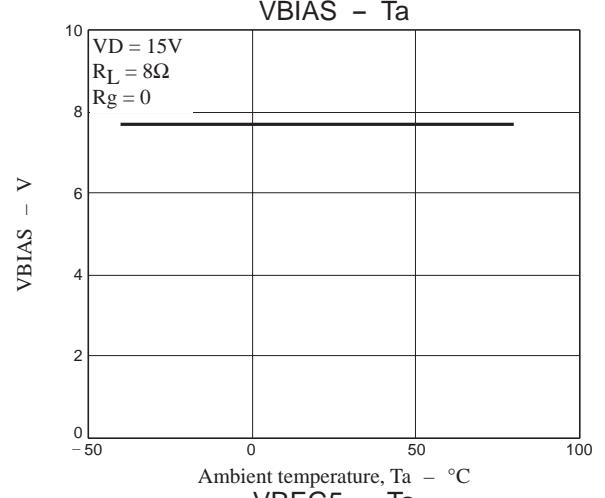
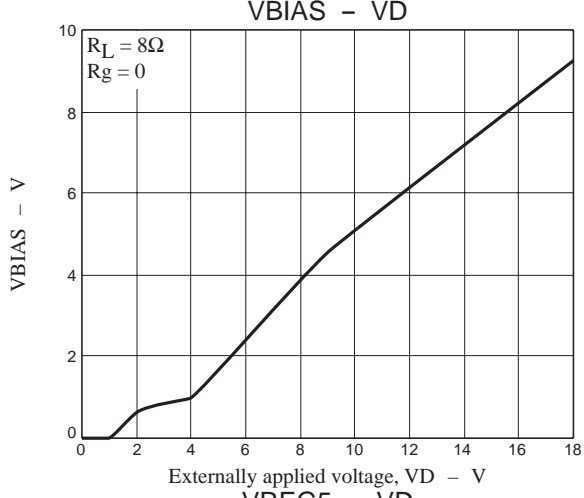
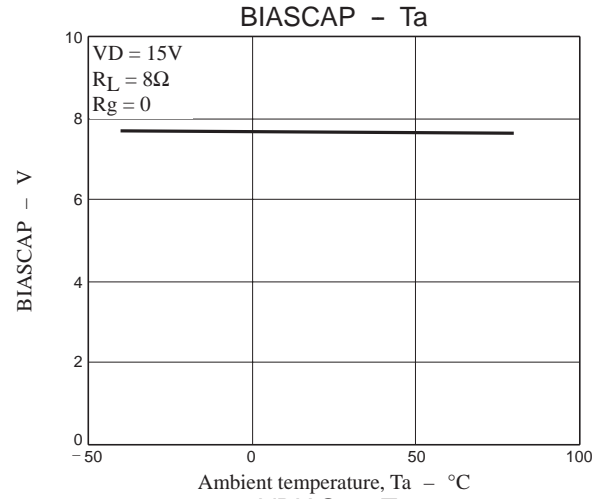
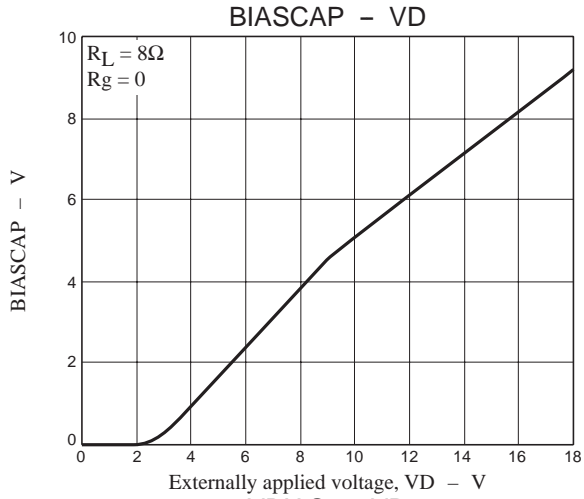
In addition, please set the fixed number to become $Q \leq 1$ in currents in the f_c neighborhood increasing if Q value of the LC filter is big.

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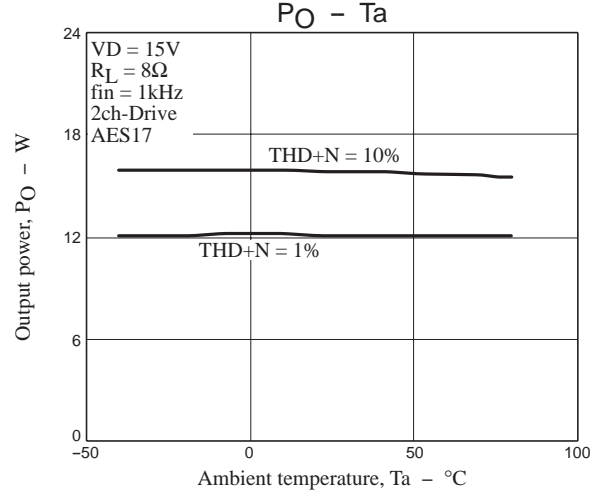
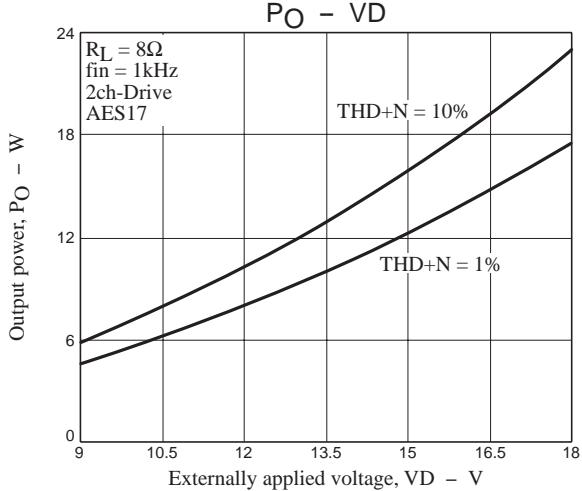
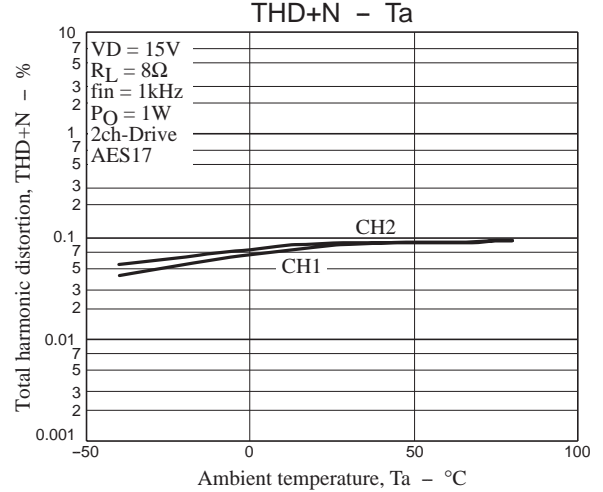
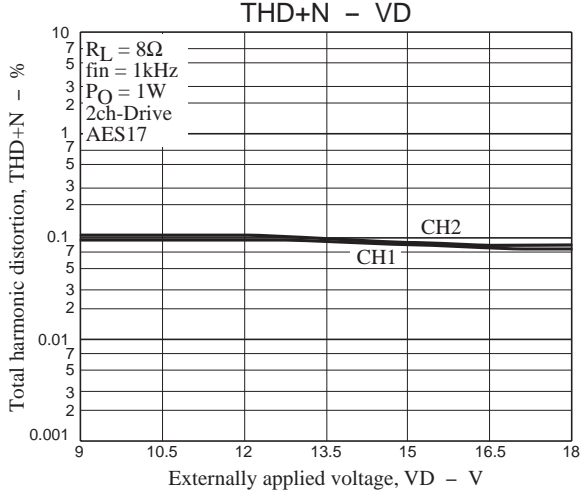
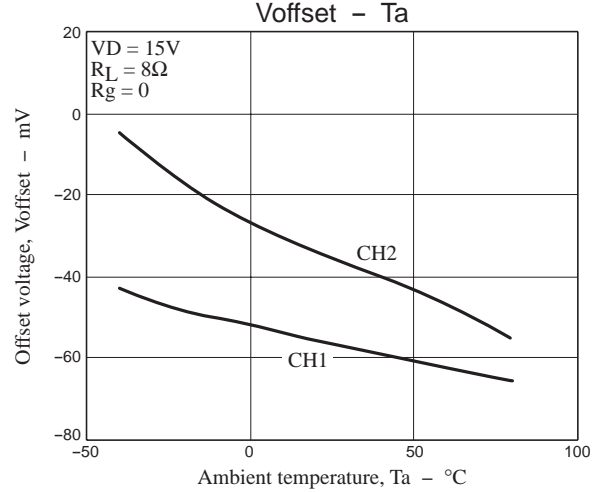
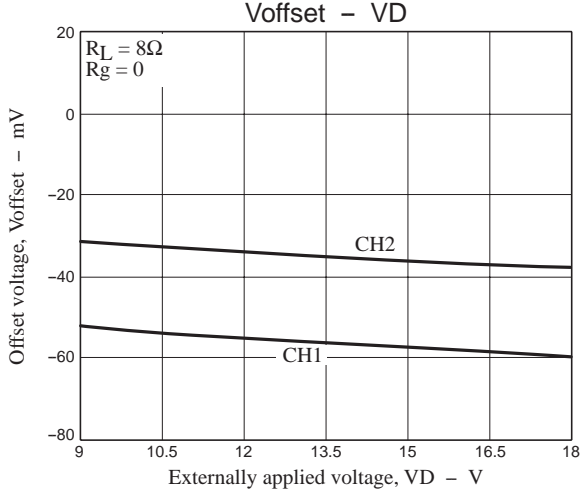
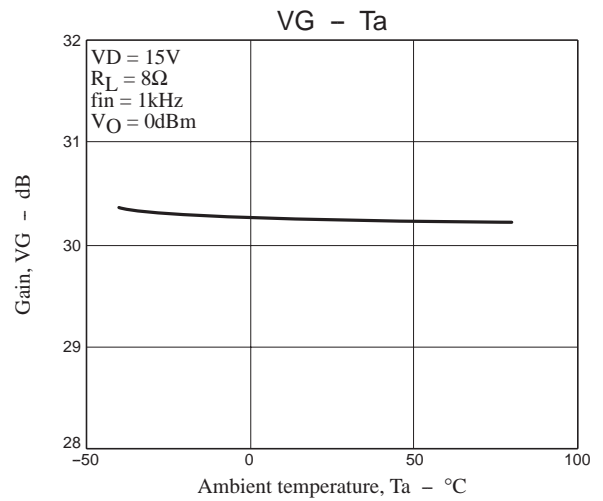
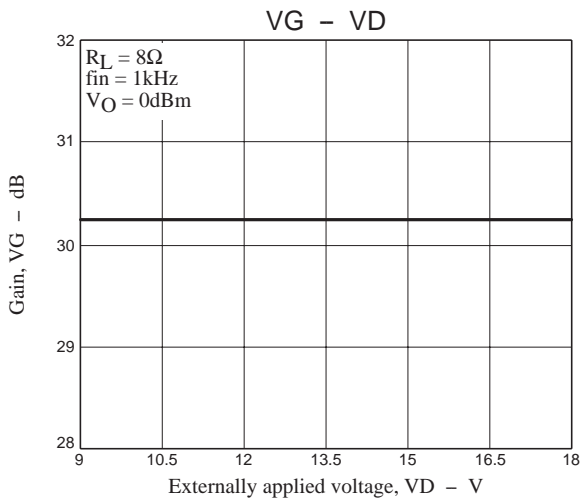
Graph deta (Digital Amplifier: $L = 33\mu\text{H}$ (TOKO : A7502BY-330M), $C = 0.1\mu\text{F}$, $C_L = 0.47\mu\text{F}$)



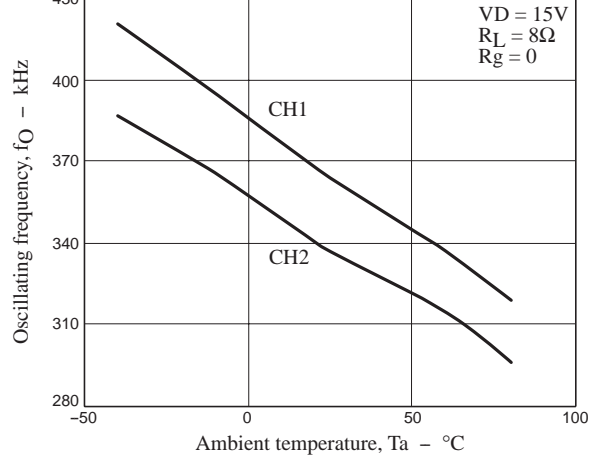
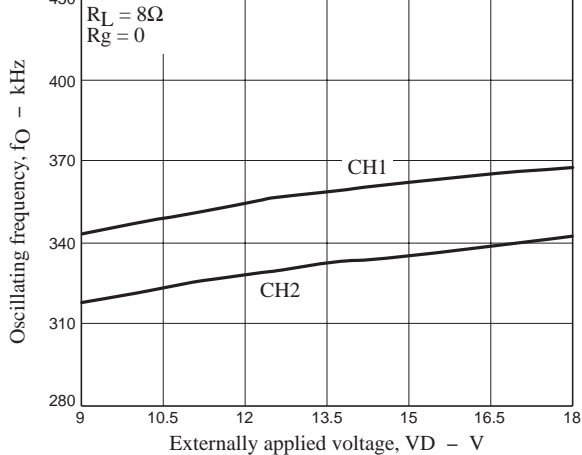
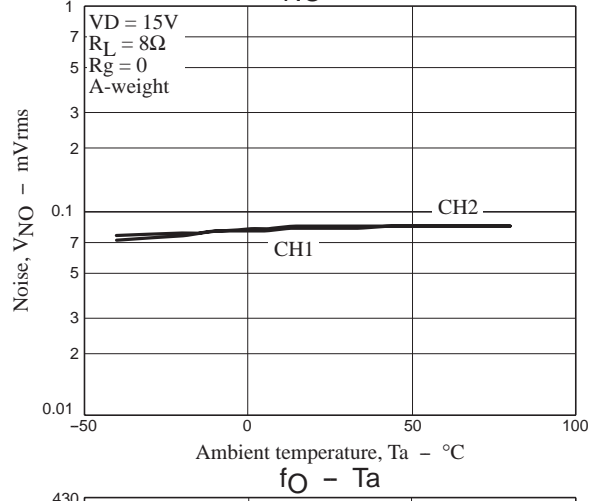
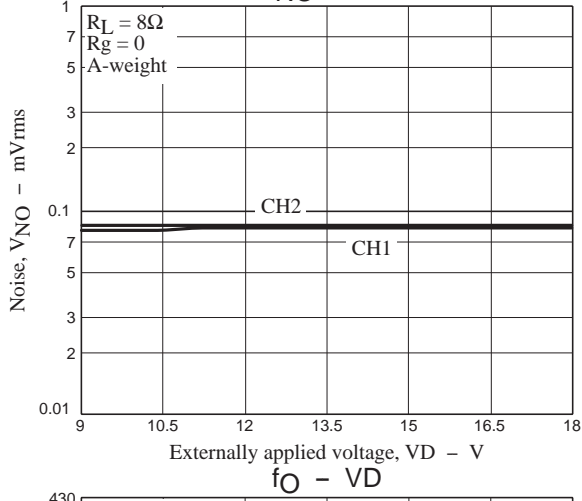
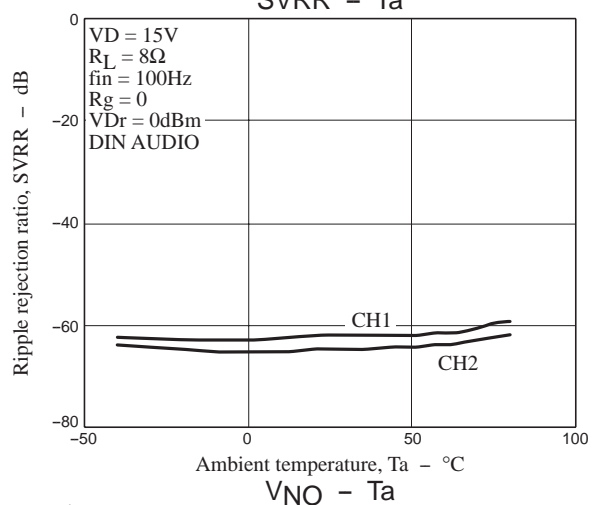
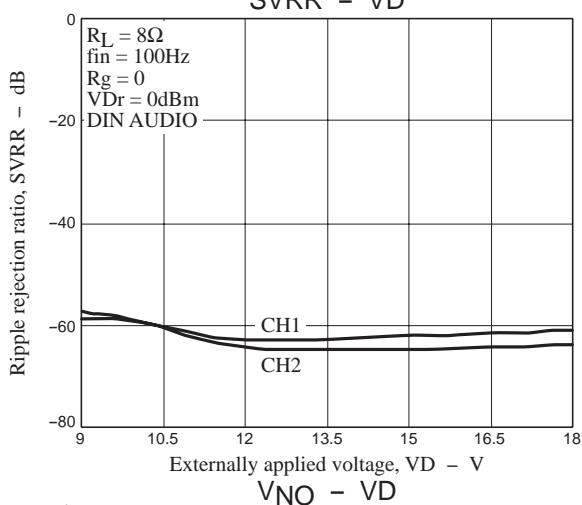
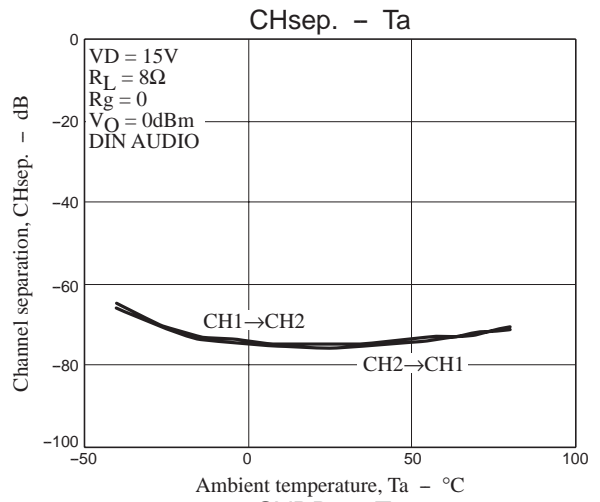
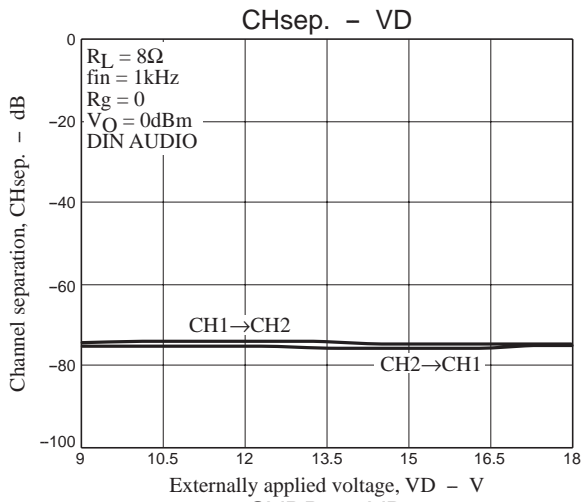
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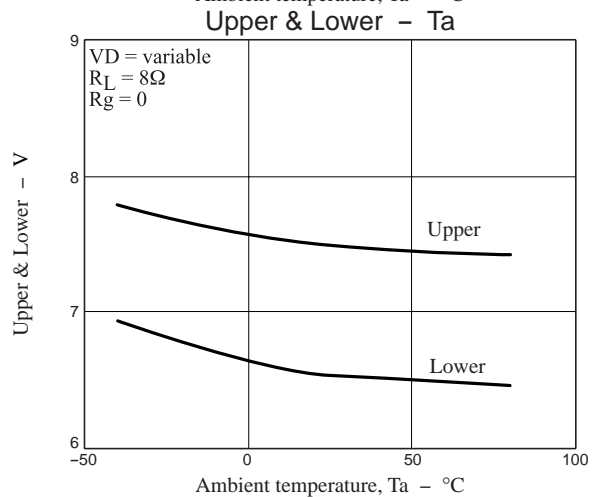
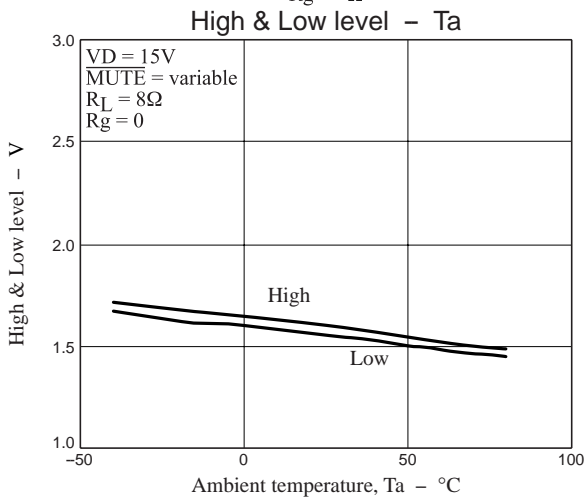
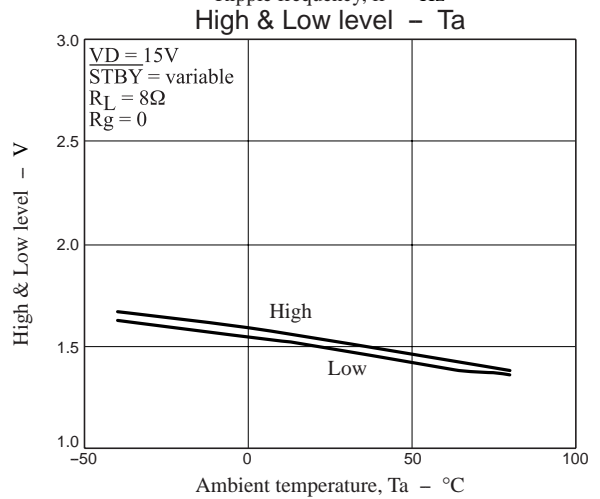
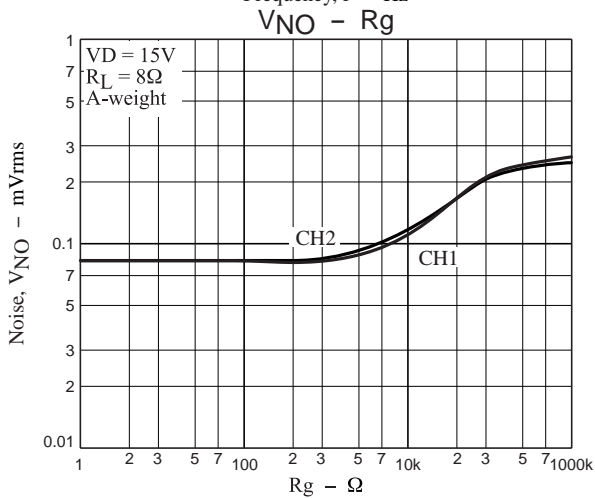
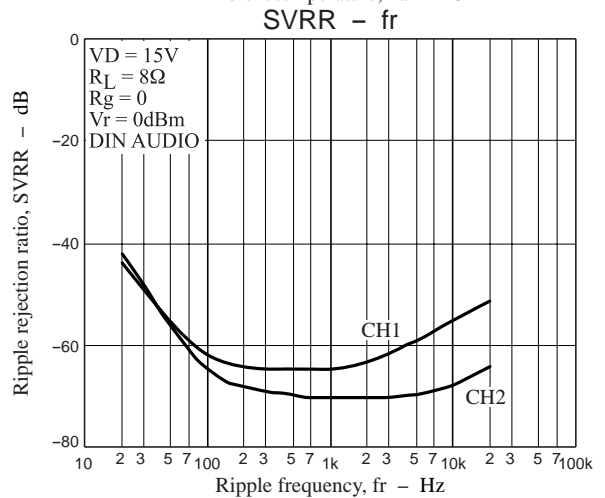
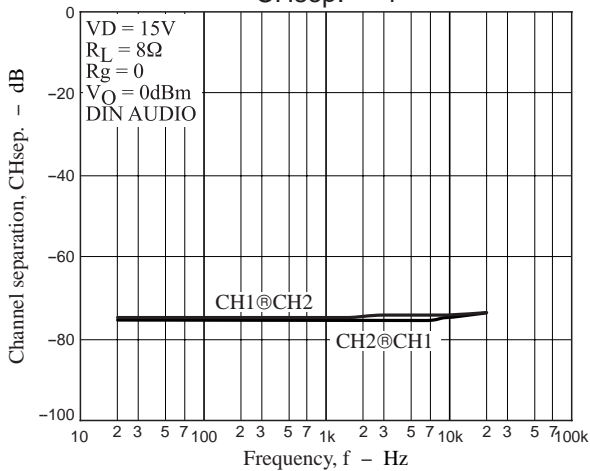
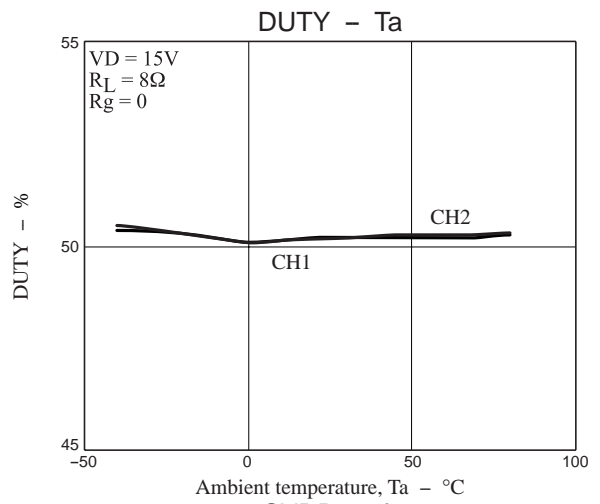
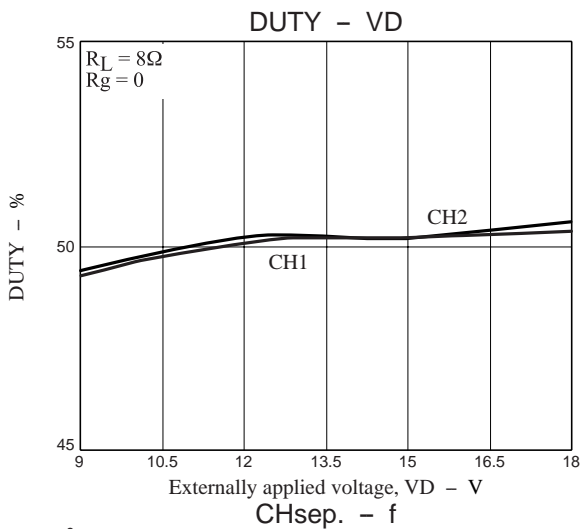
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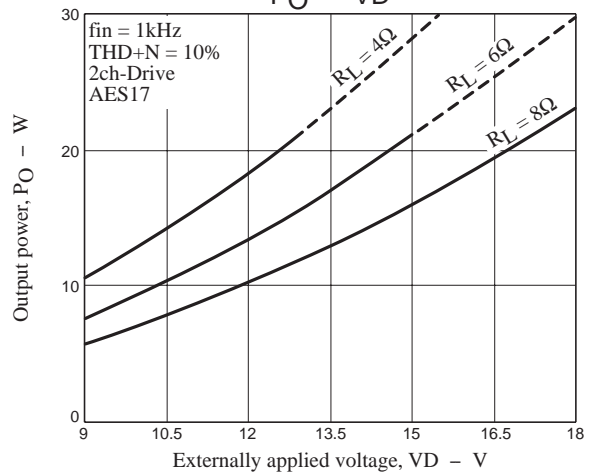
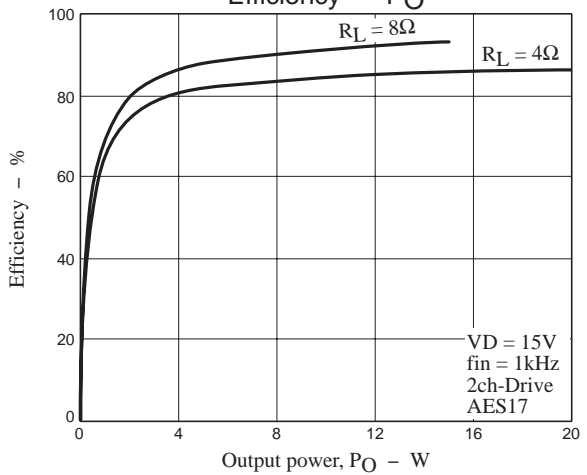
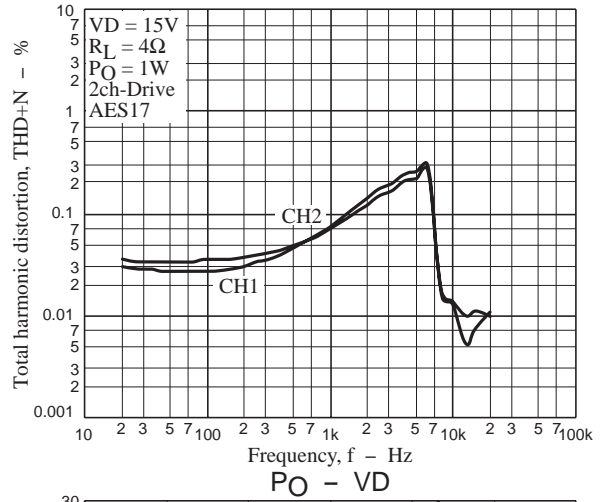
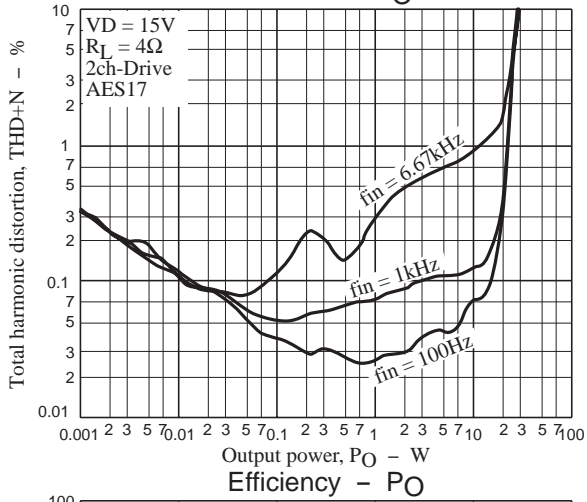
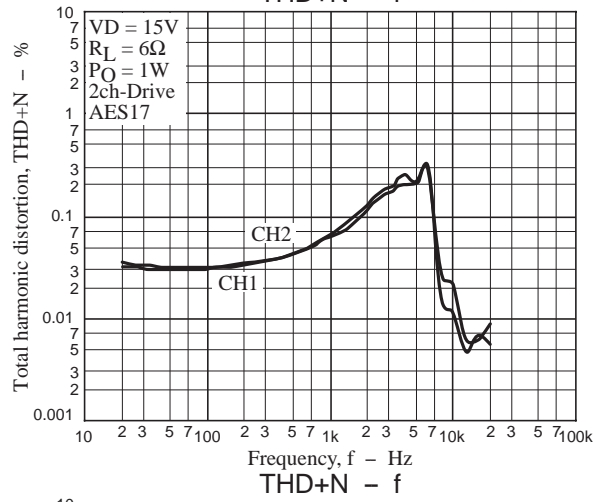
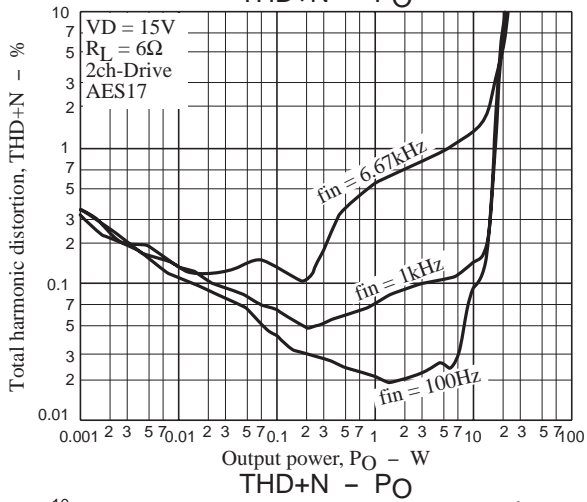
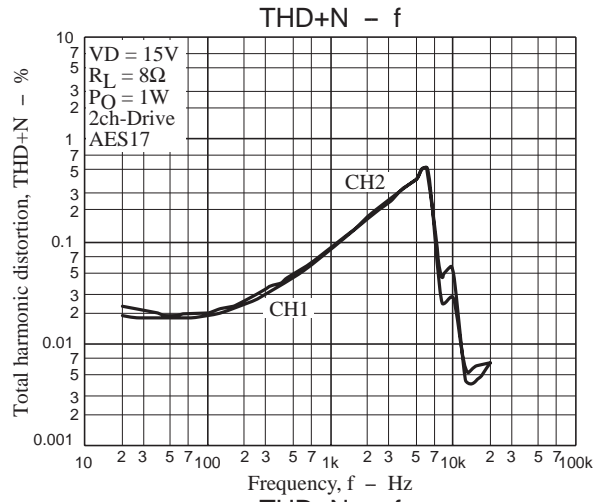
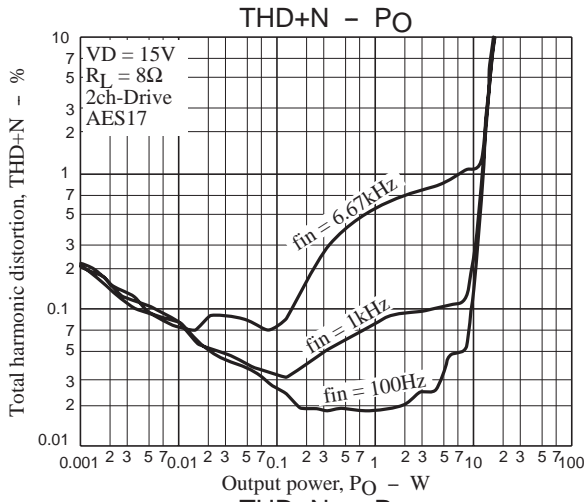


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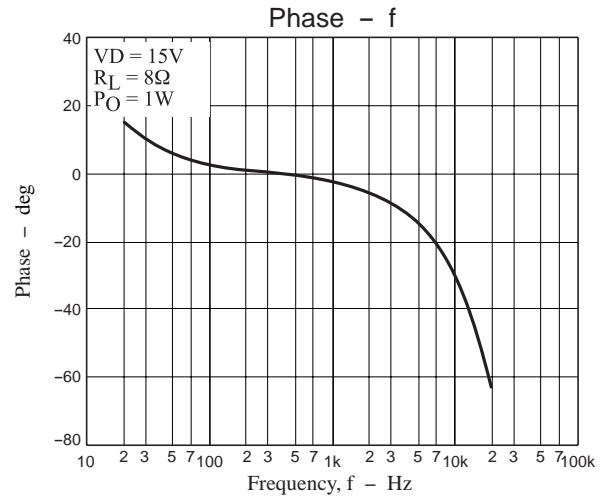
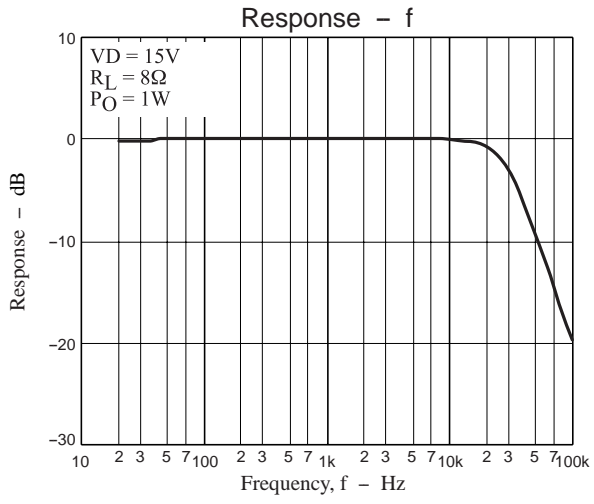


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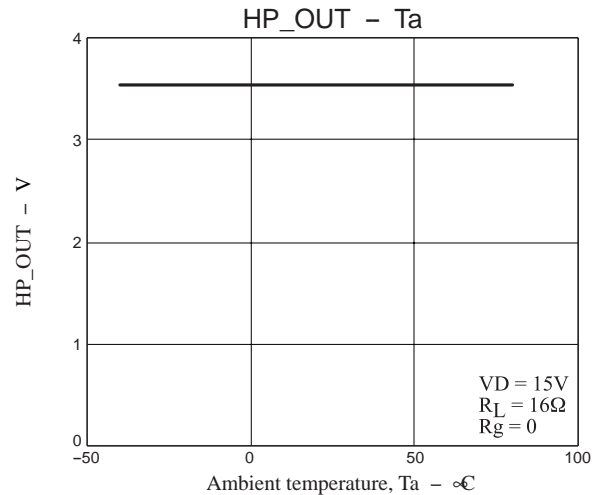
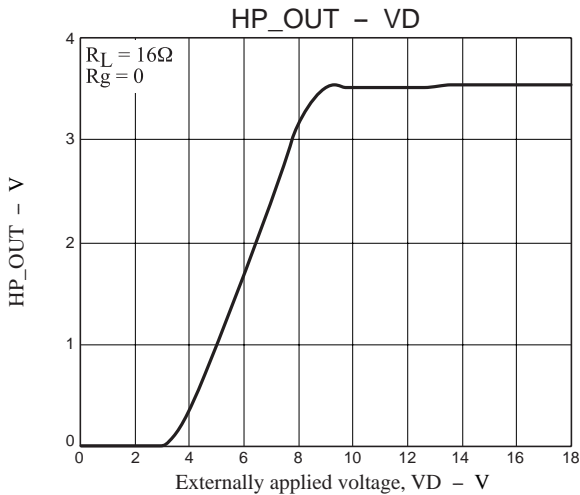
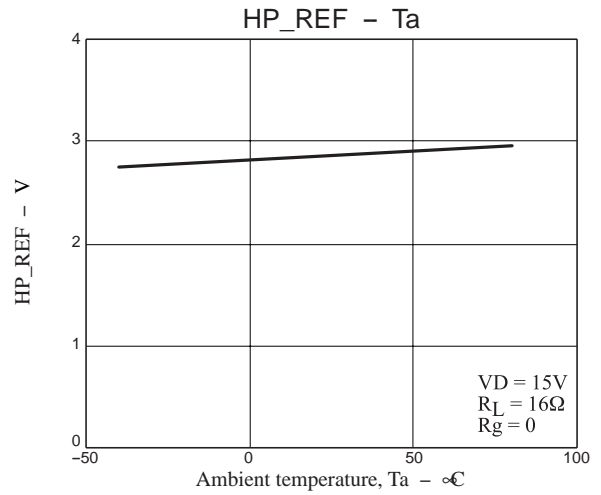
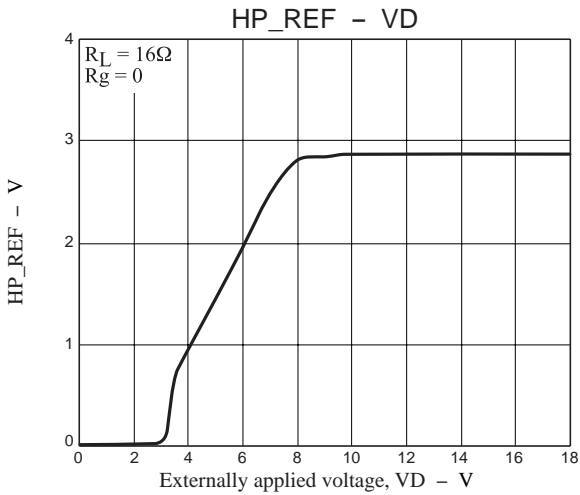
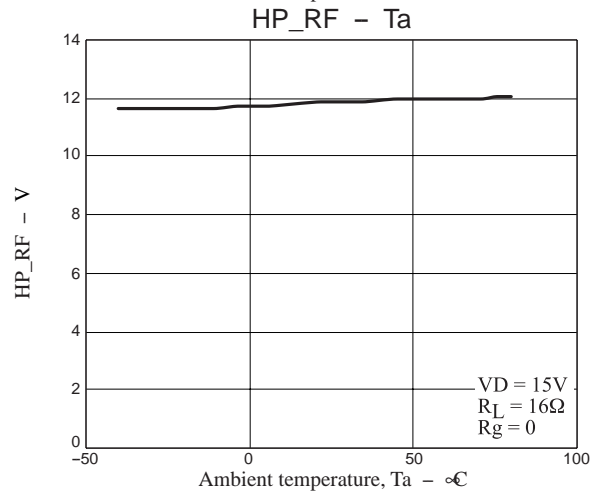
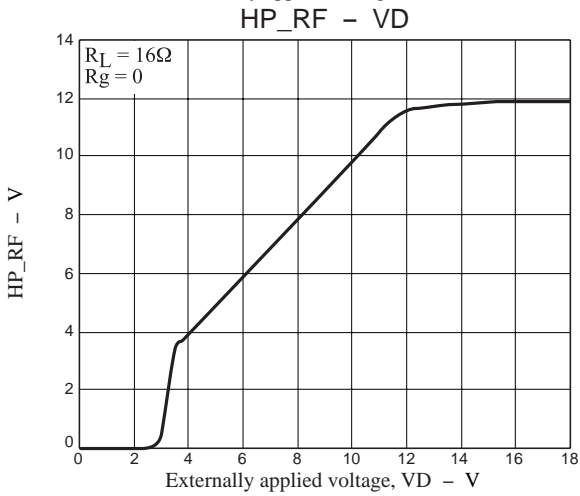
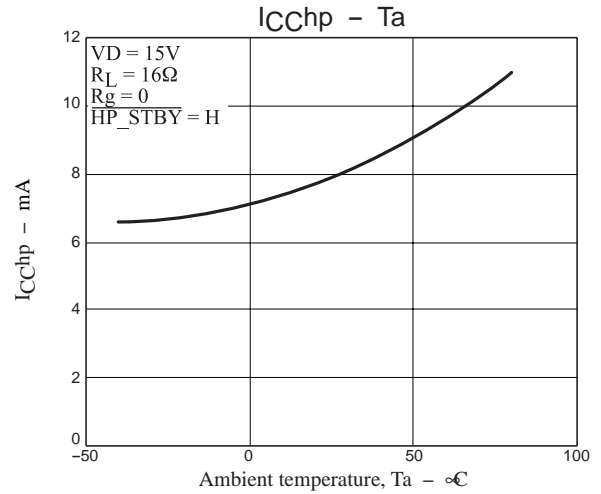
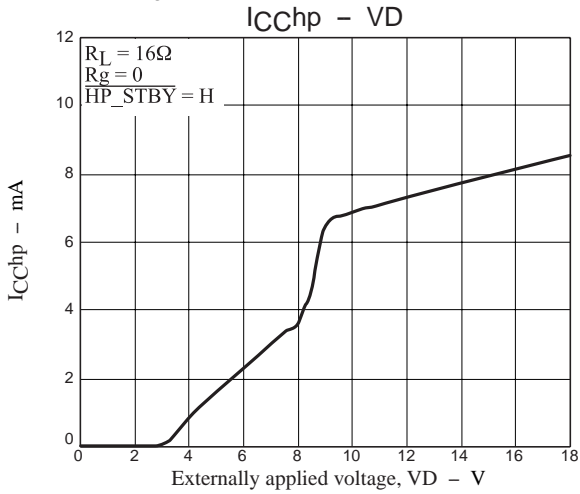


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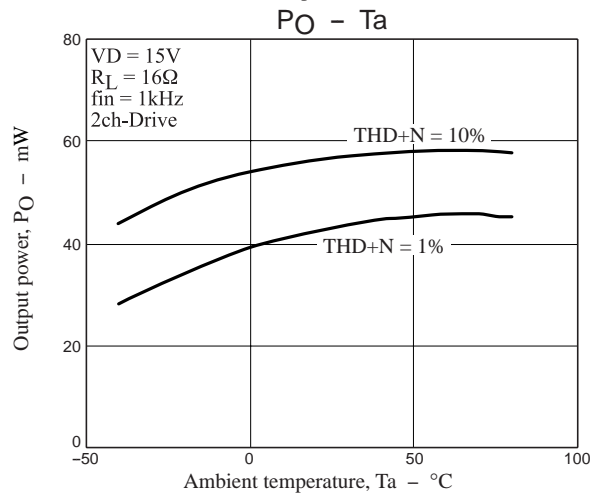
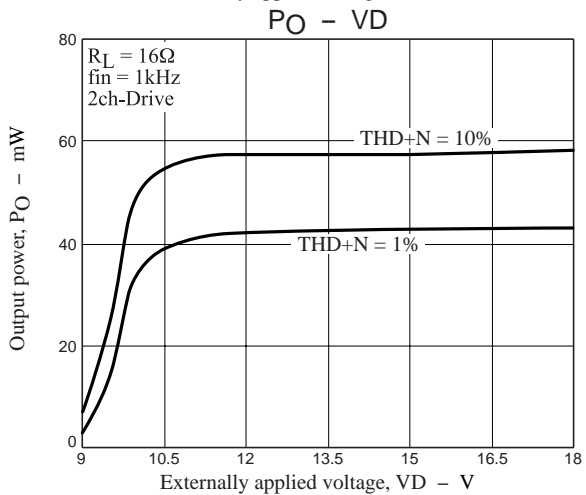
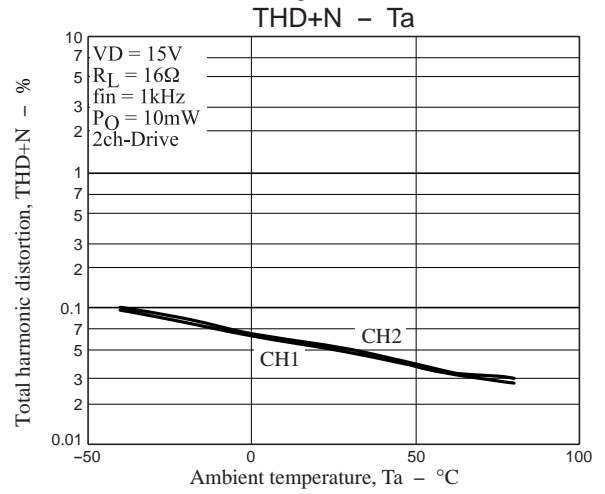
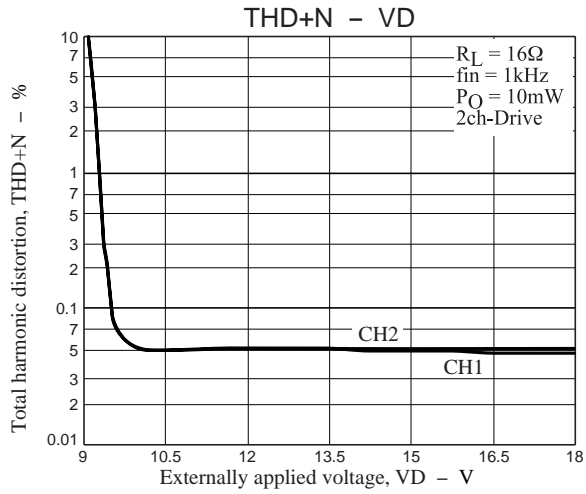
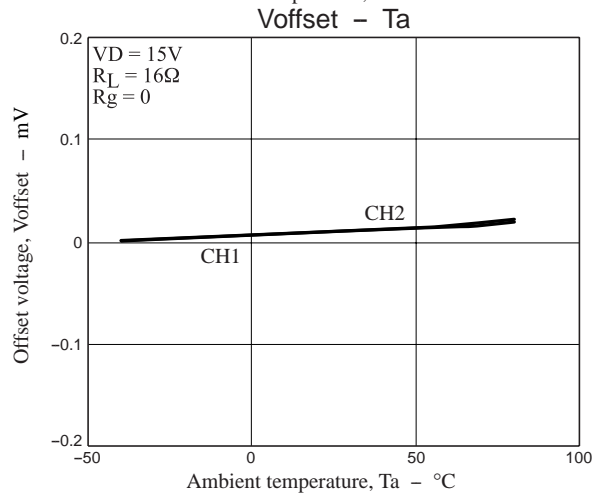
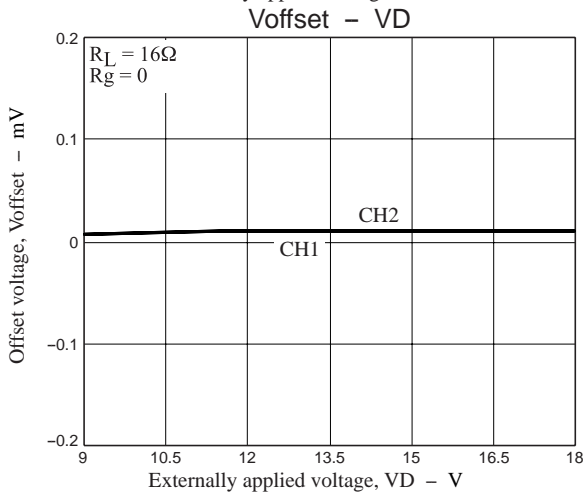
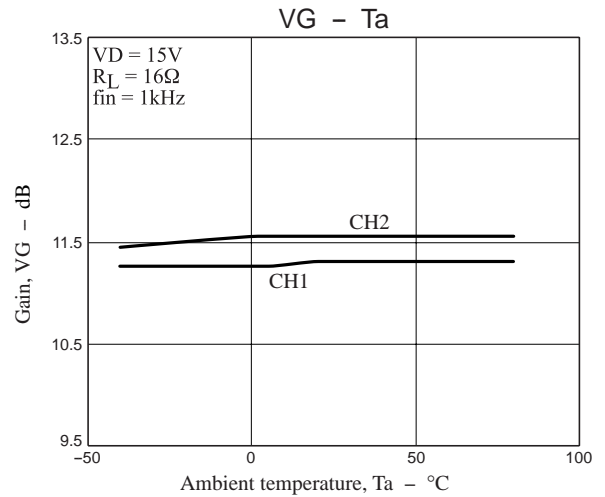
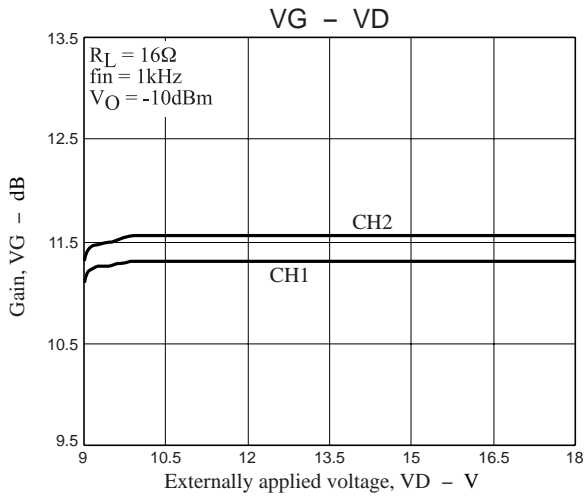


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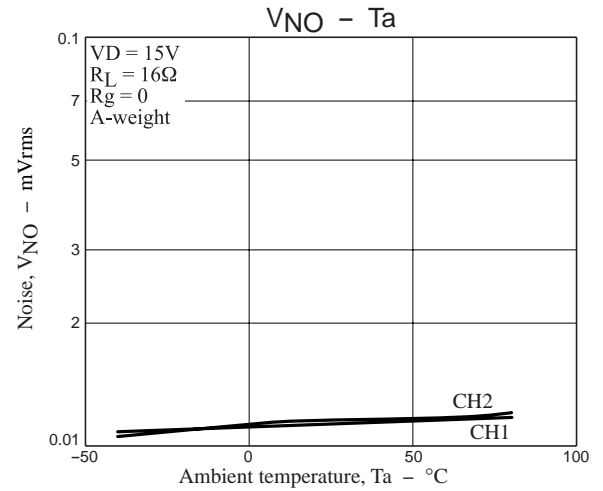
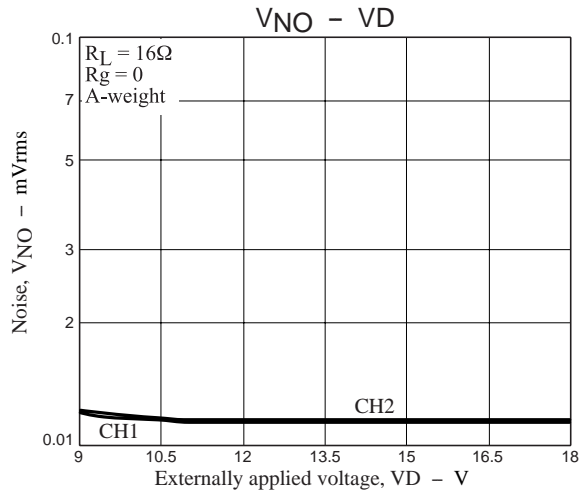
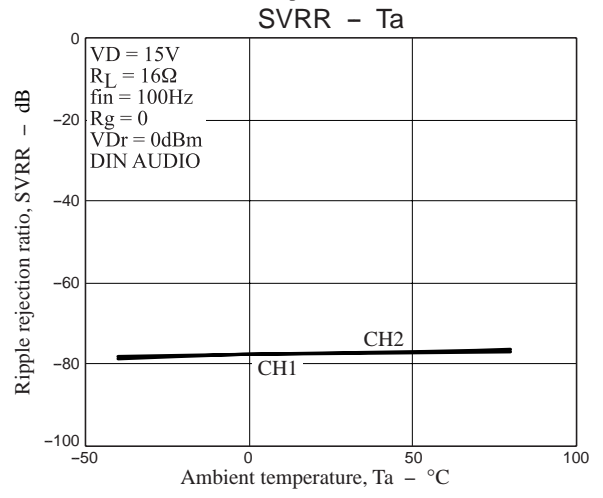
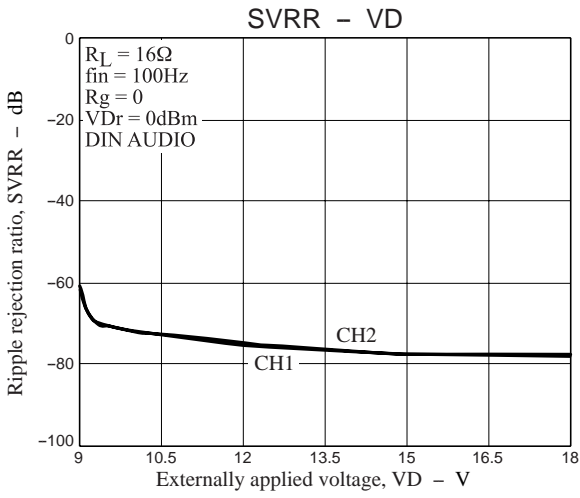
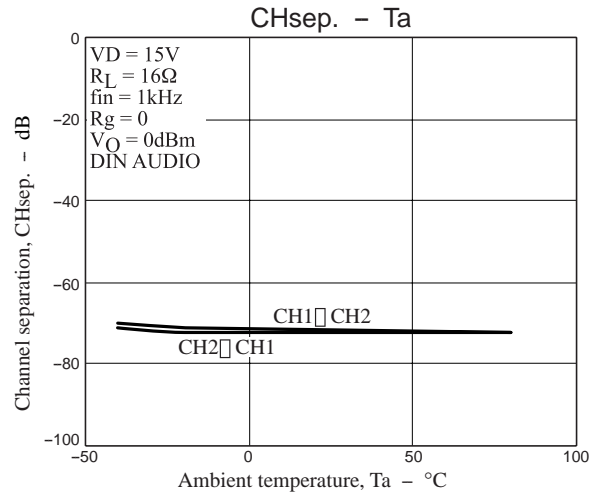
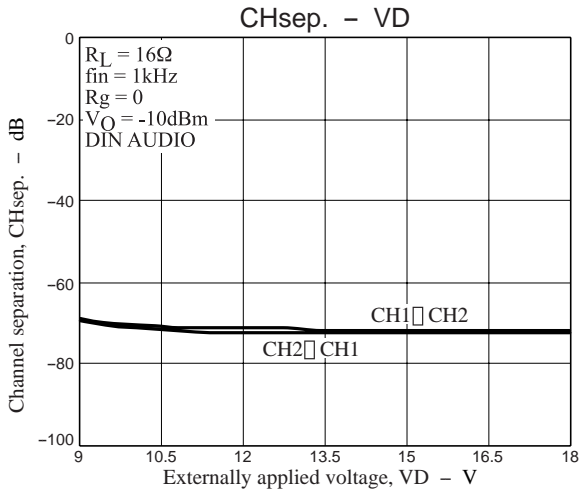
Graph deta (Digital Amplifier: $L = 33\mu\text{H}$ (TOKO : A7502BY-330M), $C = 0.1\mu\text{F}$, $C_L = 0.47\mu\text{F}$)

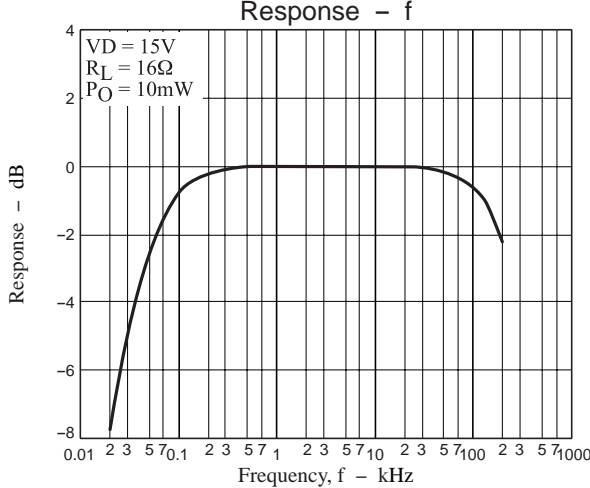
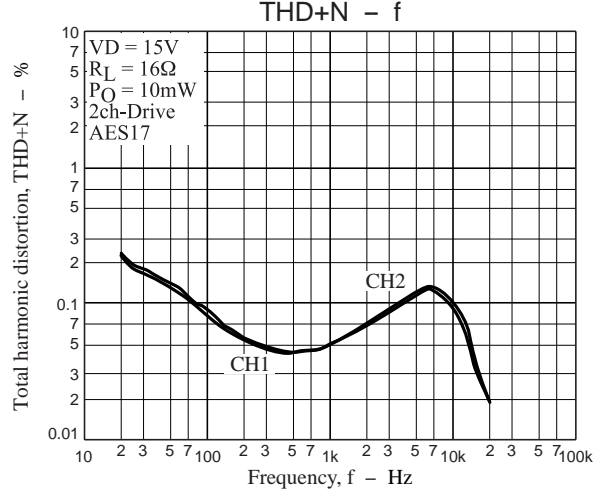
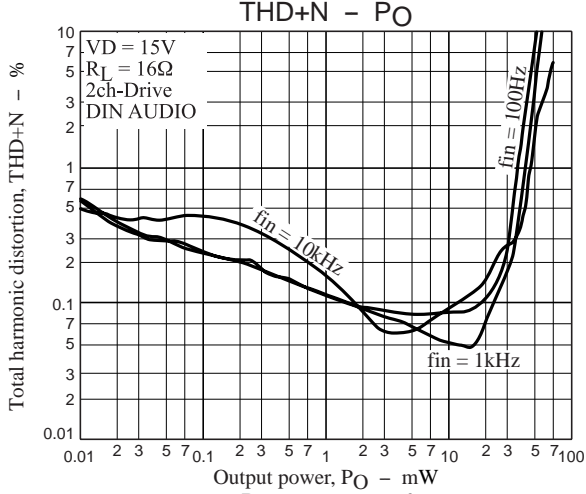
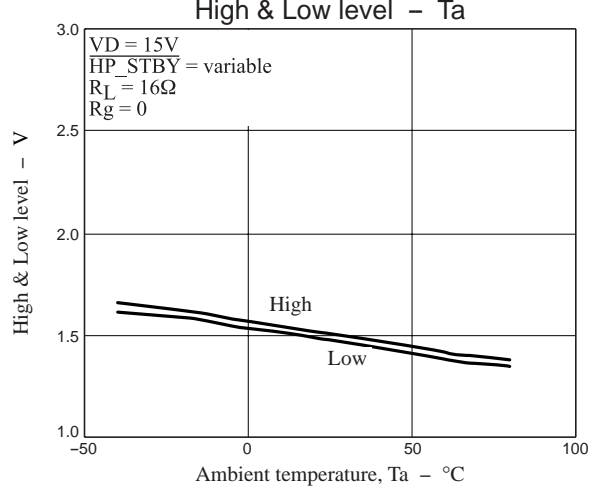
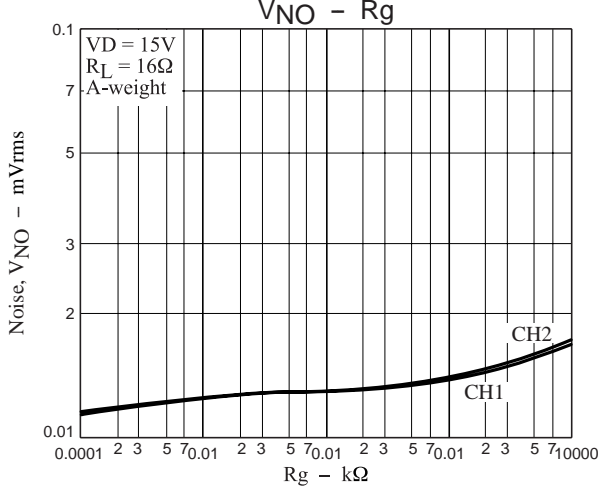
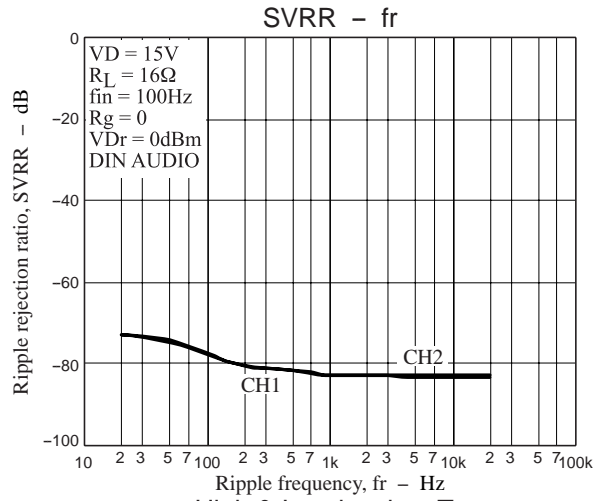
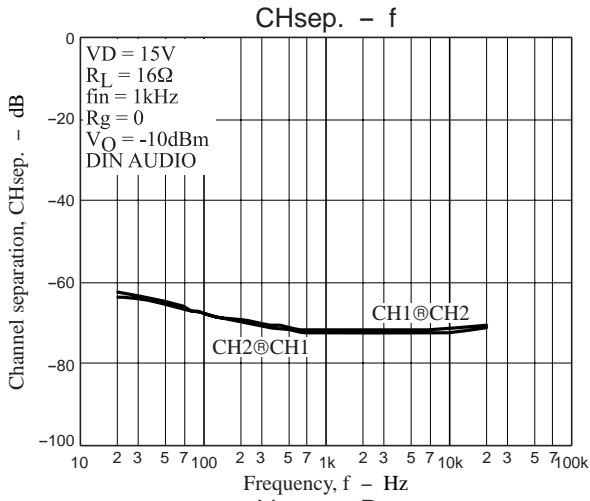


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