LXP610

Low-Jitter Multi-Rate Clock Adapter (CLAD)

General Description

The LXP610 Multi-Rate Clock Adapter (CLAD) offers pin-selectable frequency conversion between T1 and E1 rates as well as 8 additional rates from 1.544 MHz to 8.192 MHz. The output clock is frequency-locked to the input clock. When an input frame sync pulse is provided, the CLAD phase-locks the input and output clocks together, and locks the 8 kHz output frame sync pulse to the input frame sync pulse. The frame sync polarity is also pin-selectable.

Five different high frequency output clocks are available for applications which require a higher-than-baud rate backplane or system clock. The high frequency output (HFO) clock varies with the input clock frequency.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock is as accurate as the input clock.

The CLAD is an advanced CMOS device. It requires only a single +5 V power supply.

Features

- Translates between 10 different frequencies. Generates basic and high frequency output clocks and frame sync from an input clock and its frame sync.
- High Frequency Output clock for higher-than-baud rate backplane systems
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and ITU Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Pin-selectable operation mode
- Low-power 5 V only CMOS in 14-pin plastic DIP or 28-pin PLCC

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, etc.
- Conversion between T1/E1 clock rates and higher frequency backplane rates (T1/E1 converter)
- Special backplane interfaces (e.g. NTI 2.56 MHz)

LXT610 Block Diagram

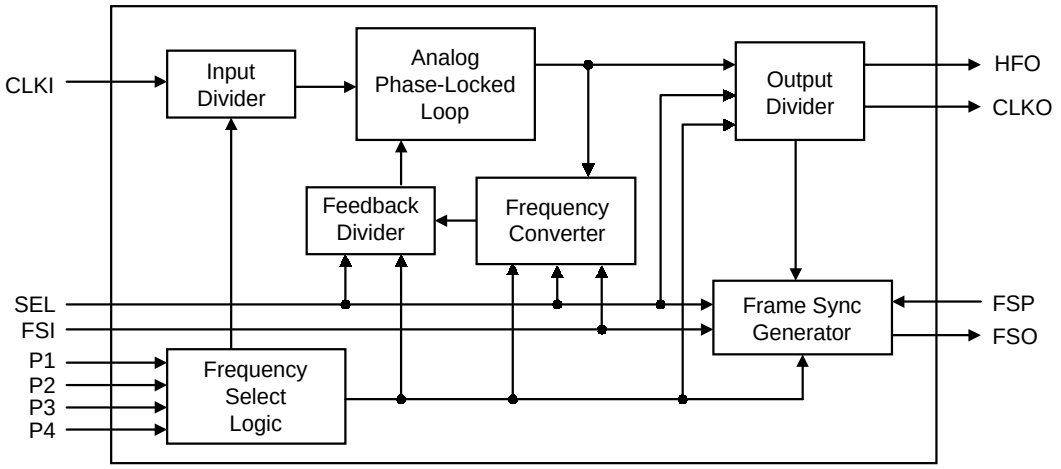


Figure 1: LXT610 Pin Assignments

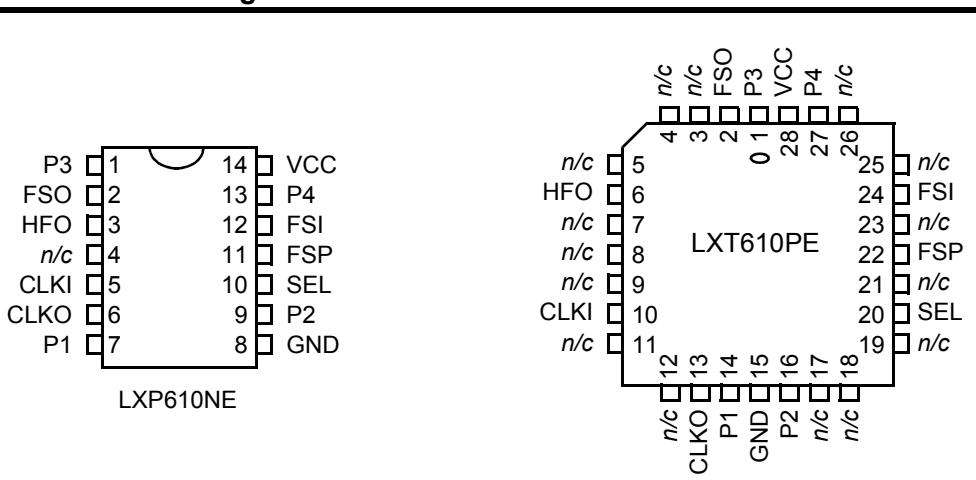


Table 1: Pin Descriptions

Pin #		Sym	I/O	Description
DIP	PLCC			
1 7 9 13	1 14 16 27	P3 P1 P2 P4	I I I I	**Program Pins 3, 1, 2, 4.** Program pins control frequency conversion and FSO pulse width in conjunction with the SEL pin as listed in Table 2.
2	2	FSO	O	**Frame Sync Output.** Frame synchronization output at 8 kHz. FSO is synched to CLKO and to FSI (if FSI is provided.) Active Low unless FSP = 1.
3	6	HFO	O	**High Frequency Output.** A high frequency output which can be used to clock external devices. HFO outputs are determined in accordance with Table 2.
5	10	CLKI	I	**Clock Input.** Primary rate clock to be converted.
6	13	CLKO	0	**Clock Output.** Primary rate clock derived from CLKI.
8	15	GND		**Ground.**
10	20	SEL	I	**Mode Select.** Controls frequency conversion and FSO pulse width in conjunction with Program pins 1-4, as listed in Table 2.
11	22	FSP	I	**Frame Sync Polarity.** When High, causes FSI and FSO to be active High pulses.
12	24	FSI	I	**Frame Sync Input**. Frame synchronization pulse (8 kHz or any sub-rate multiple). Active Low when FSP = 0. Active High when FSP = 1.
14	28	VCC	I	**Power Supply Input.** +5 V power supply input.

FUNCTIONAL DESCRIPTION

The CLAD converts an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. It also produces a frame sync output (FSO) and a high frequency output clock (HFO). The HFO frequency is a multiple (2x, 3x, 4x, or 5x) of CLKO. The specific frequencies are determined by the Mode Select (SEL) and Program (P1 - P4) inputs. Tables 2 and 3 list the CLKO and HFO frequencies available with a given input CLKI. (Table 2 is keyed to Program Pin settings; Table 3 is keyed to CLKI frequencies.) Refer to Test Specifications for output frame sync alignments.

CLKO is always frequency-locked to CLKI. When a frame sync input (FSI) is supplied, CLKI and CLKO are also phase-locked. The CLAD accepts FSI pulses at 8 kHz, or at any sub-rate multiple (i.e., 1, 2 or 4 kHz). The frame sync output (FSO) pulse is synchronized to the FSI pulse.

When an 8 kHz FSI is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms. For other FSI rates, the alignment period is correspondingly lengthened. For example, at 4 kHz, the FSI/FSO alignment is completed within a maximum of one second.

If an input frame sync pulse is not provided, the FSI pin should be tied High or Low. CLKO and FSO are still generated with the CLKO frequency locked to CLKI.

Output Jitter

The CLAD output jitter meets the following specifications:

- 2.048 MHz or 4.096 MHz to 1.544 MHz: In this mode of operation, the CLAD meets the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI in the 10 Hz - 40 kHz band, and 0.012 UI in the 8 - 40 kHz band.
- 1.544 MHz to 2.048 MHz or 4.096 MHz: In this mode of operation when there is no on, jitter input clock CLKIjitter on input clock CLKI, maximum, the jitter on CLKO is 0.035 UI pp over the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, 0.025, and UP pp in the 18-100 KHz and 0.025 UP pp in the 18-100 kHz band.

Table 2: Program Pin Functions

Mode Select				SEL = 0				SEL = 1			
P4	P3	P2	P1	CLKI	CLKO	HFO	FSO	CLKI	CLKO	HFO	FSO
0	0	0	0	1.544	2.048	6.144	Long (L)	2.048	3.088	6.176	L
0	0	0	1	3.088	2.048	8.192	Short (S)	2.048	3.088	6.176	L
0	0	1	0	1.544	2.048	6.144	L	2.048	1.544	6.176	L
0	0	1	1	1.544	2.048	8.192	S	2.048	1.544	6.176	L
0	1	0	0	1.544	2.560	7.680	L	2.560	1.544	7.720	L
0	1	0	1	6.176	4.096	8.192	L	8.192	3.088	6.176	L
0	1	1	0	1.544	2.560	7.680	L	2.560	1.544	7.720	L
0	1	1	1	6.176	2.048	8.192	S	8.192	1.544	6.176	L
1	0	0	0	3.088	2.048	6.144	L	2.048	3.088	6.176	L
1	0	0	1	3.088	4.096	8.192	L	4.096	3.088	6.176	L
1	0	1	0	3.088	2.048	6.144	L	2.048	3.088	6.176	L
1	0	1	1	1.544	4.096	8.192	L	4.096	1.544	6.176	L
1	1	0	0	6.176	2.560	7.680	L	2.560	1.544	7.720	L
1	1	0	1	6.176	4.096	8.192	L	8.192	3.088	6.176	L
1	1	1	0	6.176	2.560	7.680	L	2.560	1.544	7.720	L
1	1	1	1	6.176	4.096	8.192	L	8.192	1.544	6.176	L

Jitter Transfer

The CLAD is sensitive to jitter on the input clock in certain frequency bands The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Test Specification Figures 4 and 5 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 4. In this mode, jitter in the critical 8 kHz band is attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 5. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110. (Jitter transfer varies with the input jitter level. Performance in a particular application should be verified in the actual circuit.)

Table 3: Input to Output Frequency Conversion Options

CLKI	CLKO	HFO	FSO	P4	P3	P2	P1	SEL
1.544	2.048	6.144	Long (L)	0	0	X	0	0
1.544	2.048	8.192	Short (S)	0	0	1	1	0
1.544	2.560	7.680	L	0	1	X	0	0
1.544	4.096	8.192	L	1	0	1	1	0
2.048	1.544	6.176	L	0	0	1	X	1
2.048	3.088	6.176	L	0	0	0	X	1
2.048	3.088	6.176	L	1	0	X	0	1
2.560	1.544	7.720	L	X	1	X	0	1
3.088	2.048	6.144	L	1	0	X	0	0
3.088	2.048	8.192	S	0	0	0	1	0
3.088	4.096	8.192	L	1	0	0	1	0
4.096	1.544	6.176	L	1	0	1	1	1
4.096	3.088	6.176	L	1	0	0	1	1
6.176	2.048	8.192	S	0	1	1	1	0
6.176	2.560	7.680	L	1	1	X	0	0
6.176	4.096	8.192	L	0	1	0	1	0
6.176	4.096	8.192	L	1	1	X	1	0
8.192	1.544	6.176	L	X	1	1	1	1
8.192	3.088	6.176	L	X	1	0	1	1

APPLICATION INFORMATION

Frame Sync Generation

A frame sync pulse is required to synchronize the input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 2.

Power Supply Decoupling and Filtering

The LXP610 CLAD is designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 3, a standard 0.1 µF bypass capacitor is recommended.

The CLAD is a monolithic silicon device which incorporates both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Typical Application

Figure 3 shows a typical application circuit using a pair of LXP610 CLADs to convert between the 2.56 MHz backplane frequency and the 1.544 MHz T1 rate. The CLAD at the top of the figure provides the 1.544 MHz TCLK for the T1 framer and transceiver. For conversion from 2.56 MHz to 1.544 MHz, P1, P2, and P4 are tied Low; and P1 and SEL are tied High. In this configuration, the LXP610 HFO is 7.720 MHz.

The CLAD at the bottom of Figure 3 produces the 2.56 MHz backplane clock. For conversion from 1.544 MHz to 2.56 MHz, P1, P2, P3 and P4 are tied High; and SEL is tied Low. The HFO produced in this configuration is 7.680 MHz.

Figure 2: Frame Sync (FSI) Generation Circuit

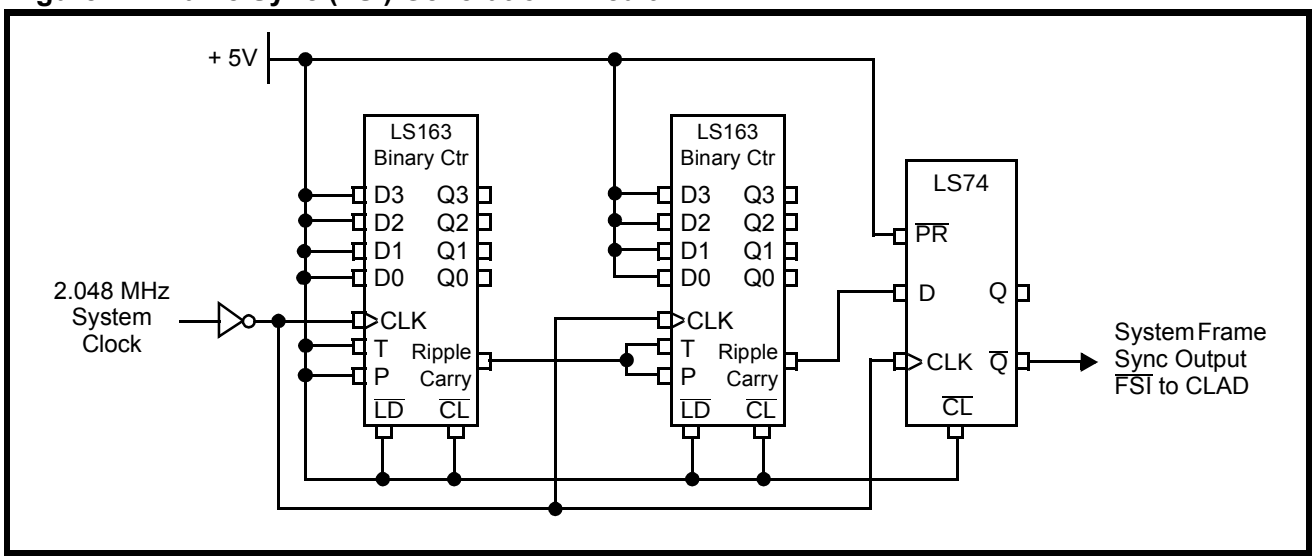
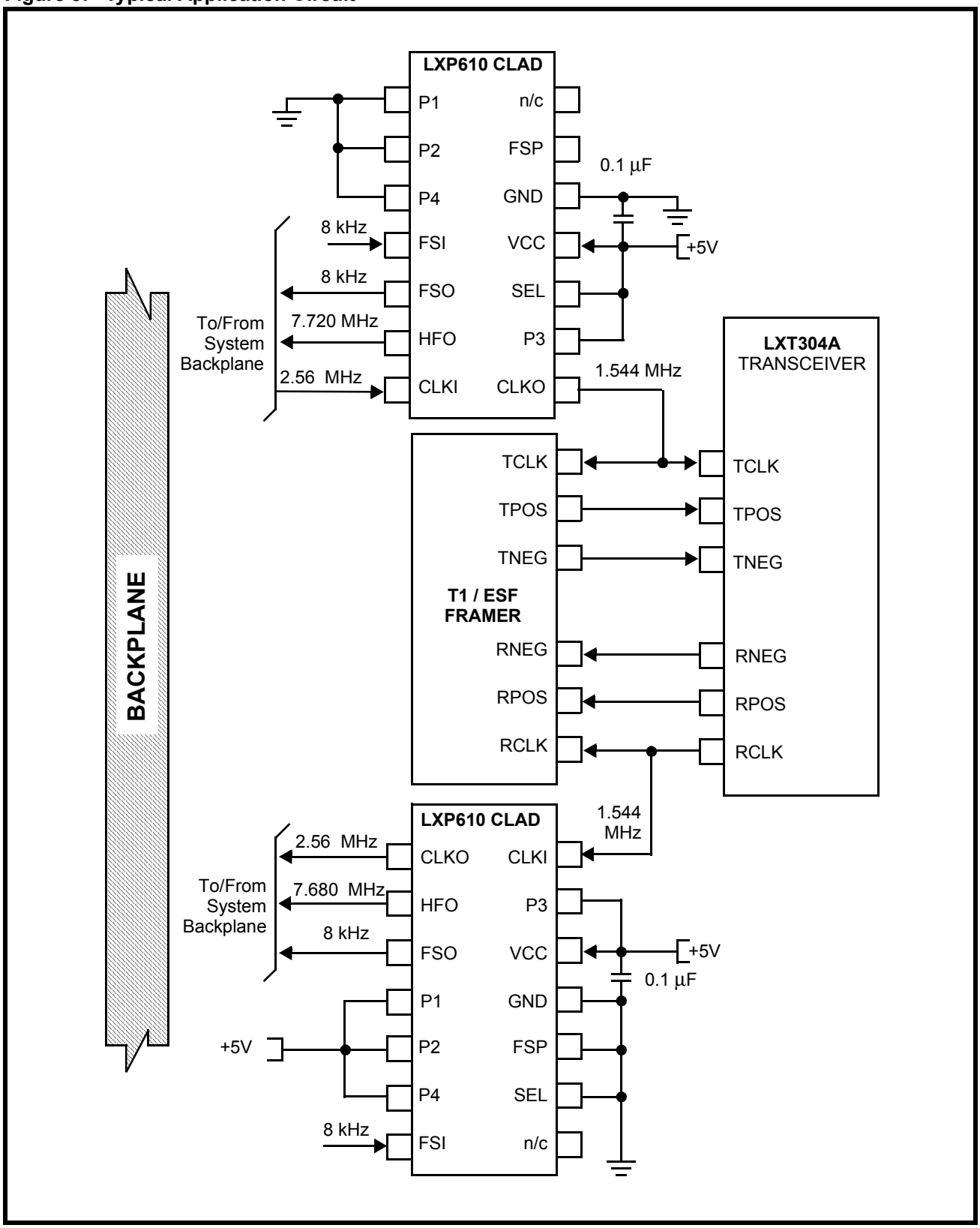


Figure 3: Typical Application Circuit



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 4 through 8 and Figures 4 through 11 represent the performance specifications of the LXT610 and are guaranteed by test, except where noted by design.

Table 4: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage (referenced to GND)	RV+, TV+	-0.3	7.0	V
Voltage, any I/O pin	V_{IO}	GND - 0.3	VCC + 0.3	V
Current, any I/O pin[1]	I_{IO}	-10	10	mA
Storage temperature	T_{STG}	-65	+150	ºC
Power dissipation	P_D	–	340	mW

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 5: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply voltage[1]	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}	–	–	8	mA	No TTL loading
	I_{CC}	–	–	14	mA	Full TTL loading
Operating temperature	T_{OP}	-40	–	85	ºC	

1. Voltages with respect to ground unless otherwise specified.

Table 6: Digital Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Max	Units
Input Low voltage	V_{IL}	–	0.8	V
Input High voltage	V_{IH}	2.0	–	V
Output Low voltage (I_{OL} = +1.6 mA)	V_{OL}	–	0.4	V
Output Low voltage (I_{OL} < +10 µA)	V_{OL}	–	0.2	V
Output High voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	–	V
Output High voltage (I_{OH} < -10 µA)	V_{OH}	4.5	–	V
Input leakage current	I_{LL}	-10	10	µA

Table 7: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Units	Test Conditions
Output Jitter on CLKO CLKO=1.544 MHz	TJ1	No Bandlimiting	0.050	0.010	0.20	UI pp	CLKI=2.048 or 4.096 MHz
		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	JI=0
		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	$\overline{FSI}$ applied
Output Jitter on CLKO CLKO=2.048 MHz	TJ2	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI=1.544 MHz, JI=0 $\overline{FSI}$ applied
		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	

1. Specifications from AT&T Publication 62411 and ITU Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

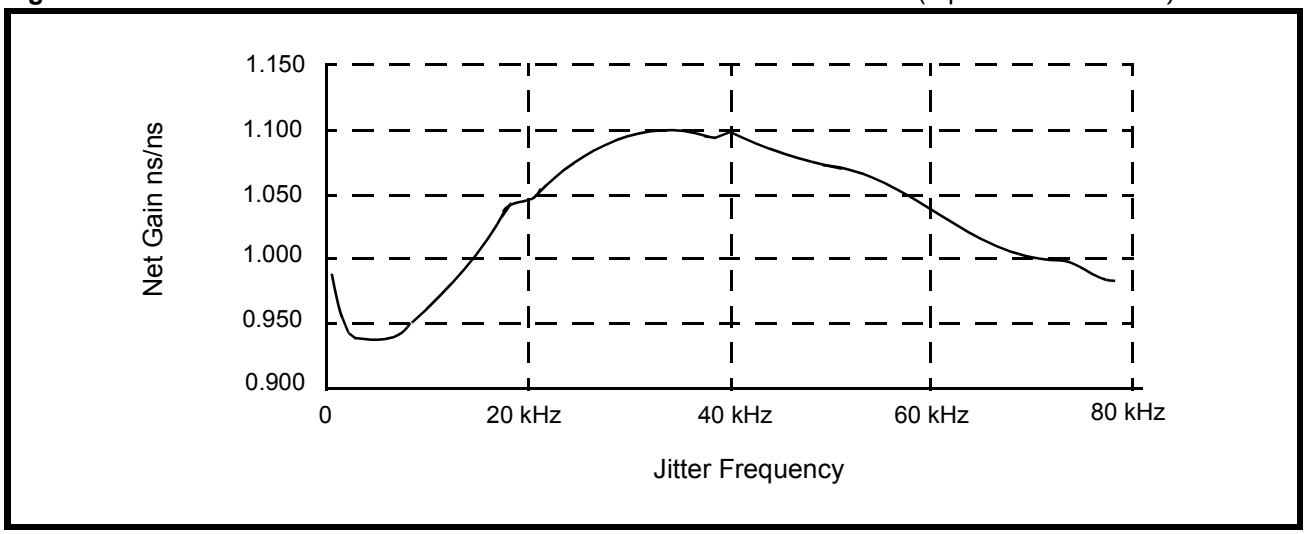


Figure 5: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)

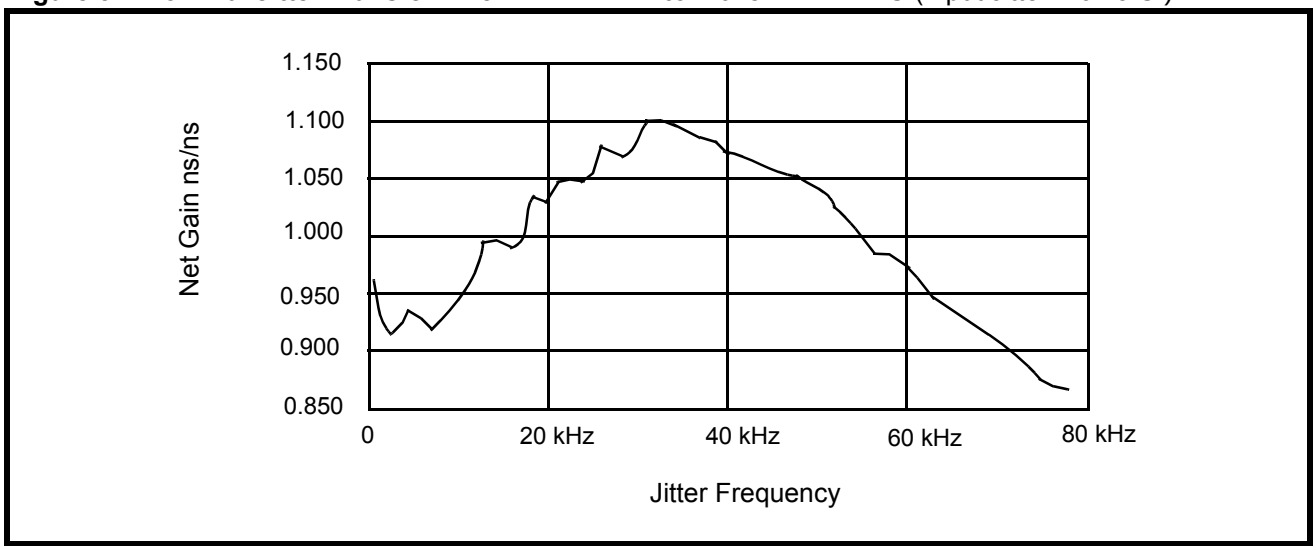


Table 8: Timing Values (see Figure 6)

Parameter	Sym	Minimum	Maximum	Units
Capture range on CLKI	–	±10000	–	ppm
Lock range on CLKI	–	±10000	–	ppm
Input clock duty cycle	–	35	65	%
Rise/fall time on CLKI, FSI	Trf	–	40	ns
Rise/fall time on CLKO, FSO, HFO with a 25 pF load	Trf	–	40	ns

Figure 6: Rise and Fall Times

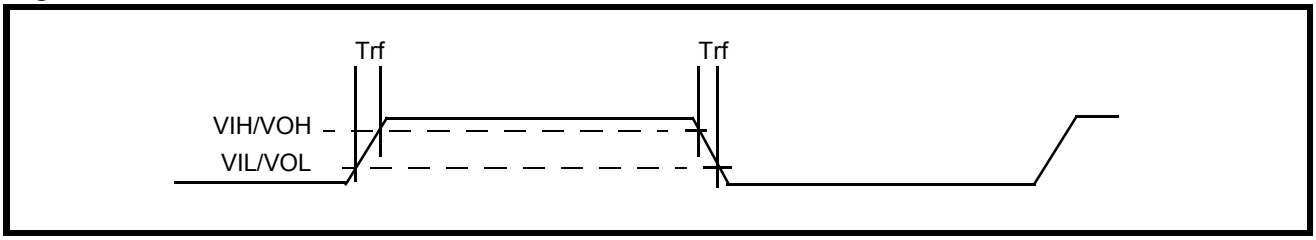


Table 9: Timing Values (see Figure 7 through Figure 11)

Parameter	Sym	Minimum	Typ	Maximum	Units
$\overline{\text{FSI}}$ setup time from CLKI rising	Tsui	46	–	–	ns
$\overline{\text{FSI}}$/CKLI hold time	Thi	30	–	–	ns
$\overline{\text{FSI}}$ pulse width (Low)	Twi	76	–	TCLKI[1]	ns
CLKO delay from CLKI	TdC	-15	0	+15	ns
CLKO duty cycle	Cdc	49	–	51	%
FSO delay from HFO	TdF	-5	–	30	ns
FSO pulse width (low)	TWO	–	–	TCLKO[2]	ns
CLKO delay from HFO	TdH	-15	–	+15	ns

1. TCLKI is the period of CLKI.
2. TCLKO is the period of CLKO.

Figure 7: Timing Relationships - FSI / CLKI to CLKO / FSO and HFO

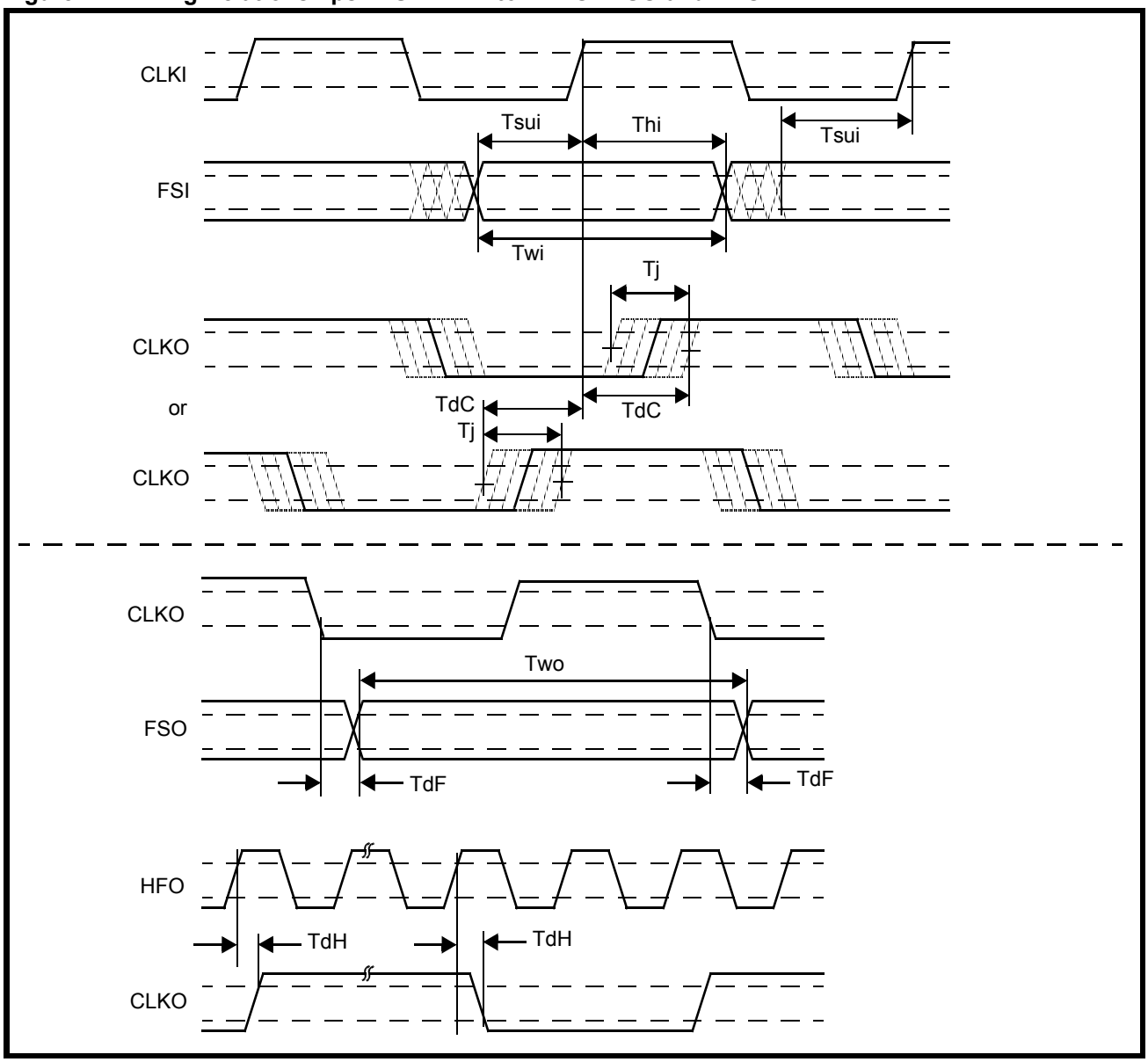


Figure 8: Output Frame Sync Alignment when HFO = 2 x CLKO

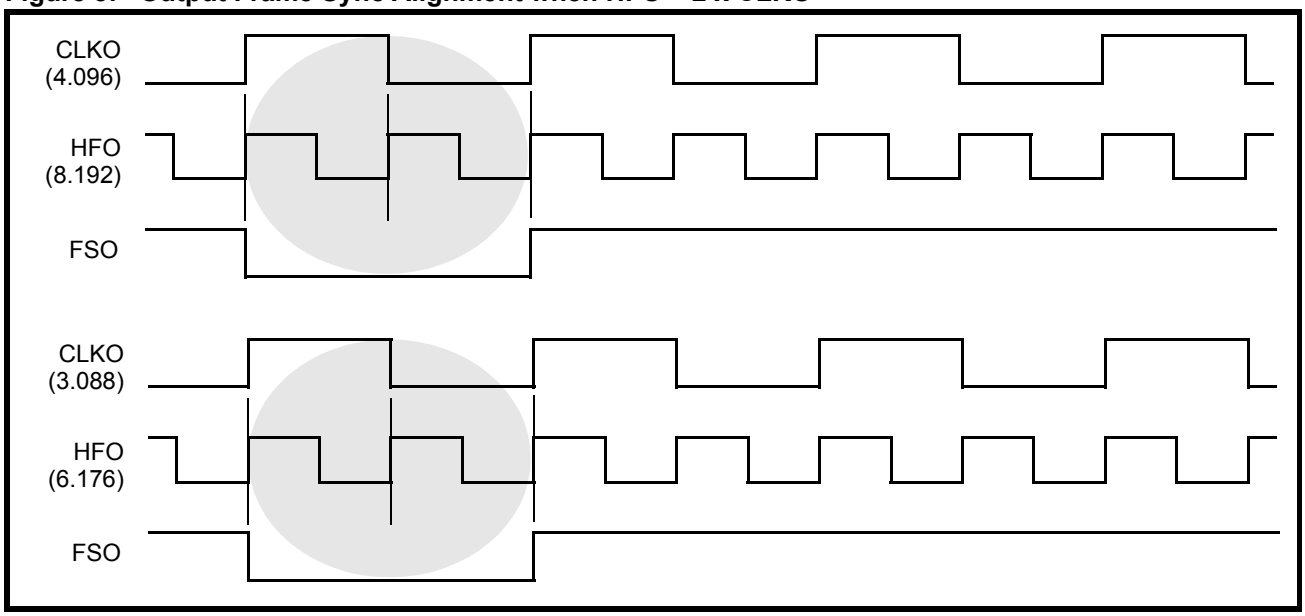


Figure 9: Output Frame Sync Alignment when HFO = 3 x CLKO

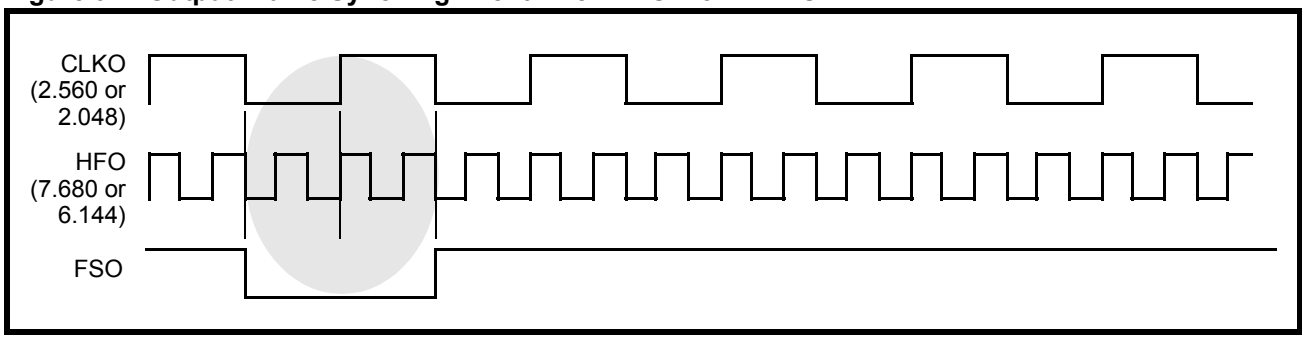


Figure 10: Output Frame Sync Alignment when HFO = 4 x CLKO

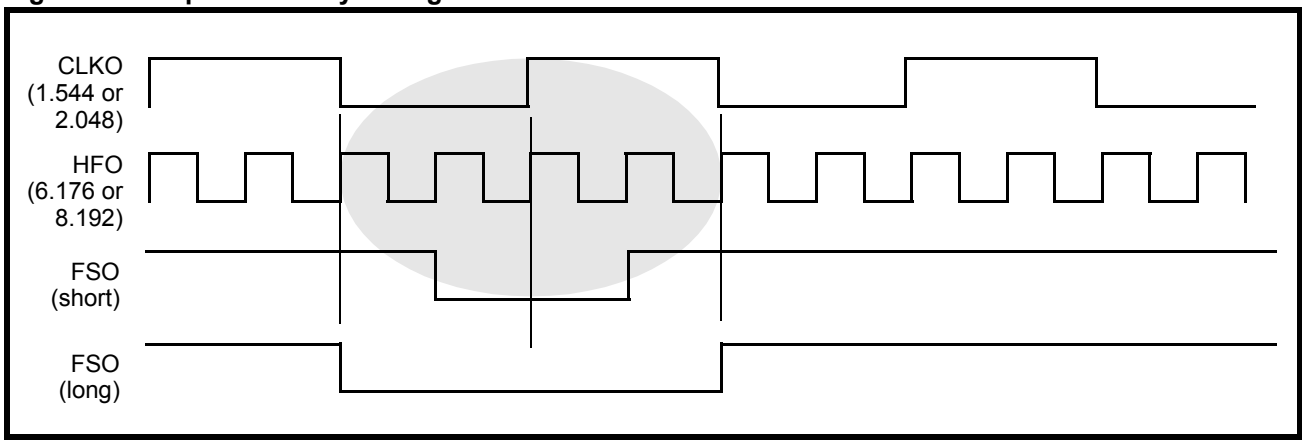


Figure 11: Output Frame Sync Alignment when HFO = 5 x CLKO