LXT317

DECT Twisted-Pair LIU Transceiver

General Description

The LXT317 is the first fully integrated, long-haul transceiver for Digital European Cordless Telephony (DECT) base station interface applications at 1.152 Mbps. The transceiver operates over twisted-pair cable to a maximum of 43 dB (3.5 km at 0.6 mm, 40 nF/km cable) with no external components.

The LXT317 offers selectable HDB3 encoding/decoding, and unipolar or bipolar data I/O. The LXT317 also offers a variety of diagnostic features including loopbacks and Loss of Signal monitoring.

Its advanced double-poly, double-metal CMOS process requires only a single 5-volt power supply.

Applications

- DECT base stations to switch/PBX interface
- NTU (interface to E1 Service)
- LAN bridge
- Private network data pump

Features

- Fully integrated transceiver comprising:
  - on-chip equalizer
  - timing recovery/control
  - data processor
  - receiver
  - transmitter
  - digital control
- Fully restores the received signal after transmission via a cable with attenuation of 43 dB @ 576 kHz
- Selectable Unipolar or Bipolar data I/O
- Selectable HDB3 encoding/decoding
- Output short circuit current limit protection
- On-line idle mode for testing or for redundant systems
- Local and remote loopback functions
- Receive monitor with Loss of Signal (LOS) output
- High input jitter tolerance
- Constant through-chip delay
- Available in 28-pin DIP and PLCC
- -40 °C to +85 °C operating temperature

LXT317 Block Diagram

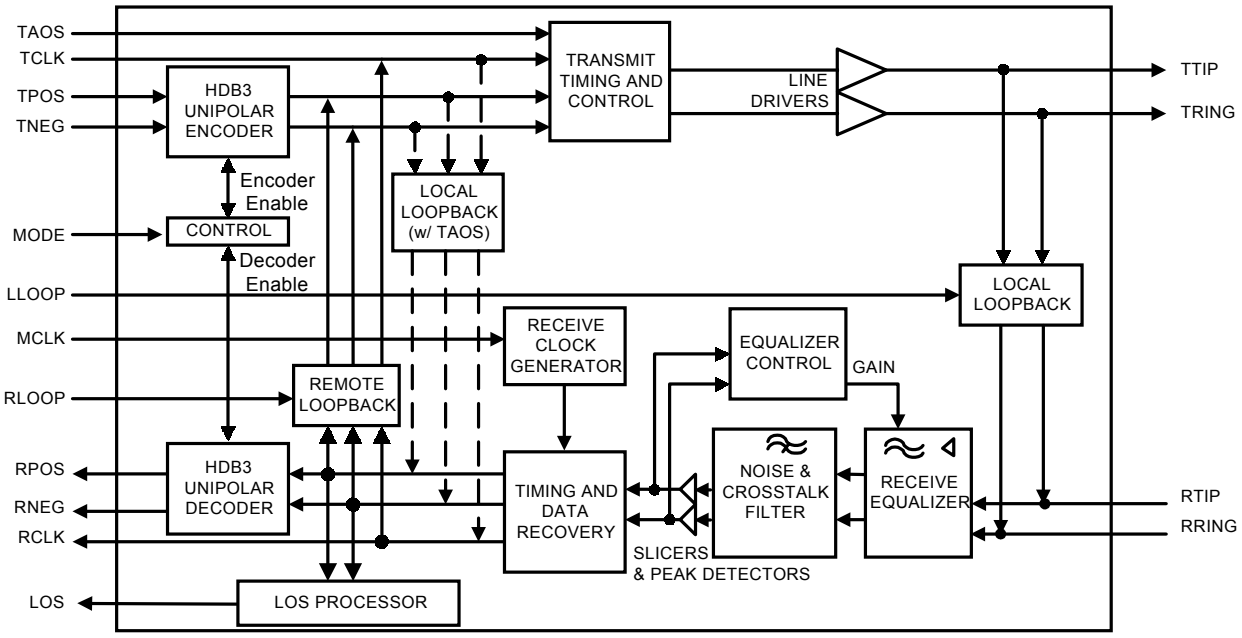
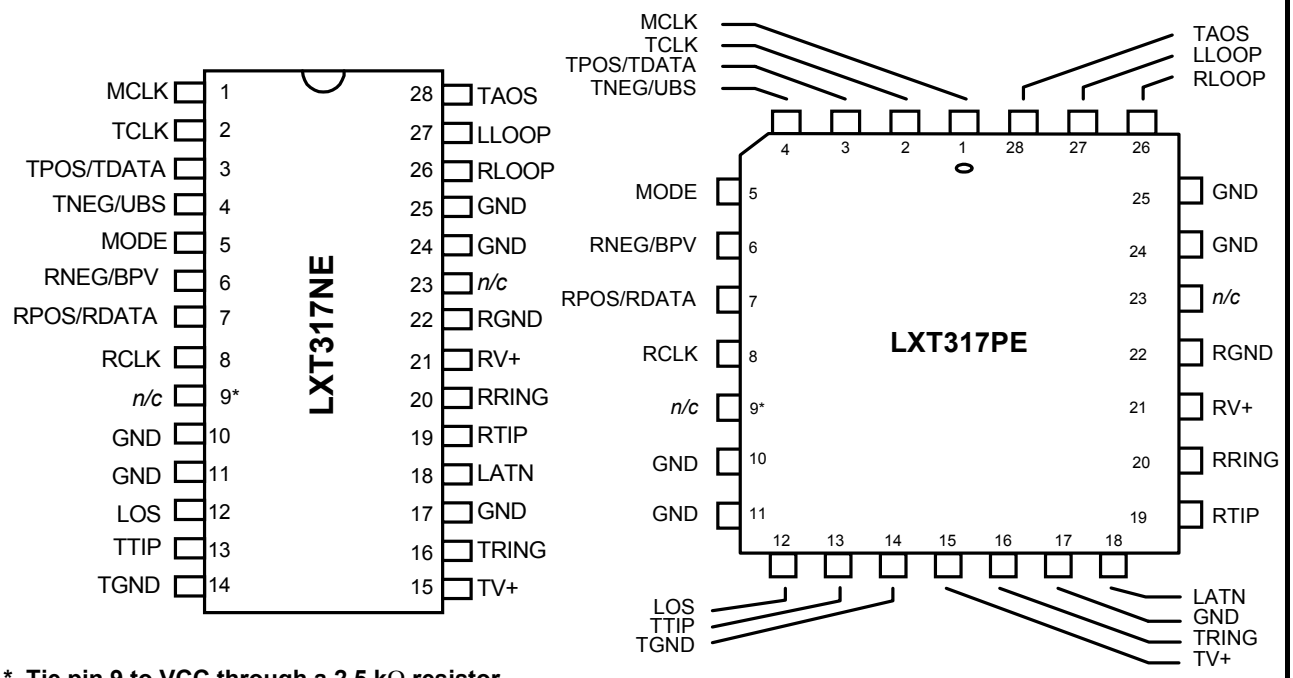


Figure 1: LXT317 Pin Assignments



*** Tie pin 9 to VCC through a 2.5 kΩ resistor.**

Table 1: Pin Descriptions

Pin #	Symbol	I/O	Description
1	MCLK	I	**Master Clock.** A 1.152 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied tie this pin Low.
2	TCLK	I	**Transmit Clock.** Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK. If TCLK is not supplied tie this pin Low.
3	TPOS/ TDATA	I	**Transmit Data Input; Data Input/Polarity Select.** Bipolar input for data to be transmitted on the twisted-pair line. Normally, pin 3 is TPOS and pin 4 is TNEG, the positive and negative sides of a bipolar input pair. However, when pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), the LXT317 switches to a unipolar mode. See Table 2 for Unipolar mode pin functions.
4	TNEG/ UBS	I	
5	MODE	I	**Mode Select.** Enables or disables zero suppression. Enables the HDB3 encoder/ decoder when tied to RCLK. Disables HDB3 encoder/decoder when tied Low.
6	RNEG/ BPV	O	**Receive Negative Data; Receive Positive Data.** Bipolar data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). Both outputs are stable and valid on the rising edge of RCLK. In Unipolar mode, pin 6 output is a bipolar violation indicator and pin 7 is the unipolar data output. See Table 2 for Unipolar mode functions.
7	RPOS/ RDATA	O	
8	RCLK	O	**Receive Clock.** This is the clock recovered from the signal received at RTIP and RRING.
9	–	–	***not used.*** Tie this pin to VCC through a 2.5 kΩ resistor.

Table 1: Pin Descriptions–continued

Pin #	Symbol	I/O	Description
10	GND	–	**Ground.** Tie this pin to ground.
11	GND	–	**Ground.** Tie this pin to ground.
12	LOS	O	**Loss Of Signal.** LOS goes High after 175 consecutive spaces and returns Low when the received signal reaches 12.5% mark density (minimum of four 1s within 32 bit periods, with no more than 15 consecutive 0s). Received marks are output on RPOS and RNEG even when LOS is High (during LOS condition).
13	TTIP	O	**Transmit Tip; Transmit Ring.** Differential Driver Outputs. These outputs are designed to drive a 50 - 200 Ω load. Line matching resistors and transformer can be selected to give the desired pulse height.
16	TRING	O	
14	TGND	–	**Tx Ground.** Ground return for the transmit drivers power supply TV+.
15	TV+	I	**Transmit Power Supply.** +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3 V.
17	GND	–	**Ground.** This pin must be tied to ground.
18	LATN	O	**Line Attenuation Indication.** Encoded output. Pulse width, relative to RCLK, indicates receive equalizer gain setting (line insertion loss at 1024 kHz). When LATN = one RCLK pulse, the equalizer is set at 10 dB of gain; two pulses = 21 dB; three pulses =32 dB and four pulses = 0 dB. Output is valid on the rising edge of RCLK.
19	RTIP	I	**Receive Tip; Receive Ring.** The AMI signal received from the line is applied at these pins. A 1:1 transformer is required. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
20	RRING	I	
21	RV+	I	**Receive Power Supply.** +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
22	RGND	–	**Rx Ground.** Ground return for power supply RV+.
23	–	–	***not used.*** This pin is inactive–*leave this pin floating*.
24	GND	–	**Ground.** This pin is inactive–*tie this pin to ground*.
25	GND	–	**Ground.** This pin is inactive–*tie this pin to ground*.
26	RLOOP	I	**Remote Loopback.** This input controls remote loopback. Setting RLOOP High enables Remote Loopback. During Remote Loopback, inline encoders and decoders are bypassed. Setting both RLOOP and LLOOP High while holding TAOS Low causes a Reset.
27	LLOOP	I	**Local Loopback.** This input controls local loopback. Setting LLOOP High enables Local Loopback Mode. Setting both RLOOP and LLOOP High while holding TAOS Low causes a Reset. Allow 32 ms to recover from Reset.
28	TAOS	I	**Transmit All Ones.** This pin controls the TAOS function. When tied High, TAOS causes the LXT317 to transmit a stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback, but can be activated simultaneously with Local Loopback.

Table 2: Unipolar Data I/O Pin Descriptions[1]

Pin #	Symbol	I/O	Description
3	TDATA	I	**Transmit Data.** Unipolar input for data to be transmitted on the twisted-pair line.
4	UBS	I	**Unipolar/Bipolar Select.** When pin 4 is held High for at least 16 TCLK cycles (equivalent to 15 successive bipolar violations), LXT317 switches to unipolar data I/O. The device immediately returns to bipolar I/O when pin 4 goes Low.
6	BPV	O	**Bipolar Violation.** Pin 6 goes High when a bipolar violation is received.
7	RDATA	O	**Receive Data.** Unipolar data output. RDATA is a Non-Return-to-Zero (NRZ) output. RDATA is stable and valid on the rising edge of RCLK.

1. Table 2 lists only those pins which are affected by the switch to unipolar data I/O.

FUNCTIONAL DESCRIPTION

NOTE

This functional description information is for design aid only

The LXT317 is a fully integrated PCM transceiver for 1.152 Mbps DECT applications. It allows full-duplex transmission of digital data over existing twisted-pair installations.

Table 1 lists the LXT317 pin assignments and signal descriptions. Table 2 lists the alternative pin assignments for unipolar data I/O mode. The LXT317 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

The figure on the front of this Data Sheet shows a block diagram of the LXT317. Individual hard-wired pins control the transceiver. It can operate in either a bipolar (default) or unipolar data transmission mode. The LXT317 can also operate in one of several diagnostic modes, including Local Loopback, Remote Loopback and Transmit All Ones (TAOS).

TRANSMITTER

Input data (bipolar or unipolar) for transmission onto the line is clocked serially into the LXT317. The bipolar data inputs are at pin 3 (TPOS) and pin 4 (TNEG). The unipolar data input is at pin 3 (TDATA) only. Input data passes through the HDB3 encoder, if selected by connecting the MODE pin to RCLK. Input synchronization is supplied by the transmit clock (TCLK). Refer to the Test Specifications section for transmit timing.

Idle Mode

The LXT317 incorporates a transmit idle mode. This allows multiple transceivers to be connected to a single line for redundant applications or for testing purposes. TTIP and TRING remain in a high impedance state when TCLK is not present (TCLK grounded). Enabling Remote Loopback temporarily disables the high impedance state.

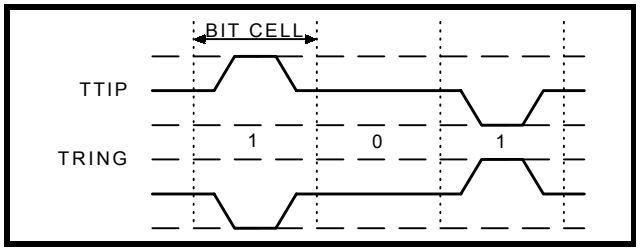
Short Circuit Limit

The LXT317 transmitter is equipped with a short-circuit limiter. This feature limits to approximately 120 mA RMS the current the transmitter will source into a low-impedance load. The limiter trips when the RMS current exceeds the limit for 120 µs (~ 150 marks). It automatically resets when the load current drops below the limit.

Line Code

The LXT317 transmits data as a 50% AMI line code as shown in Figure 2. Biasing of the transmit DC level is on-chip. Shaped pulses meeting the DECT requirements are applied to the AMI line driver for transmission onto the line at TTIP/TRING. The pulse conforms to the mask defined in ITU G.703, with the time scale expanded by a factor of $^{16}/_{9}$ for a nominal pulse width of 434 ns. Refer to Figure 11 and Table 8 for 1.152 Mbps pulse mask specifications.

Figure 2: 50% Duty Cycle Transmit Pulse



RECEIVER

The input from the twisted-pair is received via a 1:1 transformer. Recovered data is output at RPOS/RNEG (RDATA in unipolar mode), and the recovered clock is output at RCLK. Refer to the Test Specifications section for receiver timing.

The signal received at RTIP and RRING is processed through the receive equalizer which may apply up to 43 dB of gain. Insertion loss of the line, as indicated by the receive equalizer setting, is encoded in the LATN output as shown in Figure 5.

The equalized signal is filtered and applied to the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. Fifty percent of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 43 dB of cable attenuation (from 2.7 V).

After processing through the data slicers, the received signal is routed to the data and timing recovery section, then to the HDB3 decoder (if selected) and to the LOS processor. The data and timing recovery sections provide an input jitter tolerance significantly better than required by ITU G.823, as shown in the Test Specifications section. The Test Specifications section also includes the jitter tolerance template.

If the incoming bit stream has jitter, the jitter transfer limit for the LXT317 is less than 1 dB up to 25 kHz; it then decreases by 20 dB per decade from 25 kHz to 100 kHz (using a 2^{15} -1 bit, PRBS signal). Refer to Figure 15 for the jitter transfer template.

The LOS processor loads a digital counter at the RCLK frequency. The count is incremented each time a 0 (space) is received, and reset to 0 each time a 1 (mark) is received. Upon receipt of 175 consecutive 0s the LOS pin goes High, and a smooth transition replaces the RCLK output with the MCLK.

Received marks will be output regardless of the LOS status, but the LOS pin will not reset until the 1s density reaches 12.5% (receipt of at least four 1s in any 32-bit periods, with no more than 15 consecutive 0s).

SELECTING UNIPOLAR OR BIPOLAR DATA MODE

The LXT317 operates in Bipolar Data mode by default. To enable Unipolar Mode, hold pin 4 High for 16 TCLK cycles. To return to Bipolar Mode immediately, pull pin 4 Low. To enable the HDB3 encoder/decoder circuits, connect pin 5 to RCLK.

INITIALIZATION AND RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to lock the transmit and receive Phase Lock Loops. The transmitter reference is provided by TCLK; the receive reference is provided by MCLK. All PLLs are continuously calibrated.

Command reset by holding RLOOP and LLOOP High simultaneously for 200 ns while holding TAOS Low. When the reset conditions end, the device begins the 32 ms cycle to calibrate the transmit and receive PLLs.

DIAGNOSTIC MODE OPERATION

Transmit All Ones. See Figure 3. In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored and the transceiver transmits a continuous stream of 1s at the TCLK frequency. If there is no TCLK provided, TAOS is locked to the MCLK. This can be used as the AIS Alarm Indicator (AIS also called the Blue Alarm). Command TAOS by setting pin 28 High. TAOS can be commanded simultaneously with LLOOP as shown in Figure 4, but is inhibited during Remote Loopback.

Figure 3: Transmit All Ones

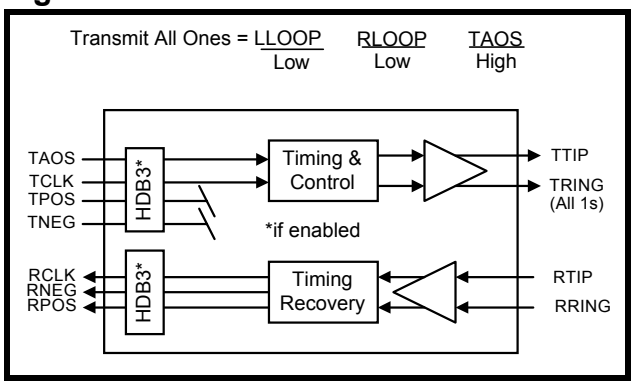


Figure 4: TAOS with LLOOP Data Path

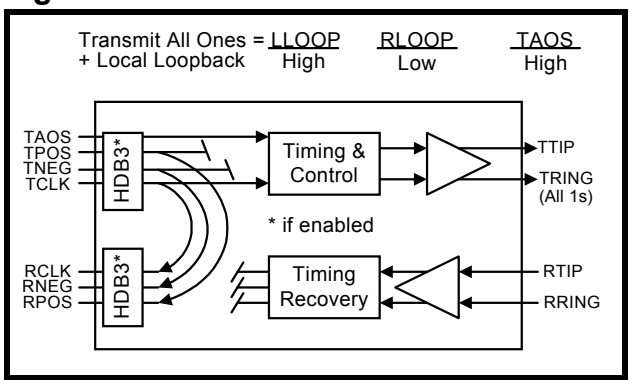
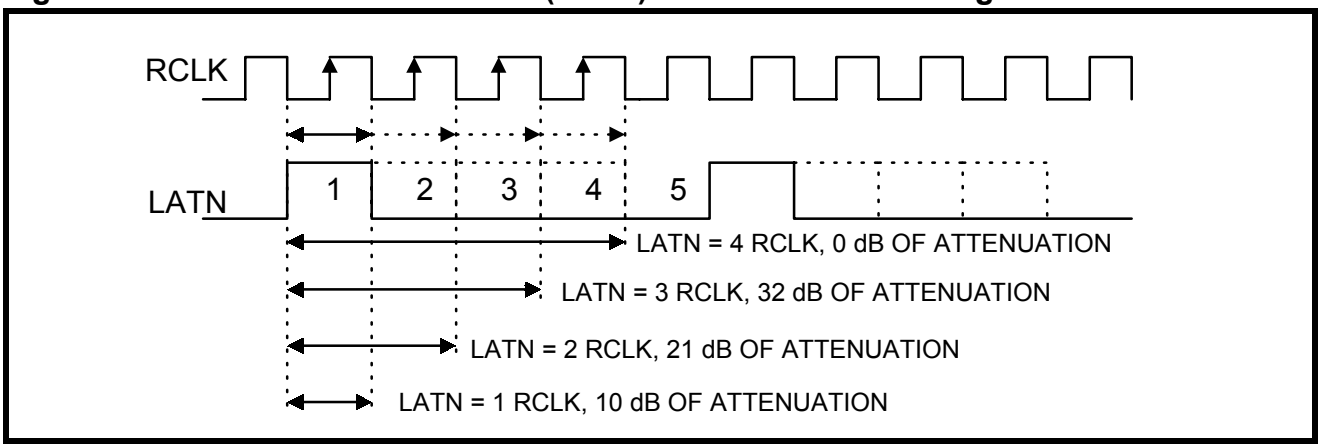


Figure 5: LXT317 Line Attenuation (LATN) Pulse Width Encoding



Local Loopback. Local Loopback (LLOOP) is designed to exercise the maximum number of functional blocks (See Figure 7). During LLOOP operation, the RTIP/RRING inputs from the line are disconnected. Instead, the transmit outputs are routed back into the receive inputs. This tests the encoders/decoders, transmitter, receiver and timing recovery sections. Enable Local Loopback by setting pin 27 High. If TAOS and LLOOP are both active, the All Ones pattern is transmitted onto the line while the TPOS/TNEG input data loops back to the RPOS/RNEG outputs.

Remote Loopback. See Figure 7. In Remote Loopback (RLOOP) mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are ignored, and the in-line encoders and decoders are bypassed. The RPOS/RNEG or RDATA outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RCLK and RPOS/RNEG or RDATA signals received from the twisted-pair line. Command Remote Loopback by setting pin 26 High.

Figure 6: Local Loopback

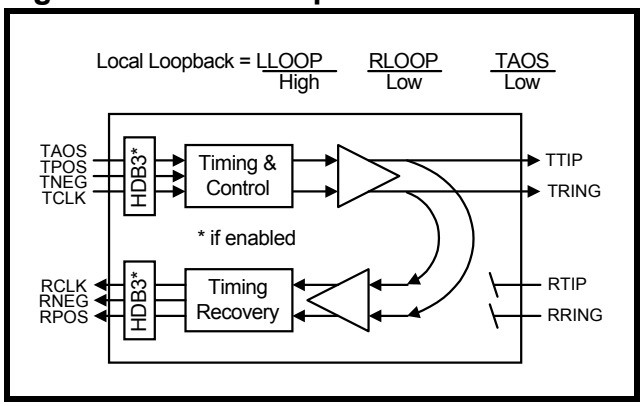
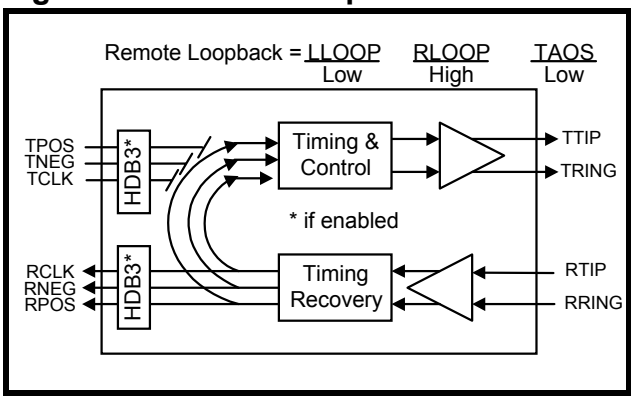


Figure 7: Remote Loopback



APPLICATION INFORMATION

NOTE

This application information is for design aid only.

LATN DECODING CIRCUITS AND EXTERNAL COMPONENTS

The line attenuation (LATN) output is encoded as a simple serial bit stream for use in line monitoring applications. Figure 8 is a typical decoding circuit for the LATN output. It uses a 2-bit synchronous counter (half of a 4-bit counter) with synchronous reset, and a pair of flip-flops. Table 3 provides the decoded output for each equalizer setting.

Figure 8: Typical LATN Decoding Circuit

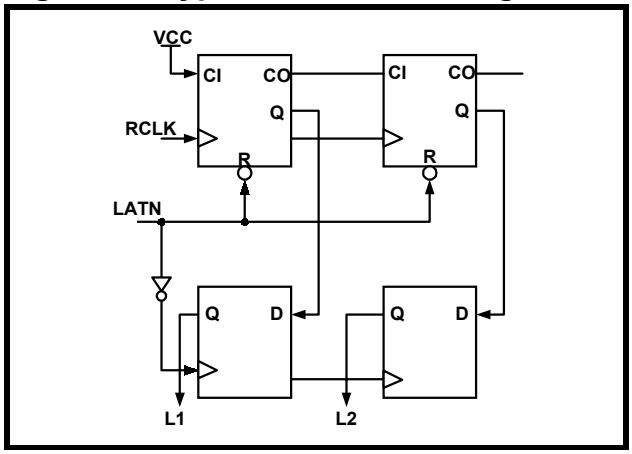


Table 3: Line Attenuation Decoding

L2	L1	Line Attenuation
0	0	0.0 dB
0	1	-10 dB
1	0	-21 dB
1	1	-32 dB

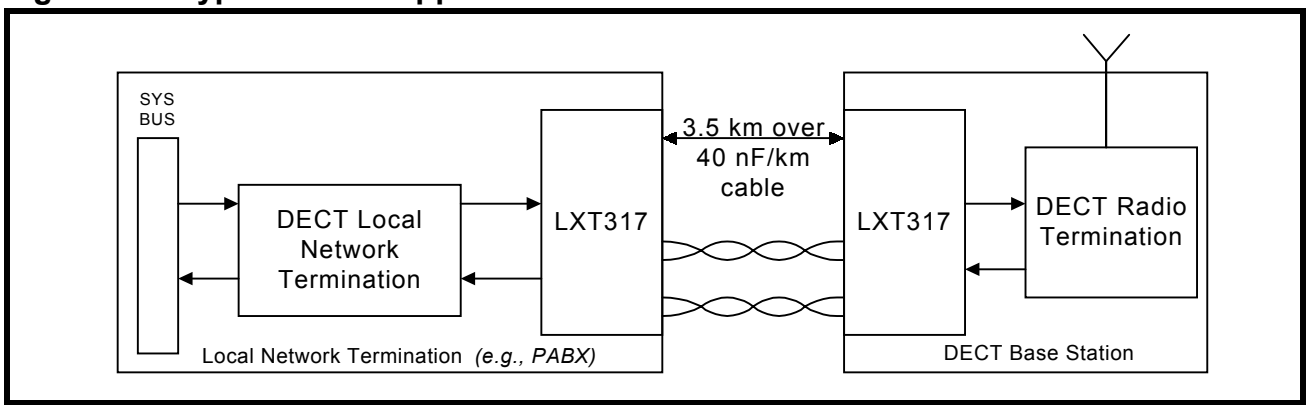
POWER REQUIREMENTS

The LXT317 is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3 V of each other, and decoupled separately to their respective grounds, as shown in Figure 10. Isolation between the transmit and receive circuits is provided internally.

Table 4: Approved Transformers

Transformer Type	Manufacturer	Part Number
Transmit (1:2)	Bell Fuse	0553-50061C
	Fil-Mag	66Z1308
	Midcom	671-5832
	Pulse	PE 65351
	Engineering	PE65771
	Schott	67127370
	Corp	67130850
Receive (1:1)	Fil-Mag	FE 8006-155
	Midcom	671-5792
	Pulse	PE 64936
	Engineering	PE 65778
	Schott	67130840
	Corp	67109510
Combination (Tx & Rx)	HALO	TD61-1205D2
	VALOR	PT5083

Figure 9: Typical DECT Application

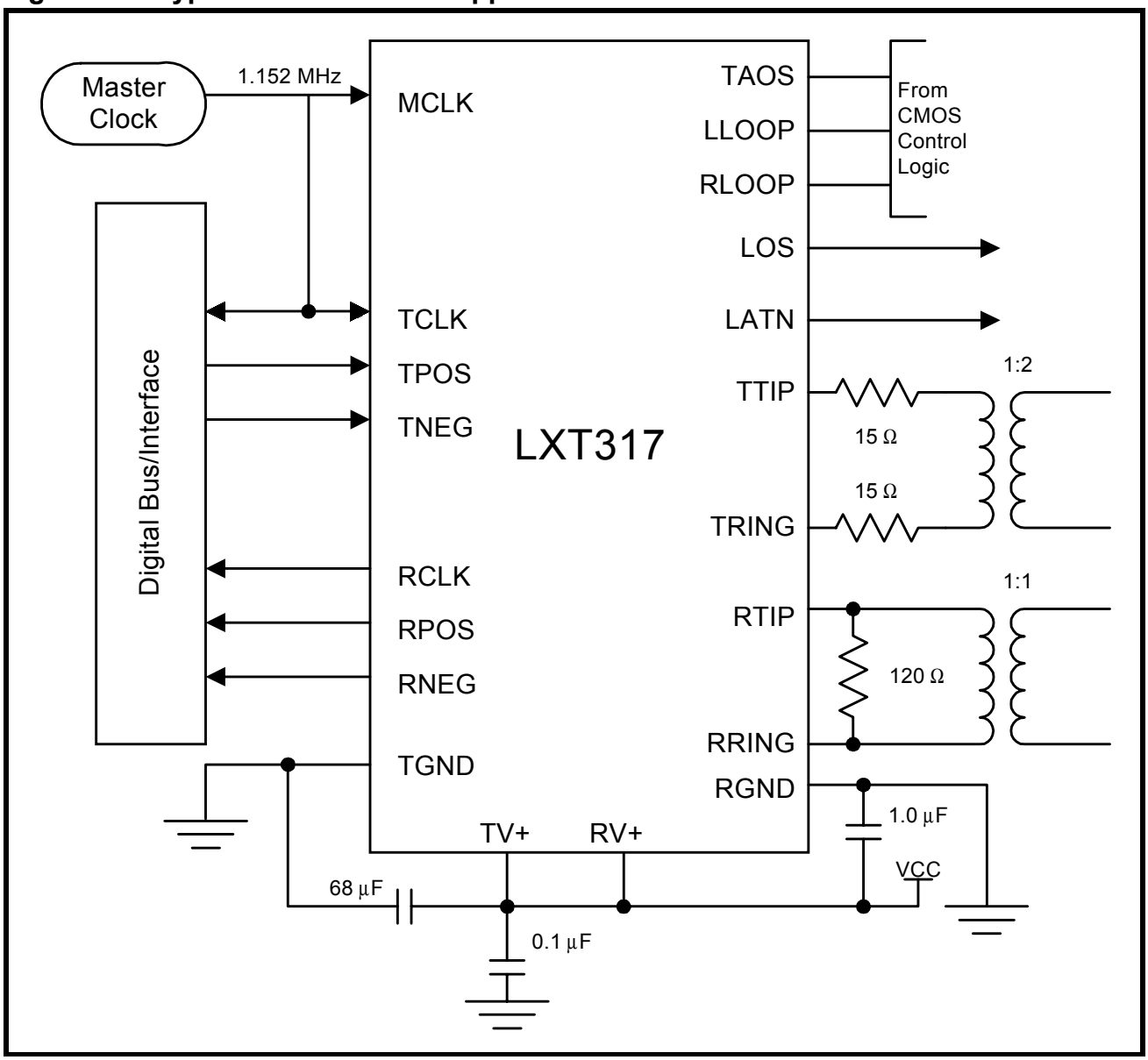


LXT317 CIRCUITRY

Figure 9 shows a typical DECT application with the LXT317. Figure 10 shows typical LXT317 circuit connections. The power supply inputs are tied to a common bus with appropriate decoupling capacitors (68 µF and 1.0 µF) installed on each side.

The line interfaces are relatively simple. A 120 Ω resistor (for TWP applications) across the input of a 1:1 transformer is used on the receive side, and a pair of 15 Ω resistors are installed in series with the 1:2 transmit transformer. (Table 4 lists approved transformers.)

Figure 10: Typical LXT317 DECT Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 5 through 11 and Figures 11 through 15 represent the performance specifications of the LXT317 and are not guaranteed by test, except where noted by design.

Table 5: Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
DC supply (referenced to GND)	RV+, TV+	–	6.0	V
Input voltage, any pin	V_{IN}	RGND, -0.3	RV+, +0.3	V
Input current, any pin [1]	I_{IN}	-10	10	mA
Ambient operating temperature	T_A	-40	85	° C
Storage temperature	T_{STG}	-65	150	° C

CAUTION
Operation at or beyond these limits may permanently damage the device.
Normal operation is not guaranteed at these extremes.

1. Transient Currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+, TGND can withstand continuous current of 100 mA.

Table 6: Recommended Operating Conditions and Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
DC supply[2]	RV+, TV+	4.75	5.0	5.25	V	
Ambient operating temperature	T_A	-40	–	+85	°C	
Power dissipation[3]	P_D	–	300	400	mW	100% ones density & maximum line length @ 5.25 V

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TV+ must not differ from RV+ by more than 0.3 V.
3. Power dissipation while driving 25 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

Table 7: Digital Characteristics (over the Recommended Range)

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
High level input voltage (pins 1-5, 10, 26-28)	V_{IH}	2.0	–	–	V	
Low level input voltage (pins 1-5, 10, 26-28)	V_{IL}	–	–	0.8	V	
High level output voltage[1] (pins 6-8, 12)	V_{OH}	3.8	–	–	V	I_{OUT} = -400 µA
Low level output voltage[1] (pins 6-8, 12)	V_{OL}	–	–	0.4	V	I_{OUT} = 1.6 mA
Input leakage current	I_{LL}	0	–	±10	µA	
Driver power down current[2]	I_{PD}	–	–	±1.2	mA	direct connection to V_{CC} or GND

1. Output drivers will output CMOS logic levels into CMOS loads.
2. TTIP.TRING only in Idle or Power Down Mode.

Figure 11: 1.152 MHz Pulse Mask

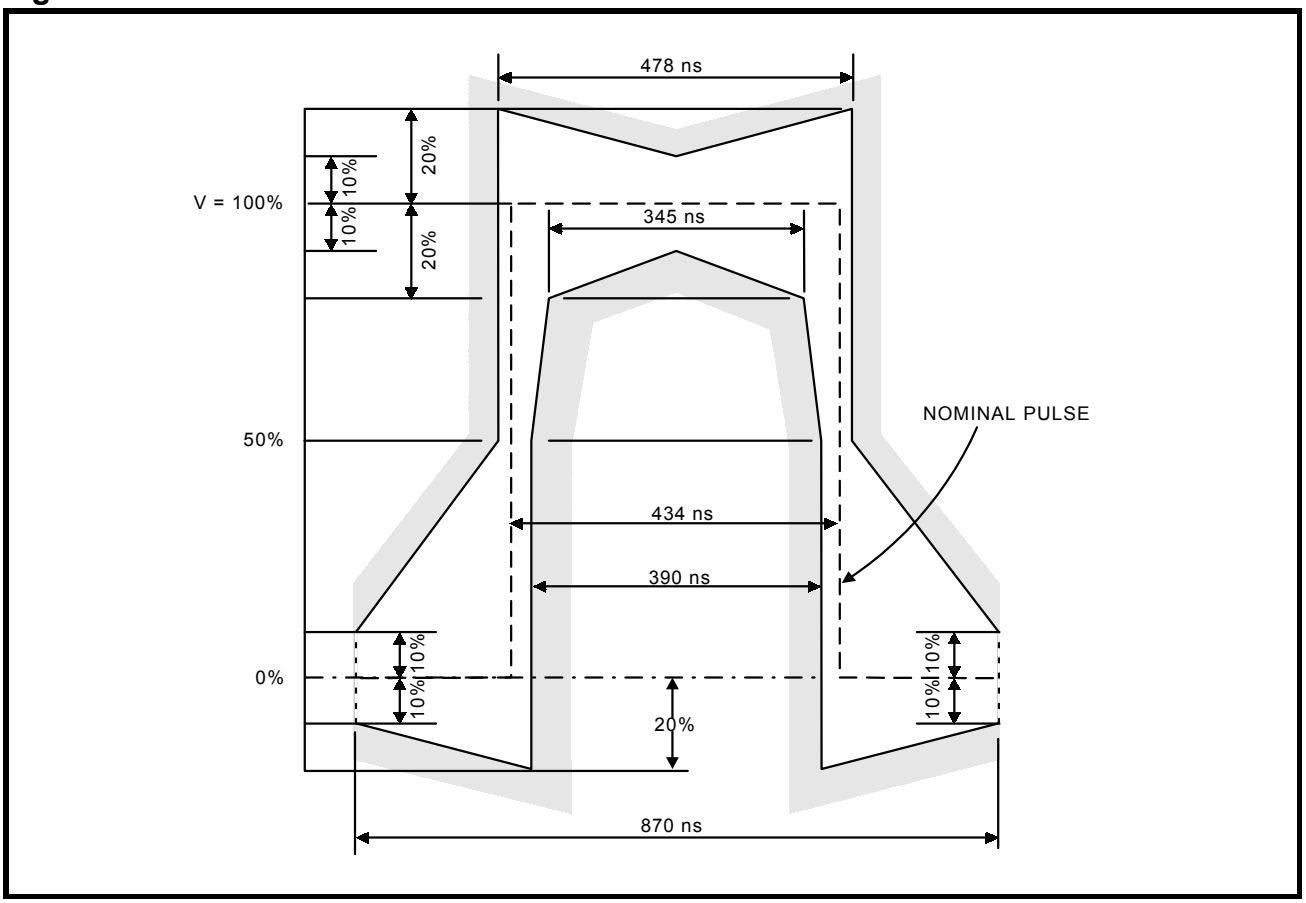


Table 8: 1.152 MHz Pulse Mask Parameters

Parameter	TPW	Units
Test load impedance	120	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ± 0.30	V
Nominal pulse width	434	ns
Ratio of positive and negative pulse amplitude at center of pulse	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	%

Table 9: Analog Characteristics (over the Recommended Range)

Parameter		Min	Typ[1]	Max	Units	Test Conditions
Recommended output load at TTIP and TRING		50	120	200	Ω	
AMI output pulse amplitudes		2.7	3.0	3.3	V	Measured at the output
Jitter added by the transmitter[2]	20 Hz - 100 kHz	–	–	0.05	UI (pp)	
Input jitter tolerance	20 kHz - 100 kHz	0.2	0.3	–	UI	0 - 43 dB line
	10 Hz	100	500	–	UI	
Round Trip Chip Data Delay[2, 3, 4]	TDATA to Transmitter	–	5.5	–	bits	
	Receiver to RDATA	–	7.0	–	bits	
Receive signal attenuation range @ 576 kHz		+1	-43.0	–	dB	
Allowable consecutive 0s before LOS declared		160	175	190		
Return loss[3]		**Transmit**		**Receive**		
		Min	**Typ**	**Min**	**Typ**	
	29 kHz - 58 kHz	12	15	12	15	dB
	58 kHz - 1.152 MHz	15	16	16	18	dB
	1.152 MHz - 2.304 MHz	14	18	14	18	dB

1. Typical values are at 25 °C and are for design aid only, not guaranteed and not subject to production testing.
2. Input signal to TCLK is jitter free.
3. Guaranteed by characterization; not subject to production testing.
4. Using HDB3 encoders and decoders in data path.

Table 10:LXT317 Master Clock and Transmit Timing Characteristics (See Figure 12)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
MCLK frequency	MCLK	–	1.152	–	MHz	
MCLK tolerance	MCLKt	–	–	±100	ppm	
MCLK duty cycle	MCLKd	40	–	60	%	
TCLK frequency	TCLK	–	1.152	–	MHz	
TCLK tolerance	TCLKt	–	–	±100	ppm	
TCLK duty cycle	TCLKd	10	–	90	%	
TPOS/TNEG to TCLK setup time	t_{SUT}	50	–	–	ns	
TCLK to TPOS/TNEG hold time	t_{HT}	50	–	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 12: LXT317 Transmit Clock Timing

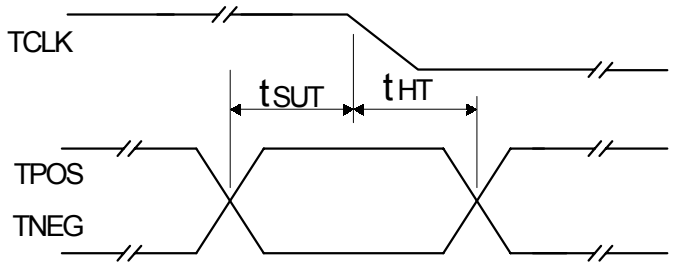


Table 11: LXT317 Receive Timing Characteristics (see Figure 13)

Parameter	Sym	Min	Typ[1]	Max	Units	Notes
RCLK duty cycle[2]	RCLKd	40	50	60	%	
RCLK width[2]	tPW	–	868	–	ns	
RCLK pulse width high	tPWH	398	434	–	ns	
RCLK pulse width low	tPWL	398	434	470	ns	
RPOS/RNEG to RCLK rising setup time	tSUR	300	384	–	ns	
RCLK rising to RPOS/RNEG hold time	tHR	300	384	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and min RCLK duty cycles are for worst case jitter conditions (0.4 UI clock displacement for 1.152 MHz.)

Figure 13: LXT317 Receive Clock Timing

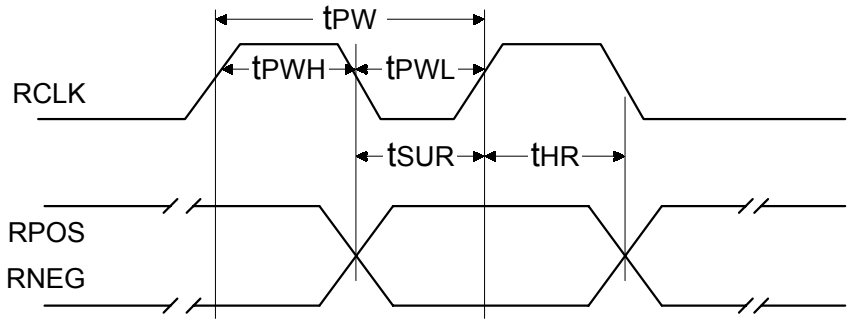


Figure 14: Typical LXT317 Jitter Tolerance @ 43 dB

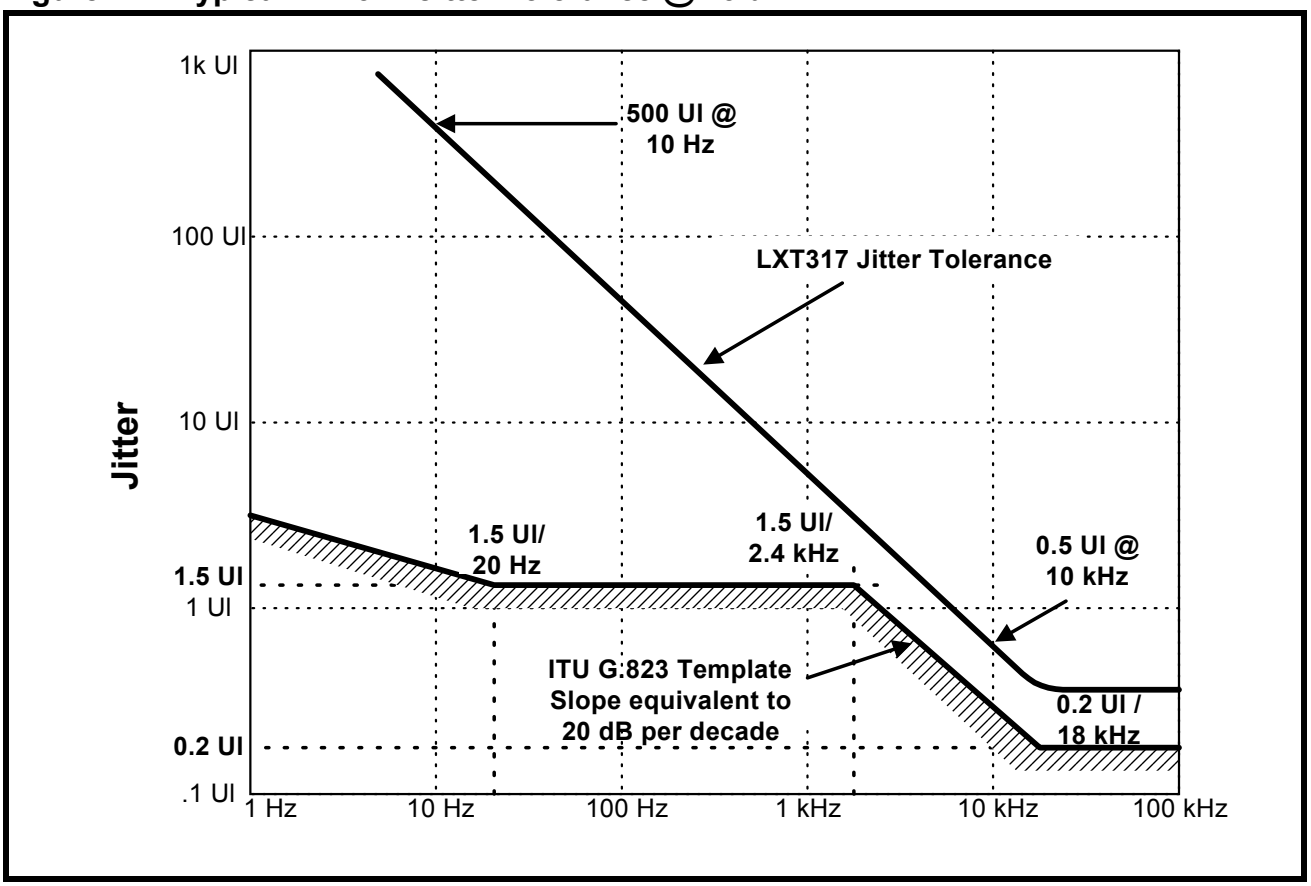
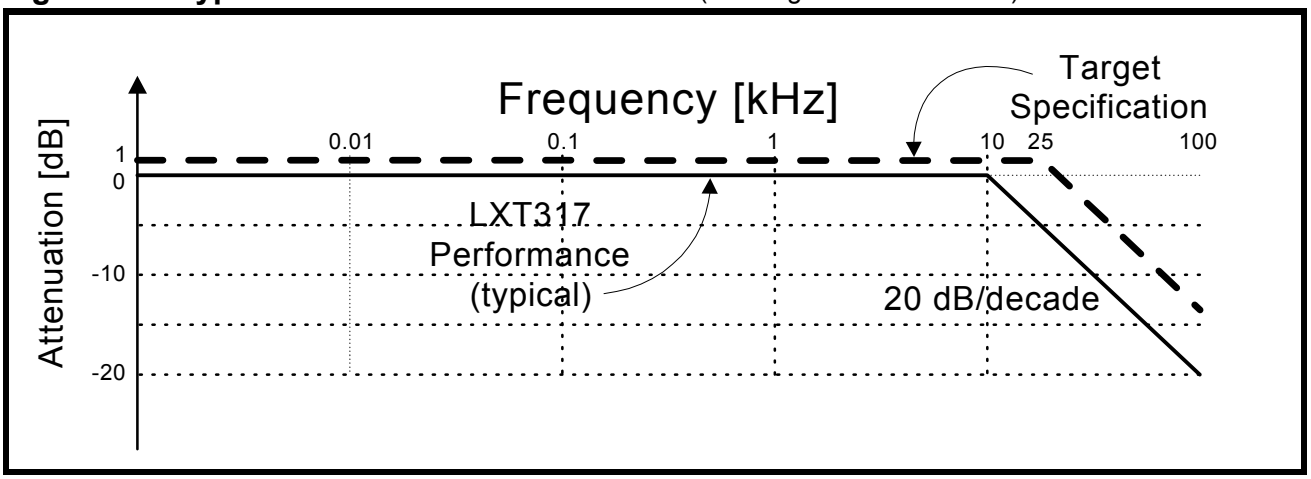


Figure 15: Typical LXT317 Jitter Attenuation (Test Signal PRBS = 2^{15}-1)



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