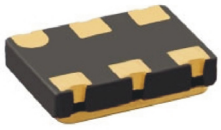
# M2001 Series

## 5x7 mm, 3.3 Volt, CMOS/LVPECL/LVDS, Clock Oscillator

- Low cost oscillator series with jitter performance optimized specifically for Fibre Channel applications. CMOS, LVPECL, and LVDS versions available.
- Ideal for Fibre Channel, Storage Area Networks (SAN), and HDD Control

**Ordering Information**

M2001 1 5 T L N 00.0000 MHz

**Product Series**

**Temperature Range**
- **1:** 0°C to +70°C
- **2:** -40°C to +85°C
- **6:** -20°C to +70°C
- **7:** 0°C to +85°C
- **8:** 0°C to +50°C

**Stability**
- **3:** ±100 ppm
- **4:** ±50 ppm
- **6:** ±25 ppm
- **5:** ±35 ppm

**Output Type**
- **F:** Fixed
- **T:** Tristate

**Symmetry/Output Logic Type**
- **C:** 45/55 CMOS
- **L:** 45/55 LVDS
- **P:** 45/55 PECL

**Package/Lead Configurations**
- **N:** Leadless Ceramic

**Frequency (customer specified)**

M2001Sxxx - Contact factory for datasheet

| | PARAMETER | Symbol | Min. | Typ. | Max. | Units | Condition/Notes |
|---|---|---|---|---|---|---|---|
| Electrical Specifications | Frequency Range | F | 53.125<br>53.125 | | 125<br>156.25 | MHz<br>MHz | CMOS<br>PECL/LVDS |
| | Operating Temperature | TA | (See ordering information) | | | | |
| | Storage Temperature | TS | -55 | | +125 | °C | |
| | Frequency Stability | ÄF/F | (See ordering information) | | | | See Note 1 |
| | Aging<br>1st Year<br>Thereafter (per year) | | | <br>±2<br>±1 | | <br>ppm<br>ppm | |
| | Input Voltage | Vcc/Vdd | 3.135 | 3.3 | 3.465 | V | |
| | Input Current | Vdd/Idd | | | 60<br>100 | mA<br>mA | CMOS/LVDS<br>PECL |
| | Output Type | | | | | | CMOS/PECL/LVDS |
| | Load | | 15 pF<br>50 Ohms to Vcc-2 VDC<br>100 Ohms differential load | | | | CMOS (See Note 2)<br>PECL (See Note 3)<br>LVDS (See Note 4) |
| | Symmetry (Duty Cycle) | | 45<br>45<br>45 | 50<br>50<br>50 | 55<br>55<br>55 | %<br>%<br>% | 50% Vdd (CMOS)<br>Vcc-1.3 VDC (PECL)<br>1.25 VDC (LVDS) |
| | Output Skew | | | | 200 | ps | PECL |
| | Differential Voltage | Vo | 250 | 340 | 450 | mV | LVDS |
| | Logic "1" Level | Voh | 90% Vdd<br>Vcc –1.02<br>1.375 | | | V<br>V<br>V | CMOS<br>PECL<br>LVDS |
| | Logic "0" Level | Vol | | | 10% Vdd<br>Vcc-1.63<br>1.125 | V<br>V | CMOS<br>PECL<br>LVDS |
| | Output Current | | -4 | | +4 | mA | CMOS |
| | Rise/Fall Time | Tr/Tf | | <br>0.35<br>.50 | 3<br>0.55<br>1.0 | ns<br>ns<br>ns | CMOS @20/80%<br>LVPECL @ 20/80%<br>LVDS @ 20/80% |
| | Tristate Function | | 80% Vdd min or floating: output active<br>20% Vdd max: output disables to high-Z | | | | |
| | Start up Time | | | | 10 | ms | |
| | Peak to Peak Jitter (+/-) | Tj | | <br>10<br>15 | <br>15<br>20 | <br>ps<br>ps | @ BER 1E-12 (See Note 5)<br>CMOS<br>PECL/LVDS |
| Environmental | Mechanical Shock | Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave) | | | | | |
| | Vibration | Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz) | | | | | |
| | Hermeticity | Per MIL-STD-202, Method 112, ($1x10^{-8}$ atm. cc/s of Helium) | | | | | |
| | Thermal Cycle | Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles) | | | | | |
| | Solderability | Per EIAJ-STD-002 | | | | | |
| | Max Soldering Conditions | See solder profile, Figure 1 | | | | | |

1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage and aging.
2. See Load circuit diagram #2.
3. See Load circuit diagram #5.
4. See Load circuit diagram #9.
5. See jitter test circuit in Figure 1.

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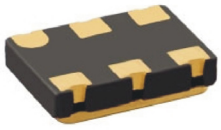
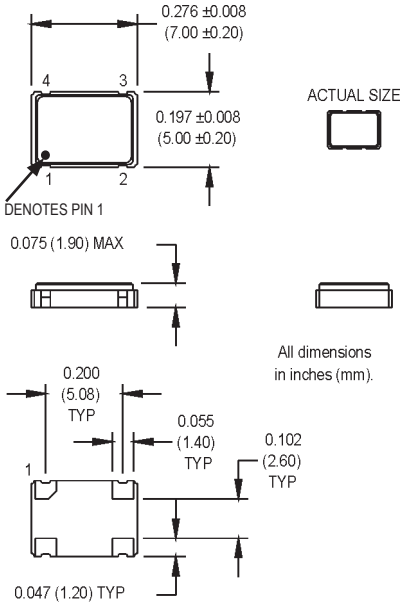
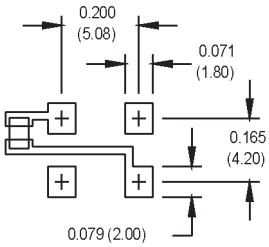


RoHS Compliant

### CMOS Output



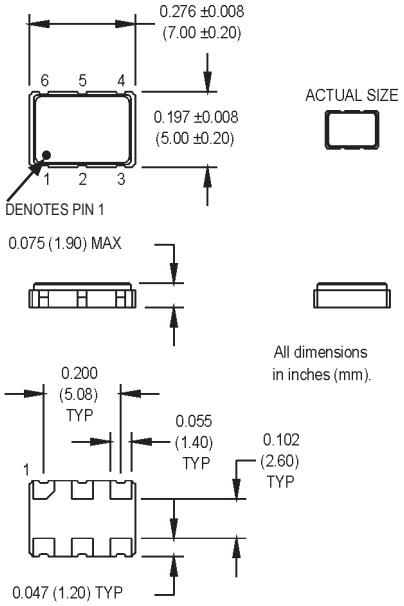

SUGGESTED SOLDER PAD LAYOUT




**Pin Connections**

| PIN | FUNCTION |
|---|---|
| 1 | Tristate/NC |
| 2 | Ground |
| 3 | Output |
| 4 | +Vdd |

### LVPECL/LVDS Output

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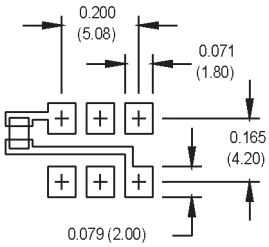
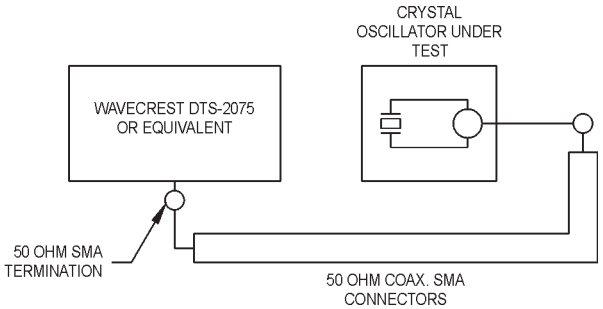



**Pin Connections**

| PIN | FUNCTION |
|---|---|
| 1 | Tristate |
| 2 | N/C |
| 3 | Ground |
| 4 | Output1/ Q |
| 5 | Output2/ $\overline{Q}$ |
| 6 | +Vdd |

**Figure 1**



# MtronPTI Lead Free Solder Profile