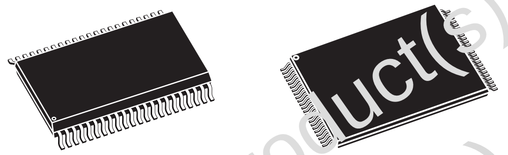
M27V320

32 Mbit (4Mb x8 or 2Mb x16) OTP EPROM

- 3.3V ± 10% SUPPLY VOLTAGE in READ OPERATION
- ACCESS TIME: 100ns
- BYTE-WIDE or WORD-WIDE CONFIGURABLE
- 32 Mbit MASK ROM REPLACEMENT
- LOW POWER CONSUMPTION
  - Active Current 30mA at 5MHz
  - Standby Current 60µA
- PROGRAMMING VOLTAGE: 12V ± 0.25V
- PROGRAMMING TIME: 50µs/word
- ELECTRONIC SIGNATURE:
  - Manufacturer Code 20h
  - Device Code: 32h



SO44 (M)

TSOP48 (N)
12 x 20 mm

DESCRIPTION

The M27V320 is a low voltage 32 Mbit EPROM offered in the OTP range (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 4 MWords of 8 bit or 2 MWords of 16 bit. The pin-out is compatible with the 32 Mbit Mask ROM.

The M27V320 is offered in SO44 and TSOP48 (12 x 20 mm) packages.

Figure 1. Logic Diagram

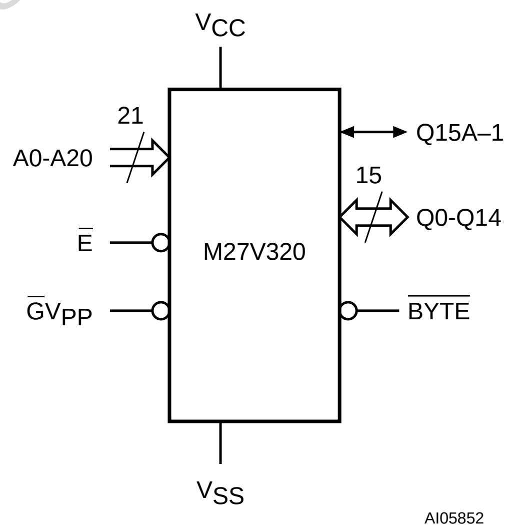


Figure 2. SO Connections

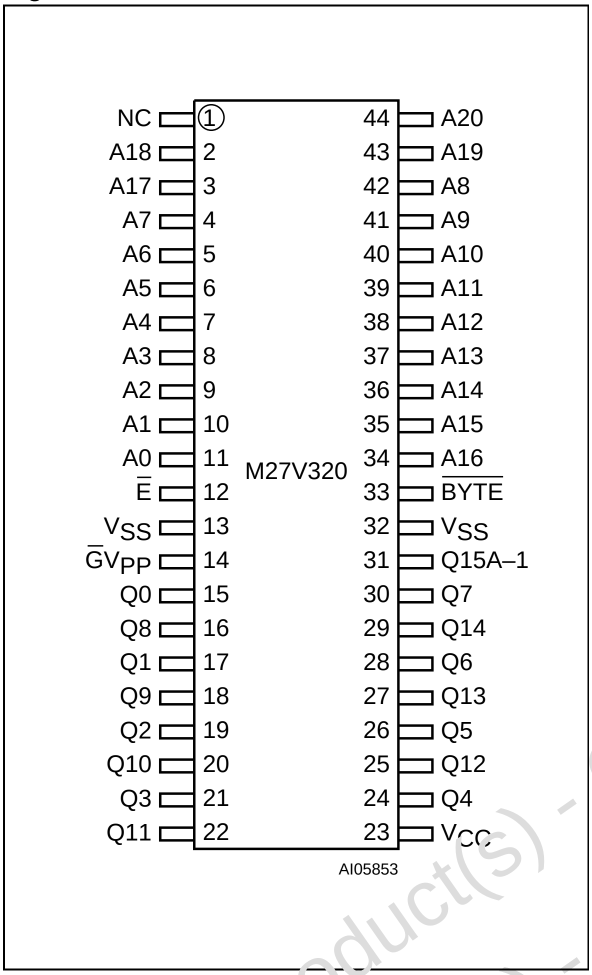


Figure 3. TSOP Connections

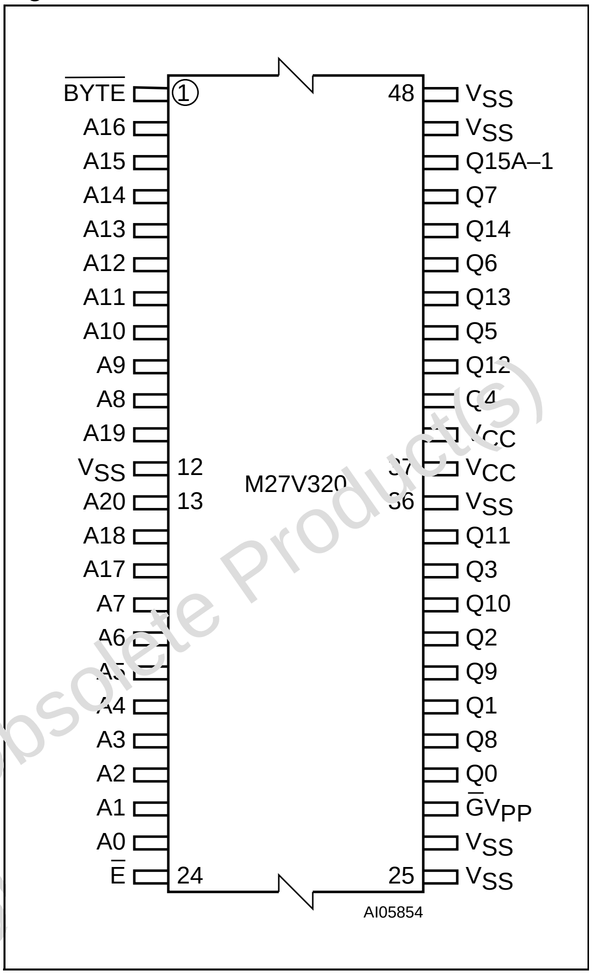


Table 1. Signal Names

A0-A20	Address Inputs
Q0-Q7	Data Outputs
Q8-Q14	Data Outputs
Q15A–1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
$\overline{BYTE}$	Byte-Wide Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

DEVICE OPERATION

The operating modes of the M27V320 are listed in the Operating Modes Table. A single power supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27V320 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}$ pin. When $\overline{BYTE}$ is at V_{IH} the Word-wide organisation is selected and the Q15A–1 pin is used for Q15 Data Output. When the $\overline{BYTE}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A–1 pin is used for the Address Input A–1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A–1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A–1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature [3]	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} [2]	Input or Output Voltage (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} [2]	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

3. Depends on range.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}V_{PP}$	$\overline{BYTE}$	A9	Q15A–1	Q14-Q8	Q7-Q0
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	Hi-Z	Data Out
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	Hi-Z	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{PP}	V_{IH}	X	Data In	Data In	Data In
Program Inhibit	V_{IH}	V_{PP}	V_{IH}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Code	Codes	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	0	1	1	0	0	1	0	32h

Note: Outputs Q15-Q8 are set to '0'.

Table 5. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 4. AC Testing Input Output Waveform

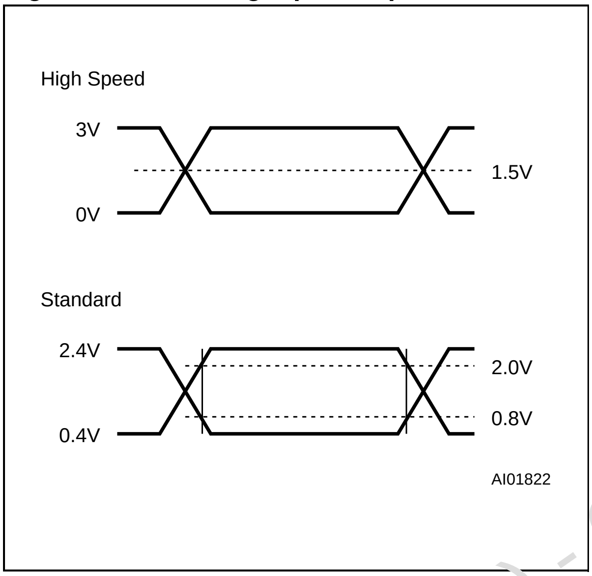


Figure 5. AC Testing Load Circuit

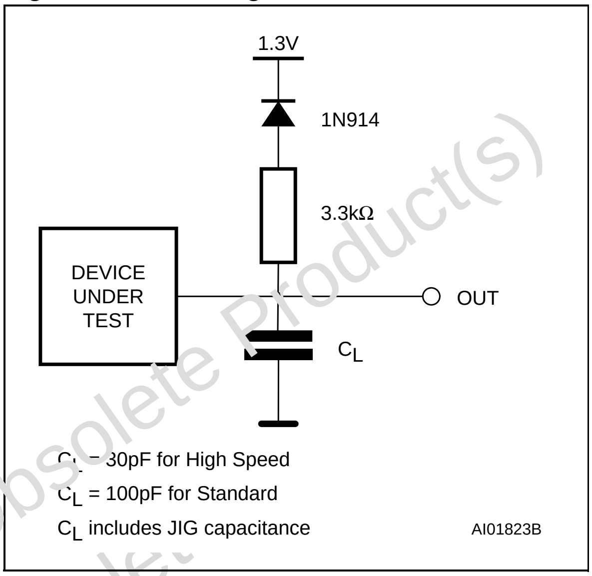


Table 6. Capacitance [(1)] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

The M27V320 has two control functions, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected.

Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}V_{PP}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}V_{PP}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27V320 has standby mode which reduces the supply current from 50mA to 100µA. The M27V320 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Table 7. Read Mode DC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 10%; V_{PP} = V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±10	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, $\overline{G}V_{PP}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz, V_{CC} ≤ 3.6V		30	mA
$I_{CC}1$	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
$I_{CC}2$	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤ 3.6V		60	µA
I_{PP}	Program Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		–0.6	0.2V_{CC}	V
V_{IH} (2)	Input High Voltage		0.7V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}V_{PP}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of $\overline{E}$.

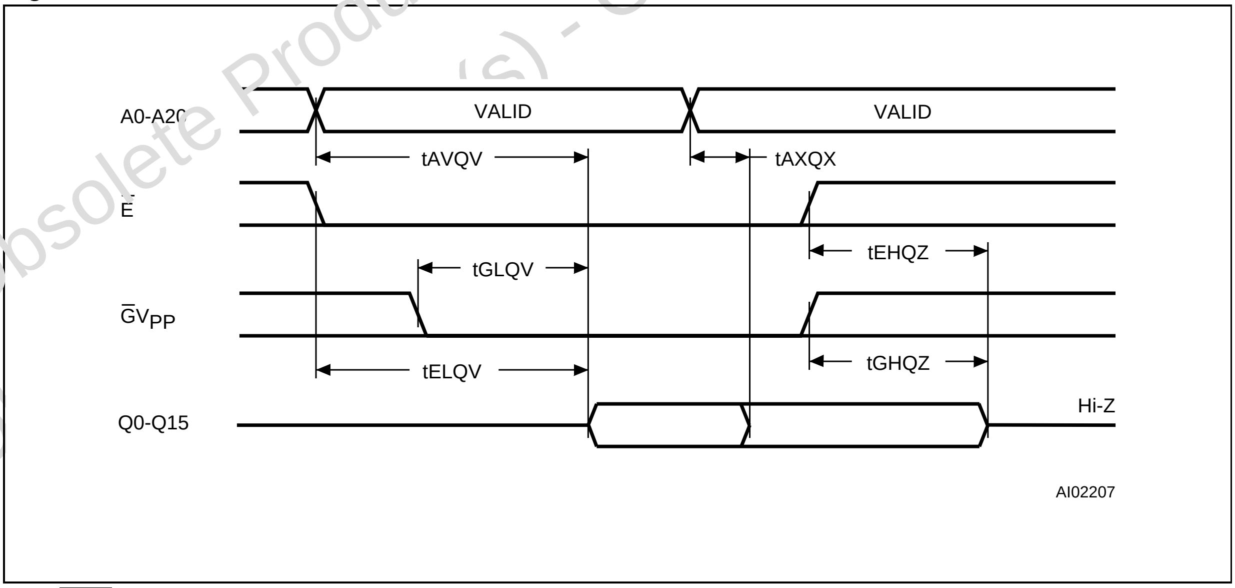
The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V_{CC} and V_{SS}. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Table 8. Read Mode AC Characteristics [1]
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 10%)

Symbol	Alt	Parameter	Test Condition	M27V320 -100 [3] Min	M27V320 -100 [3] Max	M27V320 -120 Min	M27V320 -120 Max	M27V320 -150 Min	M27V320 -150 Max	Unit
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$		100		120		150	ns
t_{BHQV}	t_{ST}	BYTE High to Output Valid	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}V_{PP} = V_{IL}$		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		45		50		60	ns
t_{BLQZ} [2]	t_{STD}	BYTE Low to Output Hi-Z	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$		45		50		50	ns
t_{EHQZ} [2]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}V_{PP} = V_{IL}$	0	45	0	50	0	50	ns
t_{GHQZ} [2]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	45	0	50	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$	5		5		5		ns
t_{BLQX}	t_{OH}	BYTE Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$	5		5		5		ns

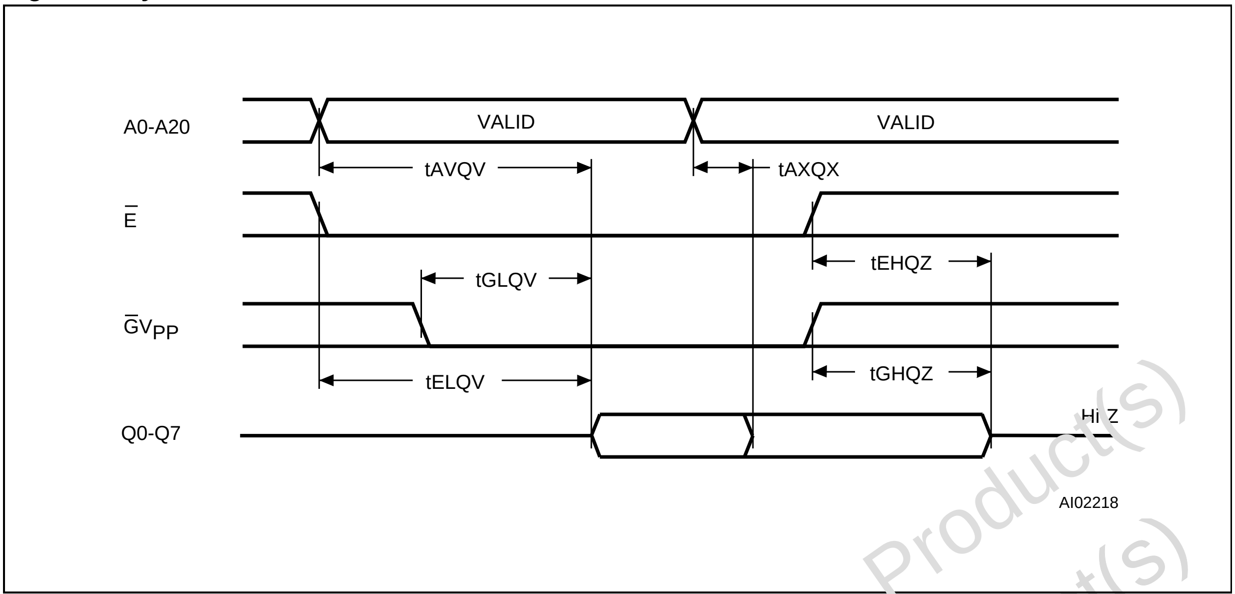
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.
3. Speed obtained with High Speed AC measurement conditions.

Figure 6. Word-Wide Read Mode AC Waveforms



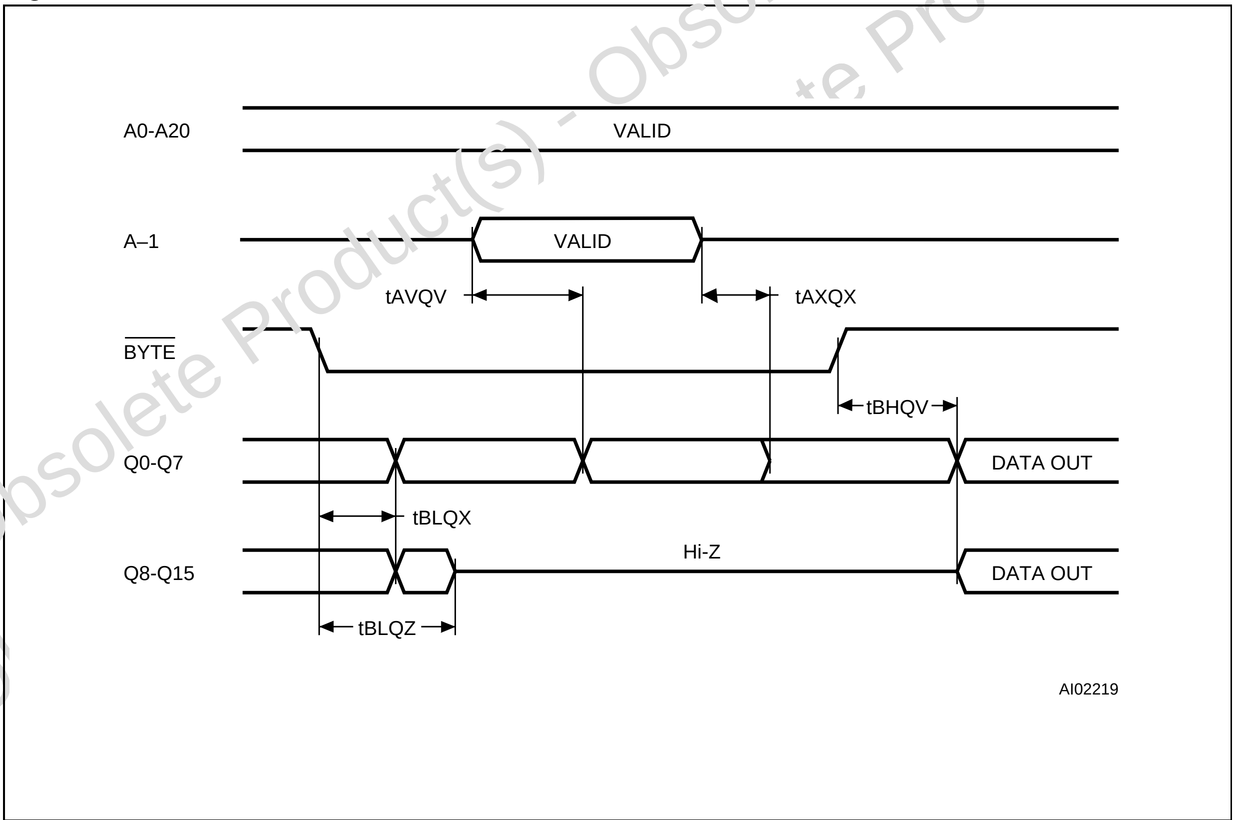
Note: $\overline{BYTE} = V_{IH}$.

Figure 7. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTE}$ = V_{IL}.

Figure 8. $\overline{BYTE}$ Transition AC Waveforms



Note: $\overline{E}$ = V_{IL}; $\overline{G}V_{PP}$ = V_{IL}.

Table 9. Programming Mode DC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. MARGIN MODE AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	V_{A9} High to V_{PP} High		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} High to Chip Enable Low		2		µs
t_{A10HEH}	t_{AS10}	V_{A10} High to Chip Enable High (Set)		1		µs
t_{A10LEH}	t_{AS10}	V_{A10} Low to Chip Enable High (Reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable Transition to V_{A10} Transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable Transition to V_{PP} Transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} Transition to V_{A9} Transition		2		µs

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Programming

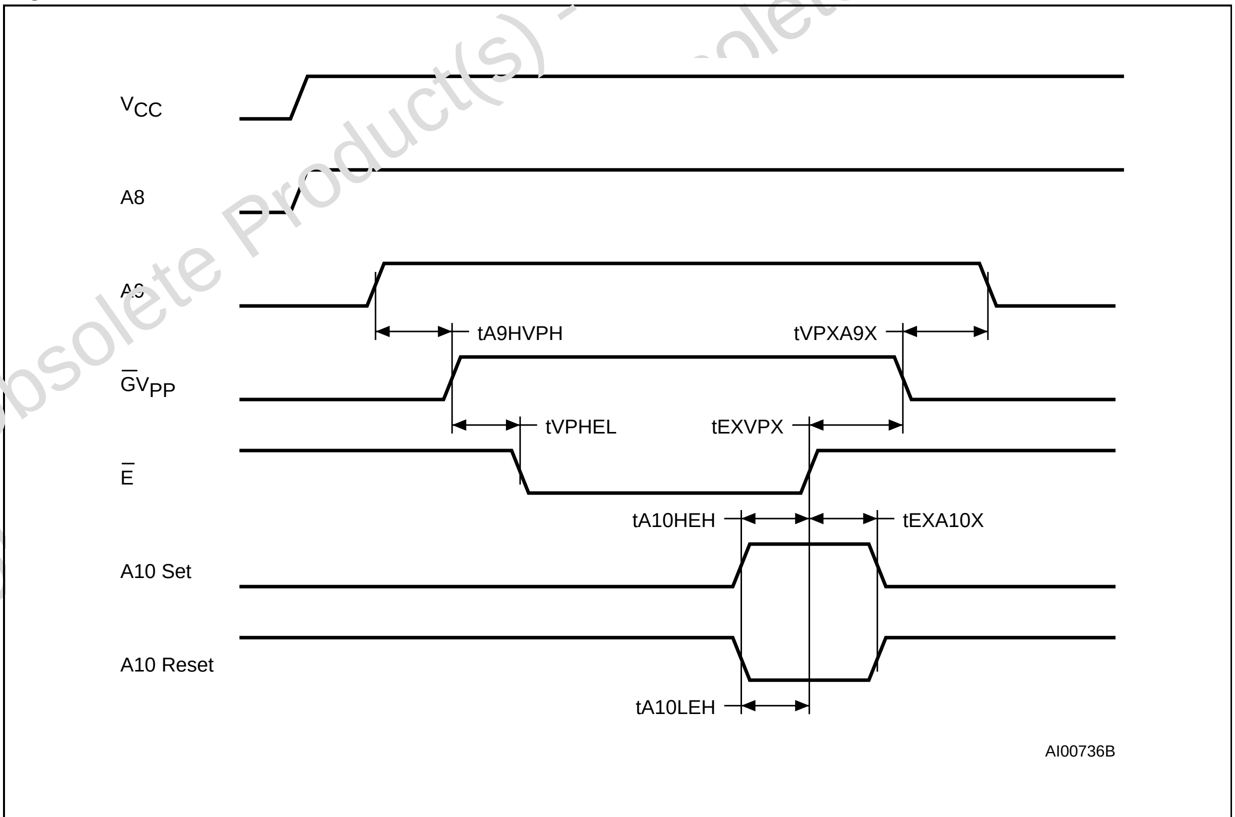
When delivered, all bits of the M27V320 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The M27V320 is in the programming mode when V_{PP} input is at 12.5V, $\overline{G}V_{PP}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Table 11. Programming Mode AC Characteristics [1]
(T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low		1		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable Low		1		µs
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} High to Chip Enable Low		1		µs
t_{VPLVPH}	t_{PRT}	V_{PP} Rise Time		50		ns
t_{ELEH}	t_{PW}	Chip Enable Program Pulse Width (Initial)		45	55	µs
t_{EHQX}	t_{DH}	Chip Enable High to Input Transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable High to V_{PP} Transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} Low to Chip Enable Low		1		µs
t_{ELQV}	t_{DV}	Chip Enable Low to Output Valid			1	µs
t_{EHQZ} [2]	t_{DFP}	Chip Enable High to Output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition		0		ns

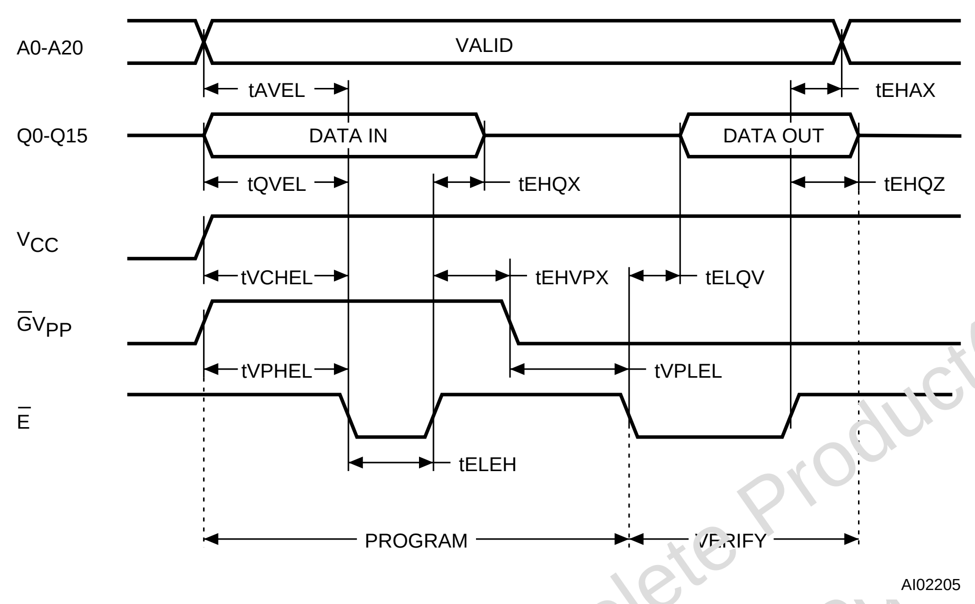
Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 9. MARGIN MODE AC Waveforms



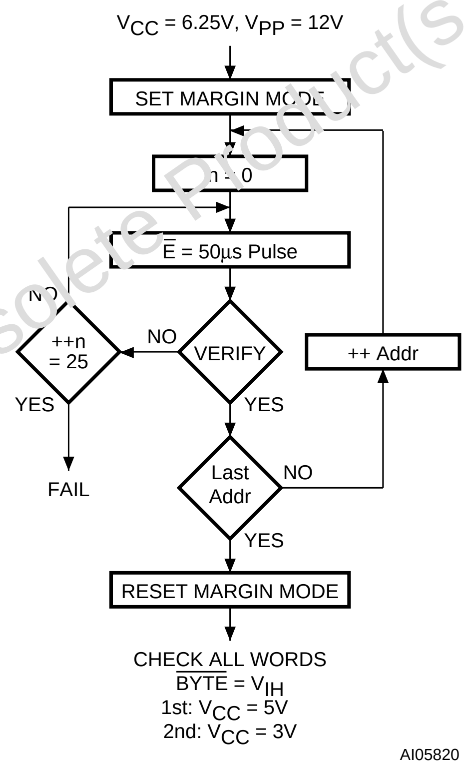
Note: A8 High level = 5V; A9 High level = 12V.

Figure 10. Programming and Verify Modes AC Waveforms



Note: $\overline{BYTE}$ = V_{IH}; $\overline{G}V_{PP}$ High level = 12V.

Figure 11. Programming Flowchart



PRESTO III Programming Algorithm

The PRESTO III Programming Algorithm allows the whole array to be programed with a guaranteed margin in a typical time of 100 seconds. Programming with PRESTO III consists of applying a sequence of 50µs program pulses to each word until a correct verify occurs (see Figure 11). During programing and verify operation a MARGIN MODE circuit must be activated to guarantee that each cell is programed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27V320s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27V320 may be common. A TTL low level pulse applied to a M27V320's $\overline{E}$ input and V_{PP} at 12V, will program that M27V320. A high level $\overline{E}$ input inhibits the other M27V320s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}V_{PP}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V320. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V320, with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the STMicroelectronics M27V320, these two identifier bytes are given in Table 4 and can be read-out on outputs Q7 to Q0.

Table 12. Ordering Information Scheme

Example: M27V320 -100 M 1

Device Type
M27

Supply Voltage
V = 3.3V ± 10%

Device Function
320 = 32 Mbit (4Mb x 8 or 2Mb x 16)

Speed
-100[(1)] = 100 ns
-120 = 120 ns
-150 = 150 ns

Package
M = SO44
N = TSOP48: 12 x 20 mm

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Note: 1. High Speed, see AC Characteristics section for further information.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

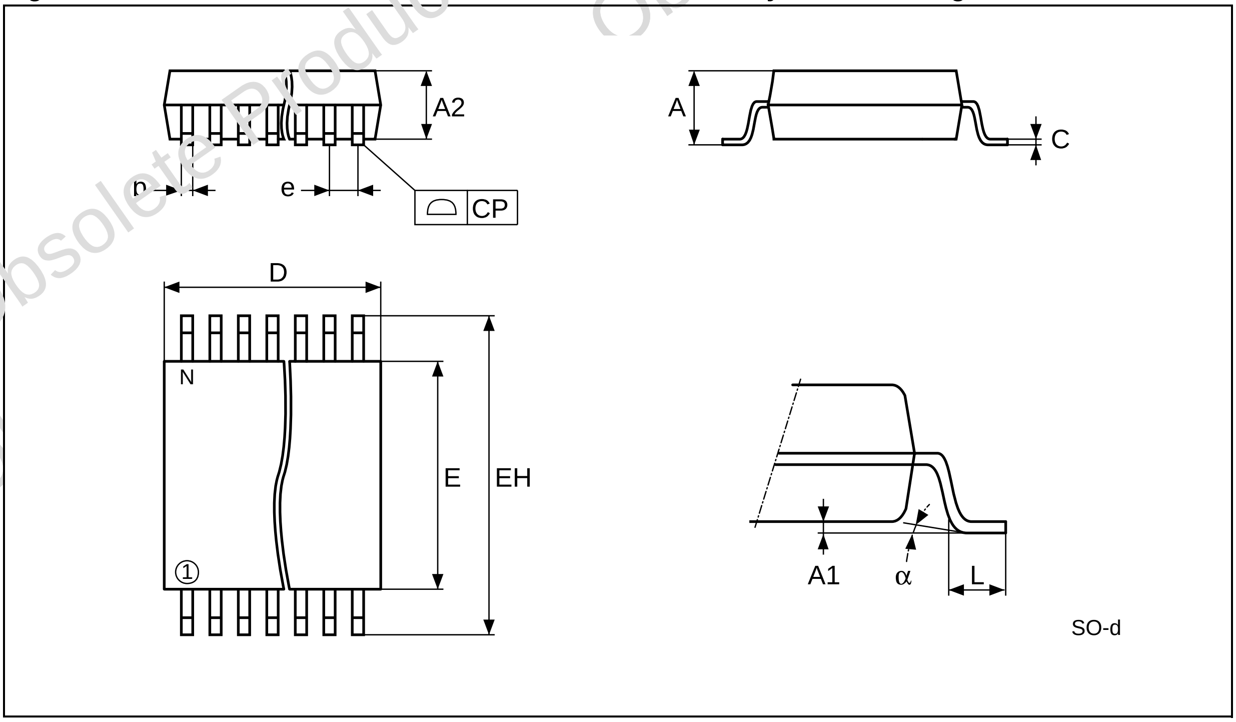
Table 13. Revision History

Date	Version	Revision Details
December 2001	1.0	First Issue
26-Aug-2002	1.1	Document status moved to Data Sheet

Table 14. SO44 - 44 lead Plastic Small Outline, 525 mils body width, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.80			0.1102
A1		0.10			0.0039	
A2	2.30	2.20	2.40	0.0906	0.0866	0.0945
b	0.40	0.35	0.50	0.0157	0.0138	0.0197
C	0.15	0.10	0.20	0.0059	0.0039	0.0079
CP			0.08			0.0030
D	28.20	28.00	28.40	1.1102	1.1024	1.1181
e	1.27	–	–	0.0500	–	–
E	13.30	13.20	13.50	0.5236	0.5197	0.5315
EH	16.00	15.75	16.25	0.6299	0.6201	0.6398
L	0.80			0.0315		
α			8°			8°
N	44			44		

Figure 12. SO44 - 44 lead Plastic Small Outline, 525 mils body width, Package Outline

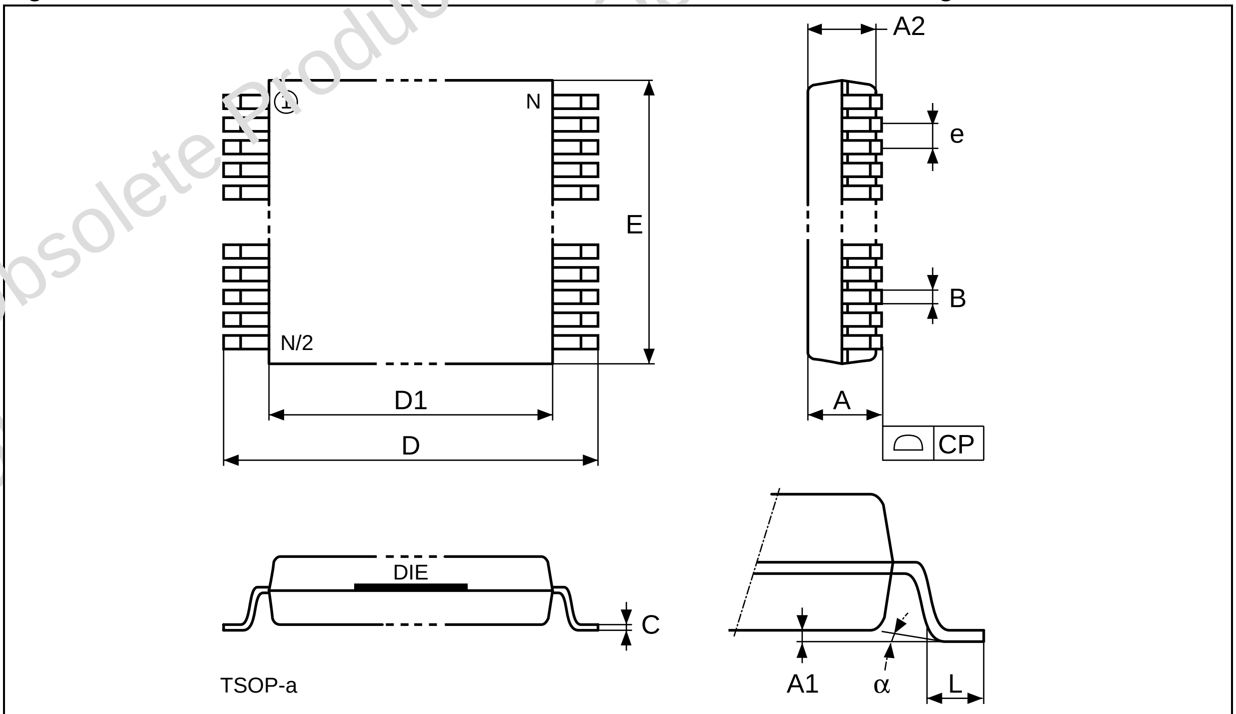


Drawing is not to scale.

Table 15. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.10			0.004
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		

Figure 13. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20 mm, Package Outline



Drawing is not to scale.

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