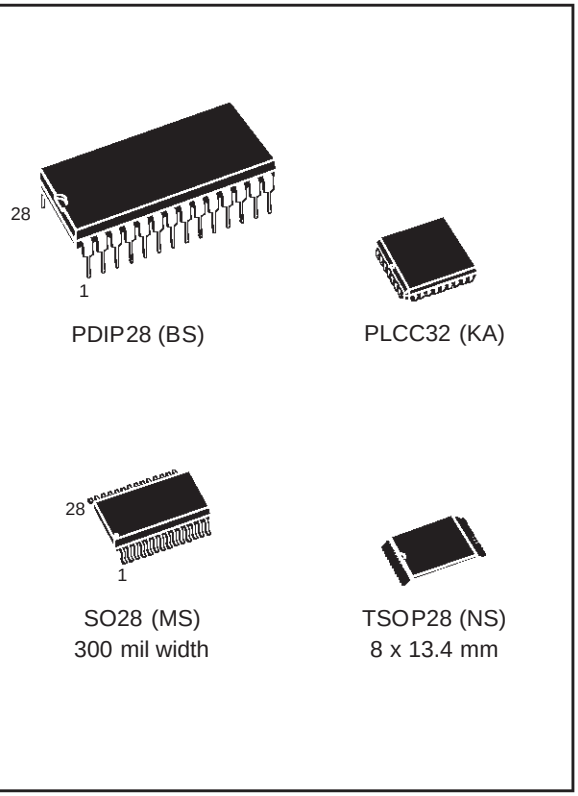
M28256

256 Kbit (32K x 8) Parallel EEPROM With Software Data Protection

NOT FOR NEW DESIGN

- Fast Access Time:
  - 90 ns at V_{CC}=5 V for M28256
  - 120 ns at V_{CC}=3 V for M28256-W
- Single Supply Voltage:
  - 4.5 V to 5.5 V for M28256
  - 2.7 V to 3.6 V for M28256-W
- Low Power Consumption
- Fast BYTE and PAGE WRITE (up to 64 Bytes)
  - 3 ms at V_{CC}=4.5 V for M28256
  - 5 ms at V_{CC}=2.7 V for M28256-W
- Enhanced Write Detection and Monitoring:
  - Data Polling
  - Toggle Bit
  - Page Load Timer Status
- JEDEC Approved Bytewide Pin-Out
- Software Data Protection
- 100,000 Erase/Write Cycles (minimum)
- 10 Year Data Retention (minimum)



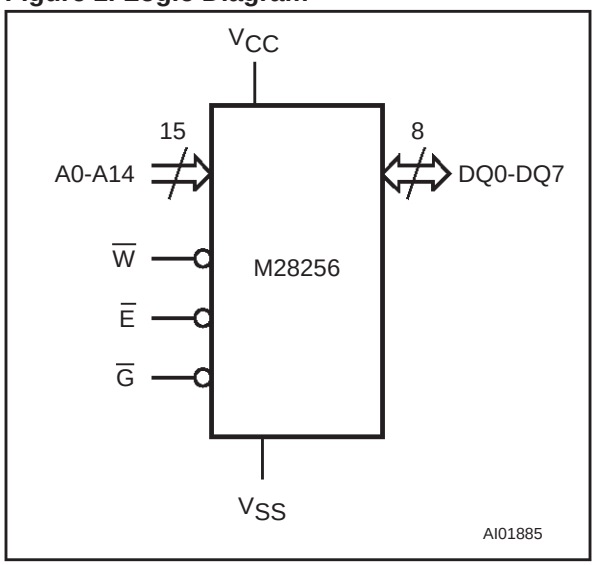
DESCRIPTION

The M28256 and M28256-W devices consist of 32K x 8 bits of low power, parallel EEPROM, fabricated with STMicroelectronics' proprietary double polysilicon CMOS technology. The devices offer fast access time, with low power dissipation,

Table 1. Signal Names

A0-A14	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is information on a product still in production but not recommended for new designs.

Figure 2A. DIP Connections

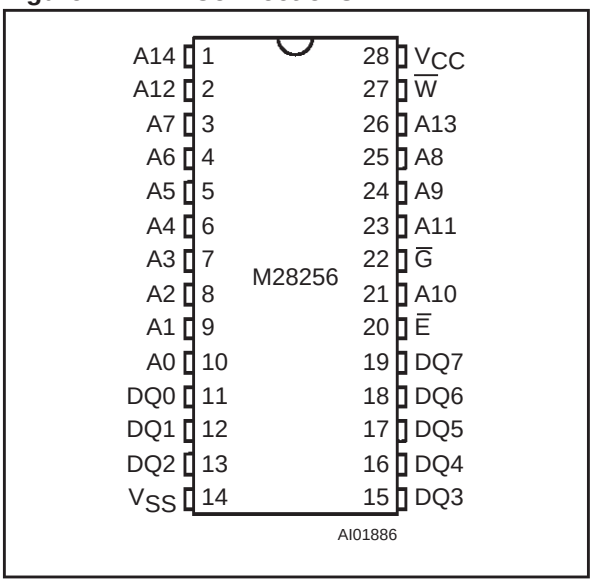
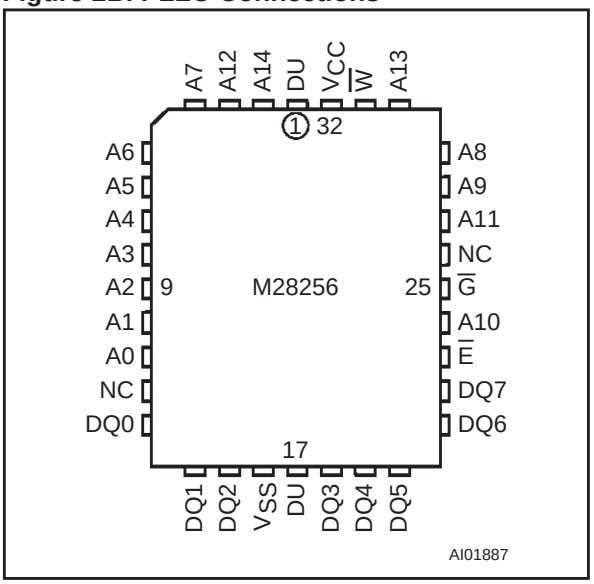


Figure 2B. PLLC Connections



Note: 1. NC = Not Connected
2. DU = Do Not Use

Figure 2C. SO Connections

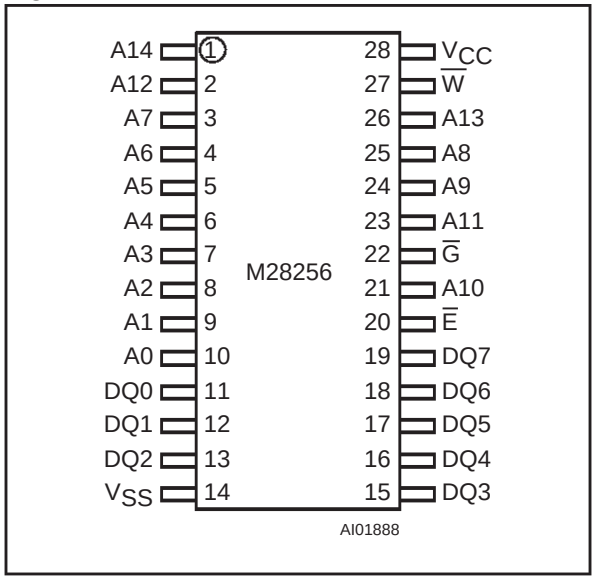
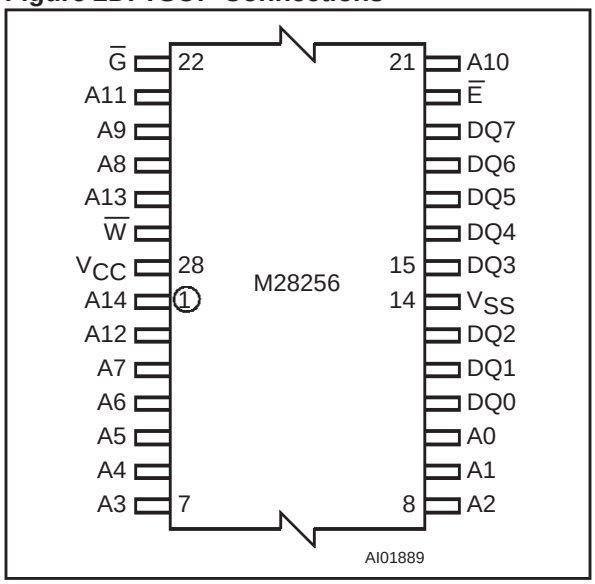


Figure 2D. TSOP Connections



and require a single voltage supply (5V or 3V, depending on the option chosen).

The device has been designed to offer a flexible microcontroller interface, featuring both hardware and software handshaking, with Ready/Busy, Data Polling and Toggle Bit. The device supports a 64 byte Page Write operation. Software Data Protection (SDP) is also supported, using the standard JEDEC algorithm.

SIGNAL DESCRIPTION

The external connections to the device are summarized in Table 1, and their use in Table 3.

Addresses (A0-A14). The address inputs are used to select one byte from the memory array during a read or write operation.

Data In/Out (DQ0-DQ7). The contents of the data byte are written to, or read from, the memory array through the Data I/O pins.

Chip Enable ($\overline{E}$). The chip enable input must be held low to enable read and write operations.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{IO}	Input or Output Voltage	–0.3 to V_{CC}+0.6	V
V_I	Input Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

Figure 3. Block Diagram

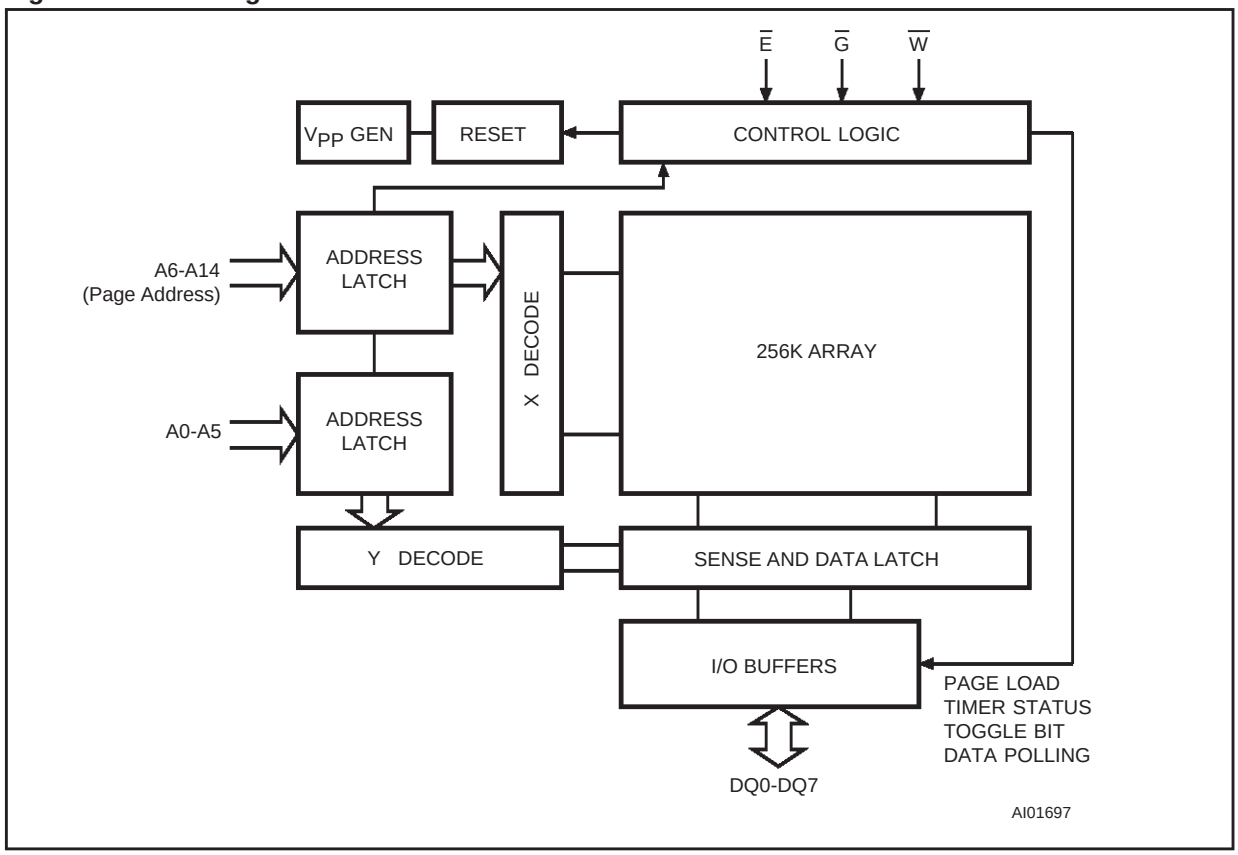


Table 3. Operating Modes [1]

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Stand-by / Write-Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: 1. X = V_{IH} or V_{IL}

When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers, and is used to initiate read operations.

Write Enable ($\overline{W}$). The Write Enable input controls whether the addressed location is to be read, from or written to.

DEVICE OPERATION

In order to prevent data corruption and inadvertent write operations, an internal V_{CC} comparator inhibits the Write operations if the V_{CC} voltage is lower than V_{WI} (see Table 4A and Table 4B). Once the voltage applied on the V_{CC} pin goes over the V_{WI} threshold (V_{CC}>V_{WI}), write access to the memory is allowed after a time-out t_{PUW}, as specified in Table 4A and Table 4B.

Further protection against data corruption is offered by the $\overline{E}$ and $\overline{W}$ low pass filters: any glitch, on the $\overline{E}$ and $\overline{W}$ inputs, with a pulse width less than 10 ns (typical) is internally filtered out to prevent inadvertent write operations to the memory.

Read

The device is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low, and $\overline{W}$ is high, the contents of the addressed location are presented on the I/O pins. Otherwise, when either $\overline{G}$ or $\overline{E}$ is high, the I/O pins revert to their high impedance state.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The device supports both $\overline{W}$-controlled and $\overline{E}$-controlled write cycles (as shown in Figure 10 and Figure 11). The address is latched during the falling edge of $\overline{W}$ or $\overline{E}$ (which ever occurs later) and the data is latched on the rising edge of $\overline{W}$ or $\overline{E}$ (which ever occurs first). After a delay, t_{WLQ5H}, that cannot be shorter than the value specified in Table 9A and Table 9B, the internal write cycle starts. It continues, under inter-

Table 4A. Power-Up Timing[1] for M28256 (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		5	ms
V_{WI}	Write Inhibit Threshold	3.0	4.2	V

Note: 1. Sampled only, not 100% tested.

Table 4B. Power-Up Timing[1] for M28256-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		10	ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

Note: 1. Sampled only, not 100% tested.

nal timing control, until the write operation is complete. The commencement of this period can be detected by reading the Page Load Timer Status on DQ5. The end of the cycle can be detected by reading the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6.

Page Write

The Page Write mode allows up to 64 bytes to be written on a single page in a single go. This is achieved through a series of successive Write operations, no two of which are separated by more than the t_{WLQ5H} value (as specified in Table 9A and Table 9B).

The page write can be initiated during any byte write operation. Following the first byte write instruction the host may send another address and data with a minimum data transfer rate of: $1/t_{WLQ5H}$.

The internal write cycle can start at any instant after t_{WLQ5H}. Once initiated, the write operation is internally timed, and continues, uninterrupted, until completion.

All bytes must be located on the same page address (A14-A6 must be the same for all bytes). Otherwise, the Page Write operation is not executed.

As with the single byte Write operation, described above, the DQ5, DQ6 and DQ7 lines can be used to detect the beginning and end of the internally controlled phase of the Page Write cycle.

Software Data Protection (SDP)

The device offers a software-controlled write-protection mechanism that allows the user to inhibit all write operations to the device. This can be useful for protecting the memory from inadvertent write cycles that may occur during periods of instability (uncontrolled bus conditions when excessive noise is detected, or when power supply levels are outside their specified values).

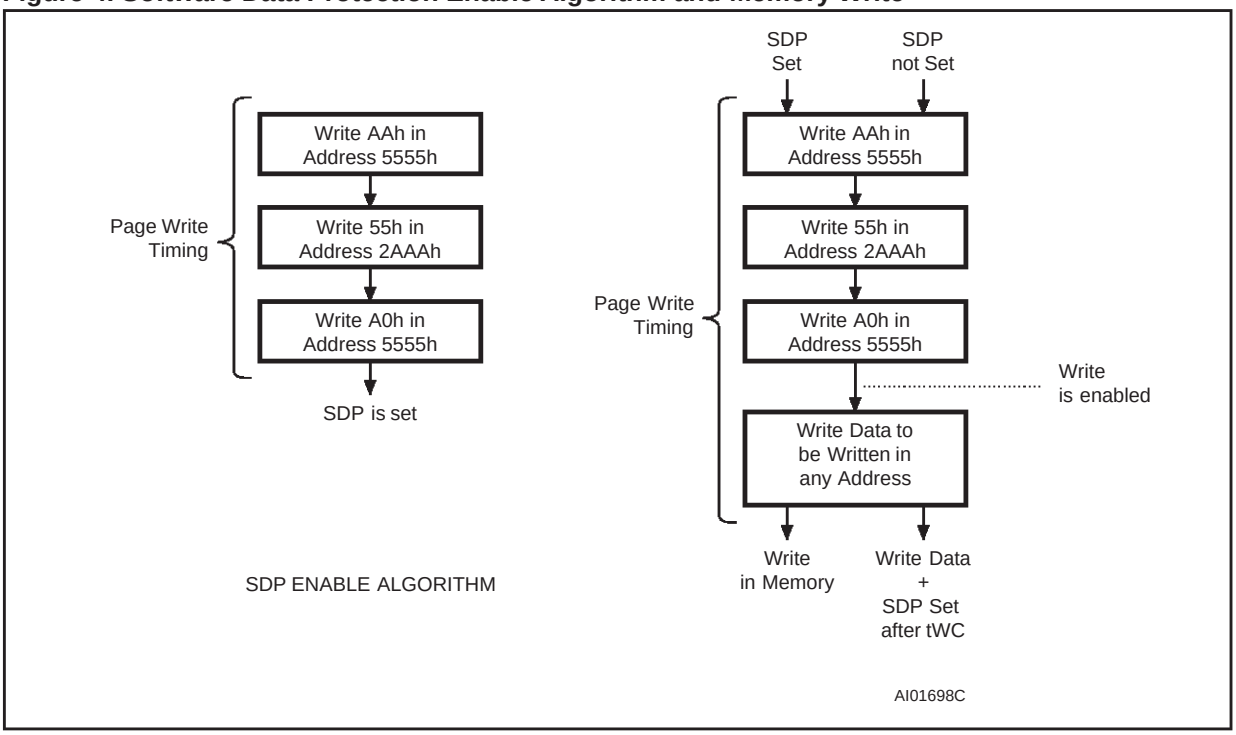
By default, the device is shipped in the “unprotected” state: the memory contents can be freely changed by the user. Once the Software Data Protection Mode is enabled, all write commands are ignored, and have no effect on the memory contents.

The device remains in this mode until a valid Software Data Protection disable sequence is received. The device reverts to its “unprotected” state.

The status of the Software Data Protection (enabled or disabled) is represented by a non-volatile latch, and is remembered across periods of the power being off.

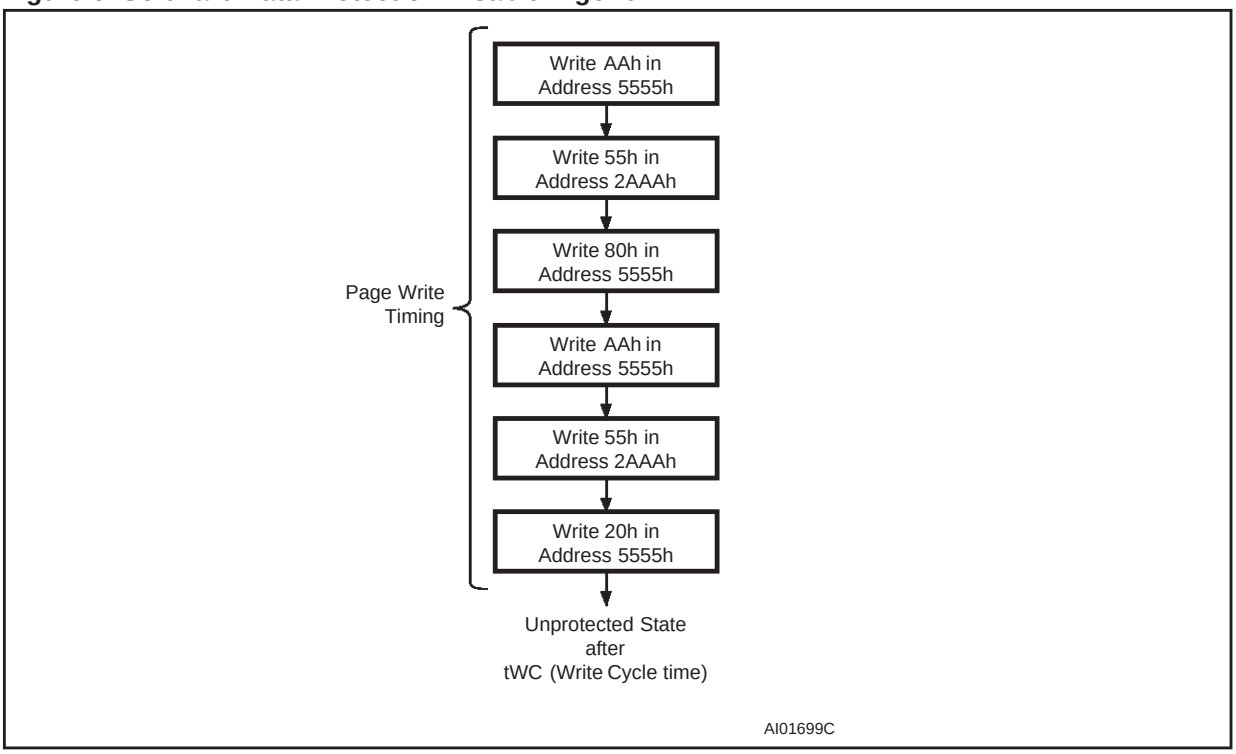
The Software Data Protection Enable command consists of the writing of three specific data bytes

Figure 4. Software Data Protection Enable Algorithm and Memory Write



Note: 1. The most significant address bits (A14 to A6) differ during these specific Page Write operations.

Figure 5. Software Data Protection Disable Algorithm



to three specific memory locations (each location being on a different page), as shown in Figure 4.

Similarly to disable the Software Data Protection, the user has to write specific data bytes into six different locations, as shown in Figure 5. This complex series of operations protects against the chance of inadvertent enabling or disabling of the Software Data Protection mechanism.

When SDP is enabled, the memory array can still have data written to it, but the sequence is more complex (and hence better protected from inadvertent use). The sequence is as shown in Figure 4. This consists of an unlock key, to enable the write action, at the end of which the SDP continues to be enabled. This allows the SDP to be enabled, and data to be written, within a single Write cycle (t_{WC}).

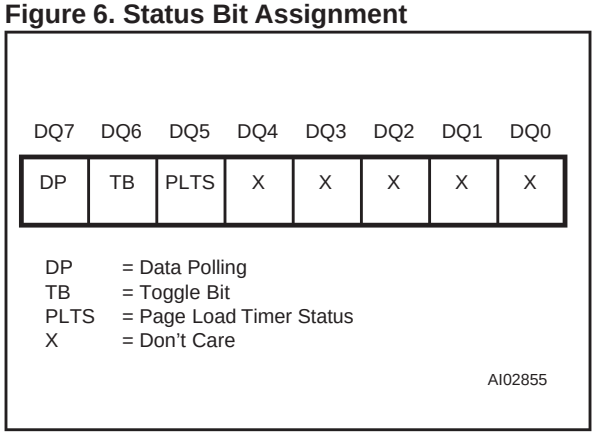
Status Bits

The devices provide three status bits (DQ7, DQ6 and DQ5), and one output pin ($\overline{RB}$), for use during write operations. These allow the application to use the write time latency of the device for getting on with other work. These signals are available on the I/O port bits DQ7, DQ6 and DQ5 (but only during programming cycle, once a byte or more has been latched into the memory) or continuously on the $\overline{RB}$ output pin.

Data Polling bit (DQ7). The internally timed write cycle starts after t_{WLQ5H} (defined in Table 9A and Table 9B) has elapsed since the previous byte was latched in to the memory. The value of the DQ7 bit of this last byte, is used as a signal throughout this write operation: it is inverted while the internal write operation is underway, and is inverted back to its original value once the operation is complete.

Toggle bit (DQ6). The device offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 toggles from '0' to '1' and '1' to '0' (the first read value being '0') on subsequent attempts to read any byte of the memory. When the internal

Figure 6. Status Bit Assignment



write cycle is complete, the toggling is stopped, and the values read on DQ7-DQ0 are those of the addressed memory byte. This indicates that the device is again available for new Read and Write operations.

Page Load Timer Status bit (DQ5). An internal timer is used to measure the period between successive Write operations, up to t_{WLQ5H} (defined in Table 9A and Table 9B). The DQ5 line is held low to show when this timer is running (hence showing that the device has received one write operation, and is waiting for the next). The DQ5 line is held high when the counter has overflowed (hence showing that the device is now starting the internal write to the memory array).

Table 5A. Read Mode DC Characteristics for M28256 (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		10	µA
I_{CC} [1]	Supply Current (TTL inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		25	mA
I_{CC1} [1]	Supply Current (Stand-by) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3V$		100	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All inputs and outputs open circuit.

Table 5B. Read Mode DC Characteristics for M28256-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		10	µA
I_{CC} [1]	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.3V		15	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.6V		15	mA
I_{CC2} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3V$		20	µA
V_{IL}	Input Low Voltage		–0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	0.8 V_{CC}		V

Note: 1. All inputs and outputs open circuit.

Table 6. Input and Output Parameters[1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 7. AC Measurement Conditions

Input Rise and Fall Times	≤ 20 ns
Input Pulse Voltages (M28256)	0.4 V to 2.4 V
Input Pulse Voltages (M28256-W)	0 V to V_{CC}–0.3V
Input and Output Timing Reference Voltages (M28256)	0.8 V to 2.0 V
Input and Output Timing Reference Voltages (M28256-W)	0.5 V_{CC}

Figure 7. AC Testing Input Output Waveforms

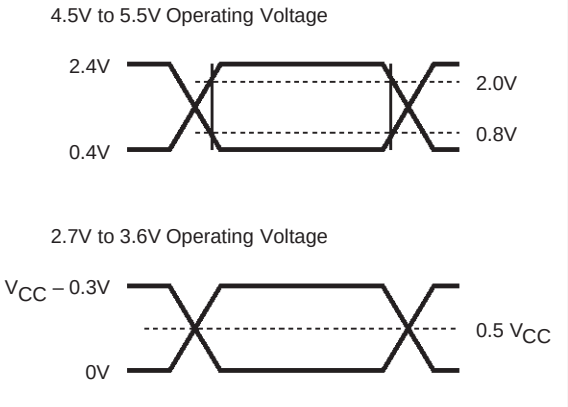


Figure 8. AC Testing Equivalent Load Circuit

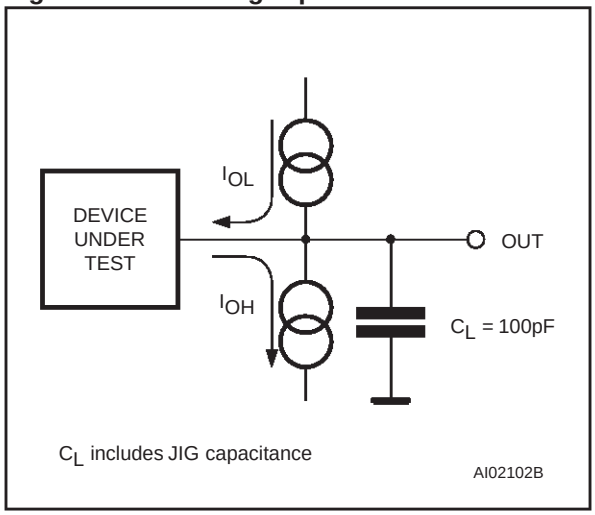


Table 8A. Read Mode AC Characteristics for M28256 (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28256								Unit
				-90		-12		-15		-20		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		45		50		50	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	45	0	50	0	50	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	45	0	50	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

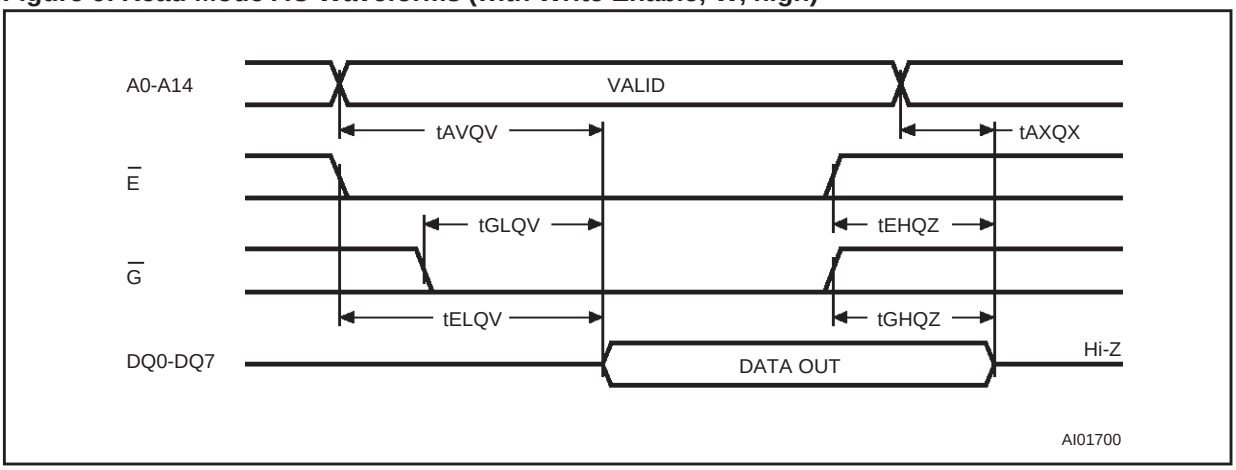
Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Table 8B. Read Mode AC Characteristics for M28256-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28256-W								Unit
				-12		-15		-20		-25		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		70		80		100	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	50	0	55	0	60	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	45	0	50	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 9. Read Mode AC Waveforms (with Write Enable, $\overline{W}$, high)



Note: 1. Write Enable ($\overline{W}$) = V_{IH}

Table 9A. Write Mode AC Characteristics for M28256 (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28256		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50	1000	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WLQ5H}	t_{BLC}	Time-out after last byte write		150		µs
t_{Q5HQ5X}	t_{WC}	Write Cycle Time			5	ms
t_{WL}		Write Enable Input Filter Pulse Width	Note 1	10		ns
t_{EL}		Chip Enable Input Filter Pulse Width	Note 1	10		ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. Characterized only; not tested in production.

Table 9B. Write Mode AC Characteristics for M28256-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28256-W		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		70		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		70		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		100	1000	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WLQ5H}	t_{BLC}	Time-out after the last byte write		200		µs
t_{Q5HQ5X}	t_{WC}	Write Cycle Time			5	ms
t_{WL}		Write Enable Input Filter Pulse Width	Note 1	10		ns
t_{EL}		Chip Enable Input Filter Pulse Width	Note 1	10		ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. Characterized only; not tested in production.

Figure 10. Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

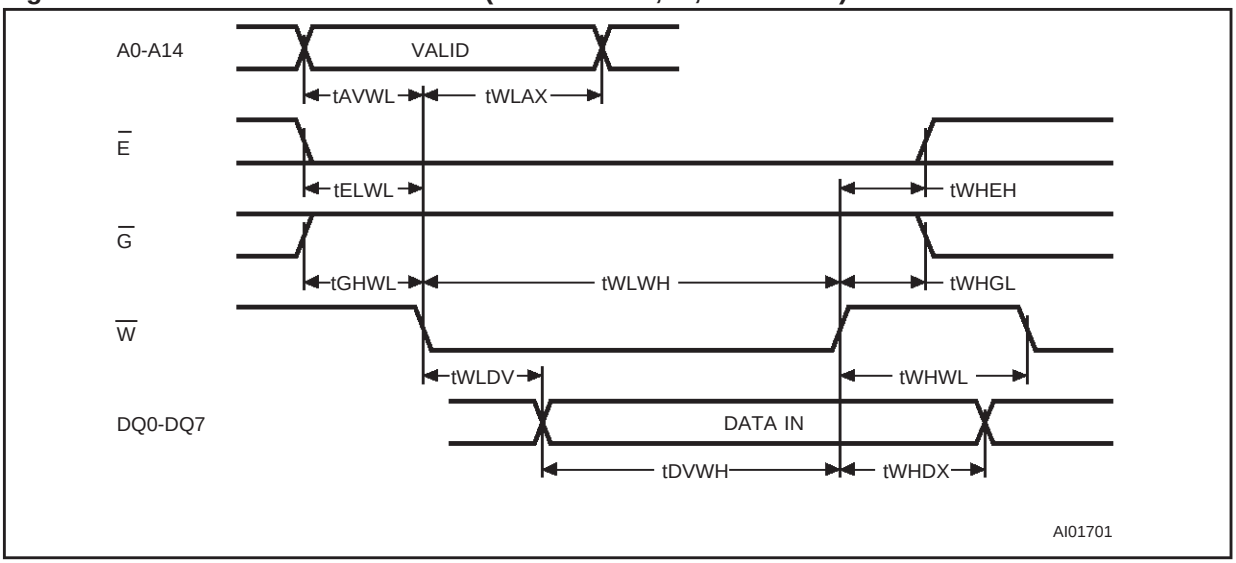


Figure 11. Write Mode AC Waveforms (Chip Enable, $\overline{E}$, controlled)

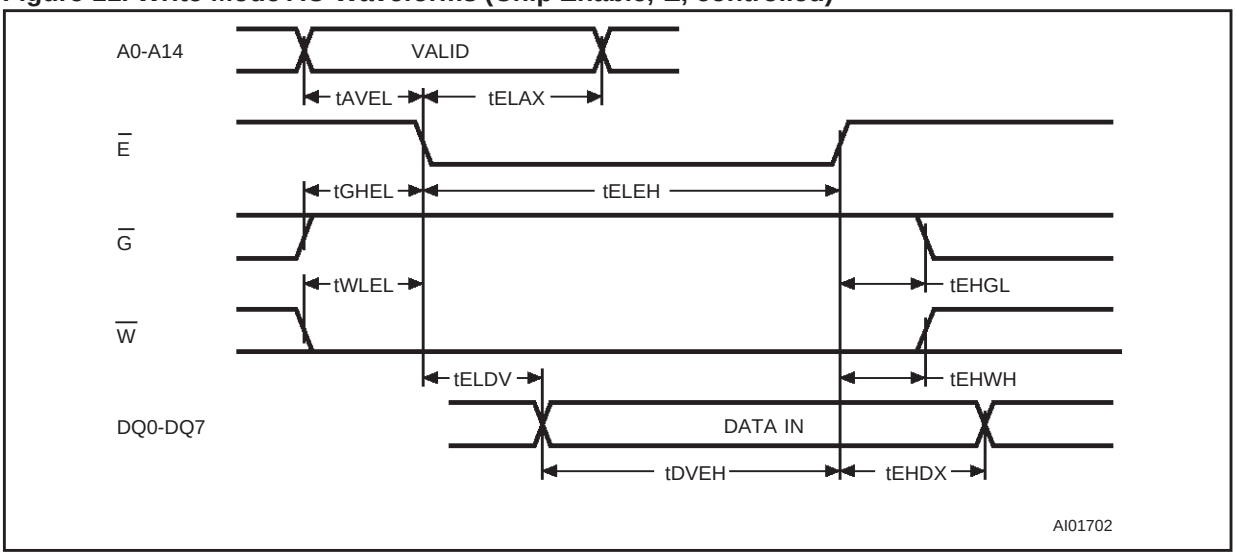


Figure 12. Page Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

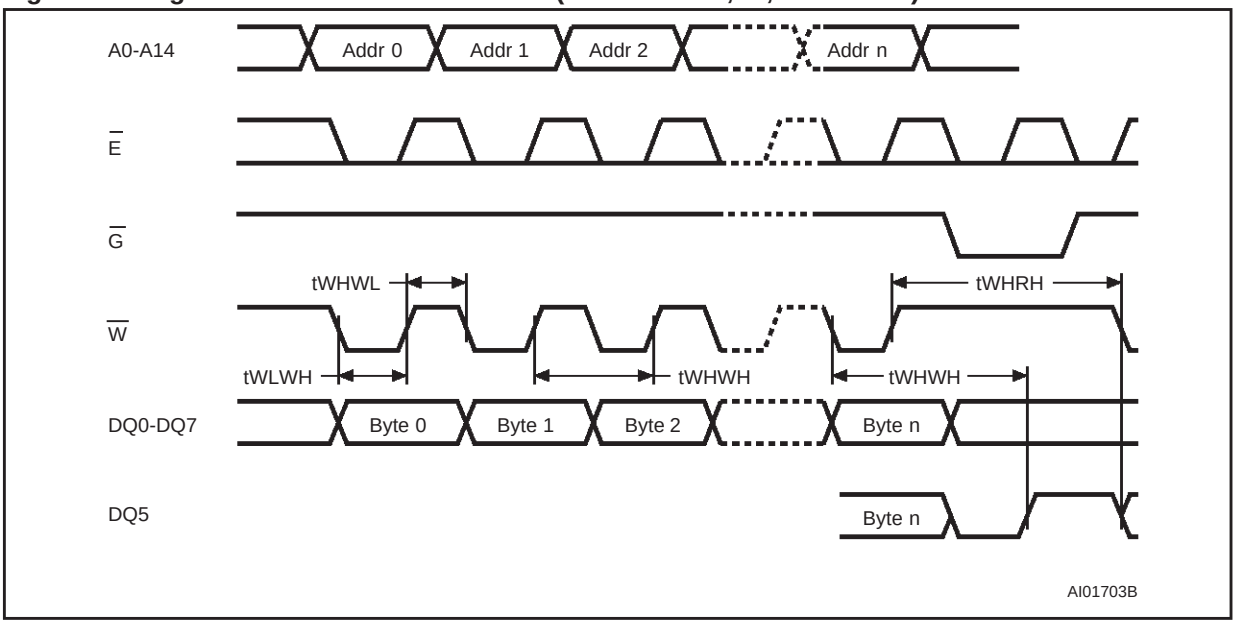
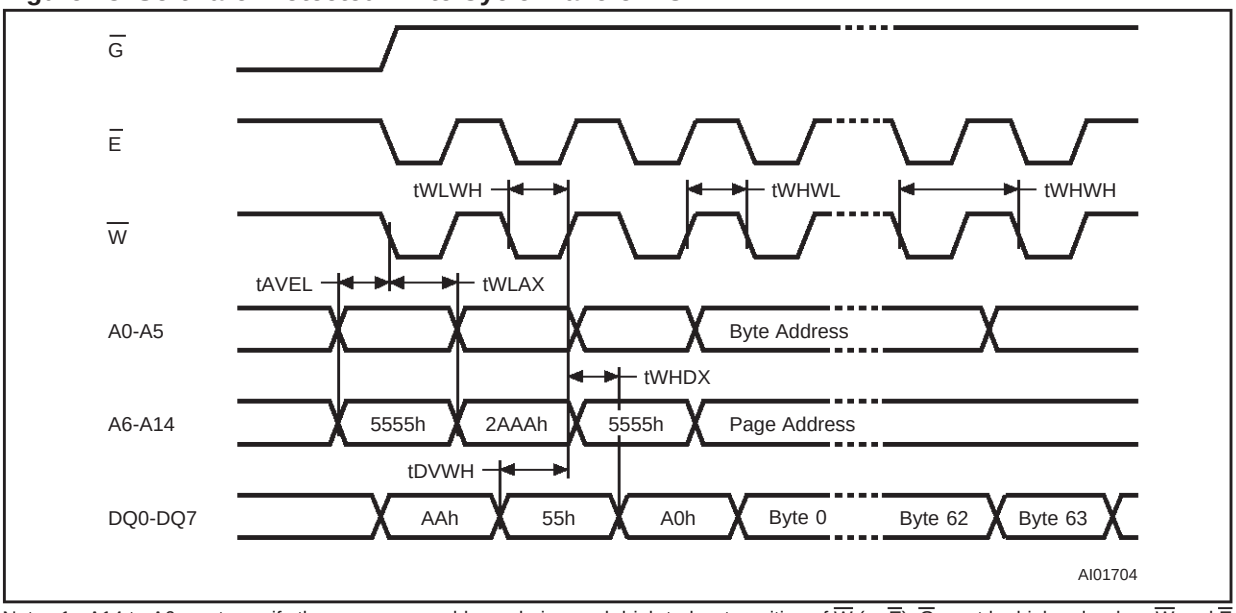


Figure 13. Software Protected Write Cycle Waveforms



Note: 1. A14 to A6 must specify the same page address during each high-to-low transition of $\overline{W}$ (or $\overline{E}$). $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Sequence Waveforms

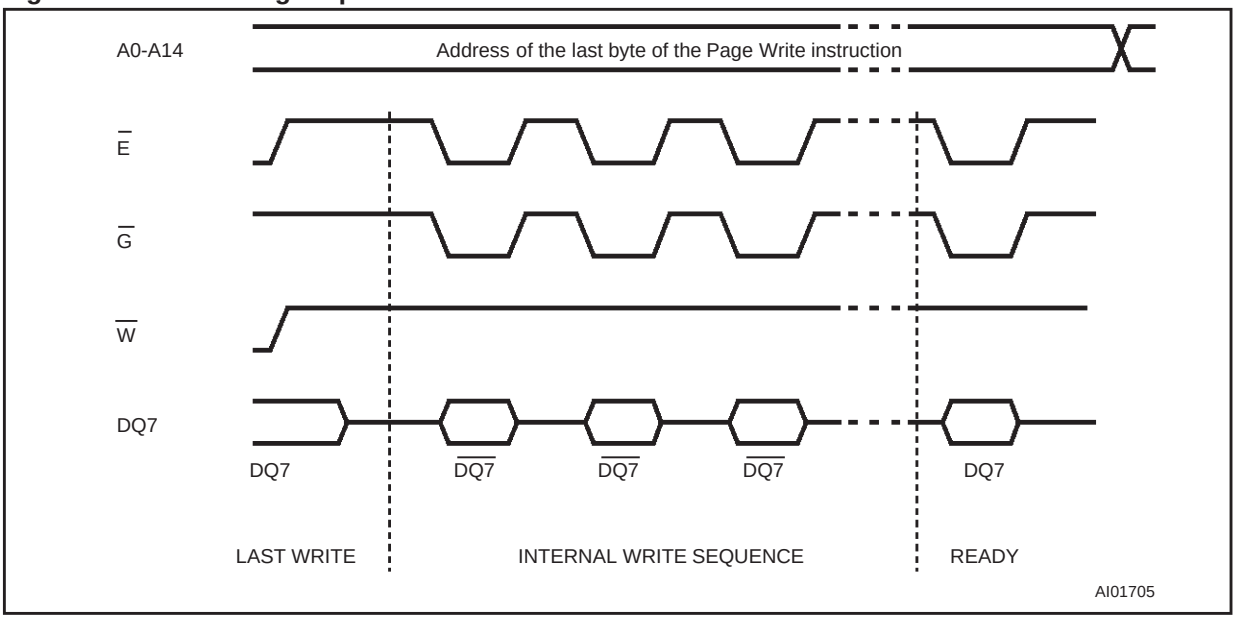
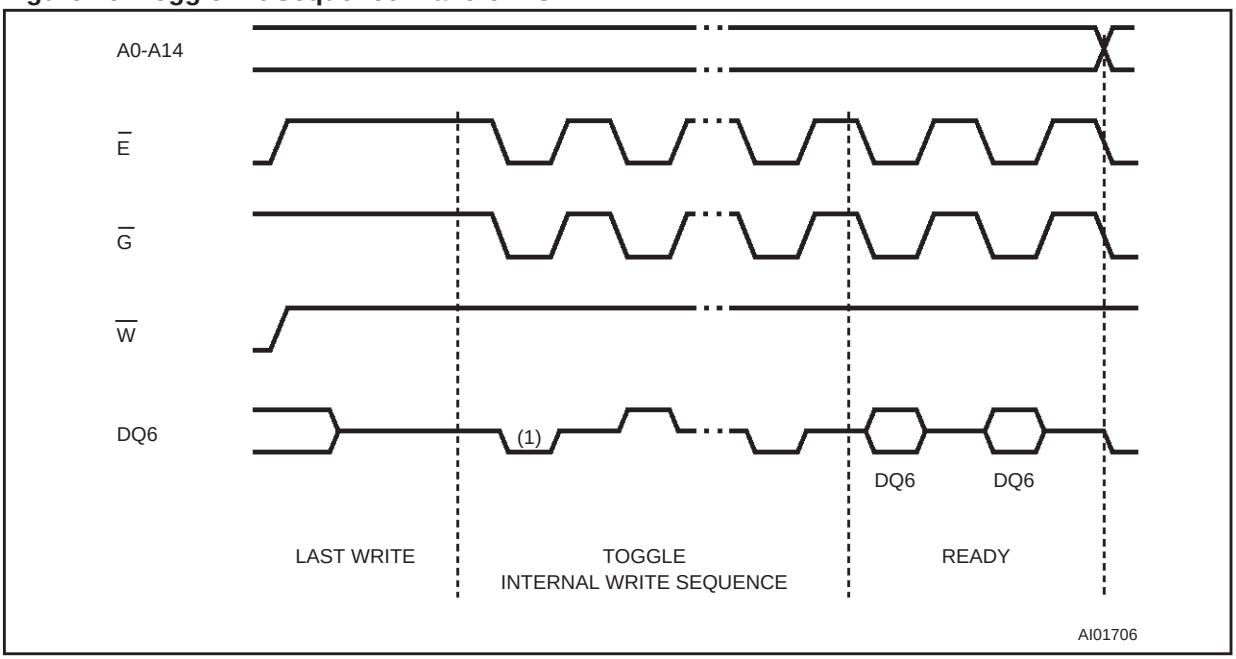


Figure 15. Toggle Bit Sequence Waveforms



Note: 1. The Toggle Bit is first set to '0'.

Table 10. Ordering Information Scheme

Example: M28256 – 15 W KA 6 T

Speed

90[1]	90 ns
12	120 ns
15	150 ns
20	200 ns
25[2]	250 ns

Operating Voltage

blank	4.5 V to 5.5 V
W	2.7 V to 3.6 V

Option

T	Tape and Reel Packing

Temperature Range

1[3]	0 °C to 70 °C
6	–40 °C to 85 °C

Package

BS	PDIP28
KA	PLCC32
MS	SO28 (300 mil width)
NS	TSOP28 (8 x 13.4 mm)

Note: 1. Available for the 3V range (M28256-W) only.
2. Available for the 5V range (M28256) only.
3. Temperature range on request only.

ORDERING INFORMATION

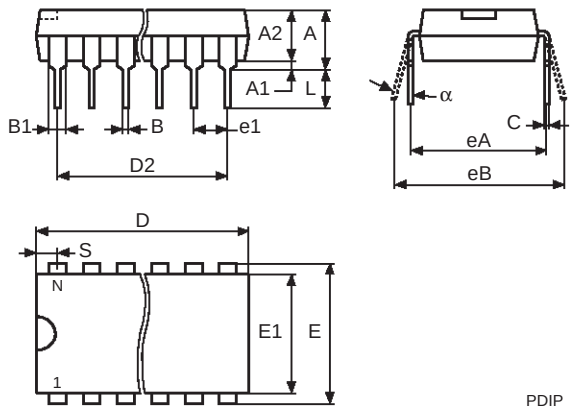
Devices are shipped from the factory with the memory content set at all ‘1’s (FFh).

The notation used for the device number is as shown in Table 10. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 11. PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

Figure 16. PDIP28 (BS)

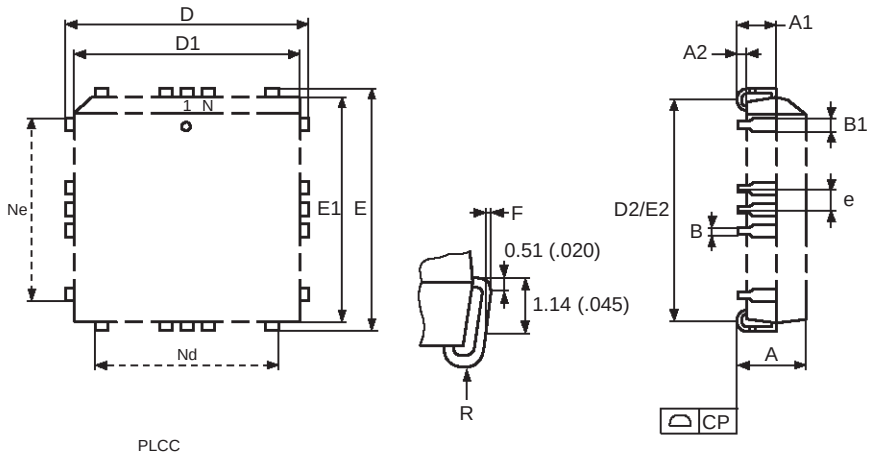


Note: 1. Drawing is not to scale.

Table 12. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

Figure 17. PLCC (KA)



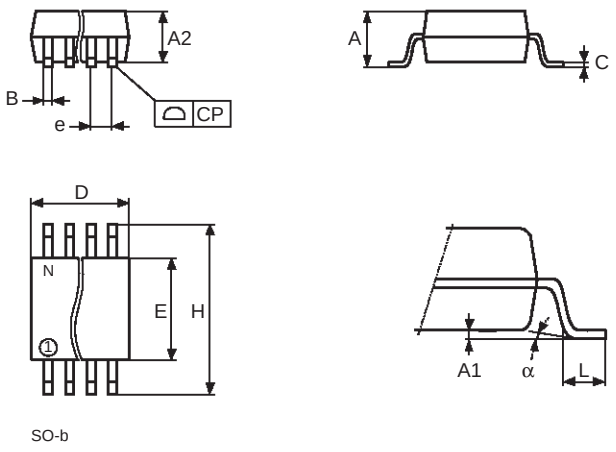
PLCC

Note: 1. Drawing is not to scale.

Table 13. SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 18. SO28 wide (MS)

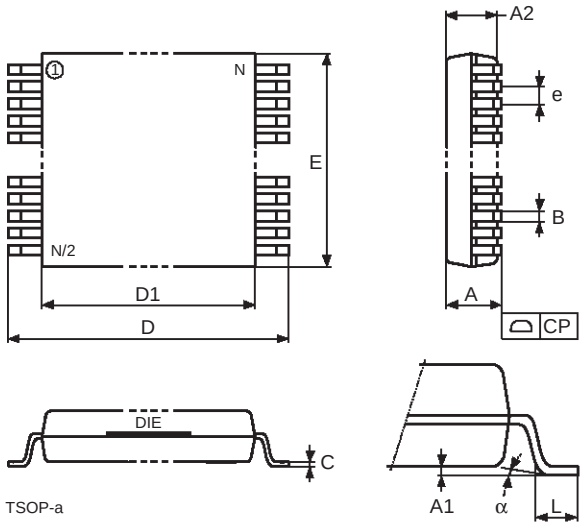


Note: 1. Drawing is not to scale.

Table 14. TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4 mm

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004

Figure 19. TSOP28 (NS)



Note: 1. Drawing is not to scale.