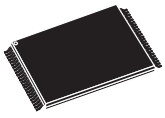
M29W160FT M29W160FB
M29W320FT M29W320FB

16 Mbit or 32 Mbit (x 8 or x 16, boot block) 3 V supply Flash memory

Features

- Supply voltage
  - V_{CC} = 2.5 V to 3.6 V (access time: 80 ns) or 2.7 to 3.6 V (access time: 70 ns) for Program, Erase and Read
  - V_{PP} = 12 V for Fast Program (optional, available in the M29W320FT/B only)
- Access time: 70, 80 ns
- Programming time
  - 10 µs per byte/word typical
- Memory organization:
  - M29W160FT/B: 35 blocks including 1 boot block (top or bottom location), 2 parameter blocks and 32 main blocks
  - M29W320FT: 67 blocks including 1 boot block (top or bottom location), 2 parameter blocks and 64 main blocks
- Program/Erase controller
  - Embedded byte/word program algorithms
- Erase Suspend and Resume modes
  - Read and Program another block during Erase Suspend
- Unlock Bypass Program command
  - Faster production/batch programming
- $V_{PP}/\overline{WP}$ pin for Fast program and Write Protect (available in the M29W320FT/B only)
- Temporary block unprotection mode
- Common Flash interface
  - 64 bit security code
- Low power consumption
  - Standby and Automatic Standby
- 100,000 Program/Erase cycles per block



TSOP48 (N)
12 x 20 mm

TFBGA48 (ZA)
6 x 8 mm

- Electronic signature
  - Manufacturer code: 0020h
  - Top device codes
    M29W160FT: 22C4h
    M29W320FT: 22CAh
  - Bottom device codes
    M29W160FB: 2249h
    M29W320FB: 22CBh
- Automotive device grade 3:
  - Temperature: –40 to 125 °C
  - Automotive grade certified
- TSOP48 package is ECOPACK®

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1 Description

The M29W160FT/B and M29W320FT/B are 16 Mbit (2 Mb x 8 or 1 Mb x 16) and 32 Mbit (4 Mb x 8 or 2 Mb x 16) non-volatile memories, respectively. They can be read, erased and reprogrammed. These operations can be performed using a single low voltage supply (2.5 to 3.6 V or 2.7 to 3.6 V for access time of 80 ns and 70 ns, respectively). On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the command interface of the memory. An on-chip Program/Erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Figures *4*, *5*, *6* and *7*, Block addresses. The first or last 64 Kbytes have been divided into four additional blocks. The 16 Kbyte Boot Block can be used for small initialization code to start the microprocessor, the two 8 Kbyte Parameter Blocks can be used for parameter storage and the remaining 32 Kbyte block is a small Main Block where the application may be stored.

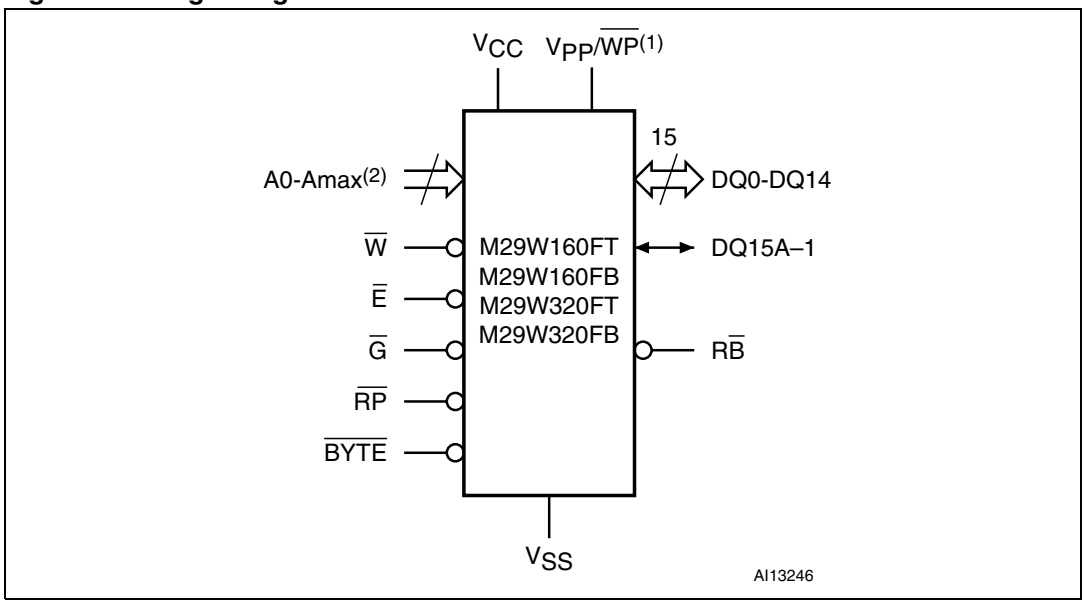
Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP48 (12 x 20 mm) and TFBGA48 (0.8 mm pitch) packages. The memory is supplied with all the bits erased (set to ’1’).

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 1. Logic diagram



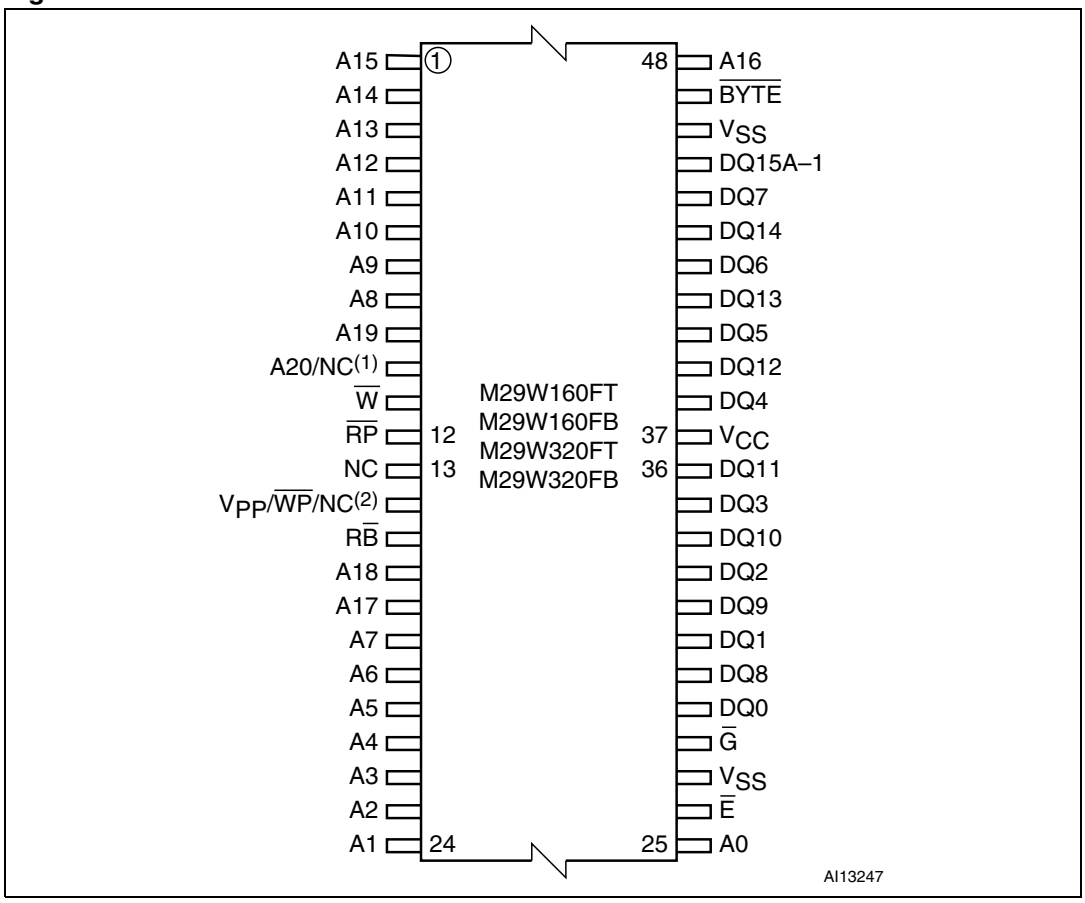
1. The $V_{PP}/\overline{WP}$ pin is available in the M29W320FT and M29W320FB only.
2. Amax is equal to A19 in the M29W160FT/B, and to A20 in the M29W320FT/B.

Table 1. Signal names

Signal name	Function	Direction
A0-Amax(1)	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15A–1	Data input/output or Address input	I/O
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{RP}$	Reset/Block Temporary Unprotect	Input
$R\overline{B}$	Ready/Busy output	Output
$\overline{BYTE}$	Byte/word Organization Select	Input
$V_{PP}/\overline{WP}$(2)	V_{PP}/Write Protect	
V_{CC}	Supply voltage	
V_{SS}	Ground	
NC	Not connected internally	

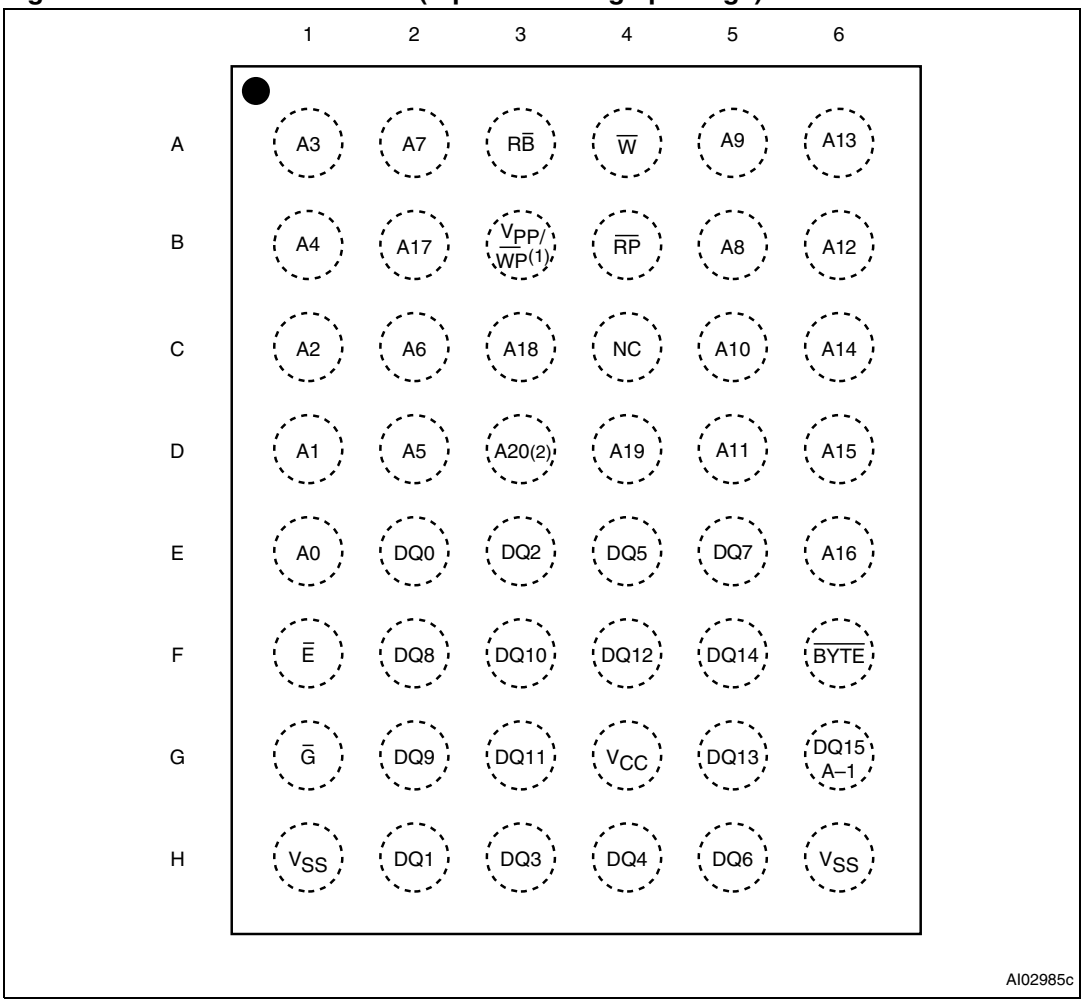
1. Amax is equal to A19 in the M29W160FT/B, and to A20 in the M29W320FT/B.
2. The $V_{PP}/\overline{WP}$ pin is available in the M29W320FT and M29W320FB only.

Figure 2. TSOP connections



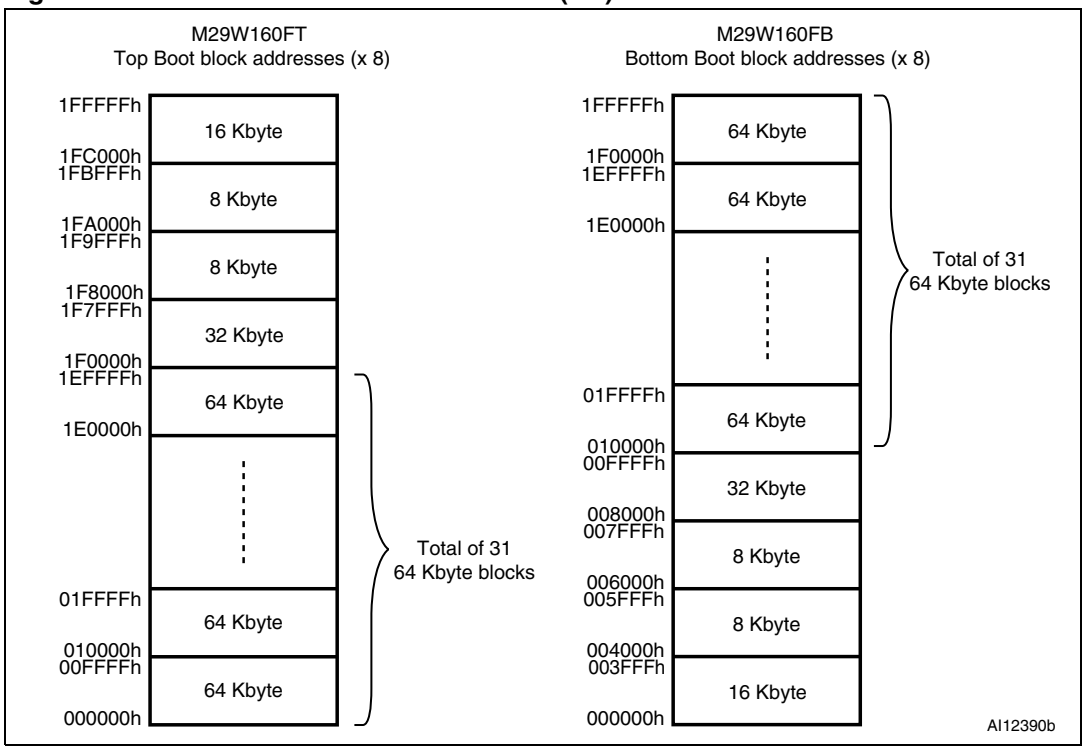
1. Pin 10 is NC (not connected) in the M29W160FT/B, and it is connected to A20 in the M29W320FT/B.
2. Pin 14 is NC (not connected) in the M29W160FT/B, and it is connected to the $V_{PP}/\overline{WP}$ pin in the M29W320FT/B.

Figure 3. TFBGA connections (top view through package)



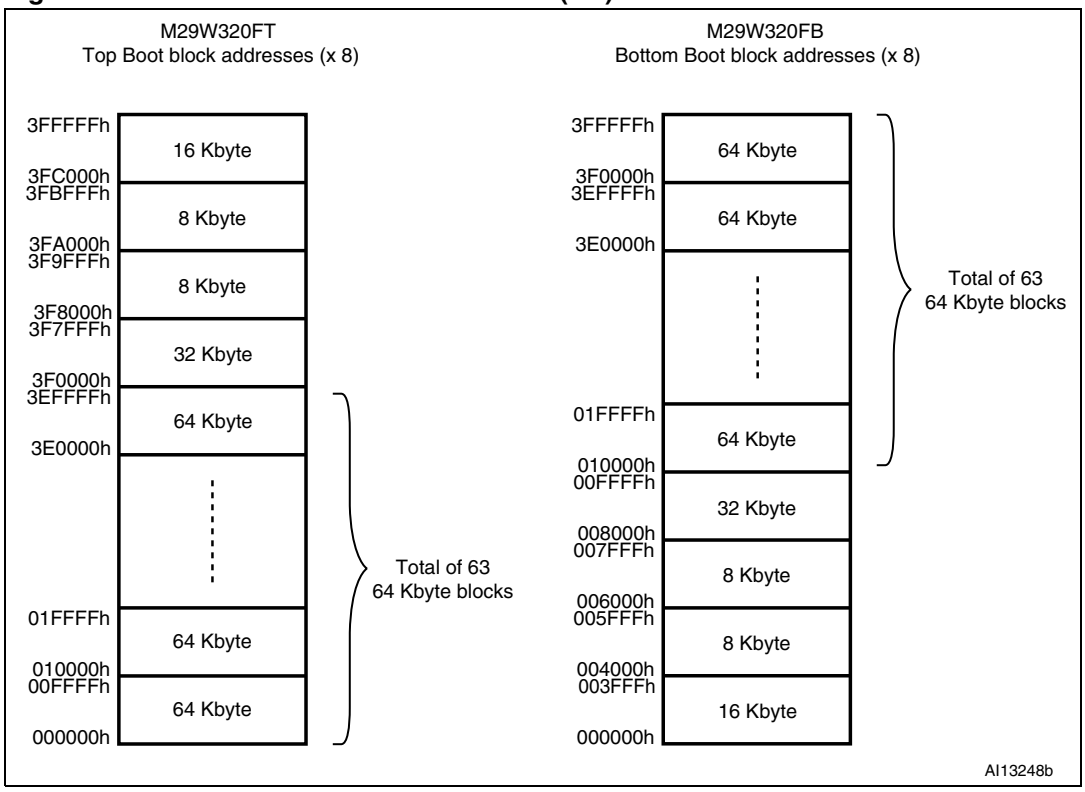
1. The above figure gives the TFBGA connections for the M29W320FT/B. On the M29W160FT/B, the $V_{PP}/\overline{WP}$ pin is NC (not connected).
2. The above figure gives the TFBGA connections for the M29W320FT/B. On the M29W160FT/B, A20 is NC (not connected).

Figure 4. M29W160FT/B block addresses (x 8)



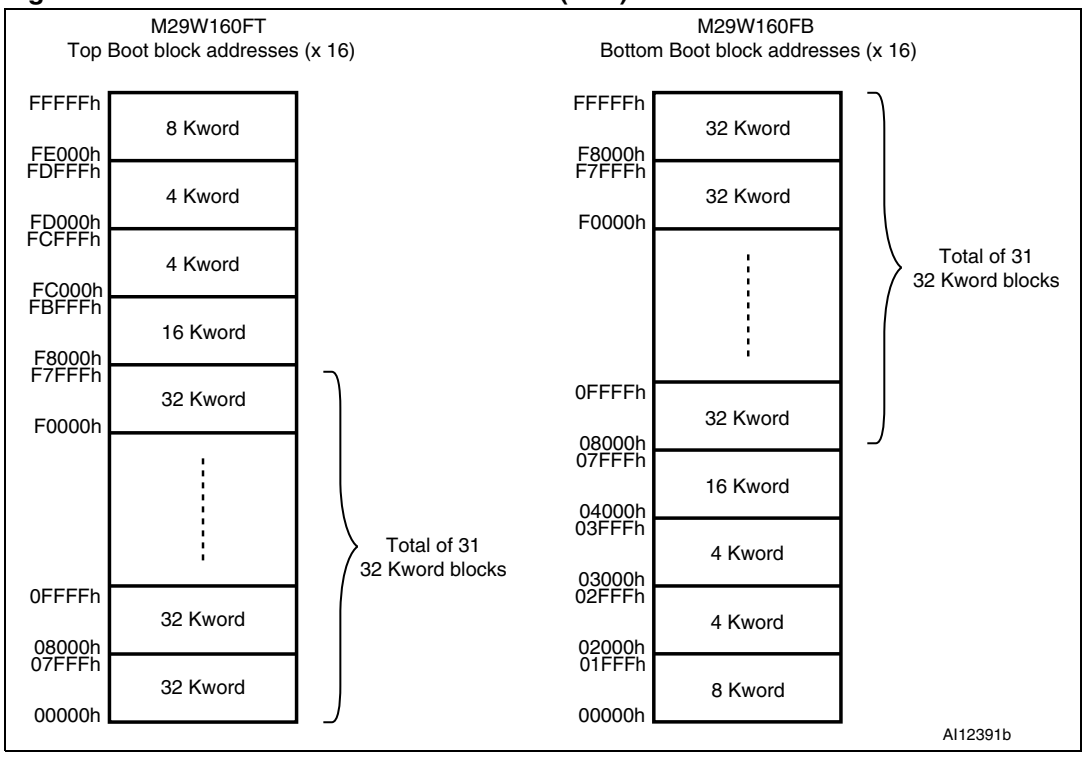
1. Also see *Appendix A*, Tables *19* and *20* for a full listing of the block addresses.

Figure 5. M29W320FT/B block addresses (x 8)



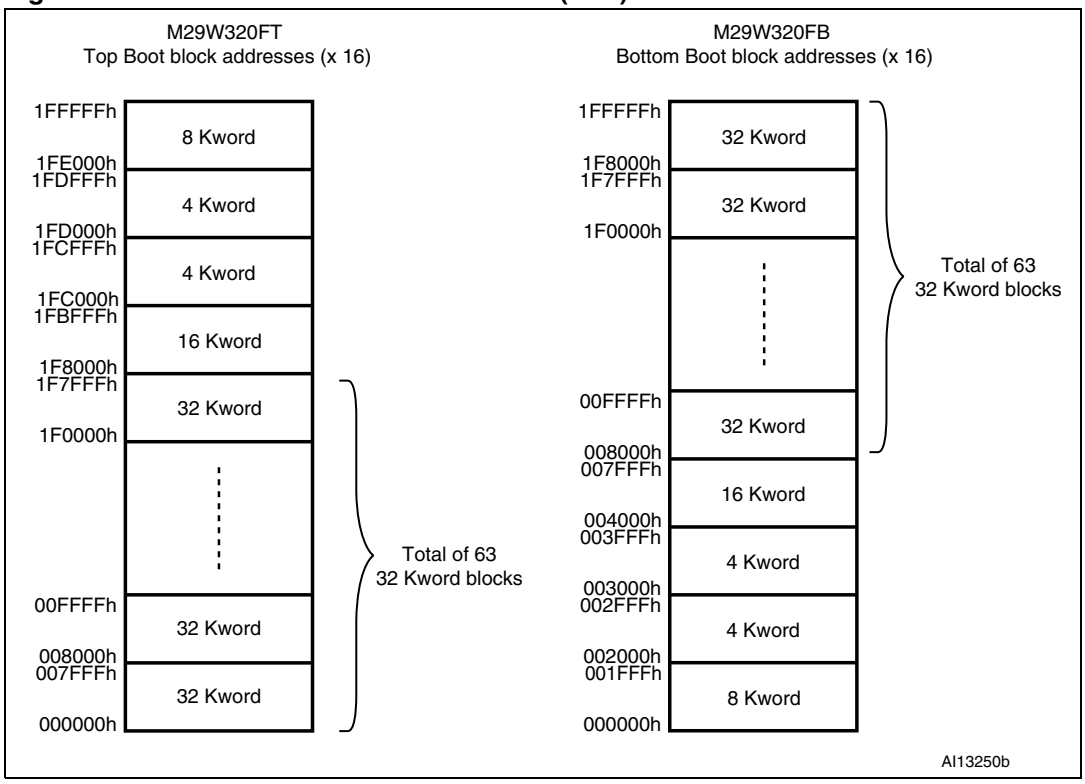
1. Also see *Appendix A*, Tables *21* and *22* for a full listing of the block addresses.

Figure 6. M29W160FT/B block addresses (x 16)



1. Also see *Appendix A*, Tables *19* and *20* for a full listing of the block addresses.

Figure 7. M29W320FT/B block addresses (x 16)



1. Also see *Appendix A*, Tables *21* and *22* for a full listing of the block addresses.

2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-Amax)

Amax is equal to A19 in the M29W160FT/B, and to A20 in the M29W320FT/B.

The Address inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the command interface of the Program/Erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The Data inputs/outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the command interface of the Program/Erase controller.

2.3 Data inputs/outputs (DQ8-DQ14)

The Data inputs/outputs output the data stored at the selected address during a Bus Read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

2.4 Data input/output or Address input (DQ15A-1)

When $\overline{BYTE}$ is High, V_{IH}, this pin behaves as a Data input/output pin (as DQ8-DQ14). When $\overline{BYTE}$ is Low, V_{IL}, this pin behaves as an address pin; DQ15A–1 Low will select the LSB of the word on the other addresses, DQ15A–1 High will select the MSB. Throughout the text consider references to the Data input/output to include this pin when $\overline{BYTE}$ is High and references to the Address inputs to include this pin when $\overline{BYTE}$ is Low except when stated explicitly otherwise.

2.5 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

2.6 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

2.7 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's command interface.

2.8 V_{PP}/Write Protect ($V_{PP}/\overline{WP}$)

The V_{PP}/Write Protect pin is only available in the M29W320FT/B devices. It provides two functions. The V_{PP} function allows the memory to use an external high voltage power supply to reduce the time required for Unlock Bypass Program operations. The Write Protect function provides a hardware method of protecting the 16 Kbyte Boot Block. The V_{PP}/Write Protect pin must not be left floating or unconnected.

When V_{PP}/Write Protect is Low, V_{IL}, the memory protects the 16 Kbyte Boot Block; Program and Erase operations in this block are ignored while V_{PP}/Write Protect is Low.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the 16 Kbyte boot block. Program and Erase operations can now modify the data in the 16 Kbyte Boot Block unless the block is protected using Block Protection.

When V_{PP}/Write Protect is raised to V_{PP} the memory automatically enters the Unlock Bypass mode. When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. During Unlock Bypass Program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than t_{VHVPP}, see *Figure 16*.

Never raise V_{PP}/Write Protect to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

A 0.1 µF capacitor should be connected between the V_{PP}/Write Protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}

2.9 Reset/Block Temporary Unprotect ($\overline{RP}$)

The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all blocks that have been protected.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/Busy Output (RB)*, *Table 15* and *Figure 15.*, Reset/Temporary Unprotect AC characteristics for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

2.10 Ready/Busy Output ($\overline{RB}$)

The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See *Table 15* and *Figure 15: Reset/Block Temporary Unprotect AC waveforms*.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.11 Byte/Word Organization Select ($\overline{BYTE}$)

The Byte/Word Organization Select pin is used to switch between the 8-bit and 16-bit Bus modes of the memory. When Byte/Word Organization Select is Low, V_{IL}, the memory is in 8-bit mode, when it is High, V_{IH}, the memory is in 16-bit mode.

2.12 V_{CC} supply voltage

The V_{CC} supply voltage supplies the power for all operations (Read, Program, Erase etc.).

The command interface is disabled when the V_{CC} supply voltage is less than the Lockout voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}.

2.13 V_{SS} ground

The V_{SS} ground is the reference for all voltage measurements. The two V_{SS} pins of the device must be connected to the system ground.

3 Bus operations

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See *Table 2.* and *Table 3.*, Bus operations, for a summary. Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.1 Bus Read

Bus Read operations read from the memory cells, or specific registers in the command interface. A valid Bus Read operation involves setting the desired address on the Address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data inputs/outputs will output the value, see *Figure 12: Read mode AC waveforms*, and *Table 12: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write to the command interface. A valid Bus Write operation begins by setting the desired address on the Address inputs. The Address inputs are latched by the command interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data inputs/outputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See *Figure 13.* and *Figure 14.*, Write AC waveforms, and Tables *13* and *14*, Write AC characteristics, for details of the timing requirements.

3.3 Output Disable

The Data inputs/outputs are in the high impedance state when Output Enable is High, V_{IH}.

3.4 Standby

When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data inputs/outputs pins are placed in the high-impedance state. To reduce the supply current to the Standby supply current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2$ V. For the Standby current level see *Table 11: DC characteristics*.

During program or erase operations the memory will continue to use the Program/Erase supply current, I_{CC3}, for Program or Erase operations until the operation completes.

3.5 Automatic Standby

If CMOS levels ($V_{CC} \pm 0.2$ V) are used to drive the bus and the bus is inactive for 150 ns or more the memory enters Automatic Standby where the internal supply current is reduced to the Standby supply current, I_{CC2}. The Data inputs/outputs will still output data if a Bus Read operation is in progress.

3.6 Special bus operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

3.7 Electronic signature

The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in *Table 2.* and *Table 3*, Bus operations.

3.8 Block protection and Blocks unprotection

Each block can be separately protected against accidental Program or Erase. Protected blocks can be unprotected to allow data to be changed.

There are two methods available for protecting and unprotecting the blocks, one for use on programming equipment and the other for in-system use. Block Protect and Blocks Unprotect operations are described in *Appendix C*.

Table 2. Bus operations, $\overline{BYTE}$ = V_{IL} (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs DQ15A–1, A0-Amax	Data inputs/outputs	
					DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell address	Hi-Z	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command address	Hi-Z	Data input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z
Read manufacturer code	V_{IL}	V_{IL}	V_{IH}	A0=V_{IL}, A1=V_{IL}, A9=V_{ID}, others V_{IL} or V_{IH}	Hi-Z	20h
Read device code	V_{IL}	V_{IL}	V_{IH}	A0=V_{IH}, A1=V_{IL}, A9=V_{ID}, others V_{IL} or V_{IH}	Hi-Z	C4h (M29W160FT) CAh (M29W320FT) 49h (M29W160FB) CBh (M29W320FB)

1. X = V_{IL} or V_{IH}.

Table 3. Bus operations, $\overline{BYTE}$ = V_{IH}(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs A0-Amax	Data inputs/outputs DQ15A–1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell address	Data output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command address	Data input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read manufacturer code	V_{IL}	V_{IL}	V_{IH}	A0=V_{IL}, A1=V_{IL}, A9=V_{ID}, others V_{IL} or V_{IH}	0020h
Read device code	V_{IL}	V_{IL}	V_{IH}	A0=V_{IH}, A1=V_{IL}, A9=V_{ID}, others V_{IL} or V_{IH}	22C4h (M29W160FT) 22CAh (M29W320FT) 2249h (M29W160FB) 22CBh (M29W320FB)

1. X = V_{IL} or V_{IH}.

4 Command interface

All Bus Write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode. See either *Table 4*, or *Table 5*, depending on the configuration that is being used, for a summary of the commands.

4.1 Read/Reset command

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to Read mode. Once the program or erase operation has started the Read/Reset command is no longer accepted. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

4.2 Auto Select command

The Auto Select command is used to read the manufacturer code, the device code and the Block Protection status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued. Read CFI Query and Read/Reset commands are accepted in Auto Select mode, all other commands are ignored.

From the Auto Select mode the manufacturer code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The manufacturer code for Numonyx is 0020h.

The device code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}.

The Block Protection status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, and A12-Amax specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data inputs/outputs DQ0-DQ7, otherwise 00h is output.

4.3 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data, and starts the Program/Erase controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in *Table 6*. Bus Read operations during the program operation will output the Status Register on the Data inputs/outputs. See the section on the Status Register for more details.

After the program operation has completed the memory returns to the Read mode, unless an error has occurred. When an error occurs the memory continues to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at ’0’ back to ’1’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

4.4 Unlock Bypass command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

4.5 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data, and starts the Program/Erase controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass mode. See the Program command for details on the behavior.

4.6 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass mode.

4.7 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase command and start the Program/Erase controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 6*. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data inputs/outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Chip Erase command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

4.8 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase controller about 50 µs after the last Bus Write operation. Once the Program/Erase controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50 µs of the last block. The 50 µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register section for details on how to identify if the Program/Erase controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command. Typical block erase times are given in *Table 6*. All Bus Read operations during the Block Erase operation will output the Status Register on the Data inputs/outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase command sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

4.9 Erase Suspend command

The Erase Suspend command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase controller will suspend within the Erase Suspend Latency time (refer to *Table 6* for value) of the Erase Suspend command being issued. Once the Program/Erase controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

4.10 Erase Resume command

The Erase Resume command must be used to restart the Program/Erase controller from Erase Suspend. An erase can be suspended and resumed more than once.

4.11 Read CFI Query command

The Read CFI Query command is used to read data from the Common Flash interface (CFI) memory area. This command is valid when the device is in the Read Array mode, or when the device is in Auto Select mode.

One Bus Write cycle is required to issue the Read CFI Query command. Once the command is issued subsequent Bus Read operations read from the Common Flash interface memory area.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Auto Select mode). A second Read/Reset command would be needed if the device is to be put in the Read Array mode from Auto Select mode.

See *Appendix B*, Tables *23*, *24*, *25*, *26*, *27* and *28* for details on the information contained in the common flash interface (CFI) memory area.

Table 4. Commands, 16-bit mode, $\overline{BYTE}$ = V_{IH}

Command	Length	Bus Write operations(1) (2) (3)											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset(4)	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select(5)	3	555	AA	2AA	55	555	90						
Program(6)	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass(7)	3	555	AA	2AA	55	555	20						
Unlock Bypass Program(6)	2	X	A0	PA	PD								
Unlock Bypass Reset(8)	2	X	90	X	00								
Chip Erase(6)	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase(6)	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend(9)	1	X	B0										
Erase Resume(10)	1	X	30										
Read CFI Query(11)	1	55	98										

1. X don't care, PA Program Address, PD Program Data, BA any address in the block.
2. All values in the table are in hexadecimal.
3. The command interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A19, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.
4. After a Read/Reset command, read the memory as normal until another command is issued.
5. After an Auto Select command, read manufacturer ID, device ID or Block Protection status.
6. After this command read the Status Register until the Program/Erase controller completes and the memory returns to Read mode. Add additional blocks during Block Erase command with additional Bus Write operations until Timeout bit is set.
7. After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.
8. After the Unlock Bypass Reset command read the memory as normal until another command is issued.
9. After the Erase Suspend command read non-erasing memory blocks as normal, issue Auto Select and Program commands on non-erasing blocks as normal.
10. After the Erase Resume command the suspended Erase operation resumes, read the Status Register until the Program/Erase controller completes and the memory returns to Read mode.
11. Command is valid when device is ready to read array data or when device is in Auto Select mode.

Table 5. Commands, 8-bit mode, $\overline{BYTE}$ = V_{IL}

Command	Length	Bus Write operations(1) (2) (3)											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset(4)	1	X	F0										
	3	AAA	AA	555	55	X	F0						
Auto Select(5)	3	AAA	AA	555	55	AAA	90						
Program(6)	4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass(7)	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program(6)	2	X	A0	PA	PD								
Unlock Bypass Reset(8)	2	X	90	X	00								
Chip Erase(6)	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase(6)	6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BA	30
Erase Suspend(9)	1	X	B0										
Erase Resume(10)	1	X	30										
Read CFI Query(11)	1	AA	98										

1. X don't care, PA Program Address, PD Program Data, BA any address in the block.
2. All values in the table are in hexadecimal.
3. The command interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A19, DQ8-DQ14 and DQ15 are don't care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.
4. After a Read/Reset command, read the memory as normal until another command is issued.
5. After an Auto Select command, read manufacturer ID, device ID or Block Protection status.
6. After this command read the Status Register until the Program/Erase controller completes and the memory returns to Read mode. Add additional blocks during Block Erase command with additional Bus Write operations until Timeout bit is set.
7. After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.
8. After the Unlock Bypass Reset command read the memory as normal until another command is issued.
9. After the Erase Suspend command read non-erasing memory blocks as normal, issue Auto Select and Program commands on non-erasing blocks as normal.
10. After the Erase Resume command the suspended Erase operation resumes, read the Status Register until the Program/Erase controller completes and the memory returns to Read mode.
11. Command is valid when device is ready to read array data or when device is in Auto Select mode.

Table 6. Program, Erase times and Program, Erase endurance cycles

Parameter	Min	Typ(1) (2)	Max(2)	Unit
Chip Erase		29	120(3)	s
Block Erase (64 Kbytes)		0.8	6(4)	s
Erase Suspend Latency time		20	25(4)	µs
Program (byte or word)		13	200(3)	µs
Chip Program (byte by byte)		26	120(3)	s
Chip Program (word by word)		13	60(3)	s
Program/Erase cycles (per block)	100,000			cycles
Data retention	20			years

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,000 program/erase cycles.
4. Maximum value measured at worst case conditions for both temperature and V_{CC}.

5 Status Register

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in *Table 7: Status Register bits*.

5.1 Data Polling bit (DQ7)

The Data Polling bit can be used to identify whether the Program/Erase controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling bit will output a ’1’ during a Bus Read operation within a block being erased. The Data Polling bit will change from a ’0’ to a ’1’ when the Program/Erase controller has suspended the Erase operation.

Figure 8: Data polling flowchart, gives an example of how to use the Data Polling bit. A Valid address is the address being programmed or an address within the block being erased.

5.2 Toggle bit (DQ6)

The Toggle bit can be used to identify whether the Program/Erase controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle bit will output when addressing a cell within a block being erased. The Toggle bit will stop toggling when the Program/Erase controller has suspended the Erase operation.

If any attempt is made to erase a protected block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 100µs. If any attempt is made to program a protected block or a suspended block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 1µs.

Figure 9: Data toggle flowchart, gives an example of how to use the Data Toggle bit.

5.3 Error bit (DQ5)

The Error bit can be used to identify errors detected by the Program/Erase controller. The Error bit is set to ’1’ when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to ’0’ back to ’1’ and attempting to do so will set DQ5 to ‘1’. A Bus Read operation to that address will show the bit is still ‘0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’

5.4 Erase Timer bit (DQ3)

The Erase Timer bit can be used to identify the start of Program/Erase controller operation during a Block Erase command. Once the Program/Erase controller starts erasing the Erase Timer bit is set to ’1’. Before the Program/Erase controller starts the Erase Timer bit is set to ’0’ and additional blocks to be erased may be written to the command interface. The Erase Timer bit is output on DQ3 when the Status Register is read.

5.5 Alternative Toggle bit (DQ2)

The Alternative Toggle bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error bit to be set the Alternative Toggle bit can be used to identify which block or blocks have caused the error. The Alternative Toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle bit does not change if the addressed block has erased correctly.

Table 7. Status Register bits(1)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	RB
Program	Any address	DQ7	Toggle	0	–	–	0
Program During Erase Suspend	Any address	DQ7	Toggle	0	–	–	0
Program Error	Any address	DQ7	Toggle	1	–	–	0
Chip Erase	Any address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing block	0	Toggle	0	0	Toggle	0
	Non-erasing block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing block	0	Toggle	0	1	Toggle	0
	Non-erasing block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing block	1	No Toggle	0	–	Toggle	1
	Non-erasing block	Data read as normal					1
Erase Error	Good block address	0	Toggle	1	1	No Toggle	0
	Faulty block address	0	Toggle	1	1	Toggle	0

1. Unspecified data bits should be ignored.

Figure 8. Data polling flowchart

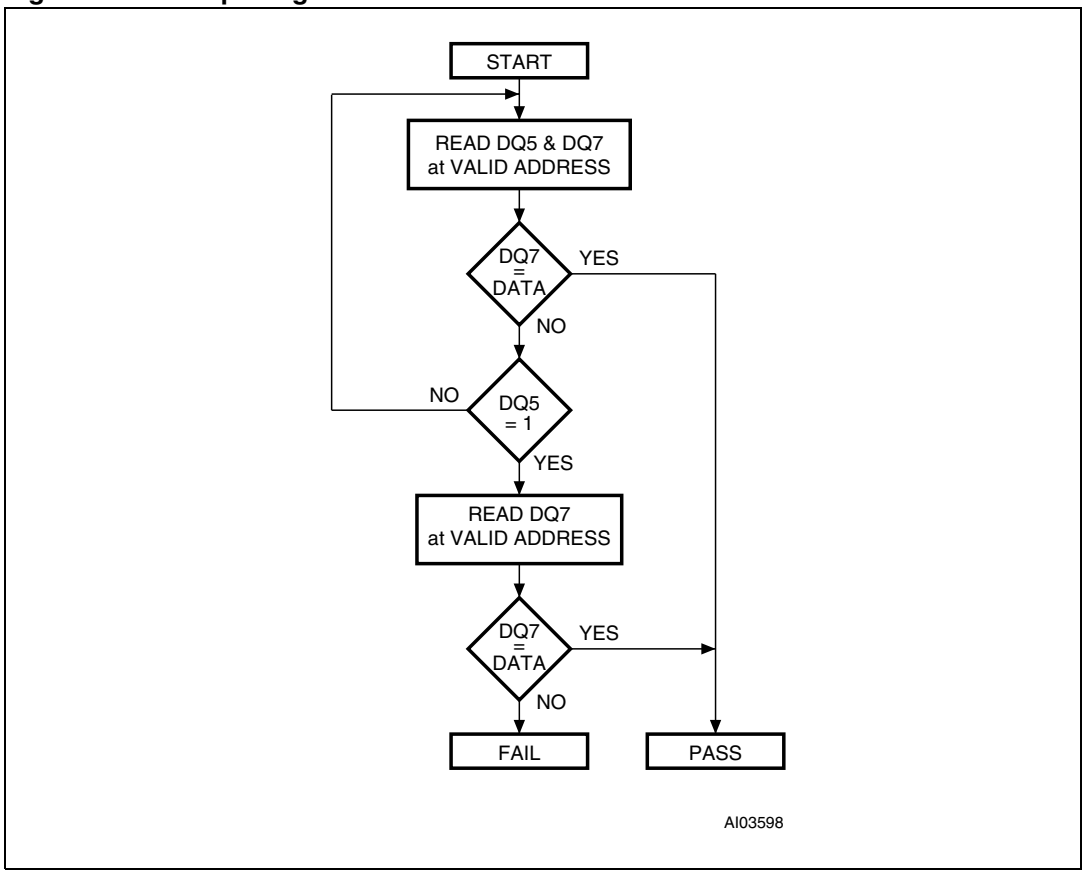
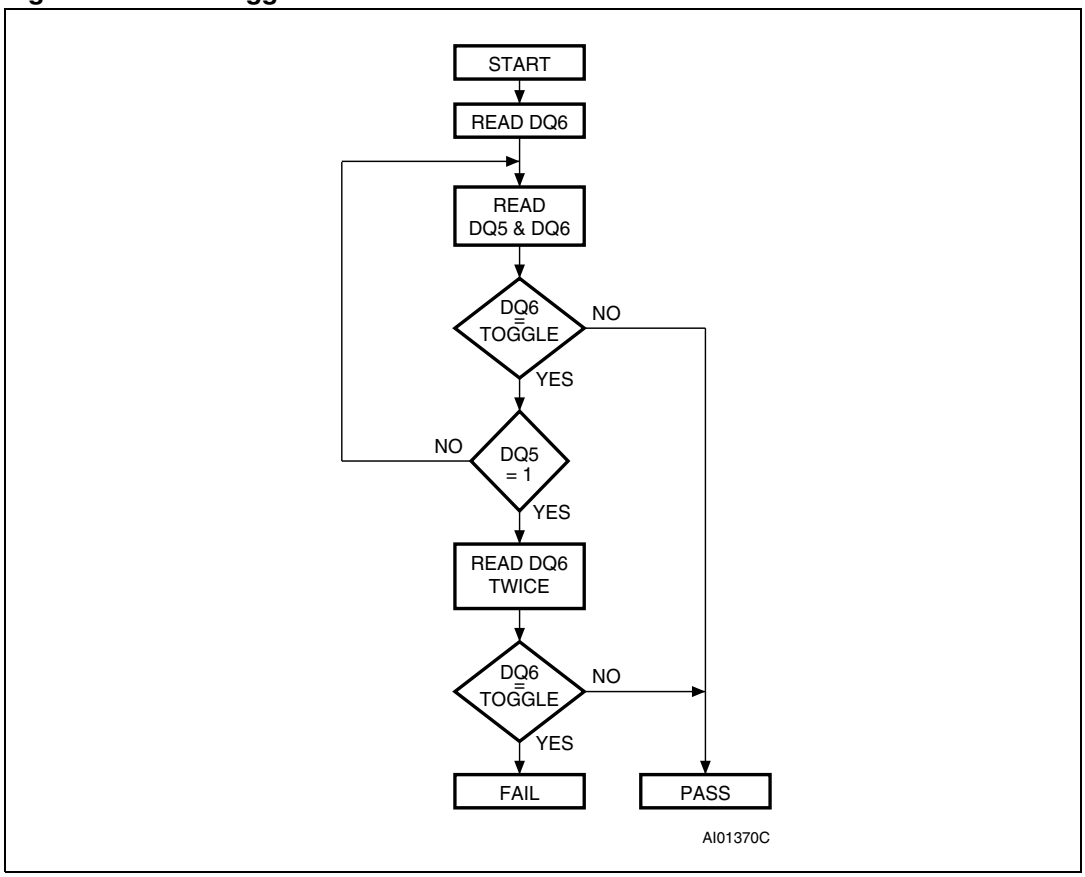


Figure 9. Data toggle flowchart



6 Maximum rating

Stressing the device above the rating listed in *Table 8: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_A	Ambient temperature grade 3	–40	125	°C
T_{BIAS}	Temperature under bias	–50	125	°C
T_{STG}	Storage temperature	–65	150	°C
V_{IO}	Input or output voltage (1)(2)	–0.6	V_{CC}+0.6	V
V_{CC}	Supply voltage	–0.6	4	V
V_{ID}	Identification voltage	–0.6	13.5	V

1. Minimum voltage may undershoot to –2 V during transition and for less than 20 ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2 V during transition and for less than 20 ns during transitions.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 9: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 9. Operating and AC measurement conditions

Parameter	M29W160FT/B, M29W320FT/B				Unit
	70		80		
	Min	Max	Min	Max	
V_{CC} supply voltage	2.7	3.6	2.5	3.6	V
Ambient operating temperature (grade 3)	–40	125	–40	125	°C
Load capacitance (C_L)	30		30		pF
Input rise and fall times		10		10	ns
Input Pulse voltages	0 to V_{CC}		0 to V_{CC}		V
Input and output timing ref. voltages	$V_{CC}/2$		$V_{CC}/2$		V

Figure 10. AC measurement I/O waveform

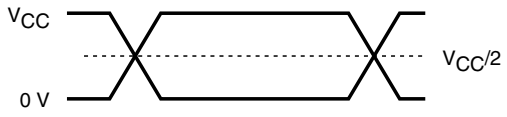


Figure 11. AC measurement load circuit

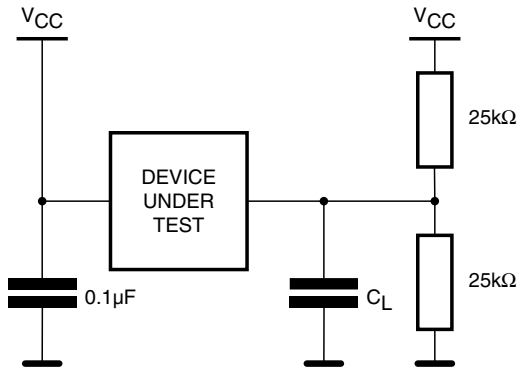


Table 10. Device capacitance(1)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		12	pF

1. Sampled only, not 100% tested.

Table 11. DC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage current	0 V ≤V_{IN} ≤V_{CC}			±1	µA
I_{LO}	Output Leakage current	0 V ≤V_{OUT} ≤V_{CC}			±1	µA
I_{CC1}	Supply current (Read)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 6 MHz		4.5	10	mA
I_{CC2}	Supply current (Standby)	$\overline{E}$ = V_{CC}±0.2 V, $\overline{RP}$ = V_{CC}±0.2 V		35	100	µA
I_{CC3}(1)	Supply current (Program/Erase)	Program/Erase controller active			20	mA
V_{IL}	Input Low voltage		–0.5		0.8	V
V_{IH}	Input High voltage		0.7V_{CC}		V_{CC}+0.3	V
V_{OL}	Output Low voltage	I_{OL} = 1.8 mA			0.45	V
V_{OH}	Output High voltage	I_{OH} = –100 µA	V_{CC}–0.4			V
V_{ID}	Identification voltage		11.5		12.5	V
I_{ID}	Identification current	A9 = V_{ID}			100	µA
V_{LKO}	Program/Erase Lockout supply voltage		1.8		2.3	V

1. Sampled only, not 100% tested.

Figure 12. Read mode AC waveforms

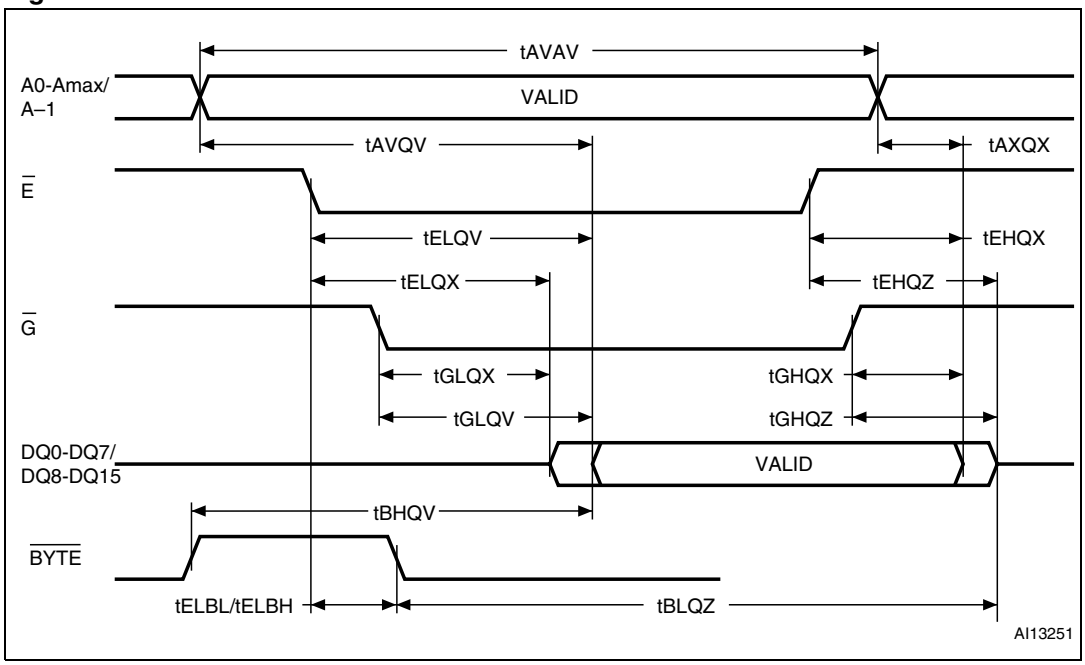


Table 12. Read AC characteristics

Symbol	Alt	Parameter	Test condition		M29Wxx0FT/B		Unit
					70	80	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Min	70	80	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	70	80	ns
t_{ELQX}(1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	70	80	ns
t_{GLQX}(1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	30	35	ns
t_{EHQZ}(1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	25	25	ns
t_{GHQZ}(1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	25	25	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Low or High		Max	5	5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		Max	25	25	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ High to Output Valid		Max	30	30	ns

1. Sampled only, not 100% tested.

Figure 13. Write AC waveforms, Write Enable controlled

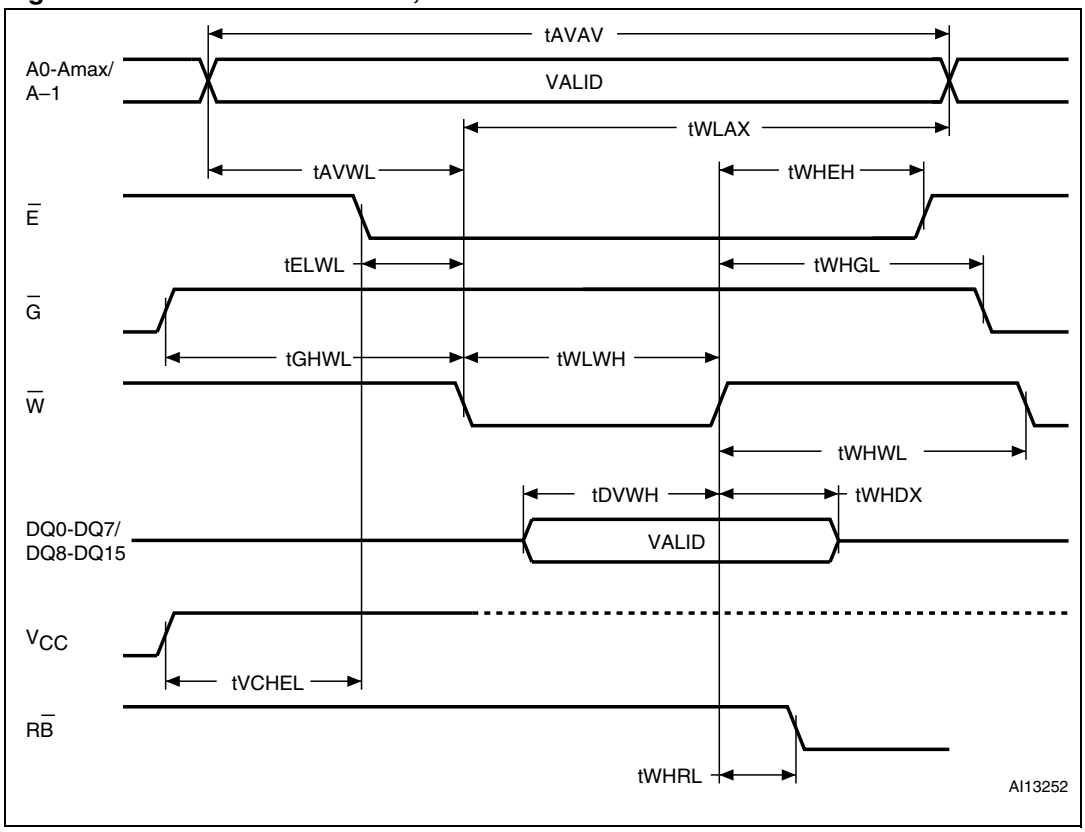


Table 13. Write AC characteristics, Write Enable controlled

Symbol	Alt	Parameter		M29Wxx0FT/B		Unit
				70	80	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	80	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

1. Sampled only, not 100% tested.

Figure 14. Write AC waveforms, Chip Enable controlled

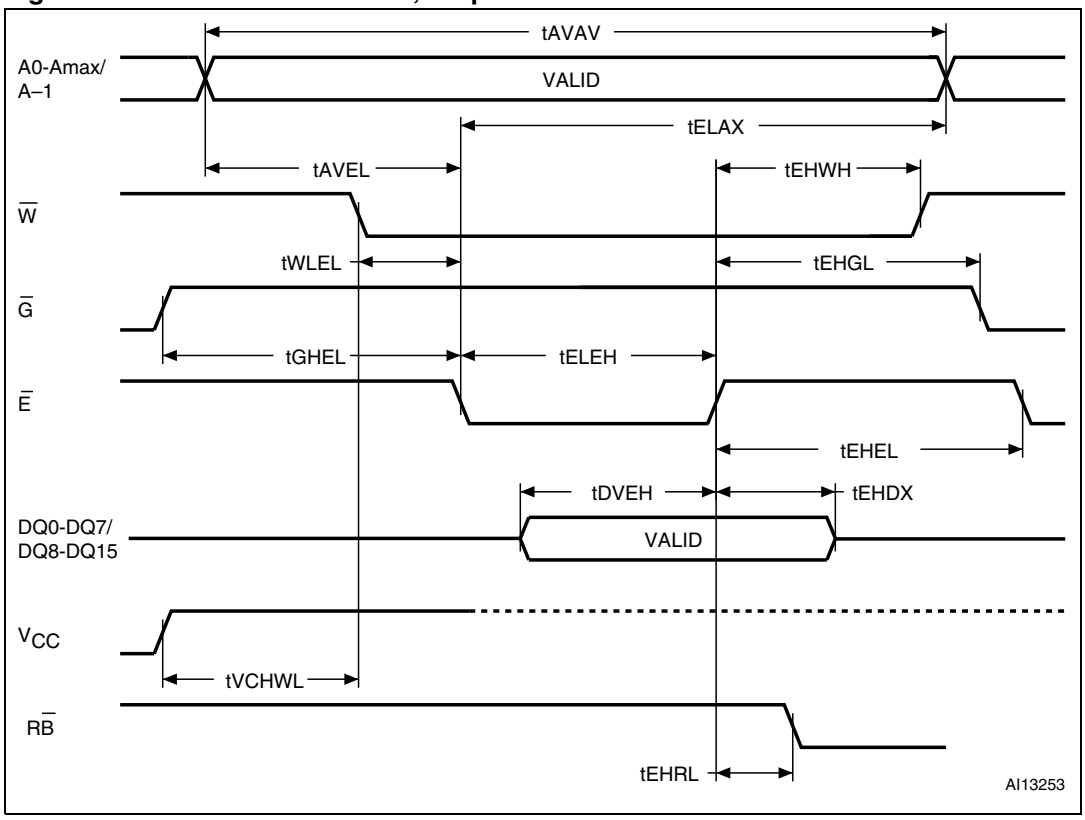


Table 14. Write AC characteristics, Chip Enable controlled

Symbol	Alt	Parameter		M29Wxx0FT/B		Unit
				70	80	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	80	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

1. Sampled only, not 100% tested.

Figure 15. Reset/Block Temporary Unprotect AC waveforms

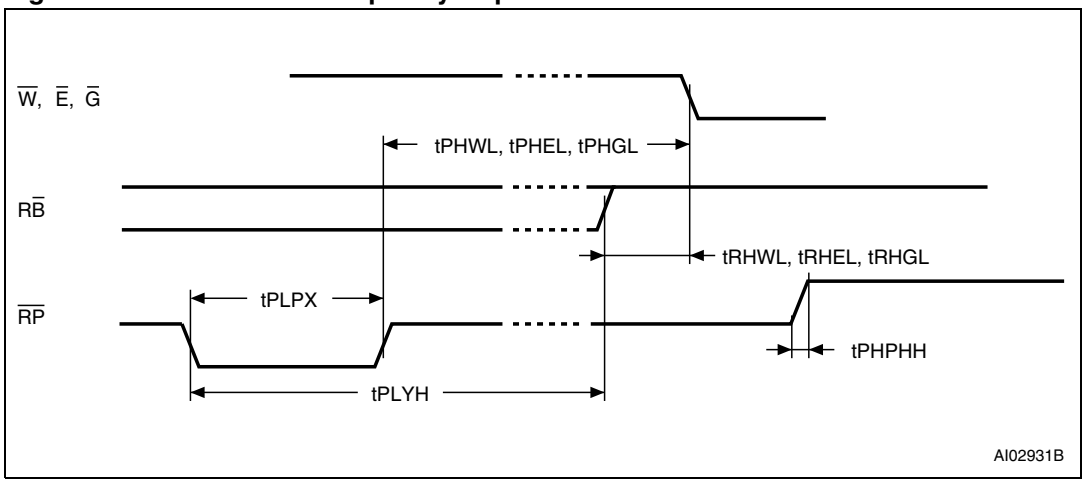
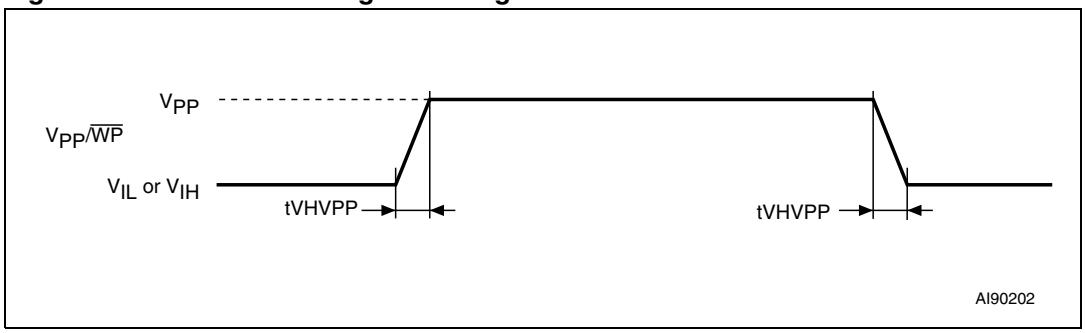


Table 15. Reset/Block Temporary Unprotect AC characteristics

Symbol	Alt	Parameter		M29Wxx0FT/B		Unit
				70	80	
t_{PHWL}(1) t_{PHEL} t_{PHGL}(1)	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{RHWL}(1) t_{RHEL}(1) t_{RHGL}(1)	t_{RB}	$R\overline{B}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	Min	500	500	ns
t_{PLYH}(1)	t_{READY}	$\overline{RP}$ Low to Read mode	Max	10	10	µs
t_{PHPHH}(1)	t_{VIDR}	$\overline{RP}$ Rise time to V_{ID}	Min	500	500	ns
t_{VHVPP}(1)		V_{PP} Rise and Fall time	Min	250	250	ns

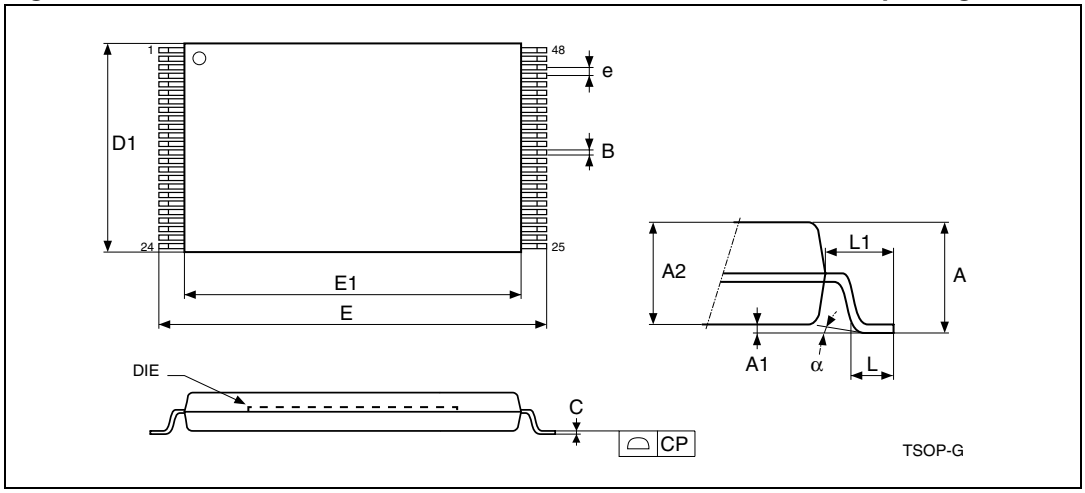
1. Sampled only, not 100% tested.

Figure 16. Accelerated Program timing waveforms



8 Package mechanical

Figure 17. TSOP48 – 48 lead Plastic Thin Small Outline, 12 × 20 mm, package outline



1. Drawing is not to scale.

Table 16. TSOP48 – 48 lead Plastic Thin Small Outline, 12 × 20 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.100	0.050	0.150	0.0039	0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
B	0.220	0.170	0.270	0.0087	0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.100			0.0039
D1	12.000	11.900	12.100	0.4724	0.4685	0.4764
E	20.000	19.800	20.200	0.7874	0.7795	0.7953
E1	18.400	18.300	18.500	0.7244	0.7205	0.7283
e	0.500	–	–	0.0197	–	–
L	0.600	0.500	0.700	0.0236	0.0197	0.0276
L1	0.800			0.0315		
α	3°	0°	5°	3°	0°	5°

Figure 18. TFBGA48 6 x 8 mm - 6 x 8 ball array, 0.80 mm pitch, package outline

Table 17. TFBGA48 6 x 8 mm - 6 x 8 ball array, 0.80 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	4.000	–	–	0.1575	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.600	–	–	0.2205	–	–
e	0.800	–	–	0.0315	–	–
FD	1.000	–	–	0.0394	–	–
FE	1.200	–	–	0.0472	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

9 Part numbering

Table 18. Ordering information scheme

Example: M29W160FB 70 N 3S E

Device type

M29

Operating voltage

W = V_{CC} = 2.7 to 3.6 V (70 ns), 2.5 to 3.6 V (80 ns)

Device function

160F = 16 Mbit (x 8/x 16), Boot block, 0.11 µm

320F = 32 Mbit (x 8/x 16), Boot block, 0.11 µm

Array matrix

T = Top Boot

B = Bottom Boot

Speed

70 = 70 ns

80 = 80 ns

Package

N = TSOP48, 12 × 20 mm

ZA = TFBGA48, 6 x 8 mm, 0.80 mm pitch

Device grade

3 = Automotive grade certified(1), –40 to 125 °C

S = Extended voltage range(2), V_{CC}(min) = 2.5 V

Option

E = ECOPACK® Package, Standard Packing

F = ECOPACK® Package, Tape & Reel Packing

1. Qualified & characterized according to AEC Q100 & Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.
2. This feature could not be available.

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the Numonyx Sales Office nearest to you.

Appendix A Block address table

Table 19. Top boot block addresses, M29W160FT

#	Size (Kbytes)	Address range (x 8)	Address range (x 16)
34	16	1FC000h-1FFFFFh	FE000h-FFFFFh
33	8	1FA000h-1FBFFFh	FD000h-FDFFFh
32	8	1F8000h-1F9FFFh	FC000h-FCFFFh
31	32	1F0000h-1F7FFFh	F8000h-FBFFFh
30	64	1E0000h-1EFFFFh	F0000h-F7FFFh
29	64	1D0000h-1DFFFFh	E8000h-EFFFFh
28	64	1C0000h-1CFFFFh	E0000h-E7FFFh
27	64	1B0000h-1BFFFFh	D8000h-DFFFFh
26	64	1A0000h-1AFFFFh	D0000h-D7FFFh
25	64	190000h-19FFFFh	C8000h-CFFFFh
24	64	180000h-18FFFFh	C0000h-C7FFFh
23	64	170000h-17FFFFh	B8000h-BFFFFh
22	64	160000h-16FFFFh	B0000h-B7FFFh
21	64	150000h-15FFFFh	A8000h-AFFFFh
20	64	140000h-14FFFFh	A0000h-A7FFFh
19	64	130000h-13FFFFh	98000h-9FFFFh
18	64	120000h-12FFFFh	90000h-97FFFh
17	64	110000h-11FFFFh	88000h-8FFFFh
16	64	100000h-10FFFFh	80000h-87FFFh
15	64	0F0000h-0FFFFFh	78000h-7FFFFh
14	64	0E0000h-0EFFFFh	70000h-77FFFh
13	64	0D0000h-0DFFFFh	68000h-6FFFFh
12	64	0C0000h-0CFFFFh	60000h-67FFFh
11	64	0B0000h-0BFFFFh	58000h-5FFFFh
10	64	0A0000h-0AFFFFh	50000h-57FFFh
9	64	090000h-09FFFFh	48000h-4FFFFh
8	64	080000h-08FFFFh	40000h-47FFFh
7	64	070000h-07FFFFh	38000h-3FFFFh
6	64	060000h-06FFFFh	30000h-37FFFh
5	64	050000h-05FFFFh	28000h-2FFFFh
4	64	040000h-04FFFFh	20000h-27FFFh
3	64	030000h-03FFFFh	18000h-1FFFFh
2	64	020000h-02FFFFh	10000h-17FFFh
1	64	010000h-01FFFFh	08000h-0FFFFh
0	64	000000h-00FFFFh	00000h-07FFFh

Table 20. Bottom boot block addresses, M29W160FB

#	Size (Kbytes)	Address range (x 8)	Address range (x 16)
34	64	1F0000h-1FFFFFh	F8000h-FFFFFh
33	64	1E0000h-1EFFFFh	F0000h-F7FFFh
32	64	1D0000h-1DFFFFh	E8000h-EFFFFh
31	64	1C0000h-1CFFFFh	E0000h-E7FFFh
30	64	1B0000h-1BFFFFh	D8000h-DFFFFh
29	64	1A0000h-1AFFFFh	D0000h-D7FFFh
28	64	190000h-19FFFFh	C8000h-CFFFFh
27	64	180000h-18FFFFh	C0000h-C7FFFh
26	64	170000h-17FFFFh	B8000h-BFFFFh
25	64	160000h-16FFFFh	B0000h-B7FFFh
24	64	150000h-15FFFFh	A8000h-AFFFFh
23	64	140000h-14FFFFh	A0000h-A7FFFh
22	64	130000h-13FFFFh	98000h-9FFFFh
21	64	120000h-12FFFFh	90000h-97FFFh
20	64	110000h-11FFFFh	88000h-8FFFFh
19	64	100000h-10FFFFh	80000h-87FFFh
18	64	0F0000h-0FFFFFh	78000h-7FFFFh
17	64	0E0000h-0EFFFFh	70000h-77FFFh
16	64	0D0000h-0DFFFFh	68000h-6FFFFh
15	64	0C0000h-0CFFFFh	60000h-67FFFh
14	64	0B0000h-0BFFFFh	58000h-5FFFFh
13	64	0A0000h-0AFFFFh	50000h-57FFFh
12	64	090000h-09FFFFh	48000h-4FFFFh
11	64	080000h-08FFFFh	40000h-47FFFh
10	64	070000h-07FFFFh	38000h-3FFFFh
9	64	060000h-06FFFFh	30000h-37FFFh
8	64	050000h-05FFFFh	28000h-2FFFFh
7	64	040000h-04FFFFh	20000h-27FFFh
6	64	030000h-03FFFFh	18000h-1FFFFh
5	64	020000h-02FFFFh	10000h-17FFFh
4	64	010000h-01FFFFh	08000h-0FFFFh
3	32	008000h-00FFFFh	04000h-07FFFh
2	8	006000h-007FFFh	03000h-03FFFh
1	8	004000h-005FFFh	02000h-02FFFh
0	16	000000h-003FFFh	00000h-01FFFh

Table 21. Top boot block addresses, M29W320FT

#	Size (Kbyte/Kword)	Address range (x 8)	Address range (x 16)
66	16/8	3FC000h-3FFFFFh	1FE000h-1FFFFFh
65	8/4	3FA000h-3FBFFFh	1FD000h-1FDFFFh
64	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
63	32/16	3F0000h-3F7FFFh	1F8000h-1FBFFFh
62	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
61	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
60	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
59	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
58	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
57	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
56	64/32	380000h-18FFFFh	1C0000h-1C7FFFh
55	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
54	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
53	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
52	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
51	64/32	330000h-33FFFFh	198000h-19FFFFh
50	64/32	320000h-32FFFFh	190000h-197FFFh
49	64/32	310000h-31FFFFh	188000h-18FFFFh
48	64/32	300000h-30FFFFh	180000h-187FFFh
47	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
46	64/32	2E0000h-2EFFFFh	170000h-177FFFh
45	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
44	64/32	2C0000h-2CFFFFh	160000h-167FFFh
43	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
42	64/32	2A0000h-2AFFFFh	150000h-157FFFh
41	64/32	290000h-29FFFFh	148000h-14FFFFh
40	64/32	280000h-28FFFFh	140000h-147FFFh
39	64/32	270000h-27FFFFh	138000h-13FFFFh
38	64/32	260000h-26FFFFh	130000h-137FFFh
37	64/32	250000h-25FFFFh	128000h-12FFFFh
36	64/32	240000h-24FFFFh	120000h-127FFFh
35	64/32	230000h-23FFFFh	118000h-11FFFFh
34	64/32	220000h-22FFFFh	110000h-117FFFh
33	64/32	210000h-21FFFFh	108000h-10FFFFh
32	64/32	200000h-20FFFFh	100000h-107FFFh

Table 21. Top boot block addresses, M29W320FT (continued)

#	Size (Kbyte/Kword)	Address range (x 8)	Address range (x 16)
31	64/32	1F0000h-1FFFFFh	0F8000h-0FBFFFh
30	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
29	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
28	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
27	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
26	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
25	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
24	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
23	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
22	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
21	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
20	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
19	64/32	130000h-13FFFFh	098000h-09FFFFh
18	64/32	120000h-12FFFFh	090000h-097FFFh
17	64/32	110000h-11FFFFh	088000h-08FFFFh
16	64/32	100000h-10FFFFh	080000h-087FFFh
15	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
14	64/32	0E0000h-0EFFFFh	070000h-077FFFh
13	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
12	64/32	0C0000h-0CFFFFh	060000h-067FFFh
11	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
10	64/32	0A0000h-0AFFFFh	050000h-057FFFh
9	64/32	090000h-09FFFFh	048000h-04FFFFh
8	64/32	080000h-08FFFFh	040000h-047FFFh
7	64/32	070000h-07FFFFh	038000h-03FFFFh
6	64/32	060000h-06FFFFh	030000h-037FFFh
5	64/32	050000h-05FFFFh	028000h-02FFFFh
4	64/32	040000h-04FFFFh	020000h-027FFFh
3	64/32	030000h-03FFFFh	018000h-01FFFFh
2	64/32	020000h-02FFFFh	010000h-017FFFh
1	64/32	010000h-01FFFFh	008000h-00FFFFh
0	64/32	000000h-00FFFFh	000000h-007FFFh

Table 22. Bottom boot block addresses, M29W320FB

#	Size (Kbyte/Kword)	Address range (x 8)	Address range (x 16)
66	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh
65	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
64	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
63	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
62	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
61	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
60	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
59	64/32	380000h-18FFFFh	1C0000h-1C7FFFh
58	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
57	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
56	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
55	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
54	64/32	330000h-33FFFFh	198000h-19FFFFh
53	64/32	320000h-32FFFFh	190000h-197FFFh
52	64/32	310000h-31FFFFh	188000h-18FFFFh
51	64/32	300000h-30FFFFh	180000h-187FFFh
50	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
49	64/32	2E0000h-2EFFFFh	170000h-177FFFh
48	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
47	64/32	2C0000h-2CFFFFh	160000h-167FFFh
46	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
45	64/32	2A0000h-2AFFFFh	150000h-157FFFh
44	64/32	290000h-29FFFFh	148000h-14FFFFh
43	64/32	280000h-28FFFFh	140000h-147FFFh
42	64/32	270000h-27FFFFh	138000h-13FFFFh
41	64/32	260000h-26FFFFh	130000h-137FFFh
40	64/32	250000h-25FFFFh	128000h-12FFFFh
39	64/32	240000h-24FFFFh	120000h-127FFFh
38	64/32	230000h-23FFFFh	118000h-11FFFFh
37	64/32	220000h-22FFFFh	110000h-117FFFh
36	64/32	210000h-21FFFFh	108000h-10FFFFh
35	64/32	200000h-20FFFFh	100000h-107FFFh
34	64/32	1F0000h-1FFFFFh	0F8000h-0FBFFFh
33	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
32	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh

Table 22. Bottom boot block addresses, M29W320FB (continued)

#	Size (Kbyte/Kword)	Address range (x 8)	Address range (x 16)
31	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
30	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
29	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
28	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
27	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
26	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
25	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
24	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
23	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
22	64/32	130000h-13FFFFh	098000h-09FFFFh
21	64/32	120000h-12FFFFh	090000h-097FFFh
20	64/32	110000h-11FFFFh	088000h-08FFFFh
19	64/32	100000h-10FFFFh	080000h-087FFFh
18	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
17	64/32	0E0000h-0EFFFFh	070000h-077FFFh
16	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
15	64/32	0C0000h-0CFFFFh	060000h-067FFFh
14	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
13	64/32	0A0000h-0AFFFFh	050000h-057FFFh
12	64/32	090000h-09FFFFh	048000h-04FFFFh
11	64/32	080000h-08FFFFh	040000h-047FFFh
10	64/32	070000h-07FFFFh	038000h-03FFFFh
9	64/32	060000h-06FFFFh	030000h-037FFFh
8	64/32	050000h-05FFFFh	028000h-02FFFFh
7	64/32	040000h-04FFFFh	020000h-027FFFh
6	64/32	030000h-03FFFFh	018000h-01FFFFh
5	64/32	020000h-02FFFFh	010000h-017FFFh
4	64/32	010000h-01FFFFh	008000h-00FFFFh
3	32/16	008000h-00FFFFh	004000h-007FFFh
2	8/4	006000h-007FFFh	003000h-003FFFh
1	8/4	004000h-005FFFh	002000h-002FFFh
0	16/8	000000h-003FFFh	000000h-001FFFh

Appendix B Common Flash interface (CFI)

The common flash interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables *23*, *24*, *25*, *26*, *27* and *28* show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see *Table 28: Security code area*). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by Numonyx. Issue a Read command to return to Read mode.

Table 23. Query structure overview(1)

Address		Sub-section name	Description
x 16	x 8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing & voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)
61h	C2h	Security code area	64 bit unique device number

1. Query data are always presented on the lowest order data outputs.

Table 24. CFI query identification string(1)

Address		Data	Description	Value
x 16	x 8			
10h	20h	0051h	Query Unique ASCII String "QRY"	"Q"
11h	22h	0052h		"R"
12h	24h	0059h		"Y"
13h	26h	0002h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm	AMD Compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for primary algorithm extended query table (see *Table 27*)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate vendor command set and control interface id code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for alternate algorithm extended query table	NA
1Ah	34h	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are '0'.

Table 25. CFI query system interface information

Address		Data	Description		Value
x 16	x 8				
1Bh	36h	0027h	V_{CC} logic supply minimum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV		2.7 V
1Ch	38h	0036h	V_{CC} logic supply maximum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV		3.6 V
1Dh	3Ah	0000h	M29W160FT/B	V_{PP} [programming] supply minimum Program/Erase voltage	NA
		00B5h	M29W320FT/B	V_{PP} [programming] supply minimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	11.5 V
1Eh	3Ch	0000h	M29W160FT/B	V_{PP} [programming] supply maximum Program/Erase voltage	NA
		00C5h	M29W320FT/B	V_{PP} [programming] supply maximum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	12.5 V
1Fh	3Eh	0004h	Typical timeout per single byte/word program = 2^n µs		16 µs
20h	40h	0000h	Typical timeout for minimum size write buffer program = 2^n µs		NA
21h	42h	000Ah	Typical timeout per individual block erase = 2^n ms		1 s
22h	44h	0000h	Typical timeout for full chip erase = 2^n ms		NA
23h	46h	0004h	M29W160FT/B	Maximum timeout for byte/word program = 2^n times typical	256 µs
		0005h	M29W320FT/B	Maximum timeout for byte/word program = 2^n times typical	512 µs
24h	48h	0000h	Maximum timeout for write buffer program = 2^n times typical		NA
25h	4Ah	0003h	M29W160FT/B	Maximum timeout per individual block erase = 2^n times typical	8 s
		0004h	M29W320FT/B	Maximum timeout per individual block erase = 2^n times typical	16 s
26h	4Ch	0000h	Maximum timeout for chip erase = 2^n times typical		NA

Table 26. Device geometry definition

Address x 16	Address x 8	Data	Description	Value
27h	4Eh	0015h	M29W160FT/B device size = 2^n in number of bytes	2 Mbyte
		0016h	M29W320FT/B device size = 2^n in number of bytes	4 Mbyte
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x 8, x 16 Async.
2Ah 2Bh	54h 56h	0000h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	NA
2Ch	58h	0004h	Number of Erase Block Regions within the device. It specifies the number of regions within the device containing contiguous Erase Blocks of the same size.	4
2Dh 2Eh	5Ah 5Ch	0000h 0000h	Region 1 information Number of identical size erase block = 0000h+1	1
2Fh 30h	5Eh 60h	0040h 0000h	Region 1 information Block size in Region 1 = 0040h * 256 byte	16 Kbyte
31h 32h	62h 64h	0001h 0000h	Region 2 information Number of identical size erase block = 0001h+1	2
33h 34h	66h 68h	0020h 0000h	Region 2 information Block size in Region 2 = 0020h * 256 byte	8 Kbyte
35h 36h	6Ah 6Ch	0000h 0000h	Region 3 information Number of identical size erase block = 0000h+1	1
37h 38h	6Eh 70h	0080h 0000h	Region 3 Information Block size in Region 3 = 0080h * 256 byte	32 Kbyte
39h 3Ah	72h 74h	001Eh 0000h	M29W160FT/B Region 4 information Number of identical-size erase block = 001Eh+1	31
		003Eh 0000h	M29W320FT/B Region 4 information Number of identical-size erase block = 003Eh+1	63
3Bh 3Ch	76h 78h	0000h 0001h	Region 4 information Block size in Region 4 = 0100h * 256 byte	64 Kbyte

Table 27. Primary algorithm-specific extended query table

Address		Data	Description	Value
x 16	x 8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string “PRI”	"P"
41h	82h	0052h		"R"
42h	84h	0049h		"I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0030h	Minor version number, ASCII	"0"
45h	8Ah	0000h	Address Sensitive Unlock (bits 1 to 0) 00 = required, 01= not required Silicon Revision Number (bits 7 to 2)	Yes
46h	8Ch	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = Read and Write	2
47h	8Eh	0001h	Block Protection 00 = not supported, x = number of blocks in per group	1
48h	90h	0001h	Temporary Block Unprotect 00 = not supported, 01 = supported	Yes
49h	92h	0004h	Block Protect /Unprotect 04 = M29W400B	4
4Ah	94h	0000h	Simultaneous operations, 00 = not supported	No
4Bh	96h	0000h	Burst mode, 00 = not supported, 01 = supported	No
4Ch	98h	0000h	Page mode, 00 = not supported, 01 = 4 page word, 02 = 8 page word	No
4Dh(1)	9Ah	00B5h	V_{PP} supply minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5 V
4Eh(1)	9Ch	00C5h	V_{PP} supply minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5 V
4Fh(1)	9Eh	000xh	Top/Bottom Boot Block Flag 02h = Bottom Boot device, 03h = Top Boot device	–

1. Only for the M29W320FT/B devices.

Table 28. Security code area

Address		Data	Description
x16	x8		
61h	C3h, C2h	XXXX	64 bit: unique device number
62h	C5h, C4h	XXXX	
63h	C7h, C6h	XXXX	
64h	C9h, C8h	XXXX	

Appendix C Block protection

Block protection can be used to prevent any operation from modifying the data stored in the Flash memory. Each Block can be protected individually. Once protected, Program and Erase operations on the block fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the signal descriptions section.

Unlike the command interface of the Program/Erase controller, the techniques for protecting and unprotecting blocks could change between different Flash memory suppliers.

9.1 Programmer technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a block follow the flowchart in *Figure 19: Programmer equipment block protect flowchart*. During the Block Protect algorithm, the Amax-A12 address inputs indicate the address of the block to be protected. The block will be correctly protected only if Amax-A12 remain valid and stable, and if Chip Enable is kept Low, V_{IL}, all along the Protect and Verify phases.

The Chip Unprotect algorithm is used to unprotect all the memory blocks at the same time. This algorithm can only be used if all of the blocks are protected first. To unprotect the chip follow *Figure 20: Programmer equipment chip unprotect flowchart*. *Table 29: Programmer technique bus operations, BYTE = V_{IH} or V_{IL}*, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

9.2 In-system technique

The in-system technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the Flash memory has been fitted to the system.

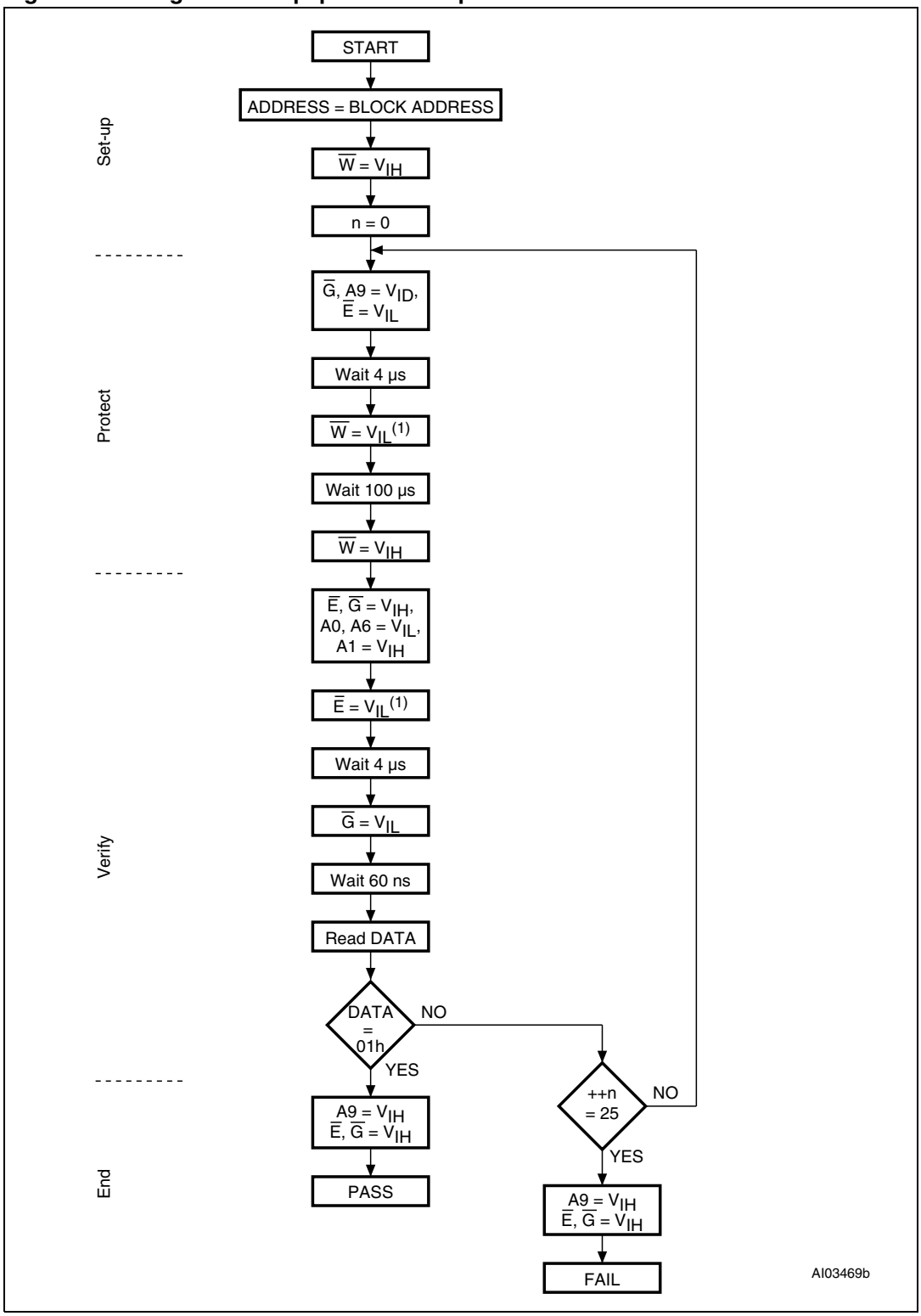
To protect a block follow the flowchart in *Figure 21: In-system equipment block protect flowchart*. To unprotect the whole chip it is necessary to protect all of the blocks first, then all the blocks can be unprotected at the same time. To unprotect the chip follow *Figure 22: In-system equipment chip unprotect flowchart*.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

Table 29. Programmer technique bus operations, $\overline{BYTE}$ = V_{IH} or V_{IL}

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs A0-Amax	Data inputs/outputs DQ15A–1, DQ14-DQ0
Block Protect	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12-Amax Block Address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12 = V_{IH}, A15 = V_{IH} Others = X	X
Block Protection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, A12-Amax Block Address Others = X	Pass = XX01h Retry = XX00h
Block Unprotection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IH}, A9 = V_{ID}, A12-Amax Block Address Others = X	Retry = XX01h Pass = XX00h

Figure 19. Programmer equipment block protect flowchart



1. Address inputs Amax-A12 give the address of the block that is to be protected. It is imperative that they remain stable during the operation.
2. During the Protect and Verify phases of the algorithm, Chip Enable $\overline{E}$ must be kept Low, V_{IL}.

Figure 20. Programmer equipment chip unprotect flowchart

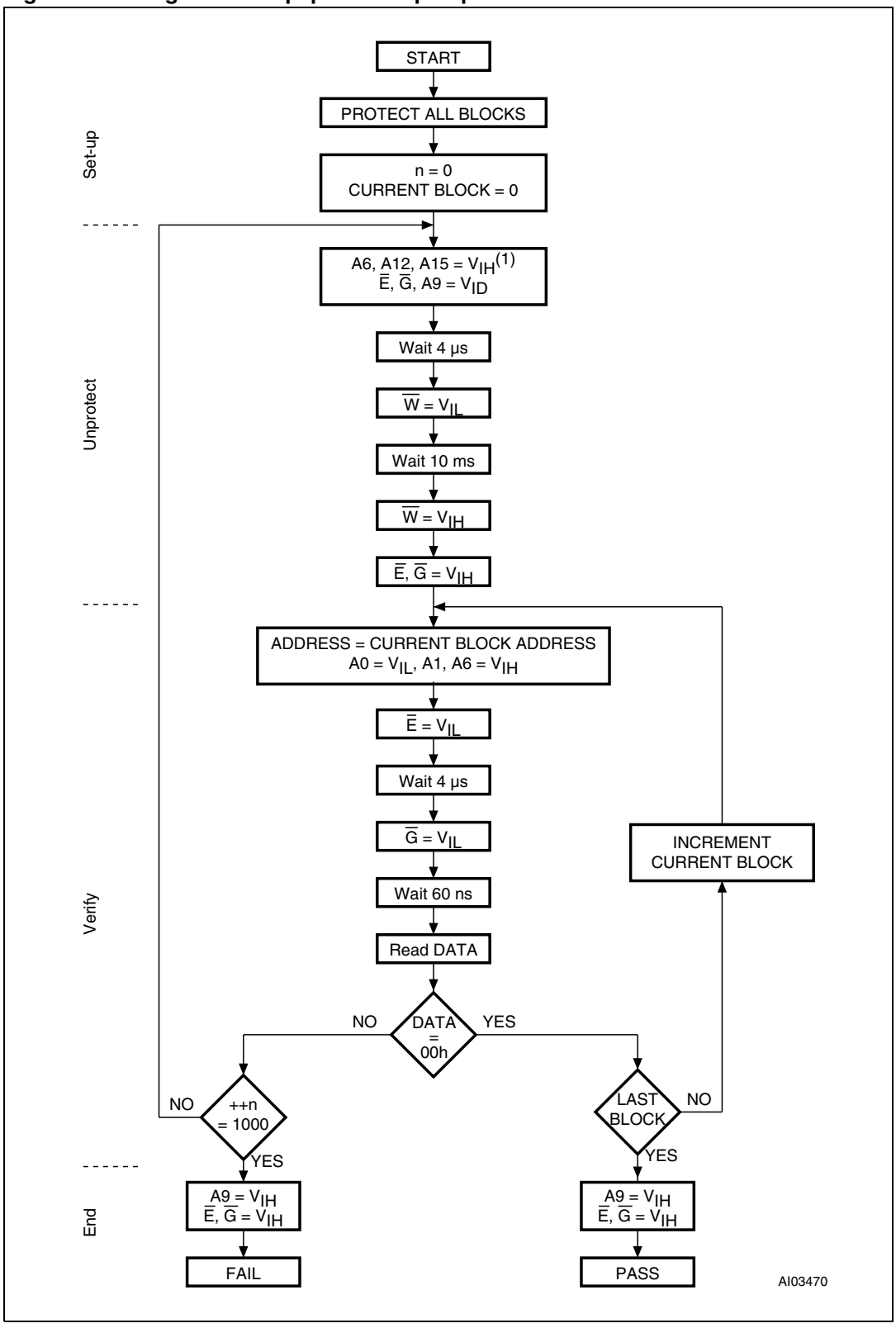


Figure 21. In-system equipment block protect flowchart

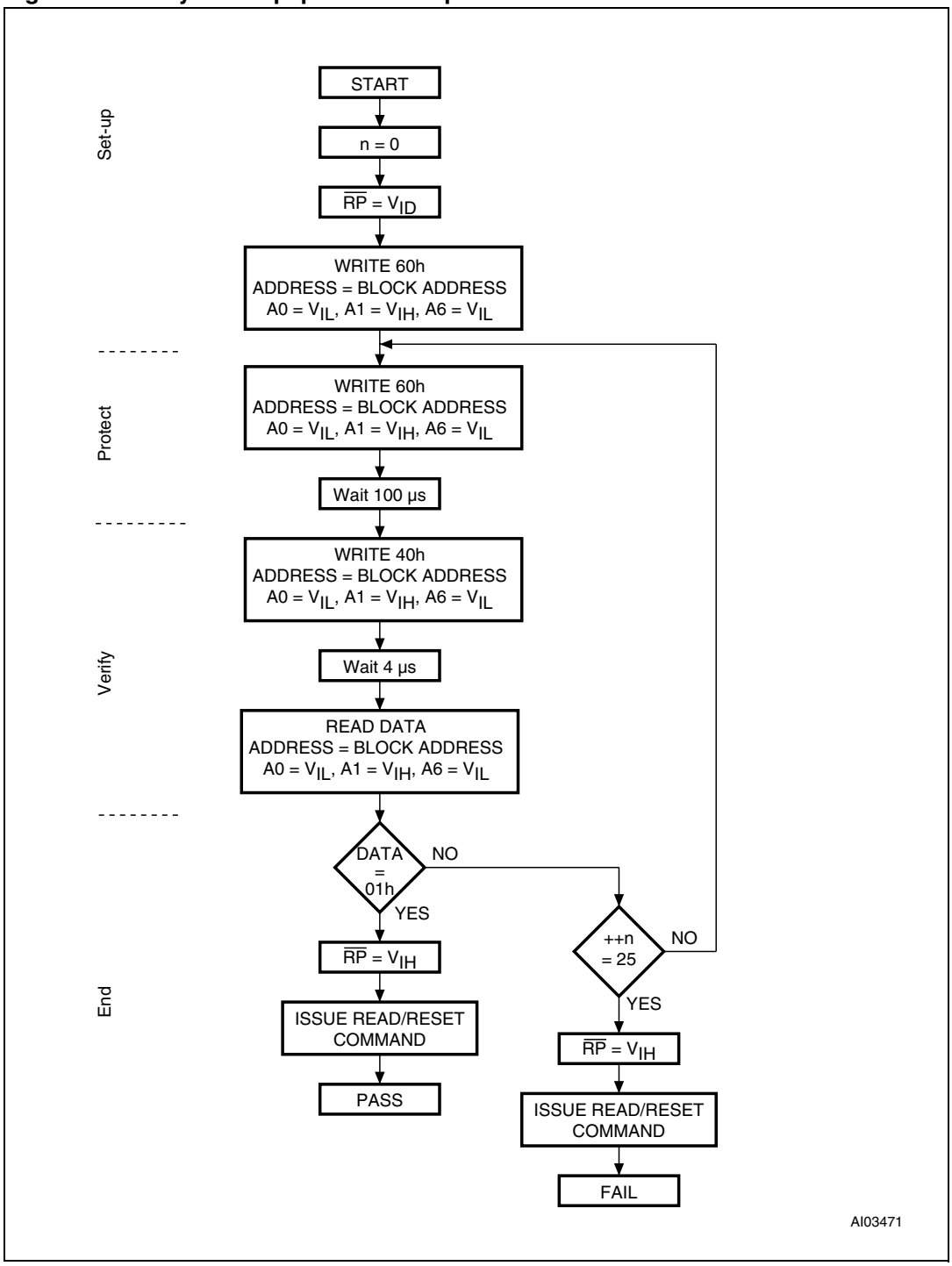
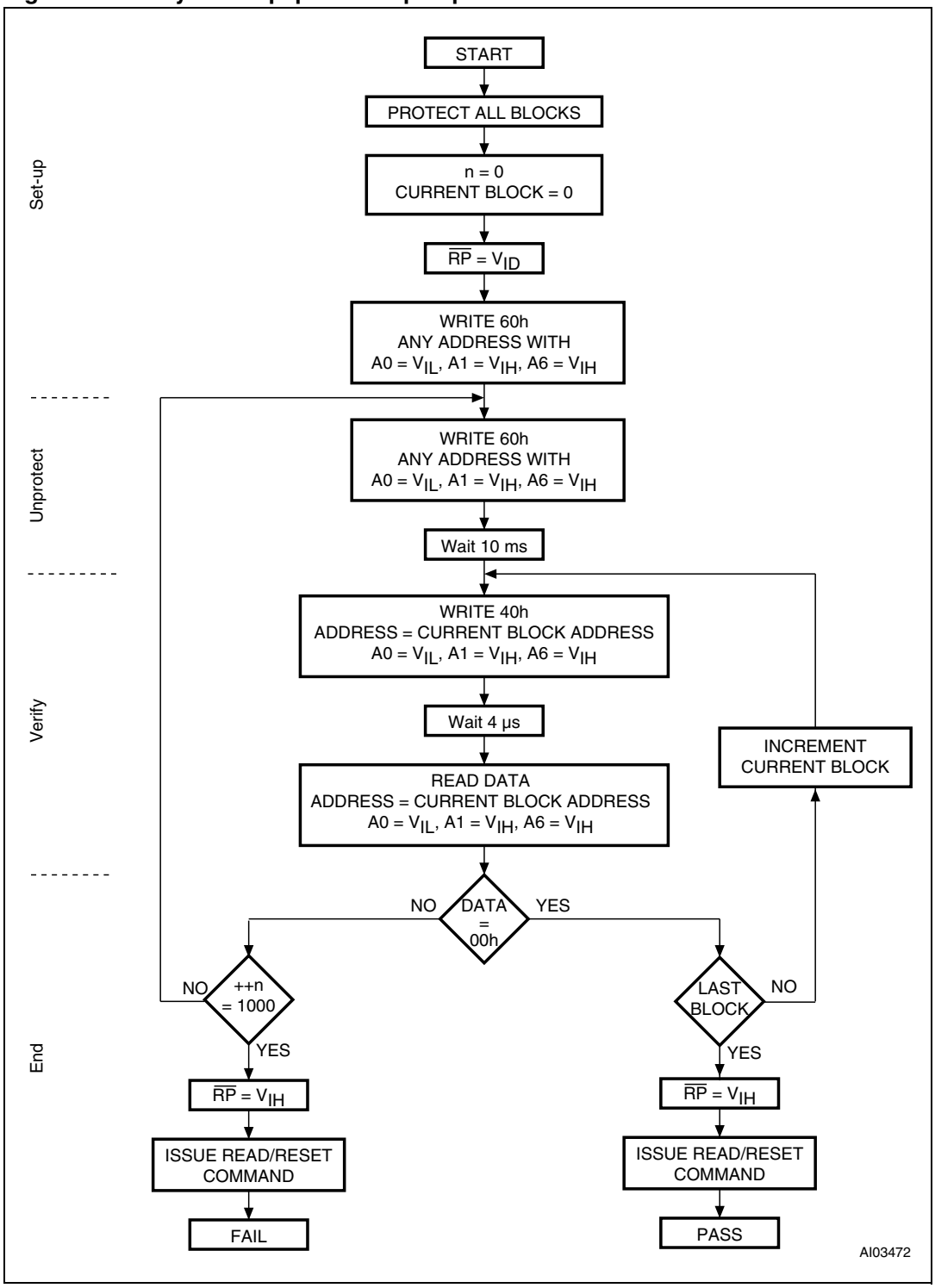


Figure 22. In-system equipment chip unprotect flowchart



10 Revision history

Table 30. Document revision history

Date	Revision	Changes
26-Jun-2006	1	Initial release.
20-Jul-2007	2	Document status promoted from Preliminary Data to full Datasheet. TFBGA48 6 x 8 mm package added. 80 ns speed class added. Voltage range extended when access time is 80 ns. Small text changes.
26-Mar-2008	3	Applied Numonyx branding.

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