PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37516F8HP is the 8-bit microcomputer based on the 740 family core technology.
The M37516F8HP is designed for household products and office automation equipment and includes serial I/O functions, 8-bit timer, A-D converter, and I²C-BUS interface.

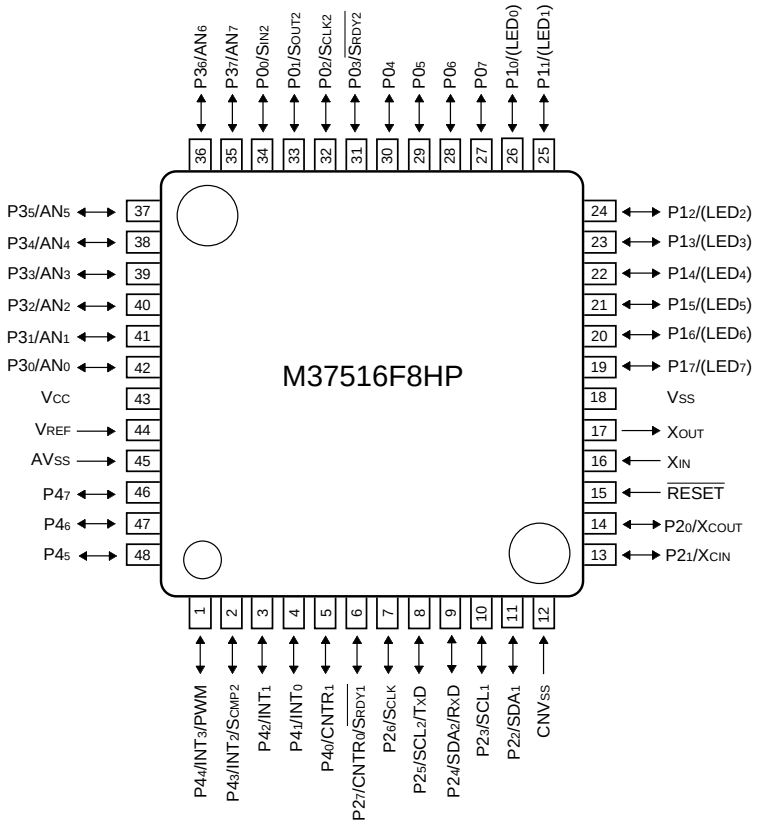
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.5 µs (at 8 MHz oscillation frequency)
- Memory size
  - Flash memory ..... 32 Kbytes
  - RAM ..... 1 Kbytes
- Programmable input/output ports 40
- Interrupts ..... 17 sources, 16 vectors
- Timers ..... 8-bit × 4
- Serial I/O1 ..... 8-bit × 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit × 1(Clock-synchronized)
- Multi-master I²C-BUS interface (option) ..... 1 channel
- PWM ..... 8-bit × 1
- A-D converter ..... 10-bit × 8 channels
- Watchdog timer ..... 16-bit × 1
- Clock generating circuit ..... Built-in 2 circuits (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  - In high-speed mode ..... 4.0 to 5.5 V (at 8 MHz oscillation frequency)
  - In high-speed mode ..... 2.7 to 5.5 V (at 4 MHz oscillation frequency)
  - In middle-speed mode ..... 2.7 to 5.5 V (at 8 MHz oscillation frequency)
  - In low-speed mode ..... 2.7 to 5.5 V (at 32 kHz oscillation frequency)
- Power dissipation
  - In high-speed mode ..... 34 mW (at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... T.B.D. (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... –20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 48P6Q-A

Fig. 1 M37516F8HP pin configuration

FUNCTIONAL BLOCK

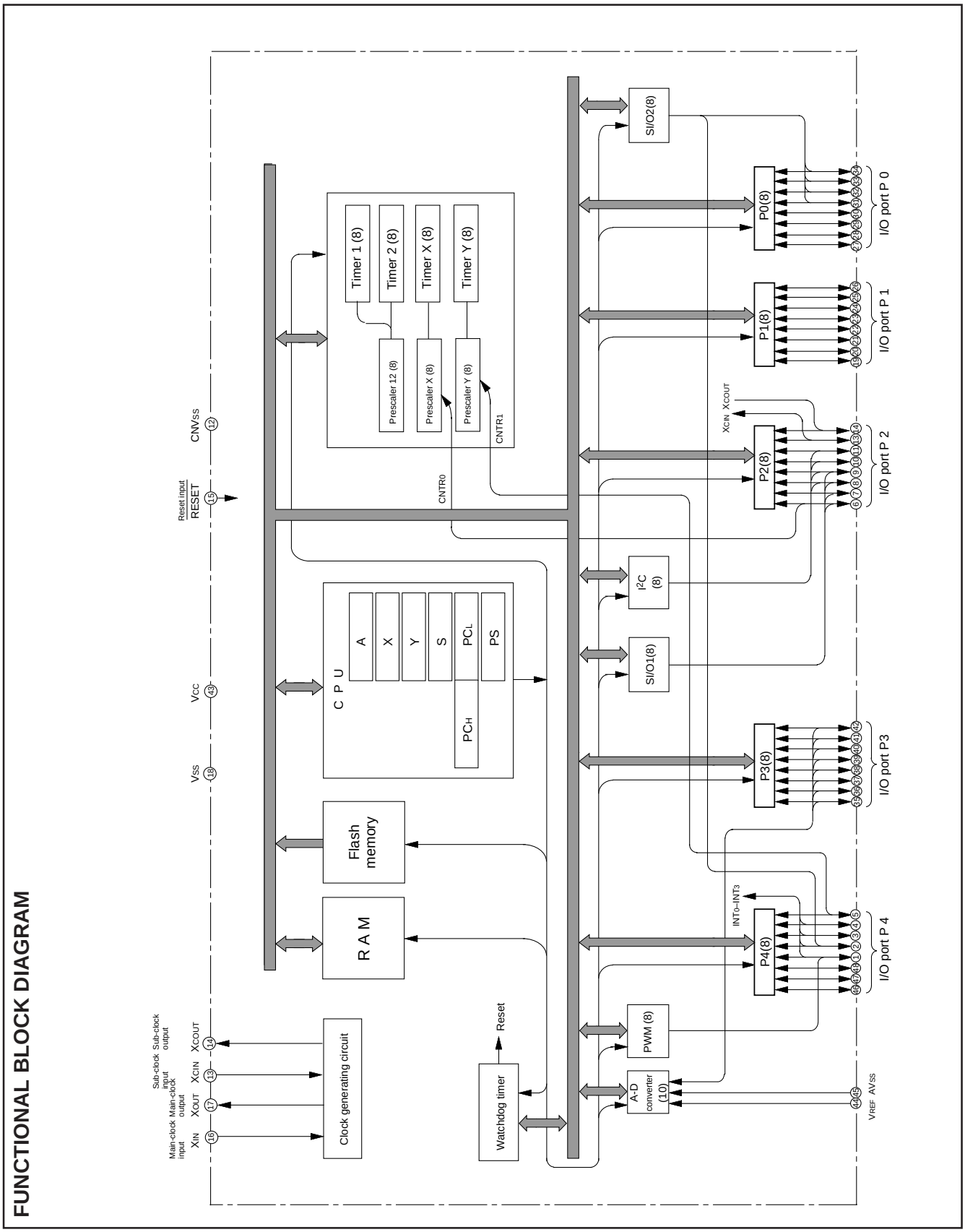


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to VSS.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active "L."	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/SIN2 P01/SOUT2 P02/$\overline{\text{SCLK2}}$ P03/$\overline{\text{SRDY2}}$	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure.	• Serial I/O2 function pin
P04–P07			
P10/–P17	I/O port P1	•P10 to P17 (8 bits) are enabled to output large current for LED drive.	
P20/XCOUT P21/XCIN	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •P22 to P25 can be switched between CMOS compatible input level or SMBUS input level in the I^2C-BUS interface function. •P20, P21, P24 to P27: CMOS3-state output structure. •P24, P25: N-channel open-drain structure in the I^2C-BUS interface function. •P22, P23: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonator)
P22/SDA1 P23/SCL1			• I^2C-BUS interface function pins
P24/SDA2/RxD P25/SCL2/TxD			• I^2C-BUS interface function pin/ Serial I/O1 function pins
P26/SCLK			• Serial I/O1 function pin
P27/$\overline{\text{CNTR0}}$/$\overline{\text{SRDY1}}$			• Serial I/O1 function pin/ Timer X function pin
P30/AN0– P37/AN7	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
P40/CNTR1	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin
P41/INT0 P42/INT1			• Interrupt input pins
P43/INT2/SCMP2			• Interrupt input pin/SCMP2 output pin
P44/INT3/PWM			• Interrupt input pin/PWM output pin
P45–P47			

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The M37516F8HP uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc. The CPU mode register is allocated at address 003B16.

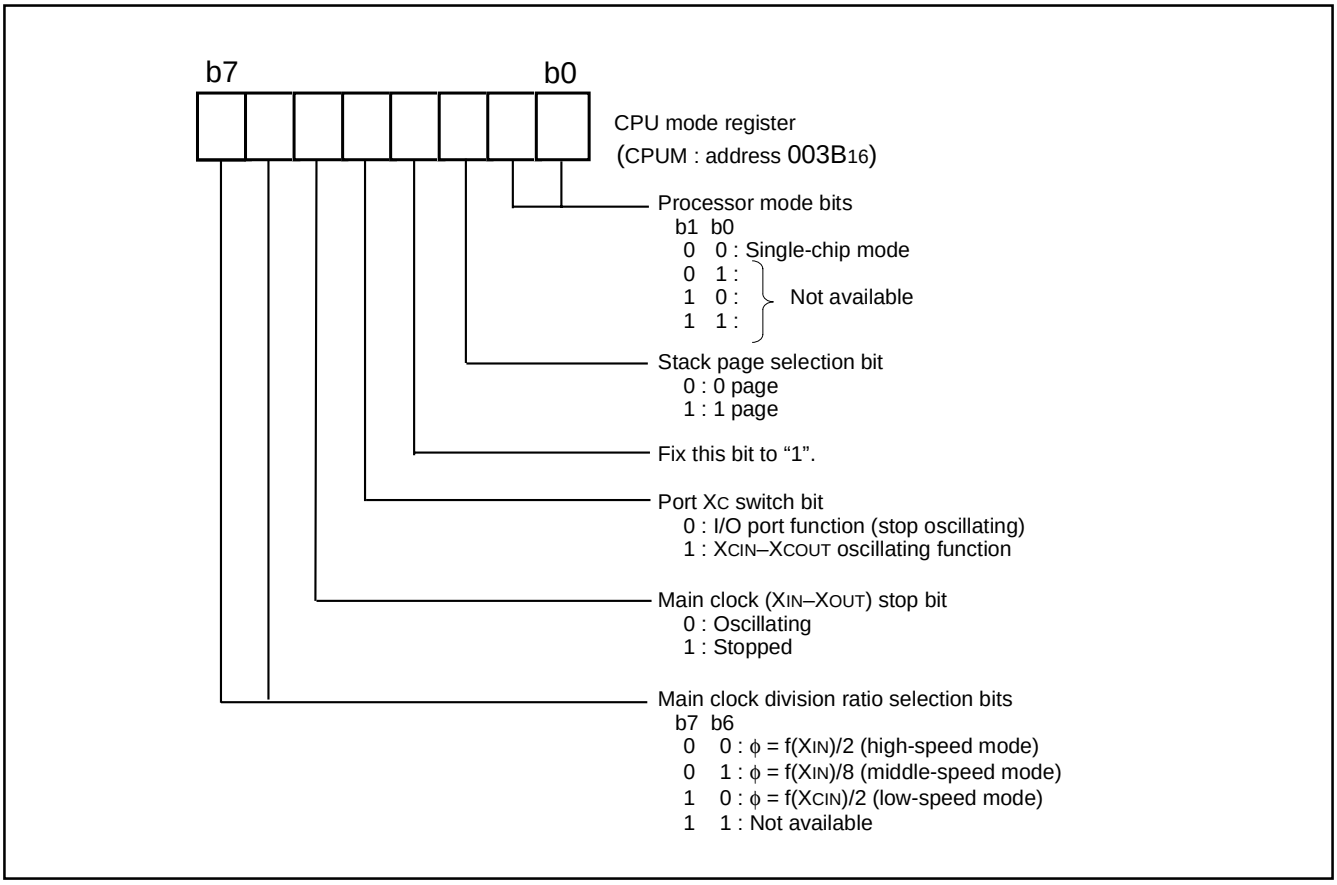


Fig. 3 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

Flash Memory

The first 128 bytes and the last 2 bytes of flash memory are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

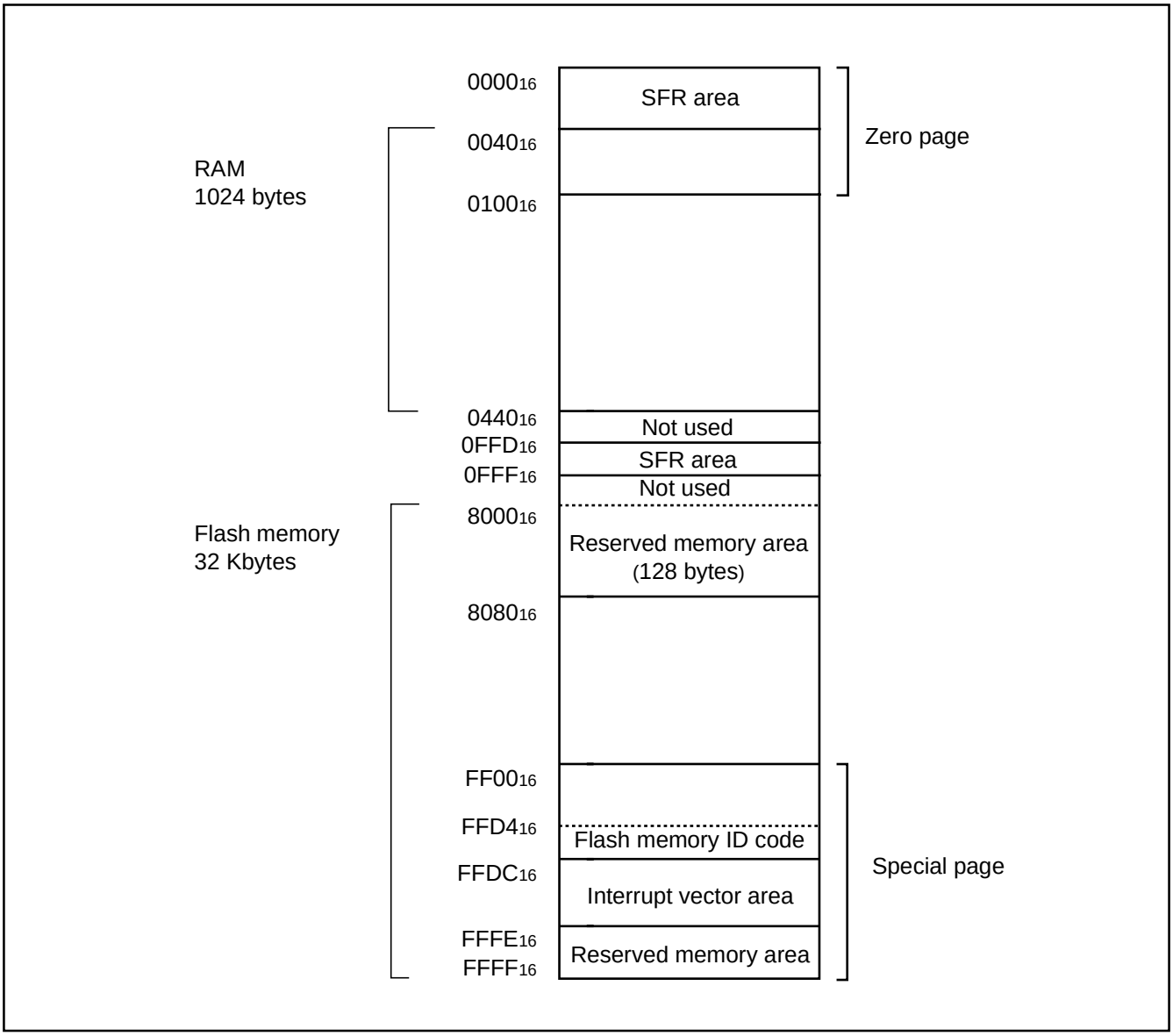


Fig. 4 Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	
000B₁₆	
000C₁₆	
000D₁₆	
000E₁₆	
000F₁₆	
0010₁₆	
0011₁₆	
0012₁₆	Reserved ✻
0013₁₆	Reserved ✻
0014₁₆	Reserved ✻
0015₁₆	Serial I/O2 control register 1 (SIO2CON1)
0016₁₆	Serial I/O2 control register 2 (SIO2CON2)
0017₁₆	Serial I/O2 register (SIO2)
0018₁₆	Transmit/Receive buffer register (TB/RB)
0019₁₆	Serial I/O1 status register (SIOSTS)
001A₁₆	Serial I/O1 control register (SIOCON)
001B₁₆	UART control register (UARTCON)
001C₁₆	Baud rate generator (BRG)
001D₁₆	PWM control register (PWMCON)
001E₁₆	PWM prescaler (PREPWM)
001F₁₆	PWM register (PWM)

0020₁₆	Prescaler 12 (PRE12)
0021₁₆	Timer 1 (T1)
0022₁₆	Timer 2 (T2)
0023₁₆	Timer XY mode register (TM)
0024₁₆	Prescaler X (PREX)
0025₁₆	Timer X (TX)
0026₁₆	Prescaler Y (PREY)
0027₁₆	Timer Y (TY)
0028₁₆	Timer count source selection register (TCSS)
0029₁₆	
002A₁₆	
002B₁₆	I^2C data shift register (S0)
002C₁₆	I^2C address register (S0D)
002D₁₆	I^2C status register (S1)
002E₁₆	I^2C control register (S1D)
002F₁₆	I^2C clock control register (S2)
0030₁₆	I^2C start/stop condition control register (S2D)
0031₁₆	Reserved ✻
0032₁₆	
0033₁₆	
0034₁₆	A-D control register (ADCON)
0035₁₆	A-D conversion low-order register (ADL)
0036₁₆	A-D conversion high-order register (ADH)
0037₁₆	Reserved ✻
0038₁₆	MISRG
0039₁₆	Watchdog timer control register (WDTCON)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)
003E₁₆	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)

0FFD₁₆	Reserved ✻
0FFE₁₆	Flash memory control register (FCON)
0FFF₁₆	Reserved ✻

✻ Reserved : Do not write any data to the reserved area.

Fig. 5 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

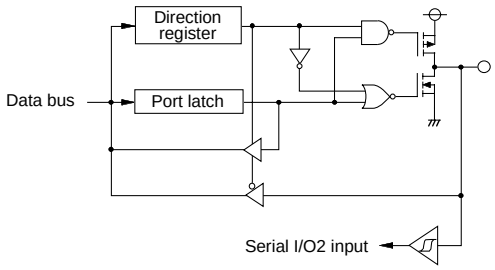
When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

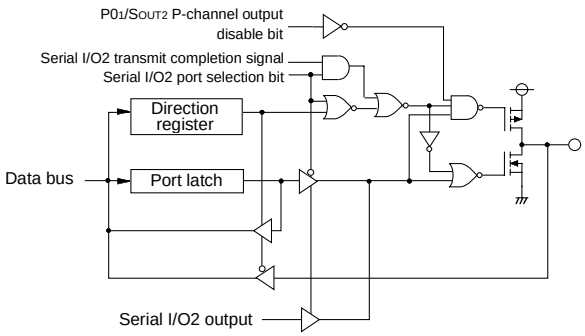
Table 2 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P0$_0$/SIN$_2$ P0$_1$/SOUT$_2$ P0$_2$/$\overline{\text{SCLK2}}$ P0$_3$/$\overline{\text{SRDY2}}$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
P0$_4$–P0$_7$						(5)
P1$_0$/–P1$_7$	Port P1					
P2$_0$/XCOUT P2$_1$/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
P2$_2$/SDA$_1$ P2$_3$/SCL$_1$			CMOS compatible input level CMOS/SMBUS input level (when selecting I^{2}C-BUS interface function) N-channel open-drain output	I^{2}C-BUS interface function I/O	I^{2}C control register	(8) (9)
P2$_4$/SDA$_2$/RxD P2$_5$/SCL$_2$/TxD			CMOS compatible input level CMOS/SMBUS input level (when selecting I^{2}C-BUS interface function) CMOS 3-state output N-channel open-drain output (when selecting I^{2}C-BUS interface function)	I^{2}C-BUS interface function I/O Serial I/O1 function I/O	I^{2}C control register Serial I/O1 control register	(10) (11)
P2$_6$/SCLK			CMOS compatible input level	Serial I/O1 function I/O	Serial I/O1 control register	(12)
P2$_7$/$\overline{\text{CNTR0}}$/$\overline{\text{SRDY1}}$			CMOS 3-state output	Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(13)
P3$_0$/AN$_0$– P3$_7$/AN$_7$	Port P3			A-D conversion input	A-D control register	(14)
P4$_0$/CNTR$_1$	Port P4			Timer Y function I/O	Timer XY mode register	(15)
P4$_1$/INT$_0$ P4$_2$/INT$_1$				External interrupt input	Interrupt edge selection register	(16)
P4$_3$/INT$_2$/SCMP2				External interrupt input SCMP2 output	Interrupt edge selection register Serial I/O2 control register	(17)
P4$_4$/INT$_3$/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(18)
P4$_5$–P4$_7$						(5)

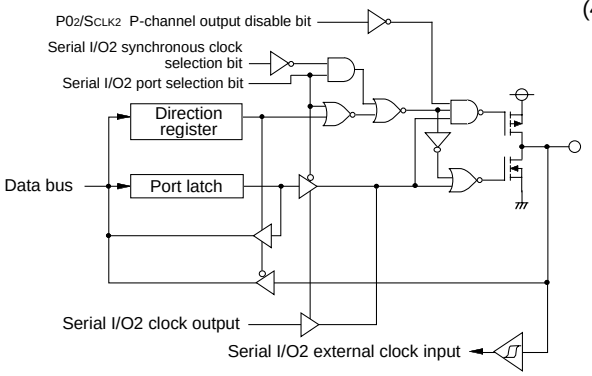
(1) Port P0$_0$



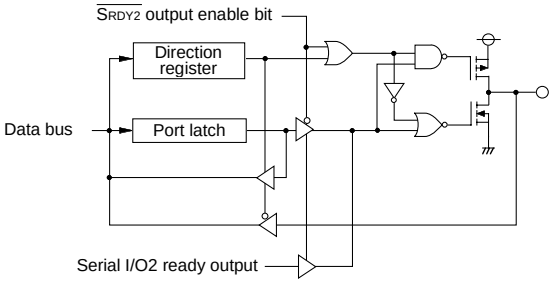
(2) Port P0$_1$



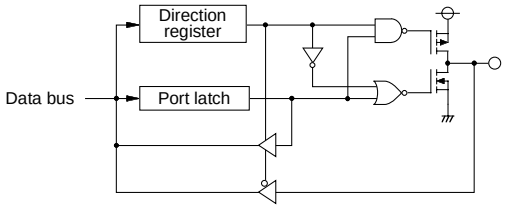
(3) Port P0$_2$



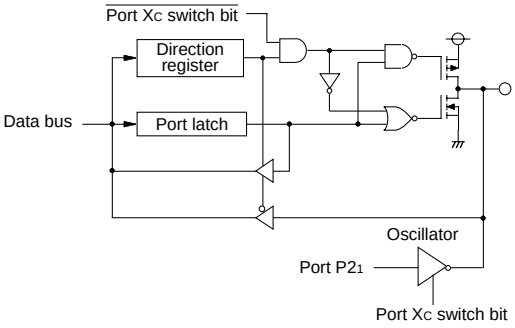
(4) Port P0$_3$



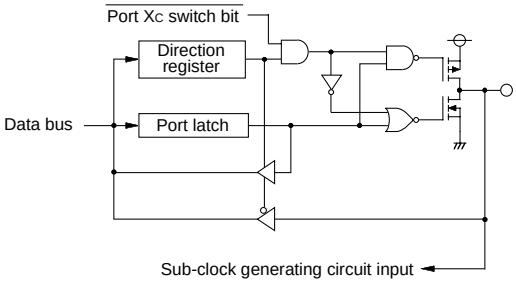
(5) Ports P0$_4$–P0$_7$, P1, P4$_5$–P4$_7$



(6) Port P2$_0$



(7) Port P2$_1$



(8) Port P2$_2$

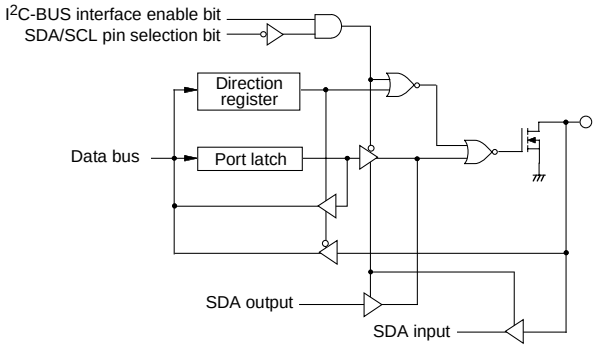


Fig. 6 Port block diagram (1)

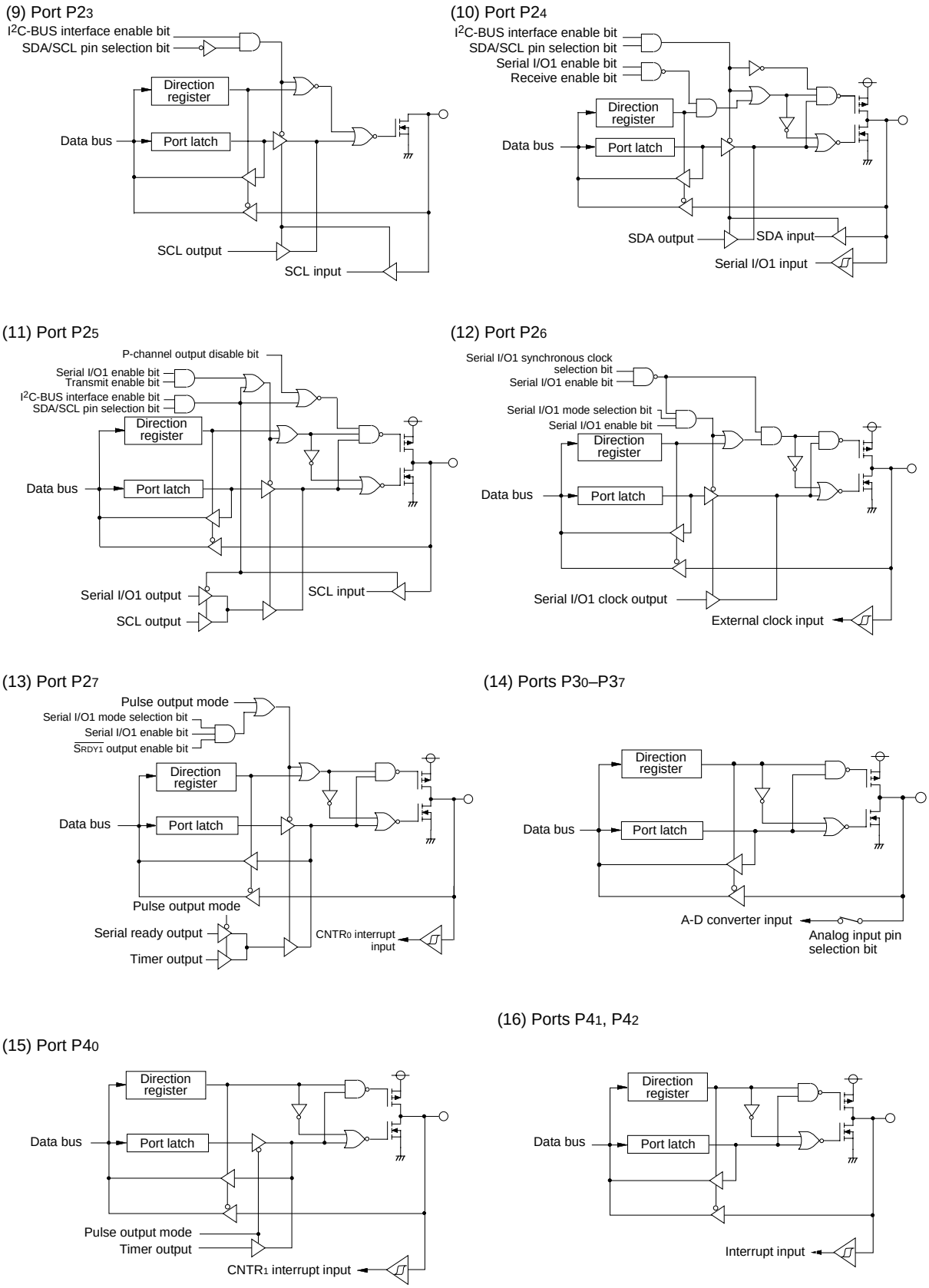


Fig. 7 Port block diagram (2)

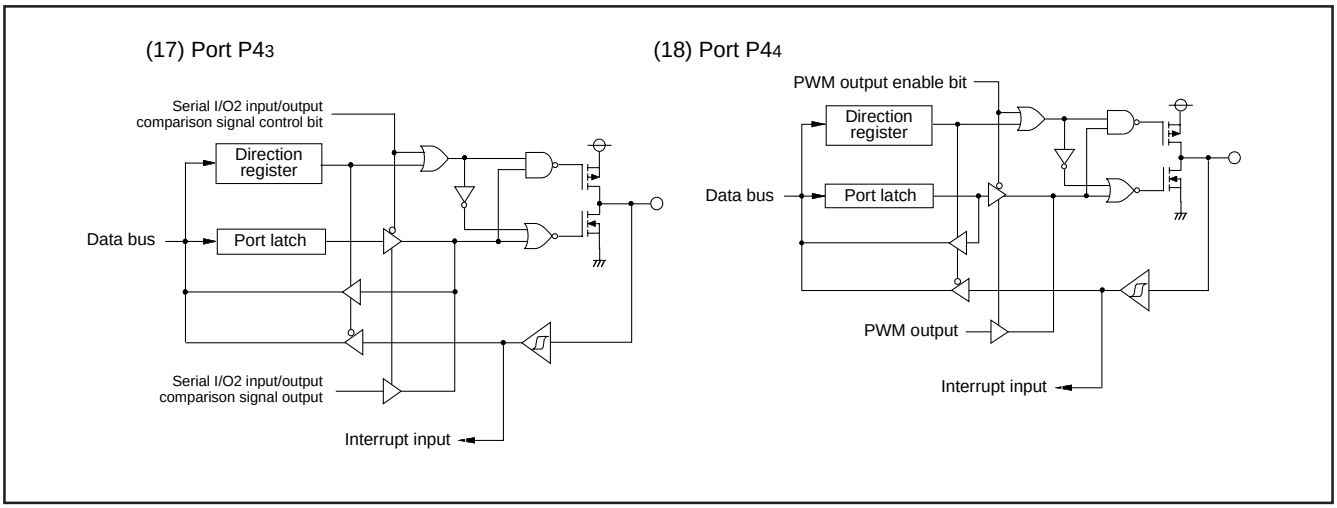


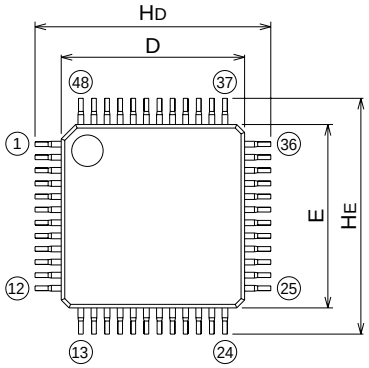
Fig. 8 Port block diagram (3)

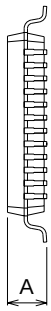
PACKAGE OUTLINE

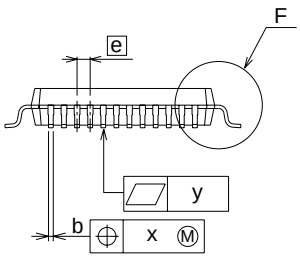
48P6Q-A

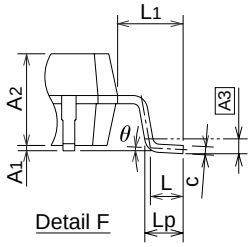
Plastic 48pin 7×7mm body LQFP

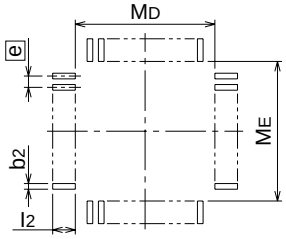
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	–	–	Cu Alloy











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.5	–
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
L	0.35	0.5	0.65
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	7.4	–
M_E	–	7.4	–

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

MITSUBISHI ELECTRIC

REVISION HISTORY	M37516F8HP DATA SHEET

Rev. No.	Revision Description	Rev. date
0.1	First Edition	2/3/00