

DESCRIPTION

The 7630 group is a single chip 8-bit microcomputer designed with CMOS silicon gate technology.

Being equipped with a CAN (Controller Area Network) module circuit, the microcomputer is suited to drive automotive equipments. The CAN module complies with CAN specification version 2.0, part B and allows priority-based message management.

In addition to the microcomputers simple instruction set, the ROM, RAM and I/O addresses are placed in the same memory map to enable easy programming.

The built-in ROM is available as mask ROM or One Time PROM. For development purposes, emulator- and EPROM-type microcomputers are available as well.

FEATURES

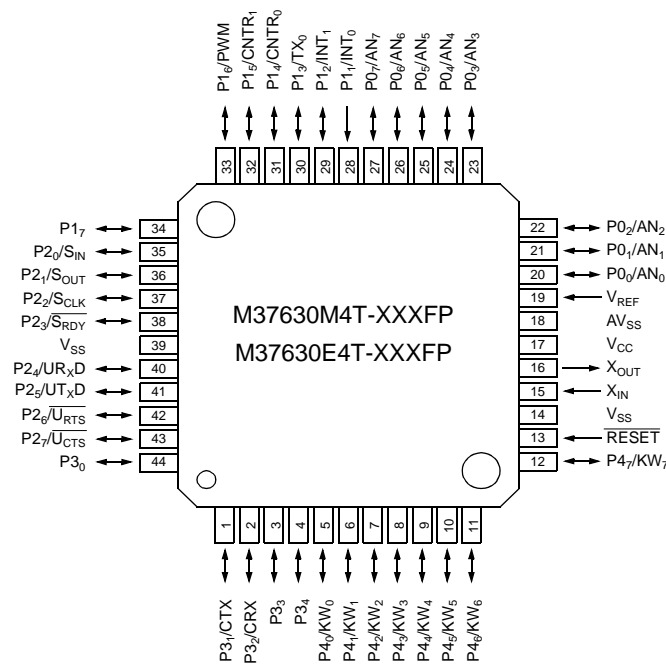
- Basic machine-language instructions 71
- Minimum instruction execution time
(at 10 MHz oscillation frequency) 0.2 μs
- Memory size
ROM 16252 bytes (M37630M4T-XXXFP)
RAM 512 bytes (M37630M4T-XXXFP)
- I/O ports
Programmable I/O ports 35
Input 1

- Interrupts 24 sources, 24 vectors
- Timers
16-bit Timers 2 channels
8-bit Timers 3 channels
- Serial I/Os
Clock synchronous 1 channel
UART 1 channel
- CAN module
(CAN specification version 2.0, part B) 1 channel
- A-D converter 8-bits x 8 channels
- Watchdog timer 1
- Clock Generating Circuit 1
Built-in with internal feedback resistor
- Power source voltage
(at 10 MHz oscillation frequency) 4.0 to 5.5 V
- Power dissipation
In high-speed mode 55 mW
(at 8 MHz oscillation frequency, at 5 V power source voltage)
- Operating temperature range -40 to 85 °C
- Package 44QFP (44P6N-A)

APPLICATION

Automotive controls

PIN CONFIGURATION (TOP VIEW)



**Package type: 44P6N-A
 44-pin plastic molded QFP**

Fig. 1 Pin configuration of M37630M4T-XXXFP

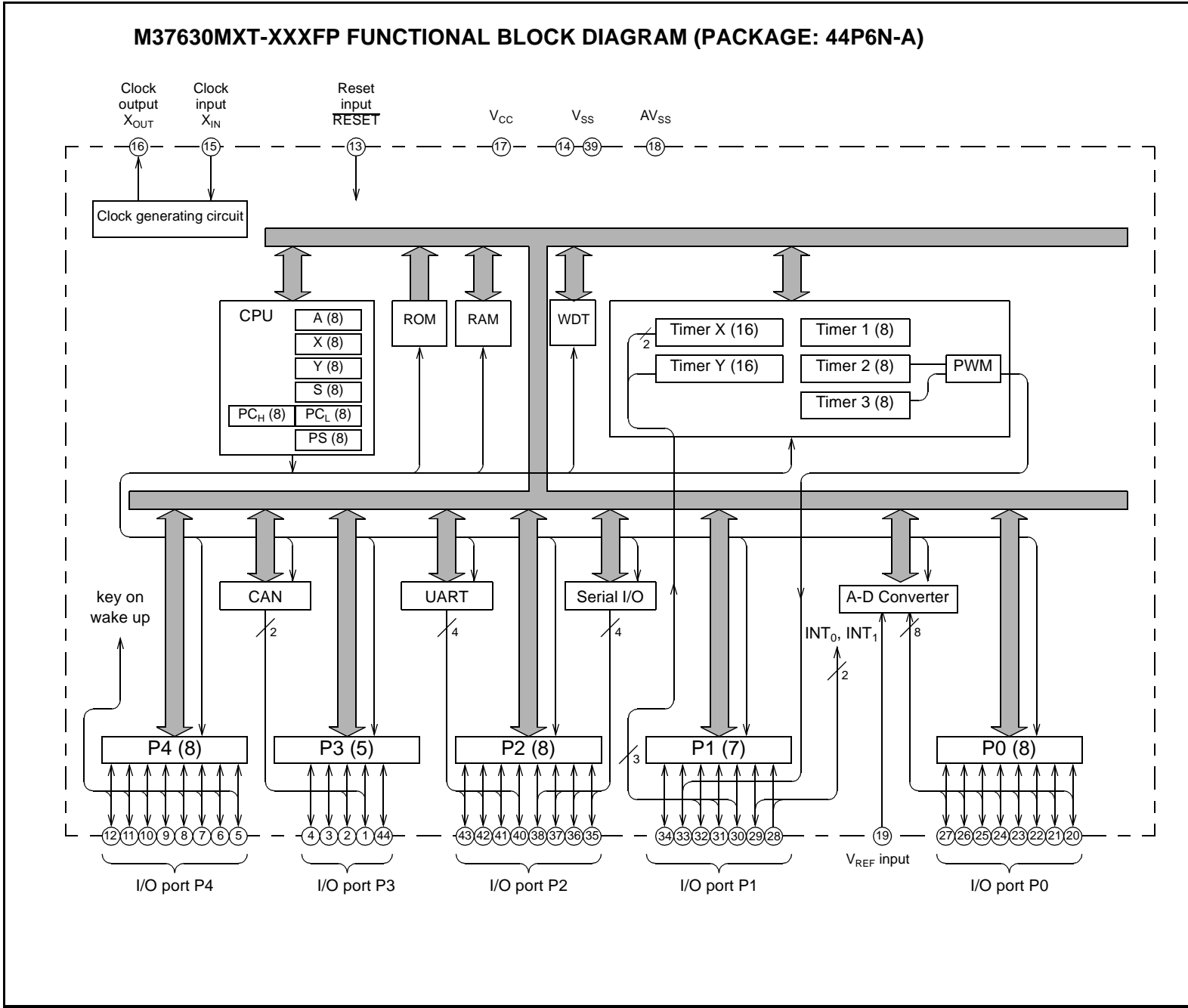


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1: Pin description

| Pin | Name | Input/Output | Description |
|--|-----------------------------|--------------|--|
| V _{CC} , V _{SS} | Power source voltage | | Power supply pins; apply 4.0 to 5.5 V to V _{CC} and 0 V to V _{SS} |
| AV _{SS} | Analog power source voltage | | Ground pin for A-D converter. Connect to V _{SS} |
| $\overline{\text{RESET}}$ | Reset input | Input | Reset pin. This pin must be kept at "L" level for more than 2 μ s, to enter the reset state. If the crystal or ceramic resonator requires more time to stabilize, extend the "L" level period. |
| X _{IN} | Clock input | Input | Input and output pins of the internal clock generating circuit. Connect a ceramic or quartz-crystal resonator between the X _{IN} and X _{OUT} pins. When an external clock source is used, connect it to X _{IN} and leave X _{OUT} open. |
| X _{OUT} | Clock output | Output | |
| V _{REF} | Reference voltage input | Input | Reference voltage input pin for A-D converter |
| P0 ₀ /AN ₀ — P0 ₇ /AN ₇ | I/O port P0 | I/O | CMOS I/O ports or analog input ports |
| P1 ₁ /INT ₀ | I/O port P1 | Input | CMOS input port or external interrupt input port. The active edge (rising or falling) of external interrupts can be selected. This pin will be used as V _{PP} pin during PROM programming of One Time PROM Versions. |
| P1 ₂ /INT ₁ | | | CMOS I/O port or external interrupt input port. The active edge (rising or falling) of external interrupts can be selected. |
| P1 ₃ /TX ₀ | | | CMOS I/O port or input pin used in the bi-phase counter mode |
| P1 ₄ /CNTR ₀ | | I/O | CMOS I/O port or timer X input pin used for the event counter, pulse width measurement and bi-phase counter mode |
| P1 ₅ /CNTR ₁ | | | CMOS I/O port or timer Y input pin used for the event counter, pulse width and pulse period measurement mode |
| P1 ₆ /PWM | | | CMOS I/O port or PWM output pin used in the PWM mode of timers 2 and 3 |
| P1 ₇ | | | CMOS I/O port |
| P2 ₀ /S _{IN} P2 ₁ /S _{OUT} P2 ₂ /S _{CLK} P2 ₃ /S _{RDY} | I/O port P2 | I/O | CMOS I/O ports or clock synchronous serial I/O pins |
| P2 ₄ /UR _X D P2 ₅ /UT _X D P2 ₆ /U _{RTS} P2 ₇ /U _{CTS} | | | |
| P3 ₀ | I/O port P3 | I/O | CMOS I/O port |
| P3 ₁ /CTX | | | CMOS I/O port or CAN transmit data pin |
| P3 ₂ /CRX | | | CMOS I/O port or CAN receive data pin |
| P3 ₃ —P3 ₄ | | | CMOS I/O port |
| P4 ₀ /KW ₀ — P4 ₇ /KW ₇ | I/O port P4 | I/O | CMOS I/O ports. These ports can be used for key-on wake-up when configured as inputs. |

PART NUMBERING

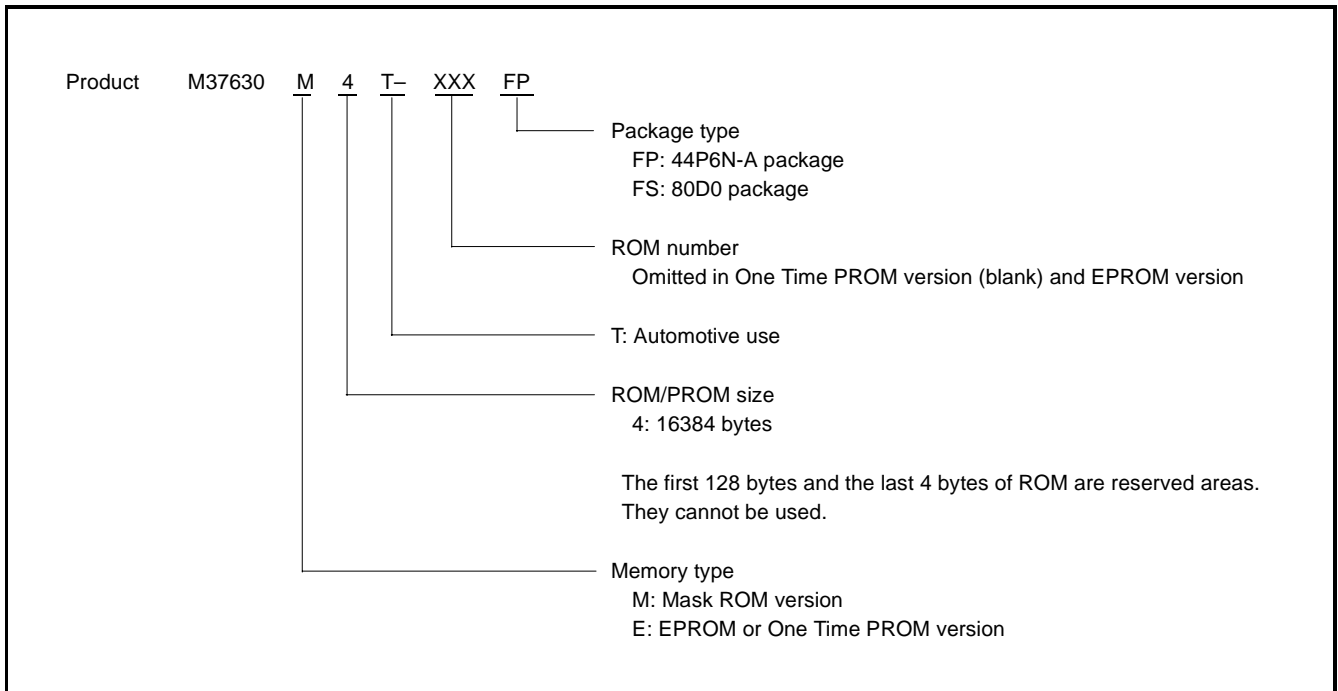


Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 7630 group as follows:

Memory Type

Support mask ROM, One Time PROM and EPROM versions.

Memory Size

ROM/PROM size 16 Kbytes
RAM size. 512 bytes

Package

44P6N-A0.8mm-pitch plastic molded QFP
80D00.8mm-pitch ceramic LCC (EPROM version)

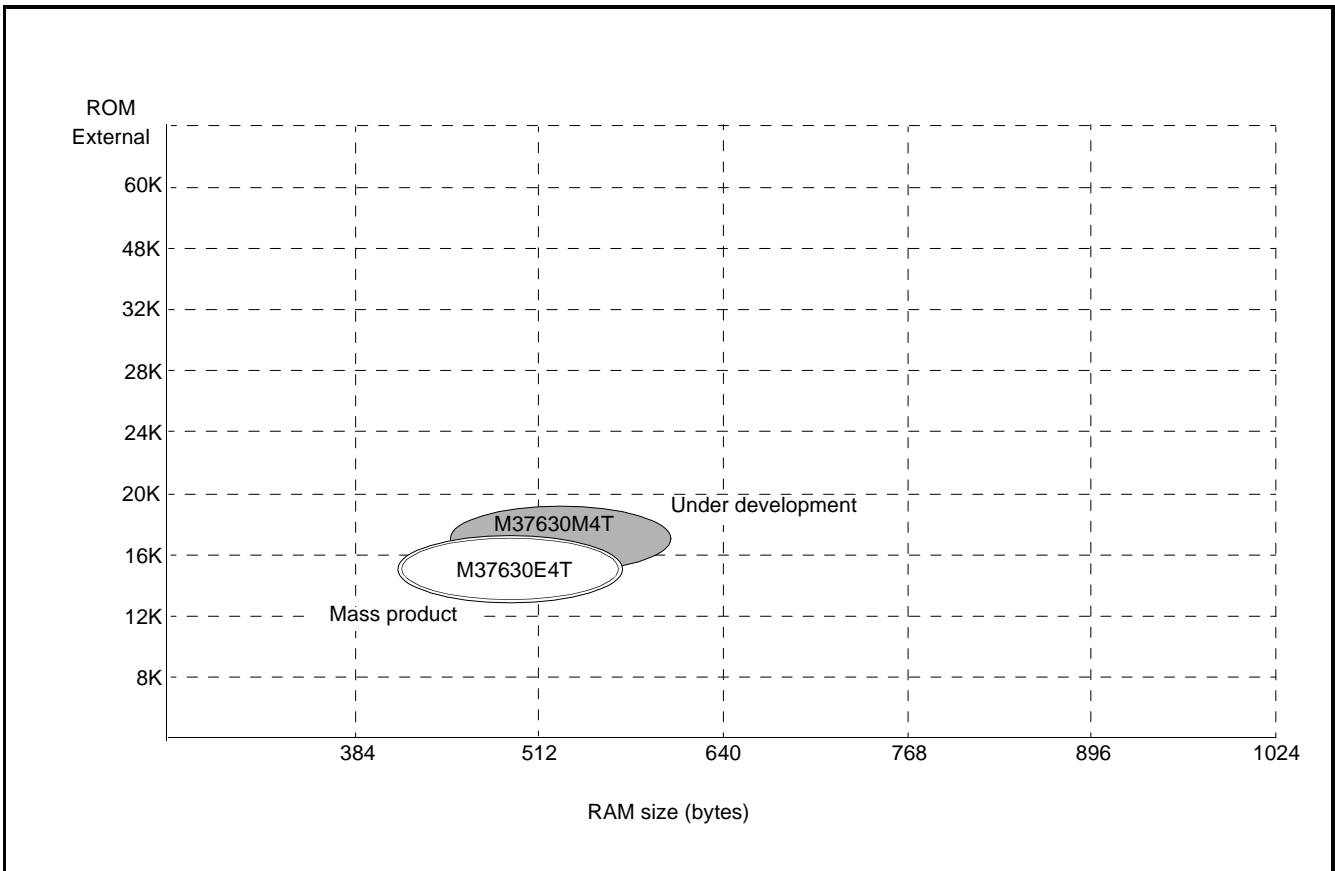


Fig. 4 Memory expansion plan

Currently supported products are listed below:

Table 2: List of supported products

As of March 1998

| Product | (P)ROM size (bytes) ROM size for User () | RAM size (bytes) | Package | Remarks |
|-----------------|--|------------------|---------|-------------------------------|
| M37630M4T-XXXFP | 16384 (16252) | 512 | 44P6N-A | Mask ROM version |
| M37630E4T-XXXFP | | | | One Time PROM version |
| M37630E4FP | | | | One Time PROM version (blank) |
| M37630E4FS | | | 80D0 | EPROM version |

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The core of 7630 group microcomputers is the 7600 series CPU. This core is based on the standard instruction set of 740 series; however the performance is improved by allowing to execute the same instructions as that of the 740 series in less cycles. Refer to the 7600 Series Software Manual for details of the instruction set.

CPU Mode Register CPUM

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated to address 0000_{16} .

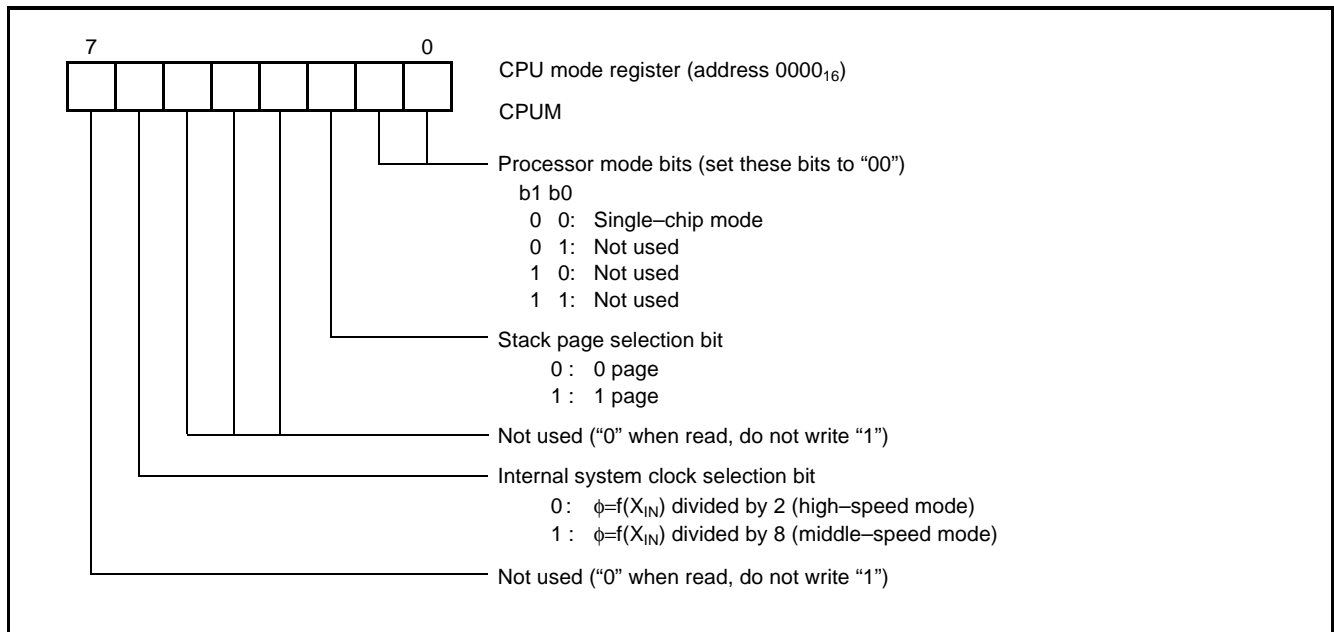


Fig. 5 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

ROM is used for storing user's program code as well as the interrupt vector area.

Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

Zero Page

This area can be accessed most efficiently by means of the zero page addressing mode.

Special Page

This area can be accessed most efficiently by means of the special page addressing mode.

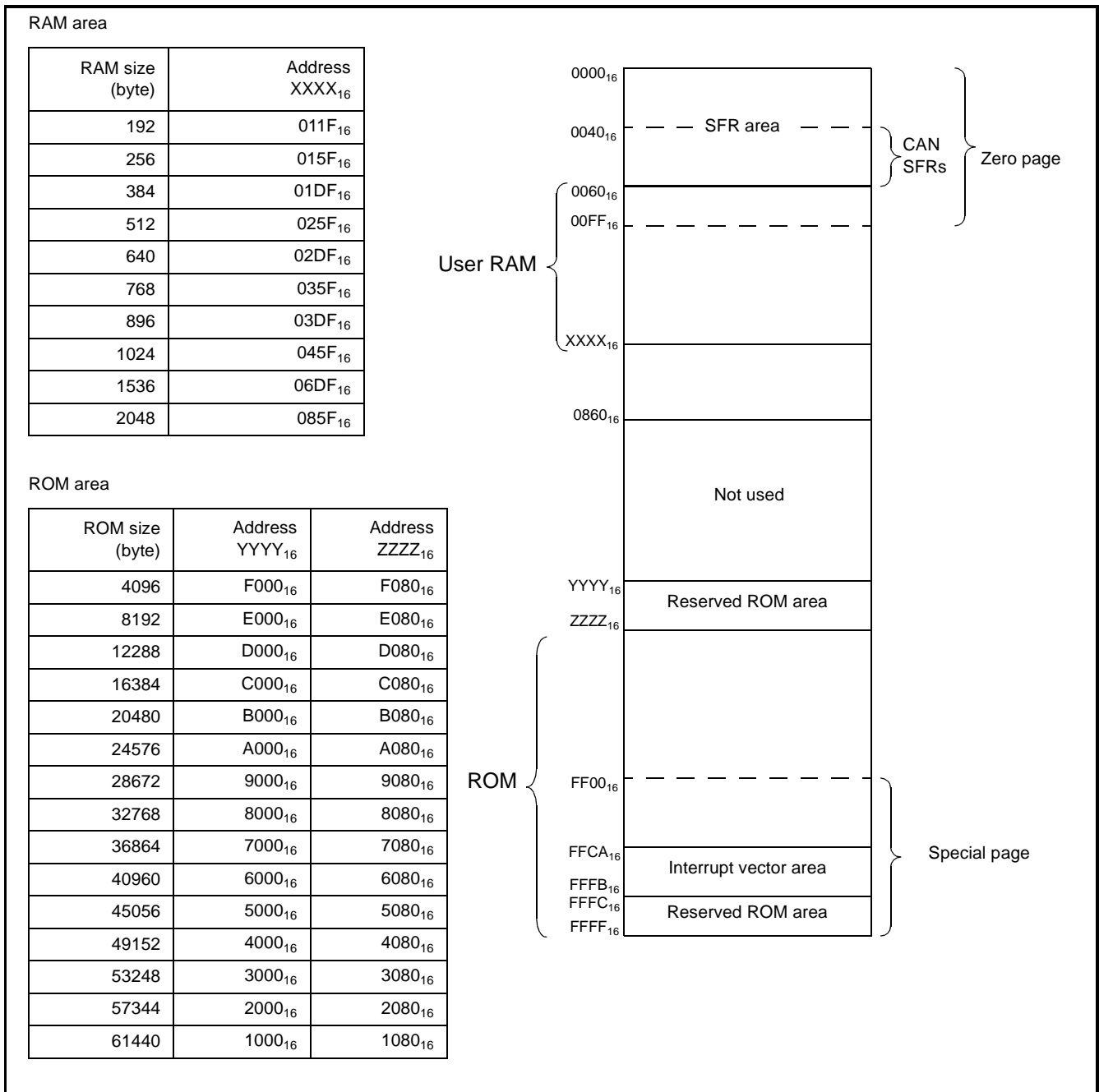


Fig. 6 Memory map diagram

SPECIAL FUNCTION REGISTERS (SFR)

| | | | | | |
|--------------------|---------------------------------------|--------|--------------------|-----------------------------------|---------|
| 0000 ₁₆ | CPU mode register | CPUM | 0030 ₁₆ | CAN transmit control register | CTRM |
| 0001 ₁₆ | Not used | | 0031 ₁₆ | CAN bus timing control register 1 | CBTCON1 |
| 0002 ₁₆ | Interrupt request register A | IREQA | 0032 ₁₆ | CAN bus timing control register 2 | CBTCON2 |
| 0003 ₁₆ | Interrupt request register B | IREQB | 0033 ₁₆ | CAN acceptance code register 0 | CAC0 |
| 0004 ₁₆ | Interrupt request register C | IREQC | 0034 ₁₆ | CAN acceptance code register 1 | CAC1 |
| 0005 ₁₆ | Interrupt control register A | ICONA | 0035 ₁₆ | CAN acceptance code register 2 | CAC2 |
| 0006 ₁₆ | Interrupt control register B | ICONB | 0036 ₁₆ | CAN acceptance code register 3 | CAC3 |
| 0007 ₁₆ | Interrupt control register C | ICONC | 0037 ₁₆ | CAN acceptance code register 4 | CAC4 |
| 0008 ₁₆ | Port P0 register | P0 | 0038 ₁₆ | CAN acceptance mask register 0 | CAM0 |
| 0009 ₁₆ | Port P0 direction register | P0D | 0039 ₁₆ | CAN acceptance mask register 1 | CAM1 |
| 000A ₁₆ | Port P1 register | P1 | 003A ₁₆ | CAN acceptance mask register 2 | CAM2 |
| 000B ₁₆ | Port P1 direction register | P1D | 003B ₁₆ | CAN acceptance mask register 3 | CAM3 |
| 000C ₁₆ | Port P2 register | P2 | 003C ₁₆ | CAN acceptance mask register 4 | CAM4 |
| 000D ₁₆ | Port P2 direction register | P2D | 003D ₁₆ | CAN receive control register | CREC |
| 000E ₁₆ | Port P3 register | P3 | 003E ₁₆ | CAN transmit abort register | CABORT |
| 000F ₁₆ | Port P3 direction register | P3D | 003F ₁₆ | Reserved | |
| 0010 ₁₆ | Port P4 register | P4 | 0040 ₁₆ | CAN transmit buffer register 0 | CTB0 |
| 0011 ₁₆ | Port P4 direction register | P4D | 0041 ₁₆ | CAN transmit buffer register 1 | CTB1 |
| 0012 ₁₆ | Serial I/O shift register | SIO | 0042 ₁₆ | CAN transmit buffer register 2 | CTB2 |
| 0013 ₁₆ | Serial I/O control register | SIOCON | 0043 ₁₆ | CAN transmit buffer register 3 | CTB3 |
| 0014 ₁₆ | A-D conversion register | AD | 0044 ₁₆ | CAN transmit buffer register 4 | CTB4 |
| 0015 ₁₆ | A-D control register | ADCON | 0045 ₁₆ | CAN transmit buffer register 5 | CTB5 |
| 0016 ₁₆ | Timer 1 | T1 | 0046 ₁₆ | CAN transmit buffer register 6 | CTB6 |
| 0017 ₁₆ | Timer 2 | T2 | 0047 ₁₆ | CAN transmit buffer register 7 | CTB7 |
| 0018 ₁₆ | Timer 3 | T3 | 0048 ₁₆ | CAN transmit buffer register 8 | CTB8 |
| 0019 ₁₆ | Timer 123 mode register | T123M | 0049 ₁₆ | CAN transmit buffer register 9 | CTB9 |
| 001A ₁₆ | Timer XL | TXL | 004A ₁₆ | CAN transmit buffer register A | CTBA |
| 001B ₁₆ | Timer XH | TXH | 004B ₁₆ | CAN transmit buffer register B | CTBB |
| 001C ₁₆ | Timer YL | TYL | 004C ₁₆ | CAN transmit buffer register C | CTBC |
| 001D ₁₆ | Timer YH | TYH | 004D ₁₆ | CAN transmit buffer register D | CTBD |
| 001E ₁₆ | Timer X mode register | TXM | 004E ₁₆ | Reserved | |
| 001F ₁₆ | Timer Y mode register | TYM | 004F ₁₆ | Reserved | |
| 0020 ₁₆ | UART mode register | UMOD | 0050 ₁₆ | CAN receive buffer register 0 | CRB0 |
| 0021 ₁₆ | UART baud rate generator | UBRG | 0051 ₁₆ | CAN receive buffer register 1 | CRB1 |
| 0022 ₁₆ | UART control register | UCON | 0052 ₁₆ | CAN receive buffer register 2 | CRB2 |
| 0023 ₁₆ | UART status register | USTS | 0053 ₁₆ | CAN receive buffer register 3 | CRB3 |
| 0024 ₁₆ | UART transmit buffer register 1 | UTBR1 | 0054 ₁₆ | CAN receive buffer register 4 | CRB4 |
| 0025 ₁₆ | UART transmit buffer register 2 | UTBR2 | 0055 ₁₆ | CAN receive buffer register 5 | CRB5 |
| 0026 ₁₆ | UART receive buffer register 1 | URBR1 | 0056 ₁₆ | CAN receive buffer register 6 | CRB6 |
| 0027 ₁₆ | UART receive buffer register 2 | URBR2 | 0057 ₁₆ | CAN receive buffer register 7 | CRB7 |
| 0028 ₁₆ | Port P0 pull-up control register | PUP0 | 0058 ₁₆ | CAN receive buffer register 8 | CRB8 |
| 0029 ₁₆ | Port P1 pull-up control register | PUP1 | 0059 ₁₆ | CAN receive buffer register 9 | CRB9 |
| 002A ₁₆ | Port P2 pull-up control register | PUP2 | 005A ₁₆ | CAN receive buffer register A | CRBA |
| 002B ₁₆ | Port P3 pull-up control register | PUP3 | 005B ₁₆ | CAN receive buffer register B | CRBB |
| 002C ₁₆ | Port P4 pull-up/down control register | PUP4 | 005C ₁₆ | CAN receive buffer register C | CRBC |
| 002D ₁₆ | Interrupt polarity selection register | IPOL | 005D ₁₆ | CAN receive buffer register D | CRBD |
| 002E ₁₆ | Watchdog timer register | WDT | 005E ₁₆ | Reserved | |
| 002F ₁₆ | Polarity control register | PCON | 005F ₁₆ | Reserved | |

Fig. 7 Memory map of special register (SFR)

I/O PORTS

The 7630 group has 35 programmable I/O pins and one input pin arranged in five I/O ports (ports P0 to P4). The I/O ports are controlled by the corresponding port registers and port direction registers; each I/O pin can be controlled separately.

When data is read from a port configured as an output port, the port latch's contents are read instead of the port level. A port configured

as an input port becomes floating and its level can be read. Data written to this port will affect the port latch only; the port remains floating.

Refer to Structure of port- and port direction registers, Structure of port I/Os (1) and Structure of port I/Os (2).

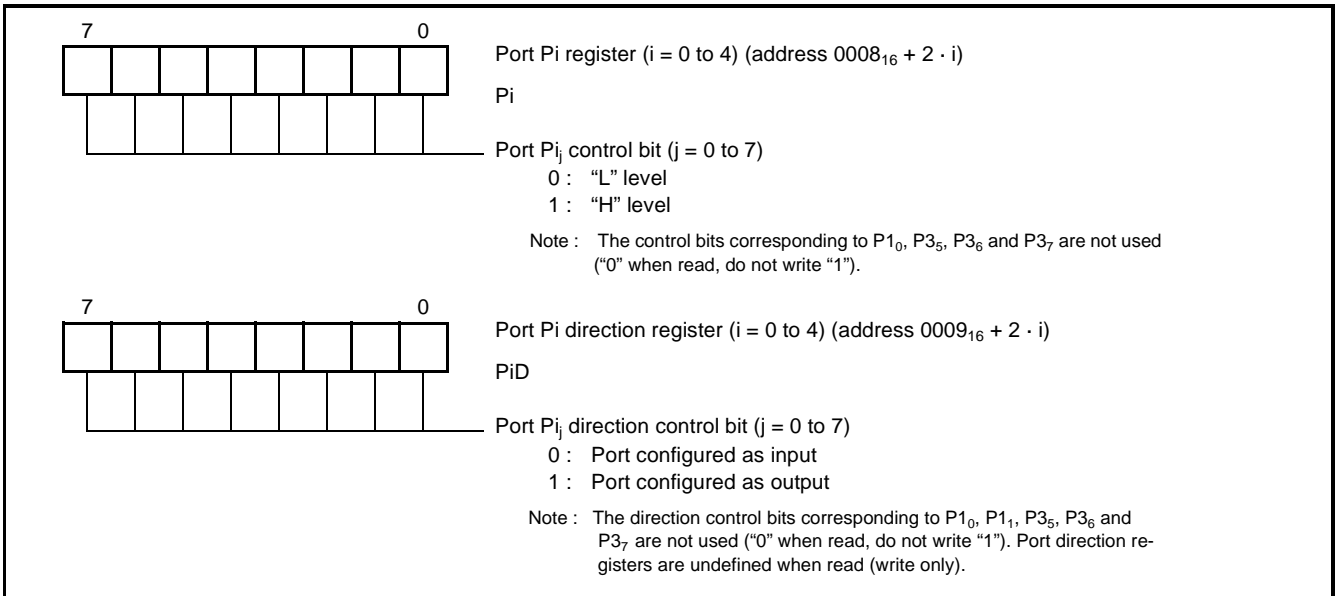


Fig. 8 Structure of port- and port direction registers

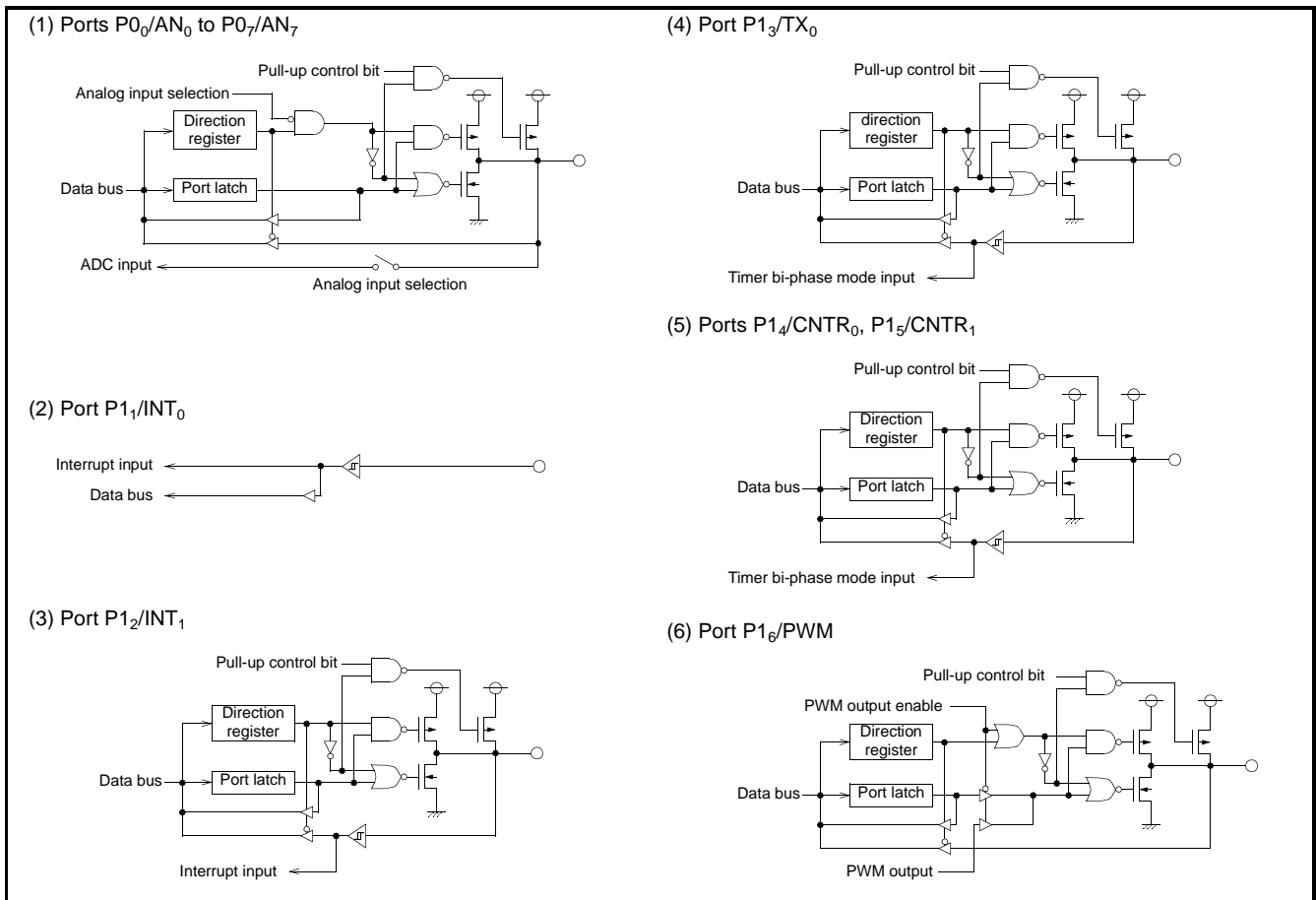


Fig. 9 Structure of port I/Os (1)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

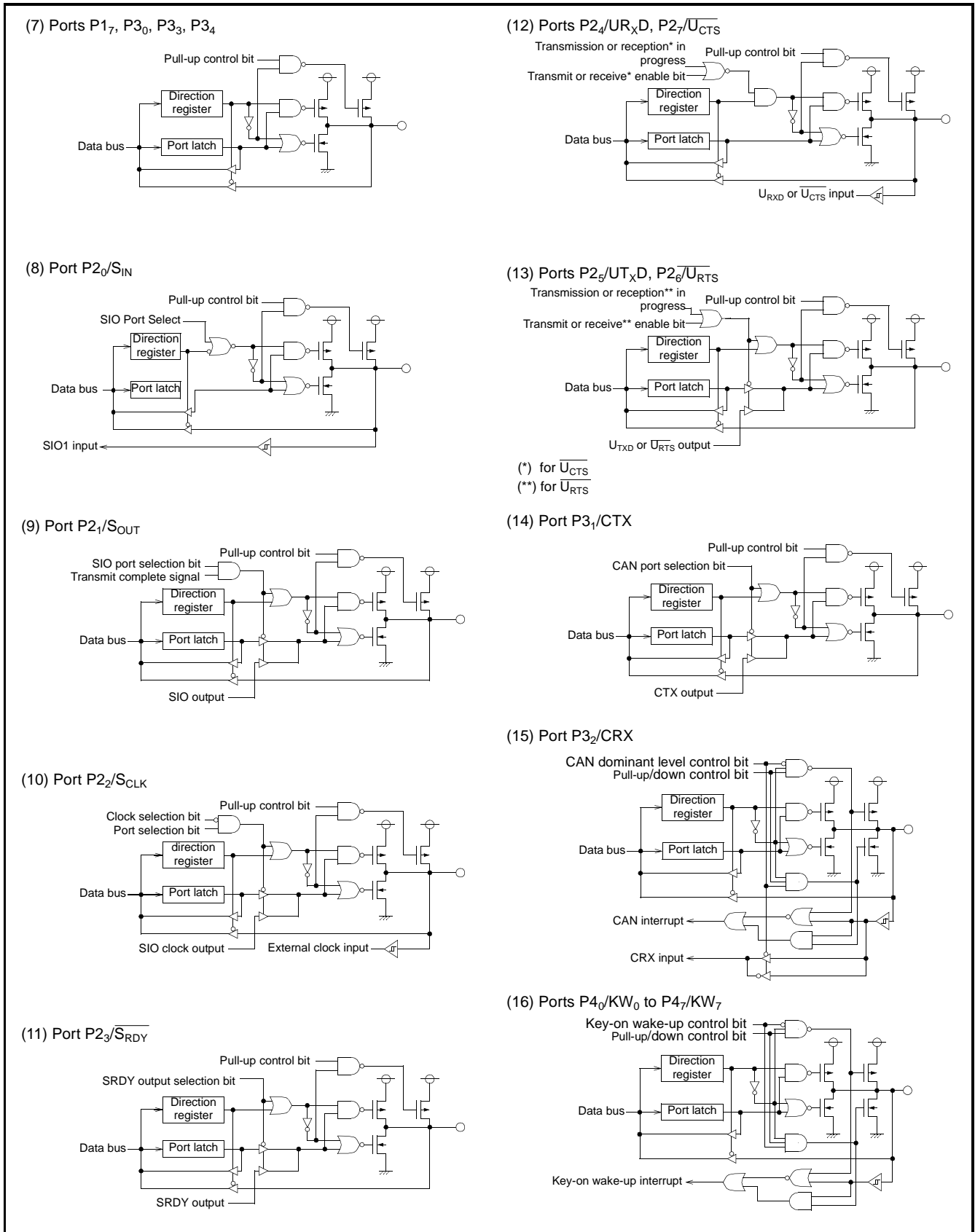


Fig. 10 Structure of port I/Os (2)

Port Pull-up/pull-down Function

Each pin of ports P0 to P4 except P₁ is equipped with a programmable pull-up transistor. P₃₂/CRX and P₄₀/KW₀ to P₄₇/KW₇ are equipped with programmable pull-down transistors as well. The pull-up function of P0 to P3 can be controlled by the corresponding

port pull-up control registers (see Structure of port pull-up/down control registers). The pull-up/down function of ports P₃₂ and P4 can be controlled by the corresponding port pull-up/pull-down registers together with the polarity control register (see Structure of polarity control register).

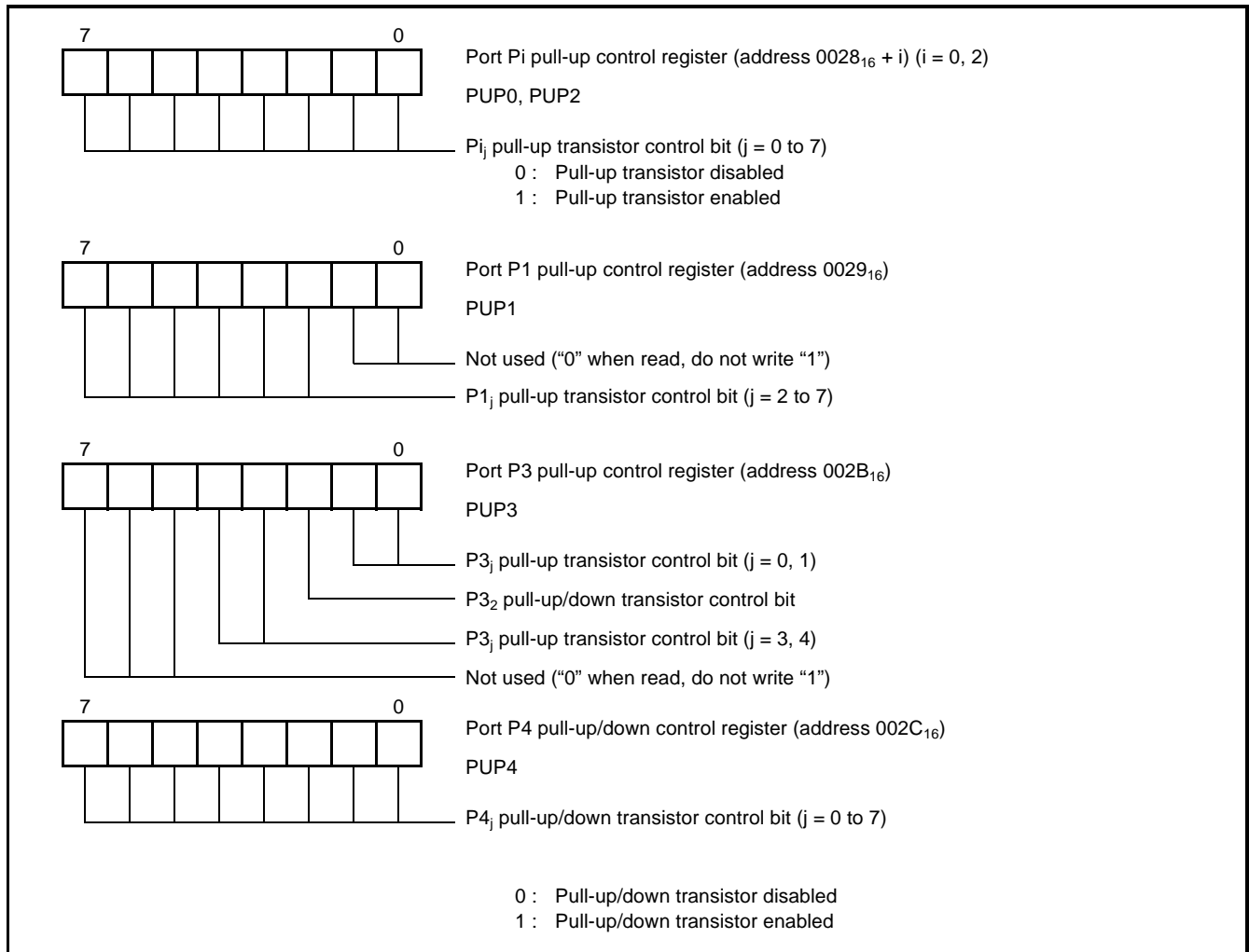


Fig. 11 Structure of port pull-up/down control registers

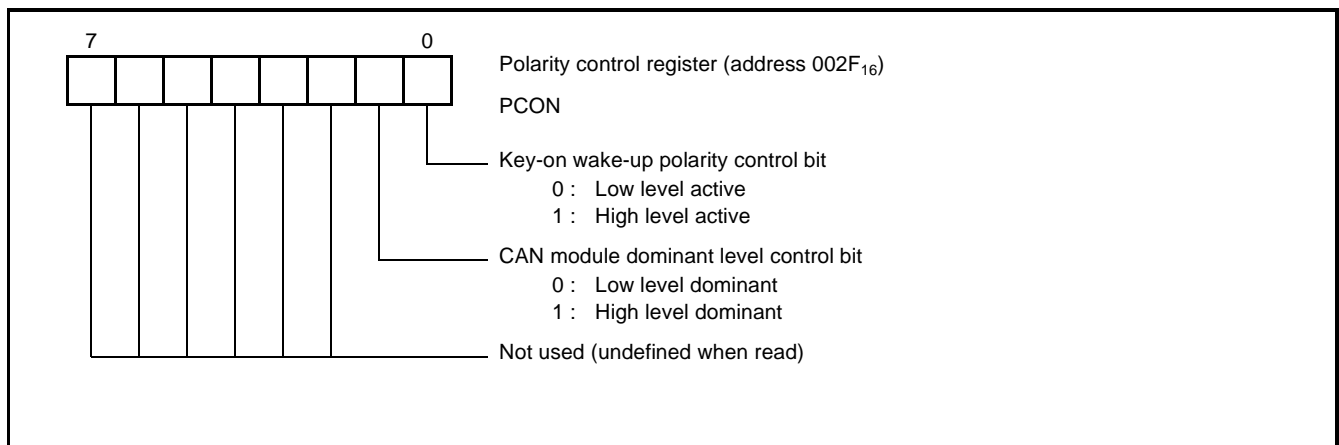


Fig. 12 Structure of polarity control register

Port Overvoltage Application

When configured as input ports, P1 to P4 may be subjected to overvoltage ($V_I > V_{CC}$) if the input current to the applicable port is limited to the specified values (see "Table 8:"). Use a serial resistor of appropriate size to limit the input current. To estimate the resistor value, assume the port voltage to be V_{CC} at overvoltage condition.

Notes:

- Subjecting ports to overvoltage may effect the supply voltage. Assure to keep V_{CC} and V_{SS} within the target limits.
- Avoid to subject ports to overvoltage causing V_{CC} to rise above 5.5 V.
- The overvoltage condition causing input current flowing through the internal port protection circuits has a negative effect on the ports noise immunity. Therefore, careful and intense testing of the target system's noise immunity is required. Refer to the "countermeasures against noise" of the corresponding users manual.
- Port P0 must not be subjected to overvoltage conditions.

INTERRUPTS

There are 24 interrupts: 6 external, 17 internal, and 1 software.

Interrupt Control

Each interrupt except the BRK instruction interrupt has both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs when the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0". Interrupt enable bits can be cleared or set by software. Interrupt request bits can be cleared by software but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupt requests occur at the same time, the interrupt with the highest priority is accepted first.

Interrupt Operation

Upon acceptance of an interrupt, the following operations are automatically performed.

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. Concurrently with the push operation, the interrupt jump destination address is read from the vector table into the program counter.
4. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.

Notes on use

When the active edge of an external interrupt (INT₀, INT₁, CNTR₀, CNTR₁, CWKU or KOI) is changed, the corresponding interrupt request bit may also be set. Therefore, take the following sequence.

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge in interrupt edge selection register.
(in the case of CNTR₀: Timer X mode register; in the case of CNTR₁: Timer Y mode register)
- (3) Clear the interrupt request bit to "0".
- (4) Enable the external interrupt which is selected.

Table 3: Interrupt vector addresses and priority

| Interrupt source | Priority | Vector Address (Note 1) | | Interrupt Request Generating Conditions | Remarks |
|----------------------------|----------|-------------------------|--------------------|---|---|
| | | High | Low | | |
| Reset (Note 2) | 1 | FFFB ₁₆ | FFFA ₁₆ | At Reset | Non-maskable |
| Watchdog timer | 2 | FFF9 ₁₆ | FFF8 ₁₆ | At Watchdog timer underflow | Non-maskable |
| INT0 | 3 | FFF7 ₁₆ | FFF6 ₁₆ | At detection of either rising or falling edge of INT ₀ interrupt | External Interrupt (active edge selectable) |
| INT1 | 4 | FFF5 ₁₆ | FFF4 ₁₆ | At detection of either rising or falling edge of INT ₁ interrupt | External Interrupt (active edge selectable) |
| CAN successful transmit | 5 | FFF3 ₁₆ | FFF2 ₁₆ | At CAN module successful transmission of message | Valid when CAN module is activated and request transmit |
| CAN successful receive | 6 | FFF1 ₁₆ | FFF0 ₁₆ | At CAN module successful reception of message | Valid when CAN module is activated |
| CAN overrun | 7 | FFEF ₁₆ | FFEE ₁₆ | If CAN module receives message when receive buffers are full. | Valid when CAN module is activated |
| CAN error passive | 8 | FFED ₁₆ | FFEC ₁₆ | When CAN module enters into error passive state | Valid when CAN module is active |
| CAN error bus off | 9 | FFEB ₁₆ | FFEA ₁₆ | When CAN module enters into bus off state | Valid when CAN module is active |
| CAN wake up | 10 | FFE9 ₁₆ | FFE8 ₁₆ | When CAN module wakes up via CAN bus | |
| Timer X | 11 | FFE7 ₁₆ | FFE6 ₁₆ | At Timer X underflow or overflow | |
| Timer Y | 12 | FFE5 ₁₆ | FFE4 ₁₆ | At Timer Y underflow | |
| Timer 1 | 13 | FFE3 ₁₆ | FFE2 ₁₆ | At Timer 1 underflow | |
| Timer 2 | 14 | FFE1 ₁₆ | FFE0 ₁₆ | At Timer 2 underflow | |
| Timer 3 | 15 | FFDF ₁₆ | FFDE ₁₆ | At Timer 3 underflow | |
| CNTR0 | 16 | FFDD ₁₆ | FFDC ₁₆ | At detection of either rising or falling edge in CNTR ₀ input | External Interrupt (active edge selectable) |
| CNTR1 | 17 | FFDB ₁₆ | FFDA ₁₆ | At detection of either rising or falling edge in CNTR ₁ input | External Interrupt (active edge selectable) |
| UART receive | 18 | FFD9 ₁₆ | FFD8 ₁₆ | At completion of UART receive | Valid when UART is selected |
| UART transmit | 19 | FFD7 ₁₆ | FFD6 ₁₆ | At completion of UART transmit | Valid when UART is selected |
| UART transmit buffer empty | 20 | FFD5 ₁₆ | FFD4 ₁₆ | At UART transmit buffer empty | Valid when UART is selected |
| UART receive error | 21 | FFD3 ₁₆ | FFD2 ₁₆ | When UART reception error occurs. | Valid when UART is selected |
| Serial I/O | 22 | FFD1 ₁₆ | FFD0 ₁₆ | At completion of serial I/O data transmit and receive | Valid when serial I/O is selected |
| A-D conversion | 23 | FFCF ₁₆ | FFCE ₁₆ | At completion of A-D conversion | |
| Key-on wake-up | 24 | FFCD ₁₆ | FFCC ₁₆ | At detection of either rising or falling edge of P4 input | External Interrupt (active edge selectable) |
| BRK instruction | 25 | FFCB ₁₆ | FFCA ₁₆ | At BRK instruction execution | Non-maskable |

Notes 1: Vector addresses contain interrupt jump destination address

2: Reset function in the same way as an interrupt with the highest priority

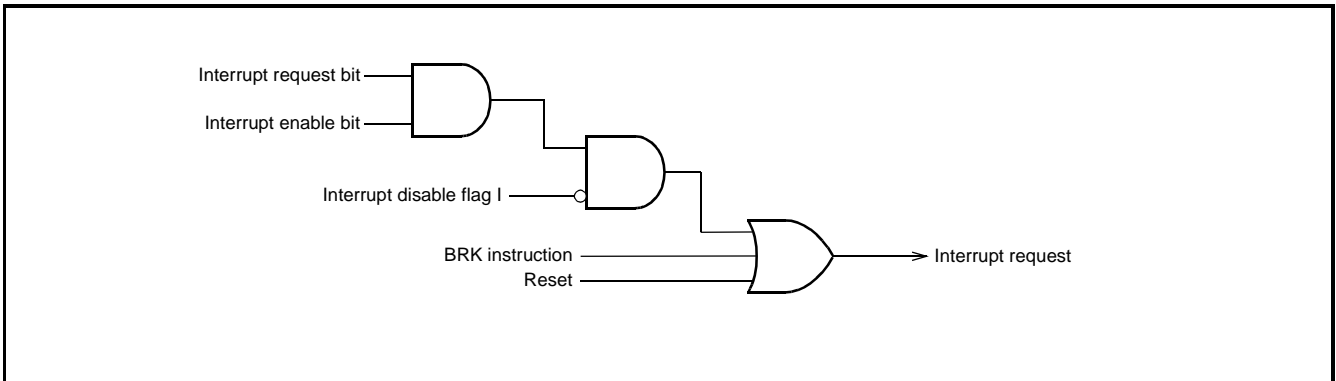


Fig. 13 Interrupt control

For the external interrupts INT0 and INT1, the active edge causing the interrupt request can be selected by the INT0 and INT1 interrupt edge selection bits of the interrupt polarity selection register (IPOL); please refer to Fig. 14 below.

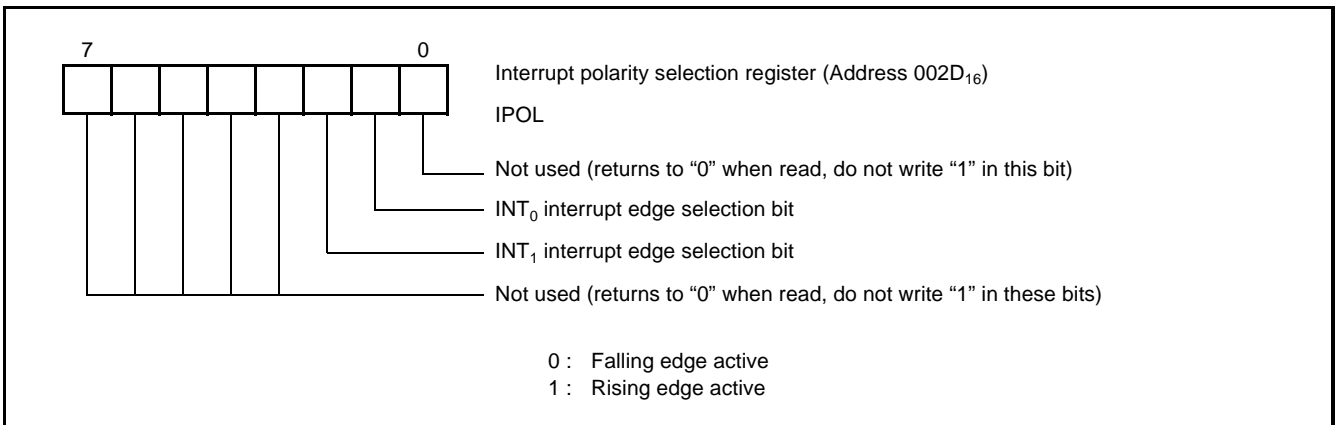


Fig. 14 Structure of interrupt polarity selection register

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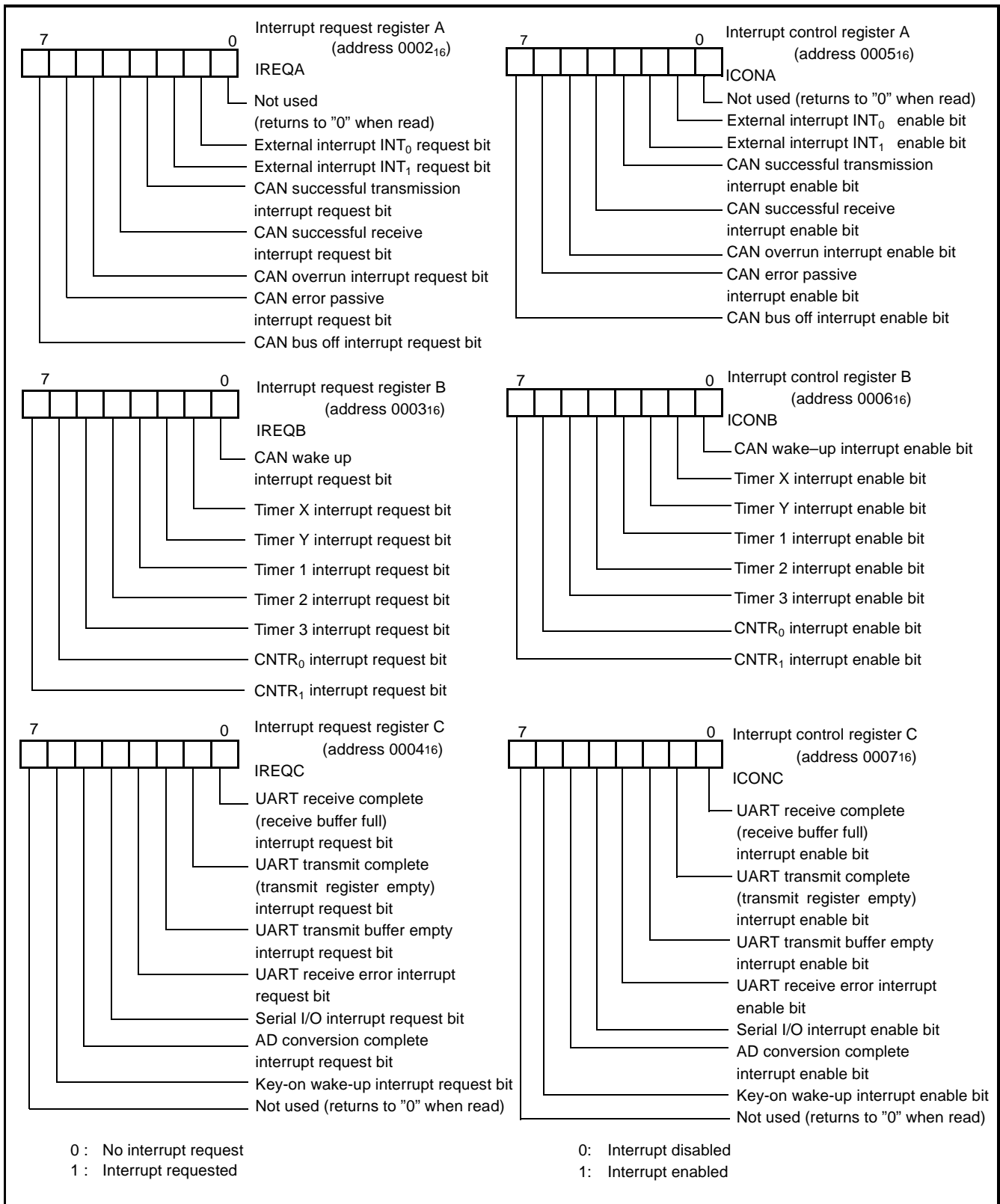


Fig. 15 Structure of interrupt request and control registers A, B and C

KEY-ON WAKE-UP

"Key-on wake-up" is one way of returning from a power-down state caused by the STP or WIT instruction. Any terminal of port P4 can be used to generate the key-on wake-up interrupt request. The active polarity can be selected by the key-on wake-up polarity con-

trol bit of PCON (see Fig. 12). If any pin of port P4 has the selected active level applied, the key-on wake-up interrupt request will be set to "1". Please refer to Fig. 16.

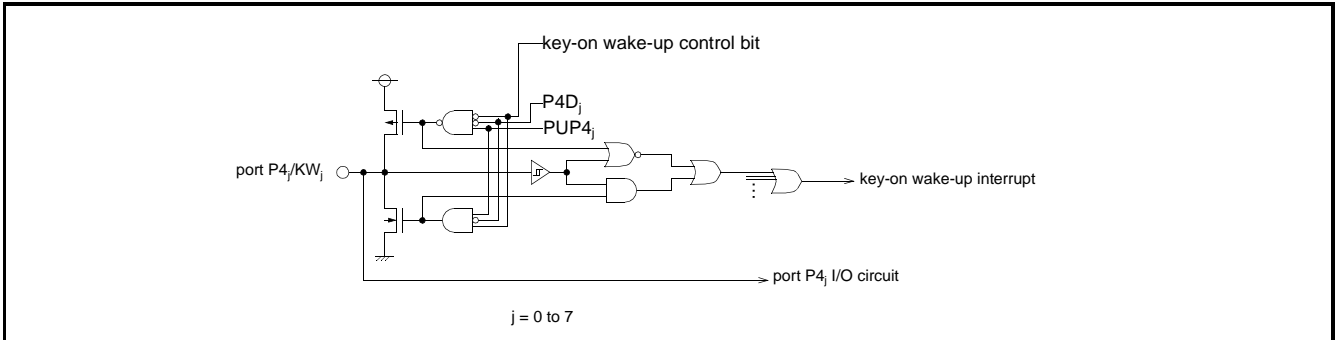


Fig. 16 Block diagram of key-on wake-up circuit

TIMERS

The 7630 group has five timers: two 16-bit timers and three 8-bit timers. All these timers will be described in detail below.

16-bit Timers

Timers X and Y are 16-bit timers with multiple operating modes. Please refer to Fig. 17.

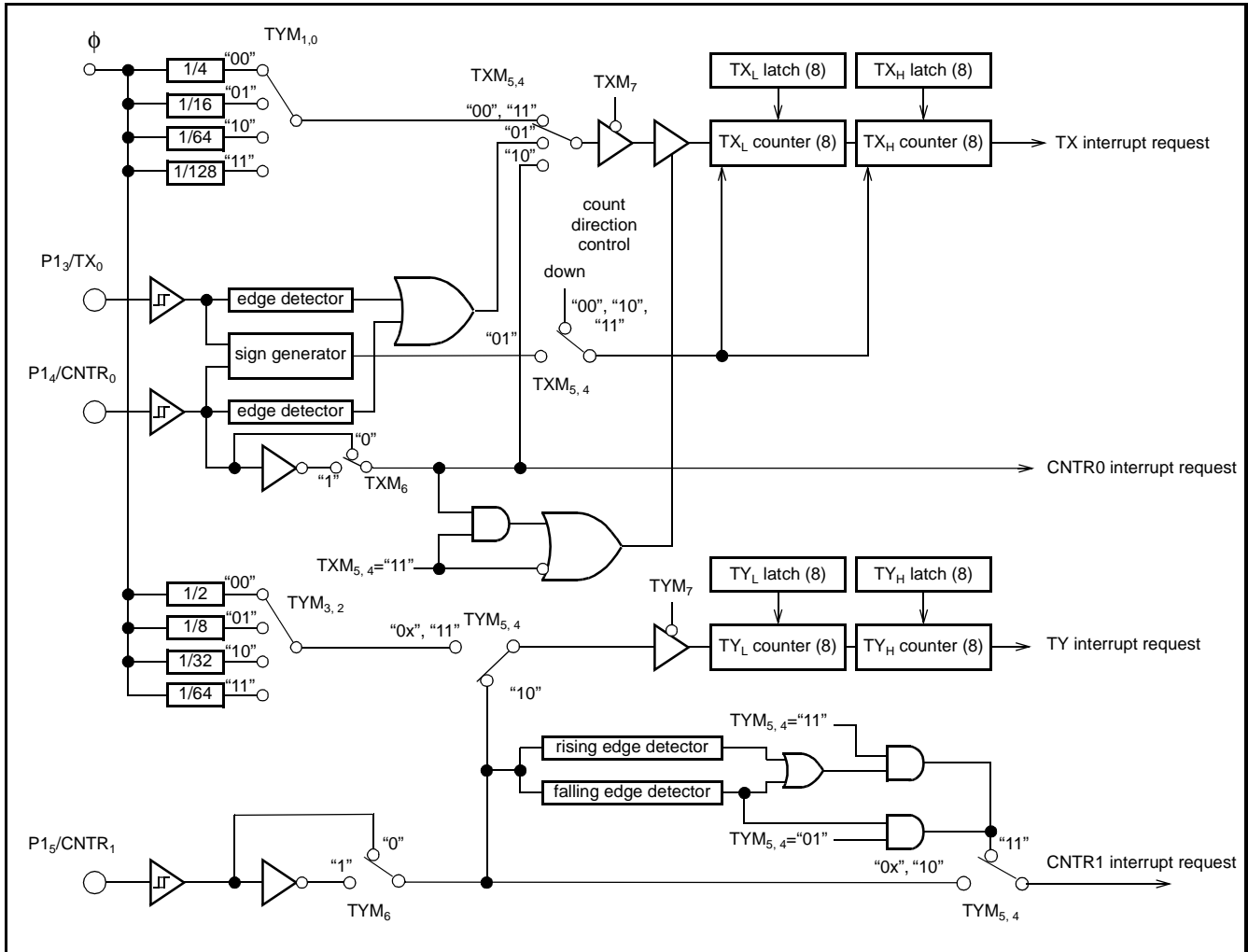


Fig. 17 Block diagram of timers X and Y (φ is internal system clock)

Timer X

Timer X is a 16-bit timer with a 16-bit reload latch supporting the following operating modes:

- (1) Timer mode
- (2) Bi-phase counter mode
- (3) Event counter mode
- (4) Pulse width measurement mode

These modes can be selected by the timer X mode register (TXM). In the timer- and pulse width measurement mode, the timer's count source can be selected by the timer X count source selection bits of the timer Y mode register (TYM). Please refer to the Figures below for the TXM and TYM bit assignment.

On read or write access to timer X, note that the high-order and low-order bytes must be accessed in the specific order.

Write method

When writing to the timer X, write the low-order byte first. The data written is stored in a temporary register which is assigned to the

same address as TX_L. Next, write the high-order byte. When this is finished, the data is placed in the timer X high-order reload latch and the low-order byte is transferred from its temporary register to the timer X low-order reload latch. Depending on the timer X write control bit, the latch contents are reloaded to the timer immediately (write control bit = "0") or on the next timer underflow (write control bit = "1").

Read method

When reading the timer X, read the high-order byte first. This causes the timer X high- and low-order bytes to be transferred to temporary registers being assigned to the same addresses as TX_H and TX_L. Next, read the low-order byte which is read from the temporary register. This method assures the correct timer value can be read during the timer count operation.

Timer X count stop control

Regardless of the actual operating mode, timer X can be stopped by setting the timer X count stop bit (bit 7 of the timer X mode register) to "1".

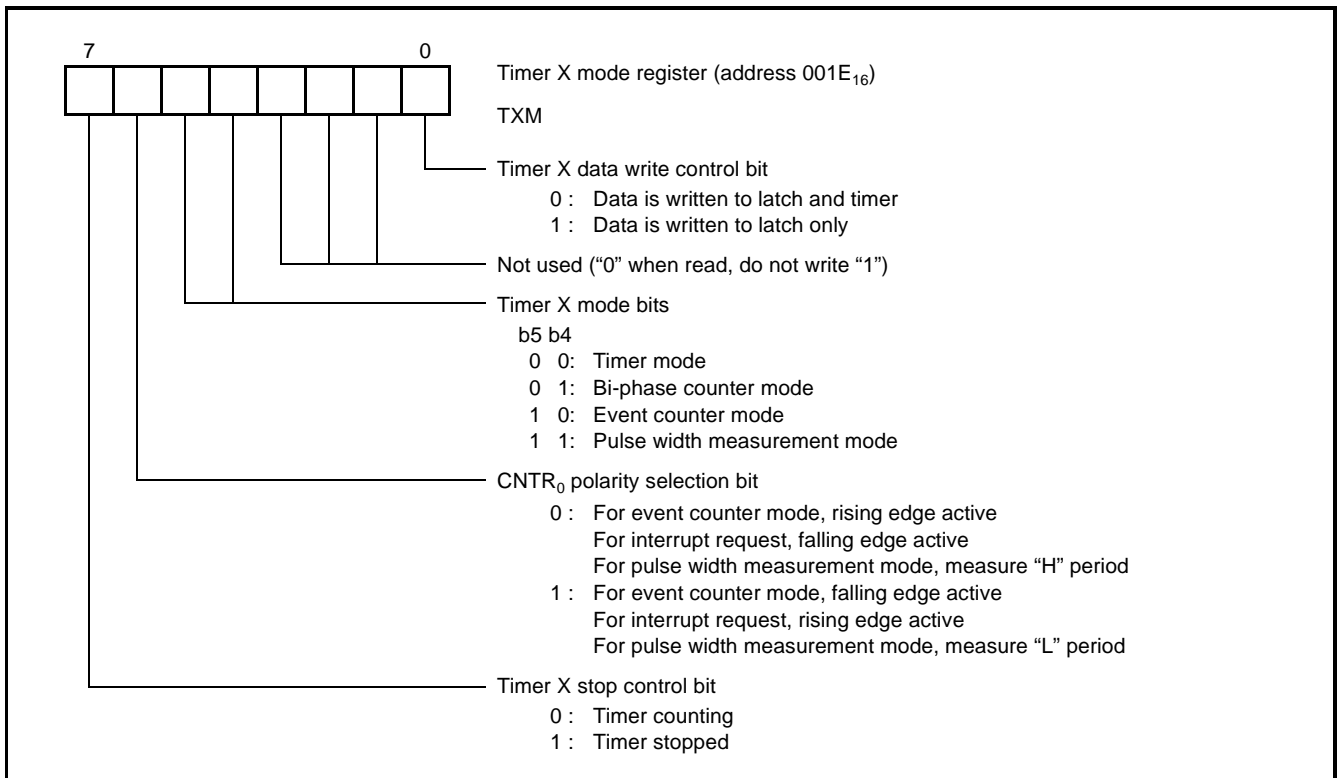


Fig. 18 Structure of Timer X mode register

Timer Y

Timer Y is a 16 bit timer with a 16-bit reload latch supporting the following operating modes:

- (1) Timer mode
- (3) Event counter mode
- (5) Pulse period measurement mode
- (6) H/L pulse width measurement mode

These modes can be selected by the timer Y mode register (TYM). In the timer, pulse period- and pulse width measurement modes' the timer's count source can be selected by the timer Y count source selection bits. Please refer to Fig. 19.

On read or write access to timer Y, note that the high-order and low-order bytes must be accessed in a specific order.

Write method

When writing to timer Y, write the low-order byte first. The data written is stored in a temporary register which is assigned to the same

address as TY_L. Next, write the high-order byte. When this is finished, the data is placed in the timer Y high-order reload latch and the low-order byte is transferred from its temporary register to the timer Y low-order reload latch.

Read method

When reading the timer Y, read the high-order byte first. This causes the timer Y high- and low-order bytes to be transferred to temporary registers being assigned to the same addresses as TY_H and TY_L. Next, read the low-order byte which is read from the temporary register. This method assures the correct timer value can be read during timer count operation.

Timer Y count stop control

Regardless of the actual operating mode, timer Y can be stopped by setting the timer Y count stop bit (bit 7 of the timer Y mode register) to "1".

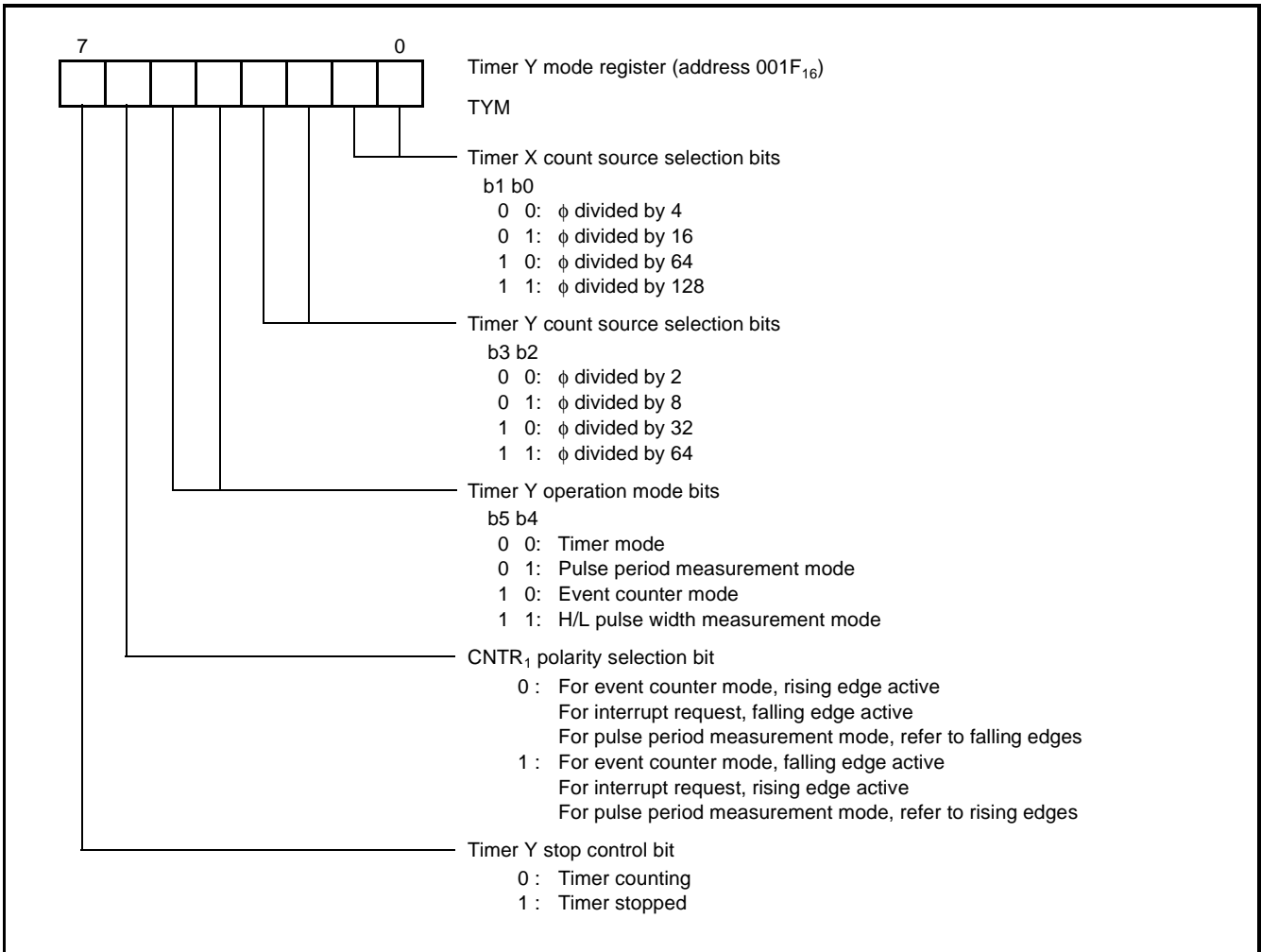


Fig. 19 Structure of timer Y mode register (ϕ is internal system clock)

Operating Modes

(1) Timer mode

This mode is available with timer X and timer Y.

- Count source
The count source for timer X and Y is the output of the corresponding clock divider. The division ratio can be selected by the timer Y mode register.
- Operation
Both timers X and Y are down counters. On a timer underflow, the corresponding timer interrupt request bit will be set to "1", the contents of the corresponding timer latches will be reloaded to the counters and counting continues.

(2) Bi-phase counter mode (quadruplicate)

This mode is available with timer X only.

- Count source
The count sources are P1₄/CNTR₀ and the P1₃/TX₀ pins.
- Operation
Timer X will count both rising and falling edges on both input pins (see above). Refer to Timer X bi-phase counter mode operation for the timing chart of the bi-phase counter mode.

The count direction is determined by the edge polarity and level of count source inputs and may change during the count operation. Refer to the table below.

Table 4: Timer X count direction in Bi-phase counter mode

| P1 ₃ /TX ₀ | P1 ₄ /CNTR ₀ | Count direction |
|----------------------------------|------------------------------------|-----------------|
| ↑ Edge | L | Up |
| | H | Down |
| ↓ Edge | L | Down |
| | H | Up |
| L | ↑ Edge | Down |
| H | | Up |
| L | ↓ Edge | Up |
| H | | Down |

On a timer over- or underflow, the corresponding interrupt request bit will be set to "1" and counting continues.

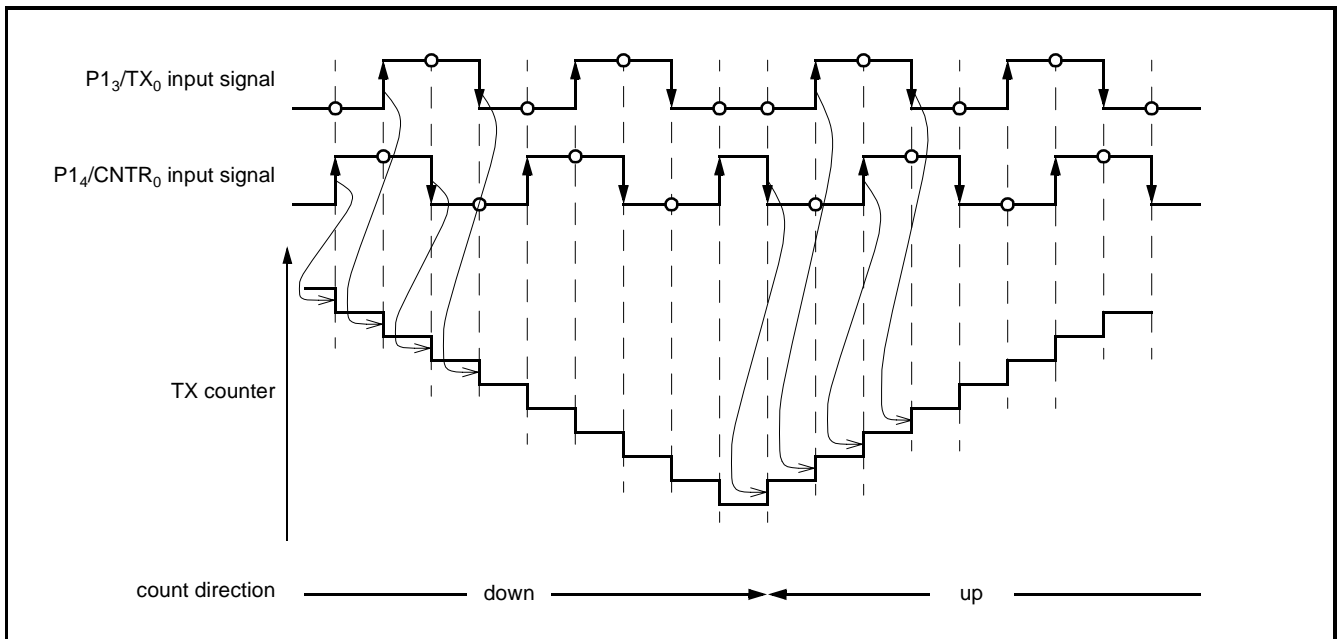


Fig. 20 Timer X bi-phase counter mode operation

(3) Event counter mode

This mode is available with timer X and timer Y.

- Count source
The count source for timer X is the input signal to the $P1_4/CNTR_0$ pin and for timer Y the input signal to $P1_5/CNTR_1$ pin.
- Operation
The timer counts down. On a timer underflow, the corresponding timer interrupt request bit will be set to "1", the contents of the corresponding timer latches will be reloaded to the counters and counting continues. The active edge used for counting can be selected by the polarity selection bit of the corresponding pin $P1_4/CNTR_0$ or $P1_5/CNTR_1$. These bits are part of TXM (Structure of Timer X mode register) and TYM (Structure of timer Y mode register (f is internal system clock)) registers.

(4) Pulse width measurement mode

This mode is available with timer X only.

- Count source
The count source is the output of timer X clock divider. The division ratio can be selected by the timer Y mode register.
- Operation
The timer counts down while the input signal level on $P1_4/CNTR_0$ matches the active polarity selected by the $CNTR_0$ polarity selection bit of TXM (Structure of Timer X mode register). On a timer underflow, the timer X interrupt request bit will be set to "1", the contents of the timer latches are reloaded to the counters and counting continues. When the input level changes from active polarity (as selected), the $CNTR_0$ interrupt request bit will be set to "1". The measurement result may be obtained by reading timer X during interrupt service.

(5) Pulse period measurement mode

This mode is available with timer Y only.

- Count source
The count source is the output of timer Y clock divider.

- Operation
The active edge of input signal to be measured can be selected by $CNTR_1$ polarity selection bit (Fig. 18). When this bit is set to "0", the time between two consecutive falling edges of the signal input to $P1_5/CNTR_1$ pin will be measured, when the polarity bit is set to "1", the time between two consecutive rising edges will be measured.
The timer counts down. On detection of an active edge of input signal, the contents of the TY counters will be transferred to temporary registers assigned to the same addresses as TY. At the same time, the contents of TY latches will be reloaded to the counters and counting continues. The active edge of input signal also causes the $CNTR_1$ interrupt request bit to be set to "1". The measurement result may be obtained by reading timer Y during interrupt service.

(6) H/L pulse width measurement mode

This mode is available with timer Y only.

- Count source
The count source is the output of the timer Y's clock divider.
- Operation
This mode measures both the "H" and "L" periods of a signal input to $P1_5/CNTR_1$ pin continuously. On detection of any edge (rising or falling) of input signal to $P1_5/CNTR_1$ pin, the contents of timer Y counters are stored to temporary registers which are assigned to the same addresses as timer Y. At the same time, the contents of timer Y latches are reloaded to the counters and counting continues. The detection of an edge causes the $CNTR_1$ interrupt request bit to be set to "1" as well. The result of measurement may be obtained by reading timer Y during interrupt service. This read access will address the temporary registers. On a timer underflow, the timer Y interrupt request bit will be set to "1", the contents of timer Y latches will be transferred to the counters and counting continues.

TIMER 1, TIMER 2, TIMER 3

Timers 1 to 3 are 8-bit timers with 8-bit reload latches and one common pre-divider. Timer 1 can operate in the timer mode only,

whereas timers 2 and 3 can be used to generate a PWM output signal timing as well. Timers 1 to 3 are down count timers. See Fig. 21.

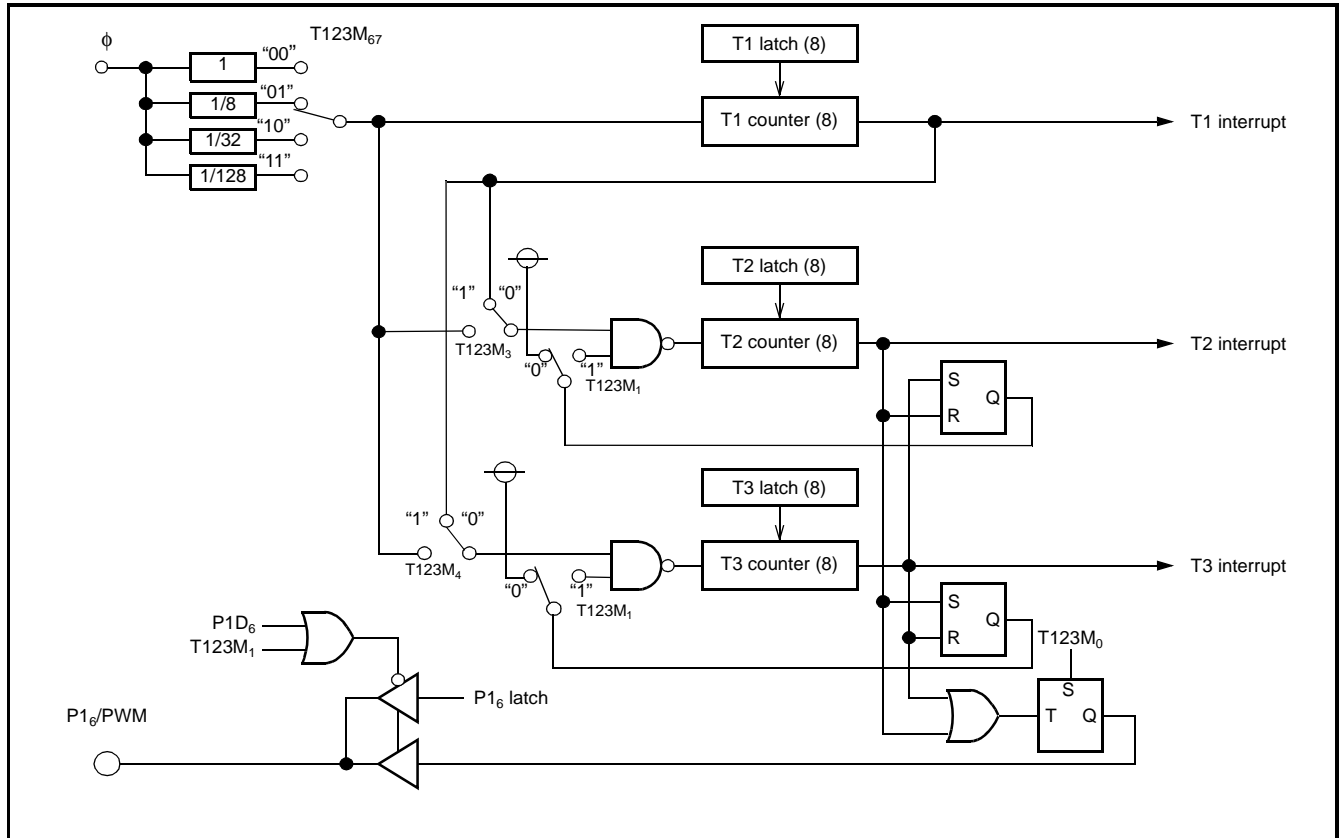


Fig. 21 Block diagram of timers 1 to 3 (ϕ is internal system clock)

Timer 1

The count source of timer 1 is the output of timer 123 pre-divider. The division ratio of the pre-divider can be selected by the pre-divider division ratio bits of timer 123 mode register (T123M). Refer to Timer 123 mode register configuration (f is internal system clock). On a timer 1 underflow, the timer 1 interrupt request bit will be set to "1".

Writing to timer 1 initializes the latch and counter.

Timers 2 and 3

The count source of timers 2 and 3 can be either the output of the timer 123 pre-divider or the timer 1 underflow. The count source can

be selected by the timer count source selection bits of timer 123 mode register (T123M).

Writing to timer 2 register affects the reload latch only or both of the reload latch and counter depending on the timer 2 write control bit of T123M. When the timer write control bit is set to "0", both latch and counter will be initialized simultaneously; when set to "1" only the reload latch will be initialized, on an underflow, the counter will be set to the modified reload value. Writing to timer 3 initializes latch and counter both.

Timer 2 or 3 underflow causes the timer 2 or 3 interrupt request bit to be set to "1".

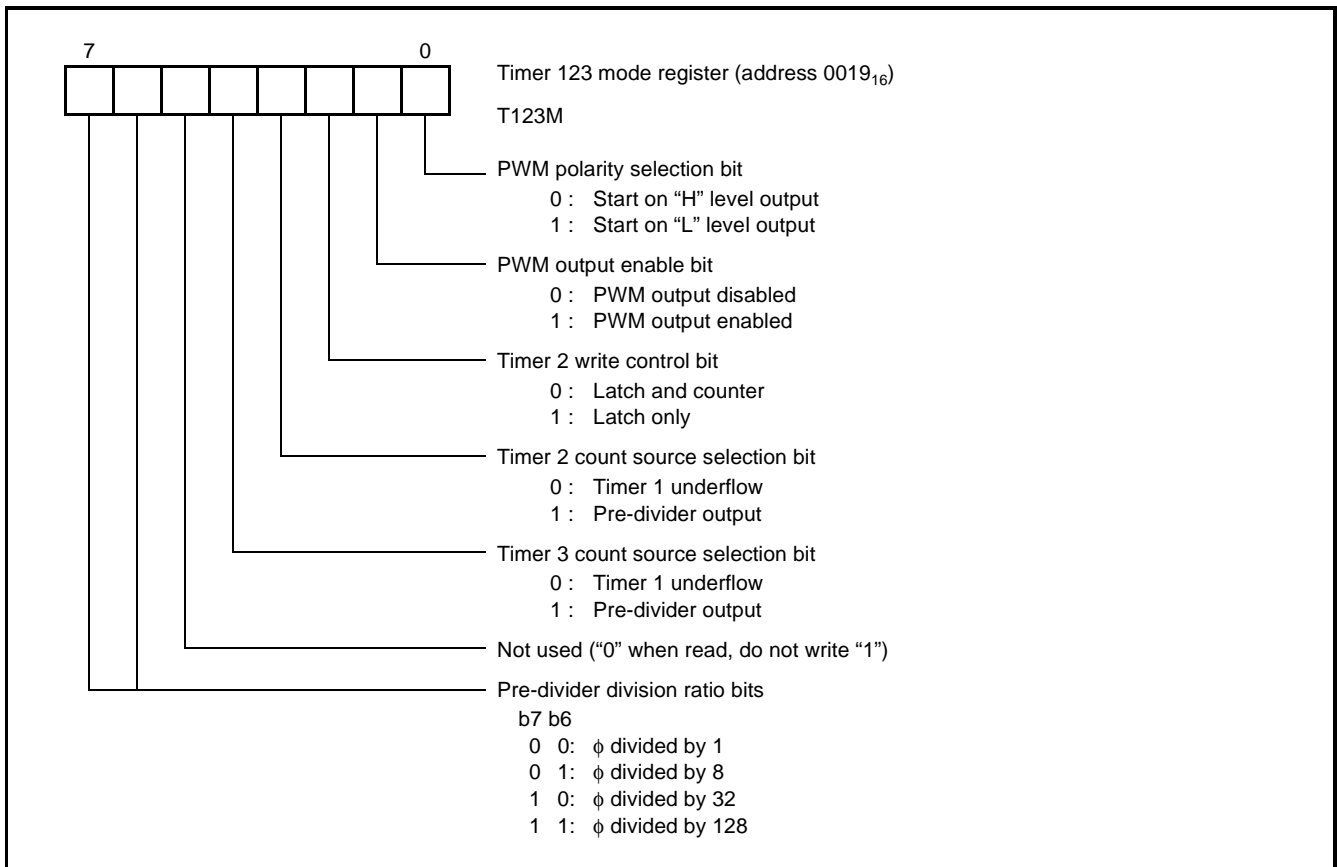


Fig. 22 Timer 123 mode register configuration (ϕ is internal system clock)

Operating Modes

(1) Timer Mode

This mode is available with timers 1 to 3.

- Count source
For timer 1, the count source is the output of the corresponding pre-divider. For timers 2 and 3, the count source can be separately selected to be either the pre-divider output or timer 1 underflow.
- Operation
The timer counts down. On a timer underflow, the corresponding timer interrupt request bit will be set to "1", the contents of the corresponding timer latch will be reloaded to the counter and counting continues.

(2) PWM Mode

This mode is available with timer 2 and 3.

- Count source
The count source can be separately selected to be either the pre-divider output or timer 1 underflow.
- Operation
When the PWM-mode is enabled, timer 2 starts counting. As soon as timer 2 underflows, timer 2 stops and timer 3 starts counting. If bit 0 is set, timer 2 determines the low duration and the initial output level is low. Timer 3 determines the high duration. If bit 0 is zero timer 2 determines the high duration and the initial output level is high. In this case timer 3 determines the low duration.

Note: Be sure to configure the P1₆/PWM pin as an output port before using PWM mode.

SERIAL I/Os

The serial I/O section of 7630 group consists of one clock synchronous and one asynchronous (UART) interface.

Clock Synchronous Serial I/O (SIO)

The clock synchronous interface allows full duplex communication based on 8 bit word length. The transfer clock can be selected from an internal or external clock. When an internal clock is selected, a programmable clock divider allows eight different transmission

speeds. Refer to Block diagram of clock synchronous I/O (f is internal system clock). The operation of the clock synchronous serial I/O can be configured by the serial I/O control register SIOCON; refer to Fig. 25.

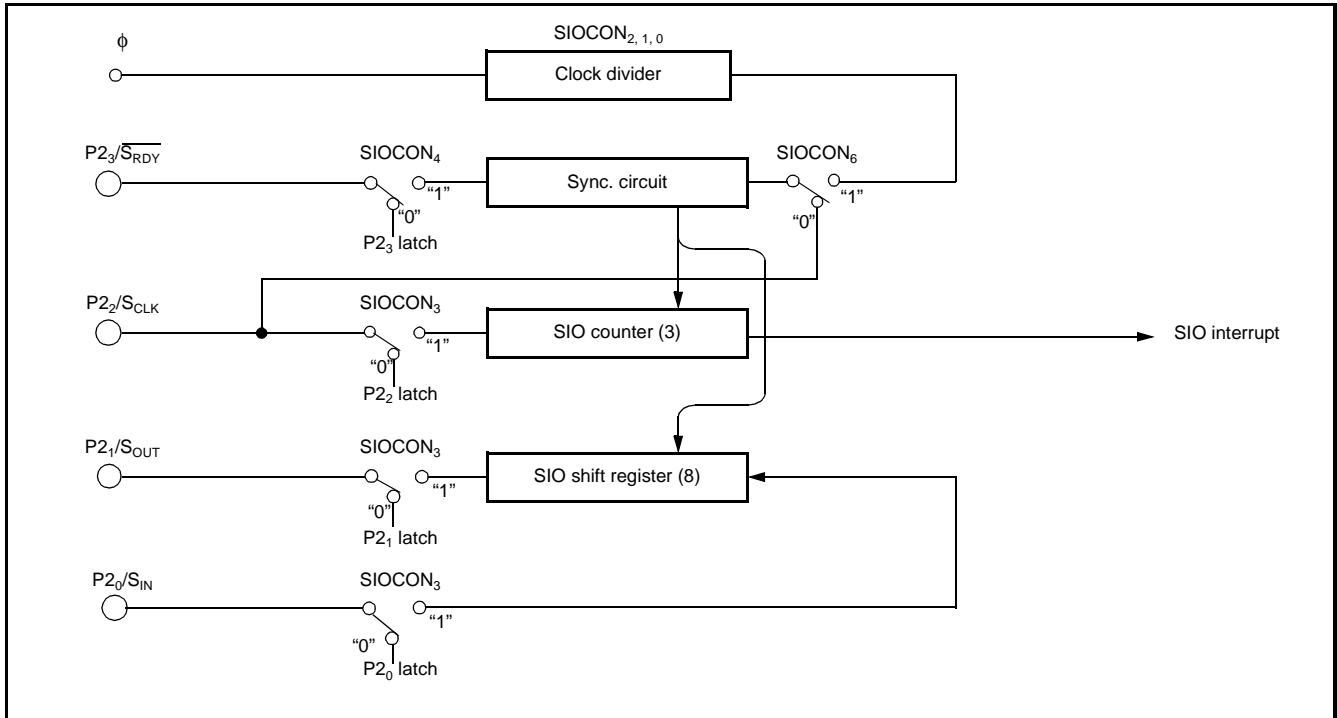


Fig. 23 Block diagram of clock synchronous I/O (phi is internal system clock)

(1) Clock synchronous serial I/O operation

Either an internal or external transfer clock can be selected by bit 6 of SIOCON. The internal clock divider can be programmed by bits 0 to 2 of SIOCON. Bit 3 of SIOCON determines whether the double function pins P2₀ to P2₂ will act as I/O ports or serve as SIO pins. Bit 4 of SIOCON allows the same selection for pin P2₃.

When an internal transfer clock is selected, transmission can be triggered by writing data to the SIO shift register (SIO, address

0012₁₆). After an 8-bit transmission has been completed, the S_{OUT} pin will change to high impedance and the SIO interrupt request bit will be set to "1".

When an external transfer clock is selected, the SIO interrupt request bit will be set to "1" after 8 cycles but the contents of the SIO shift register continue to be shifted while the transfer clock is being input. Therefore, the clock needs to be controlled externally; the S_{OUT} pin will not change to high impedance automatically.

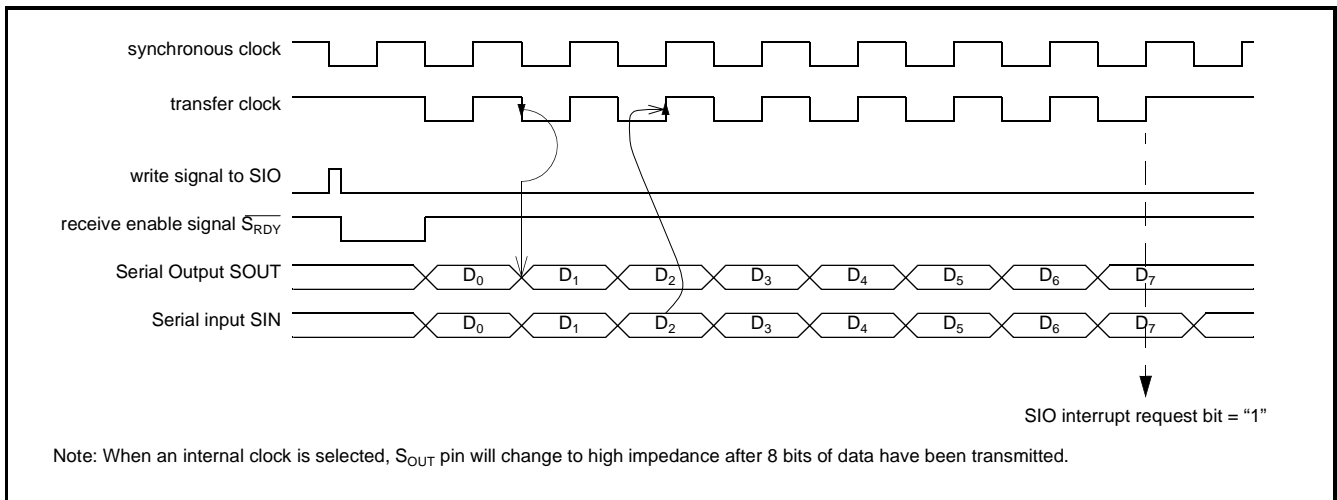


Fig. 24 Timing of clock synchronous SIO function (LSB first selected)

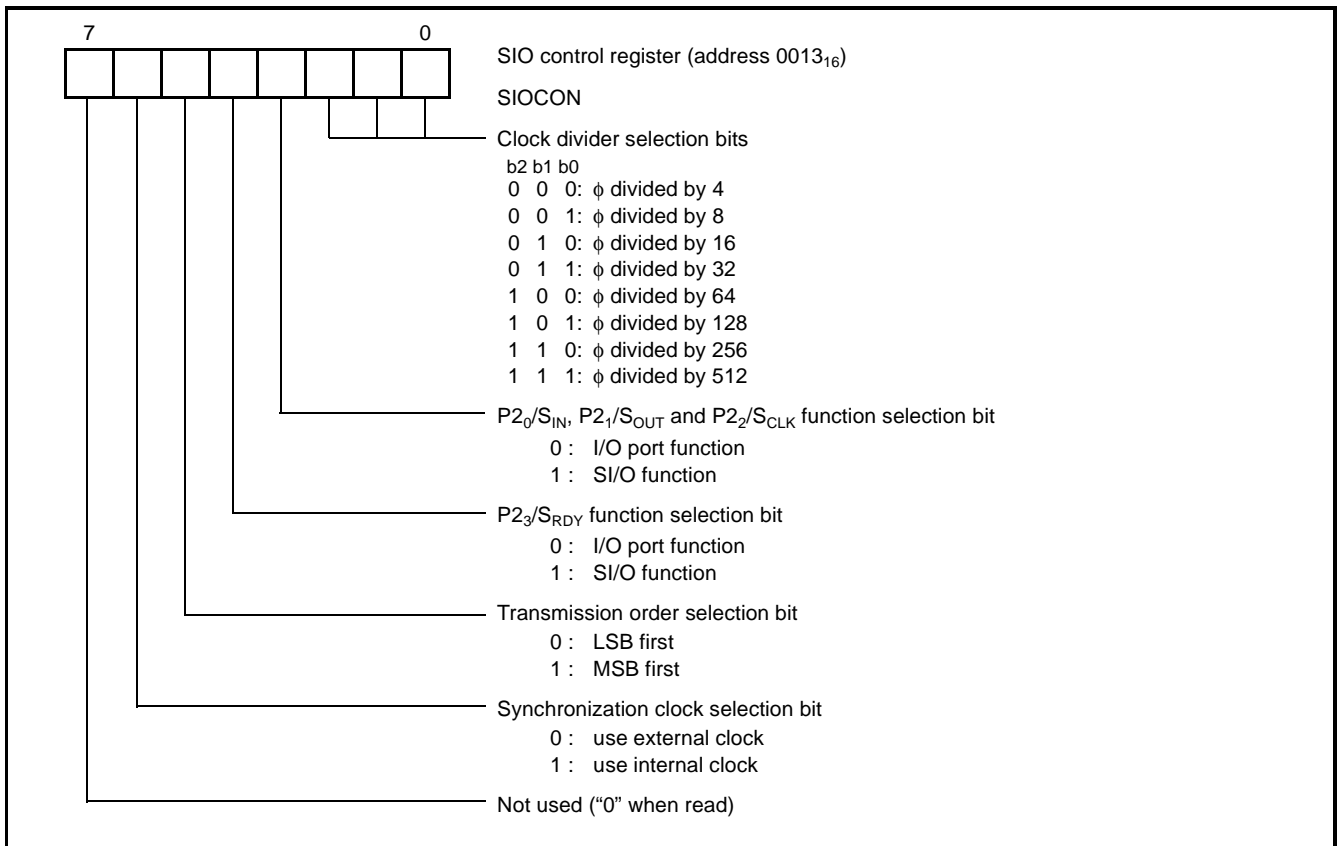


Fig. 25 Structure of serial I/O control register (ϕ is internal system clock)

Clock Asynchronous Serial I/O (UART)

The UART is a full duplex asynchronous transmit/receive unit. The built-in clock divider and baud rate generator enable a broad range of transmission speeds. Please refer to Block diagram of UART.

(1) Description

The transmit and receive shift registers have a buffer (consisting of high and low order byte) each. Since the shift registers cannot be

written to or read from directly, transmit data is written to the transmit buffer and receive data is read from the receive buffer. A transmit or receive operation will be triggered by the transmit enable bit and receive enable bit of the UART control register UCON (see Structure of UART control register). The double function terminals P₂₅/UT_xD, P₂₆/UR_TS and P₂₄/UR_xD, P₂₇/UR_TS will be switched to serve as UART pins automatically.

(2) Baud rate selection

The baud rate of transmission and reception is determined by the setting of the prescaler and the contents of the UART baud rate generator register. It is calculated by: where p is the division ratio of

$$b = \frac{\phi}{16 \cdot p \cdot (n + 1)}$$

the prescaler and n is the content of UART baud rate generator register. The prescaler's division ratio can be selected by the UART mode register (see below).

UART mode register (UMOD, Structure of UART mode register)

The UART mode register allows to select the transmission and reception format with the following options:

- word length: 7, 8 or 9 bits
- parity: none, odd or even
- stop bits: 1 or 2

It allows to select the prescaler's division ratio as well.

UART baud rate generator (UBRG)

This 8 bit register allows to select the baud rate of the UART (see above). Set this register to the desired value before enabling reception or transmission.

UART control register (UCON, Structure of UART control register)

The UART control register consists of four control bits (bit 0 to bit 3) which allow to control reception and transmission.

UART status register (USTS, Structure of UART status register)

The read-only UART status register consists of 7 bits (bit 0 to bit 6) which indicate the operating status of the UART function and various errors.

(3) Handshaking signals

When used as transmitter the UART will recognize the clear-to-send signal via $P2_7/\overline{UCTS}$ terminal for handshaking. When used as receiver it will issue a request-to-send signal through $P2_6/\overline{URTS}$ pin.

Clear-to-send input

When used as a transmitter (transmit enable bit set to "1"), the UART starts transmission after recognizing "L" level on $P2_7/\overline{UCTS}$. After started the UART will continue to transmit regardless of the actual level of $P2_7/\overline{UCTS}$ or status of the transmit enable bit.

Request-to-send output

The UART controls the $P2_6/\overline{URTS}$ output according to the following conditions.

Table 5: Output control conditions

| Condition | $P2_6/\overline{URTS}$ |
|---|------------------------|
| Receive enable bit is set to "1" | "L" |
| Reception completed during receive enable bit set to "1" | |
| Start bit (falling edge) detected | "H" |
| Receive enable bit is set to "0" before reception started | |
| Hardware reset | |
| Receive initialization bit is set to "1" | |

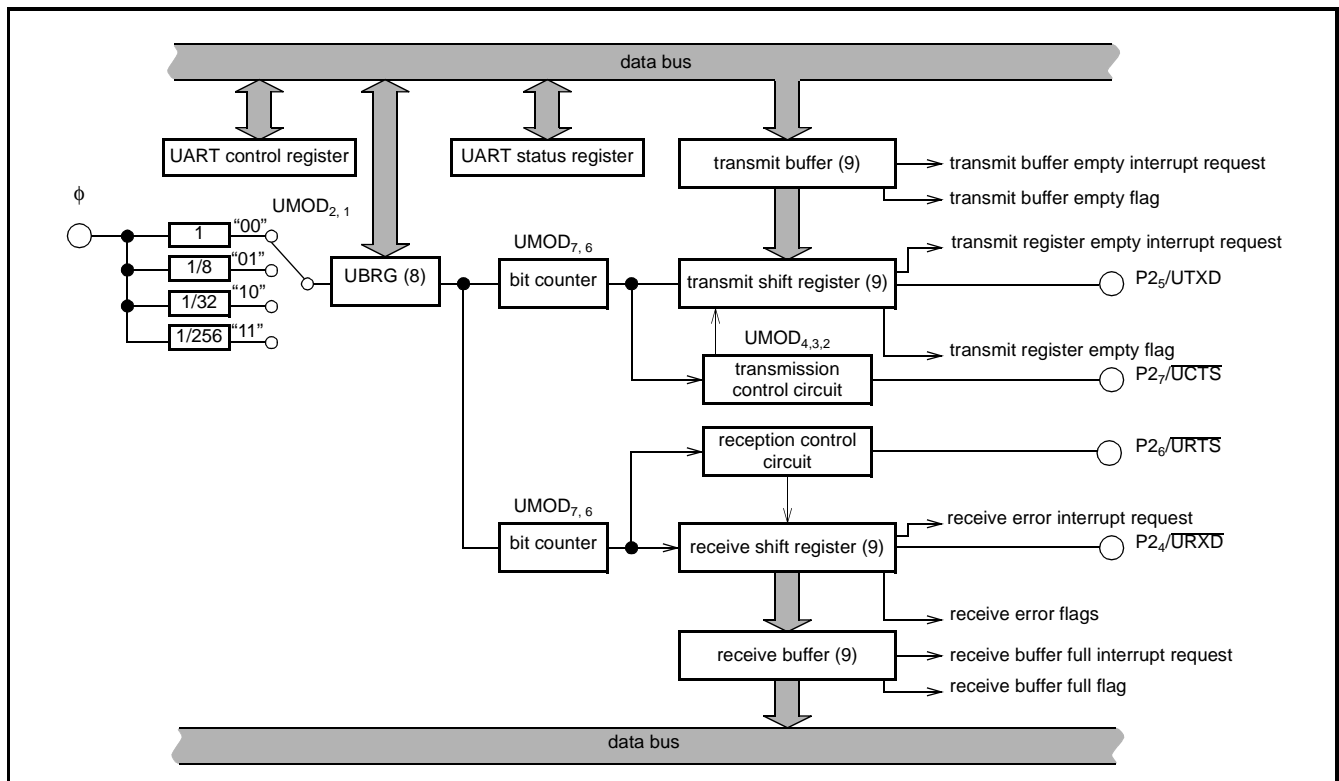


Fig. 26 Block diagram of UART

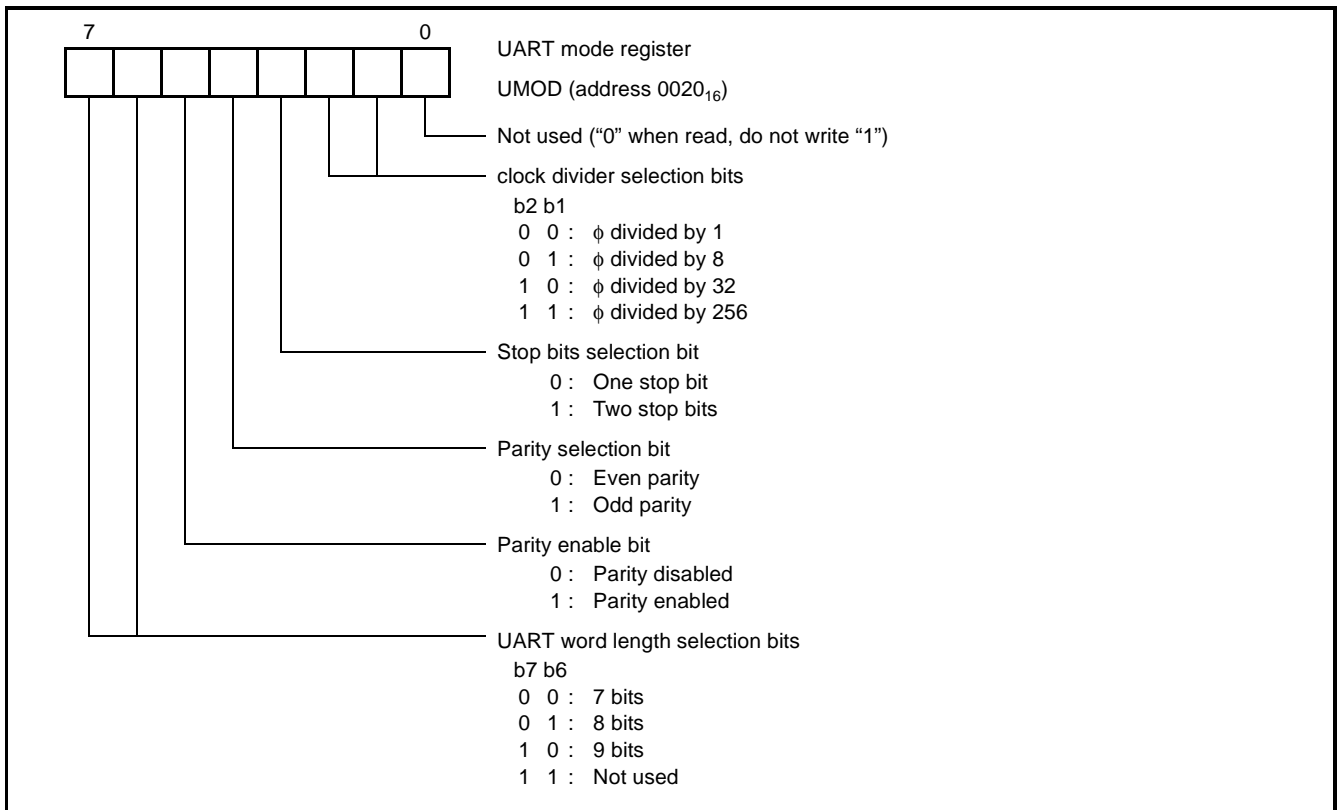


Fig. 27 Structure of UART mode register

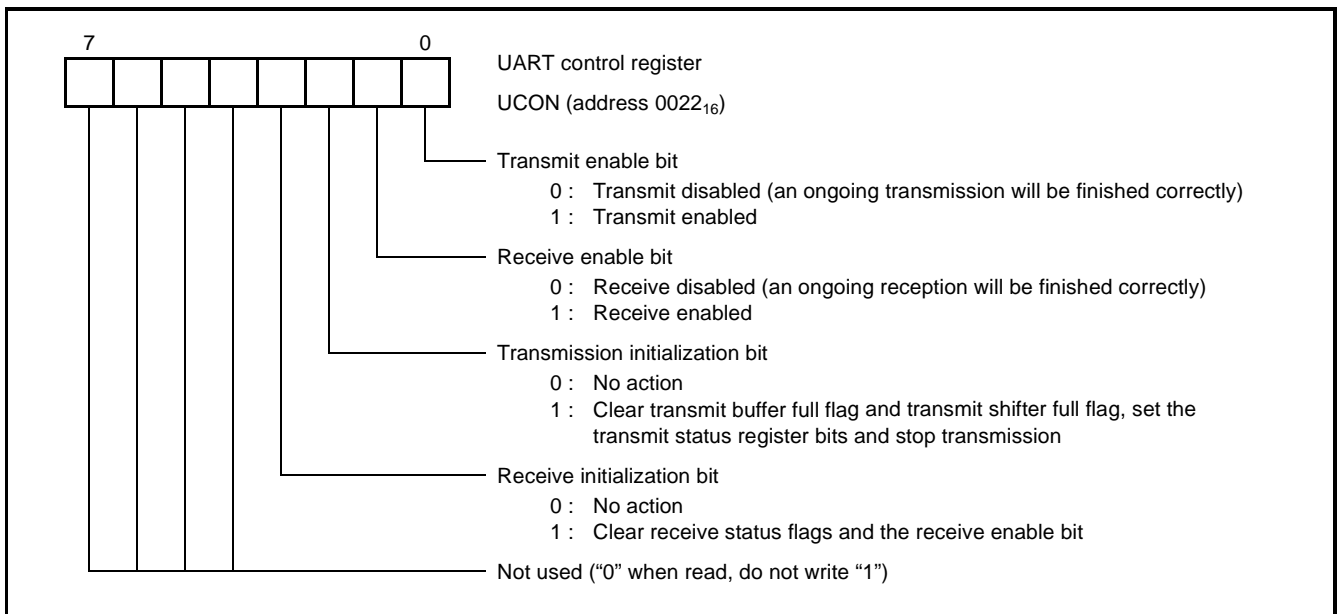


Fig. 28 Structure of UART control register

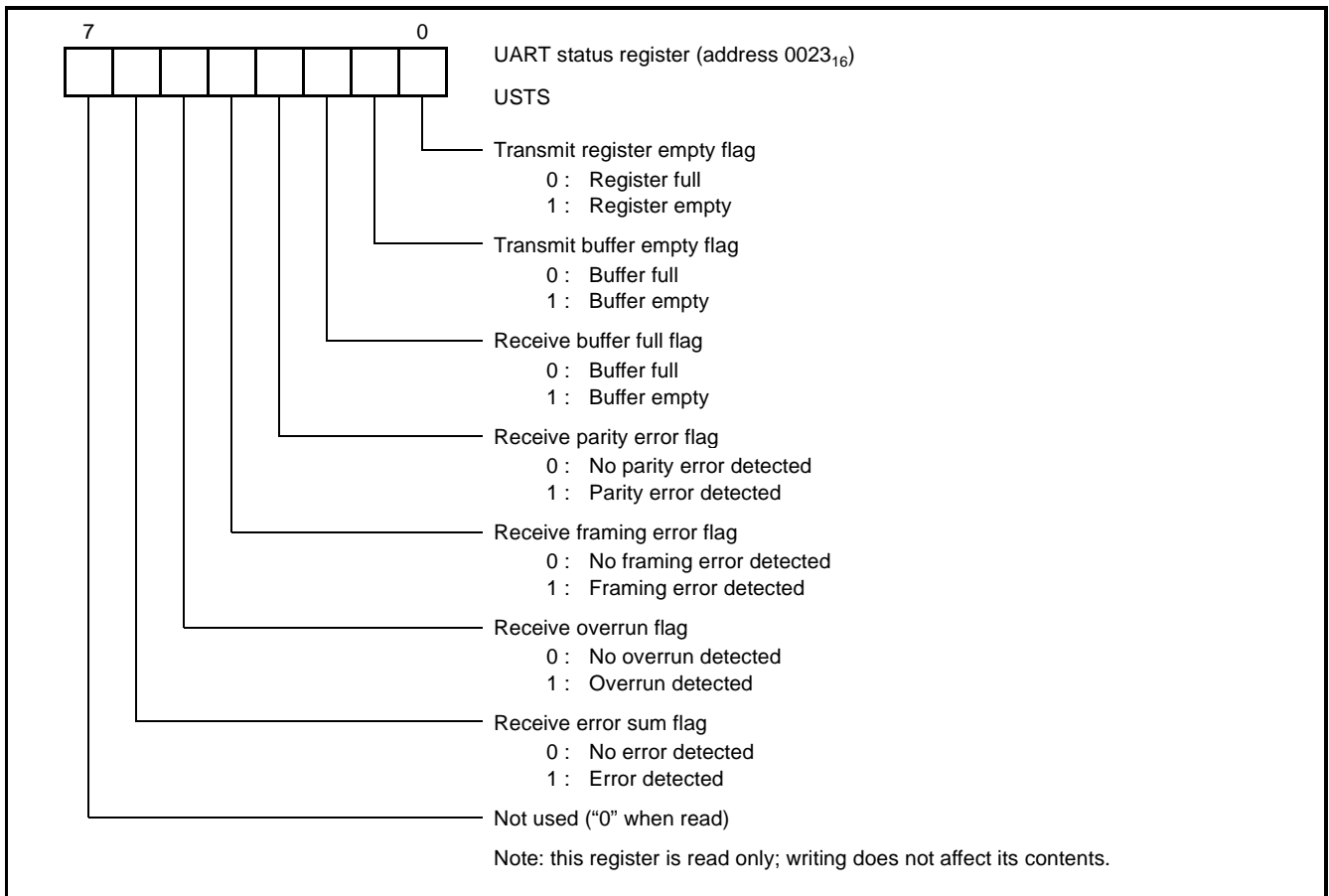


Fig. 29 Structure of UART status register

CAN MODULE

The CAN (Controller Area Network) interface of the 7630 group complies with the 2.0B specification, enabling reception and transmission of frames with either 11- or 29- bit identifier length. Refer to Fig. 31 for a block diagram of the CAN interface.

The programmer's interface to the CAN module is formed by three status/control registers (Fig. 32, Fig. 33, Fig. 34), two bus timing control registers (Fig. 35 Fig. 36), several registers for acceptance filtering (Fig. 37), the transmit and receive buffer registers (Fig. 38) and one dominant level control bit (Fig. 22).

Baud Rate Selection

A programmable clock prescaler is used to derive the CAN module's basic clock from the internal system clock frequency (ϕ). Bit 0 to bit 3 of the CAN bus timing control register represent the prescaler allowing a division ratio from 1 to 1/16 to be selected. So the CAN module basic clock frequency f_{CANB} can be calculated as follows:

$$f_{CANB} = \frac{\phi}{p + 1}$$

where p is the value of the prescaler (selectable from 1 to 15). The effective baud rate of the CAN bus communication depends on the CAN bus timing control parameters and will be explained below.

CAN Bus Timing Control

Each bit-time consists of four different segments (see Fig. 30):

- Synchronization segment (SS),
- Propagation time segment (PTS),
- Phase buffer segment 1 (PBS1) and
- Phase buffer segment 2 (PBS2).

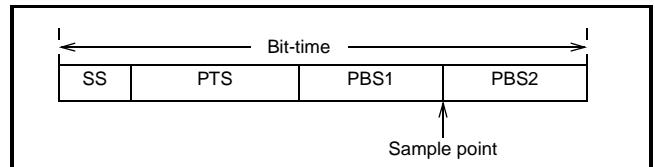


Fig. 30 Bit time of CAN module

The first of these segments is of fixed length (one Time Quantum) and the latter three can be programmed to be 1 to 8 Time Quanta by the CAN bus timing control register 1 and 2 (see Fig. 35 and Fig. 36). The whole bit-time has to consist of minimum 8 and maximum 25 Time Quanta. The duration of one Time Quantum is the cycle time of f_{CANB} . For example, assuming $\phi = 5$ MHz, $p = 0$, one Time Quantum will be 200 ns long. This allows the maximum transmission rate of 625 kb/s to be reached (assuming 8 Time Quanta per bit-time).

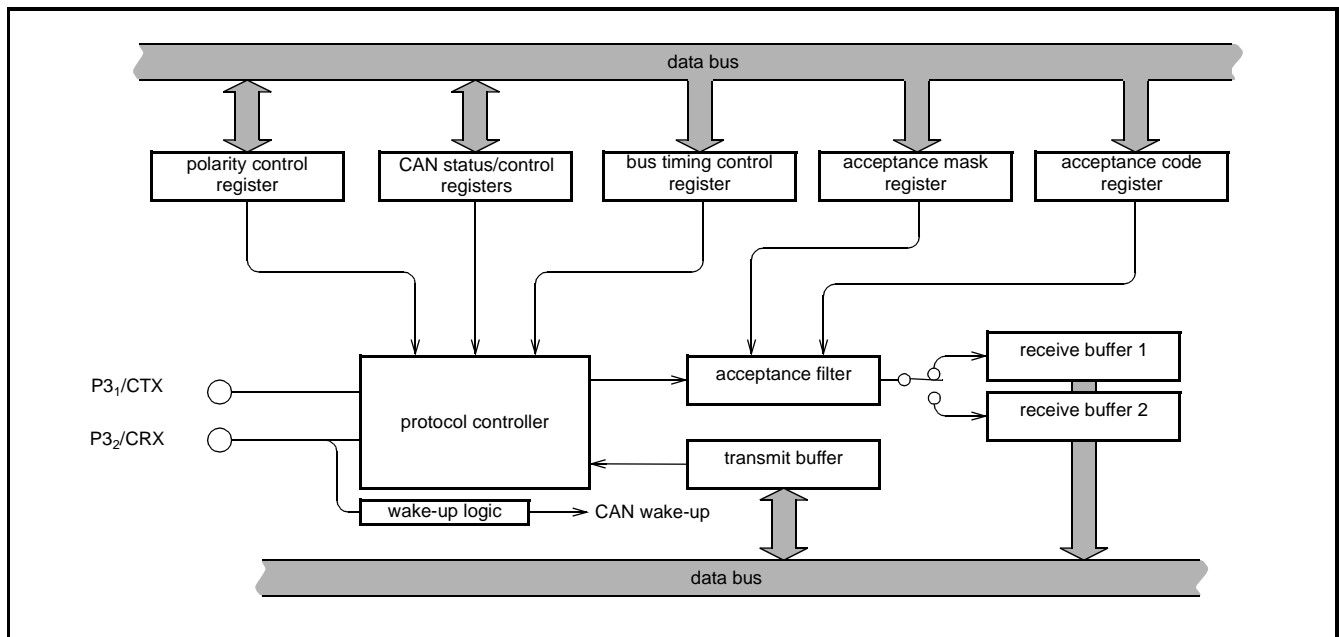


Fig. 31 Block diagram of CAN module

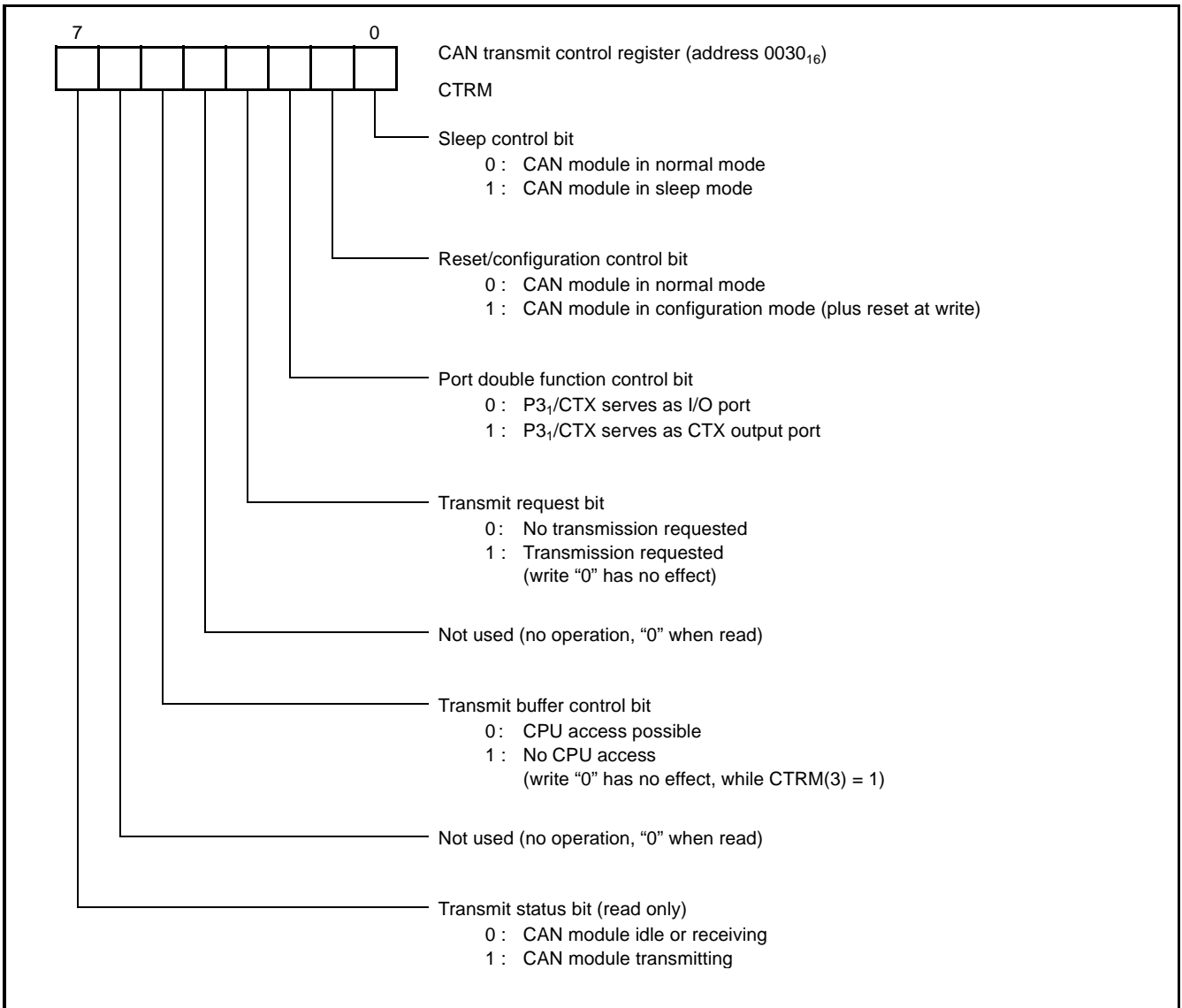


Fig. 32 Structure of CAN transmit control register

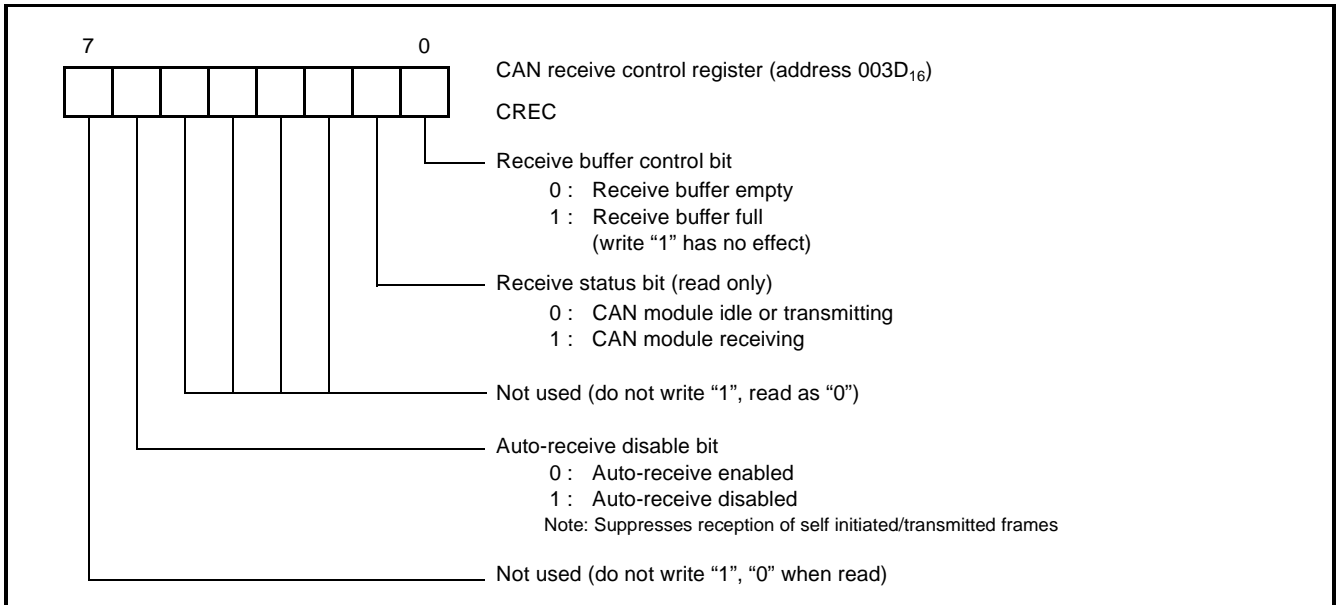


Fig. 33 Structure of CAN receive control register

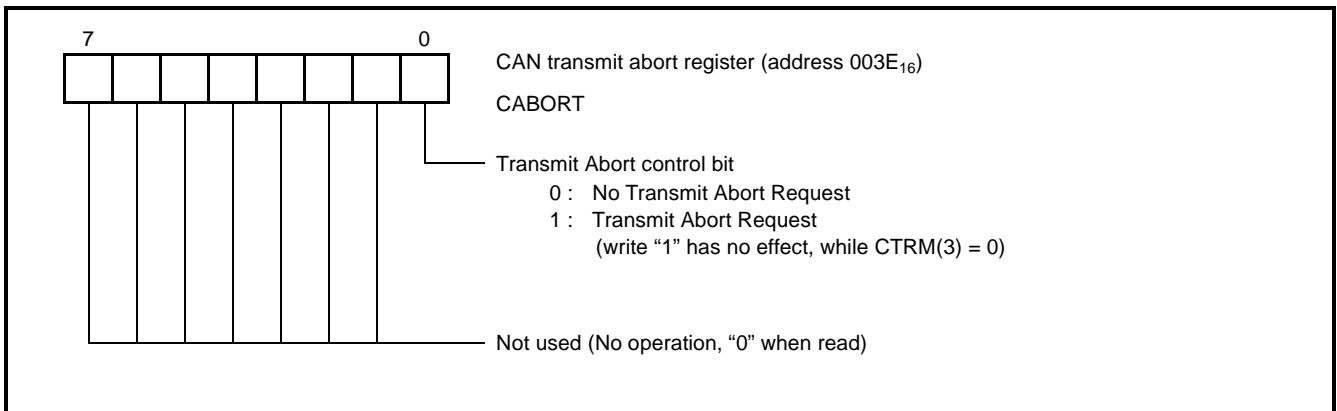


Fig. 34 Structure of CAN transmit abort register

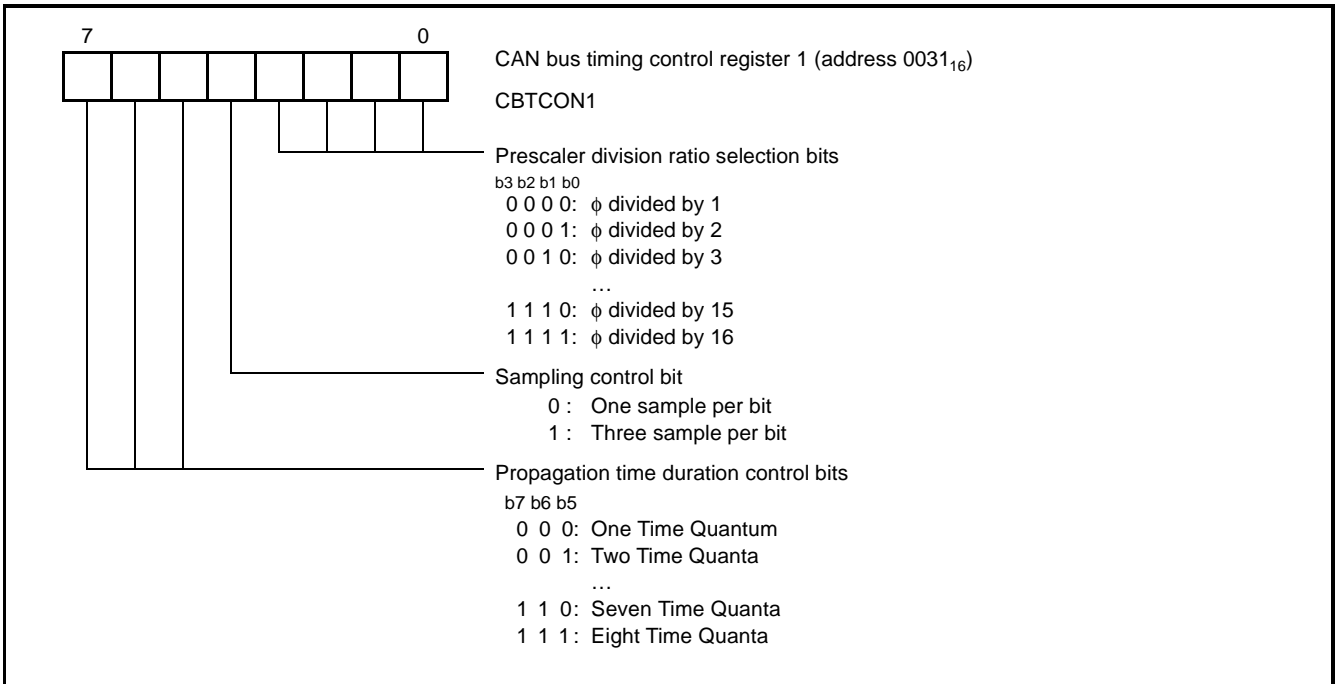


Fig. 35 Structure of CAN bus timing control register 1

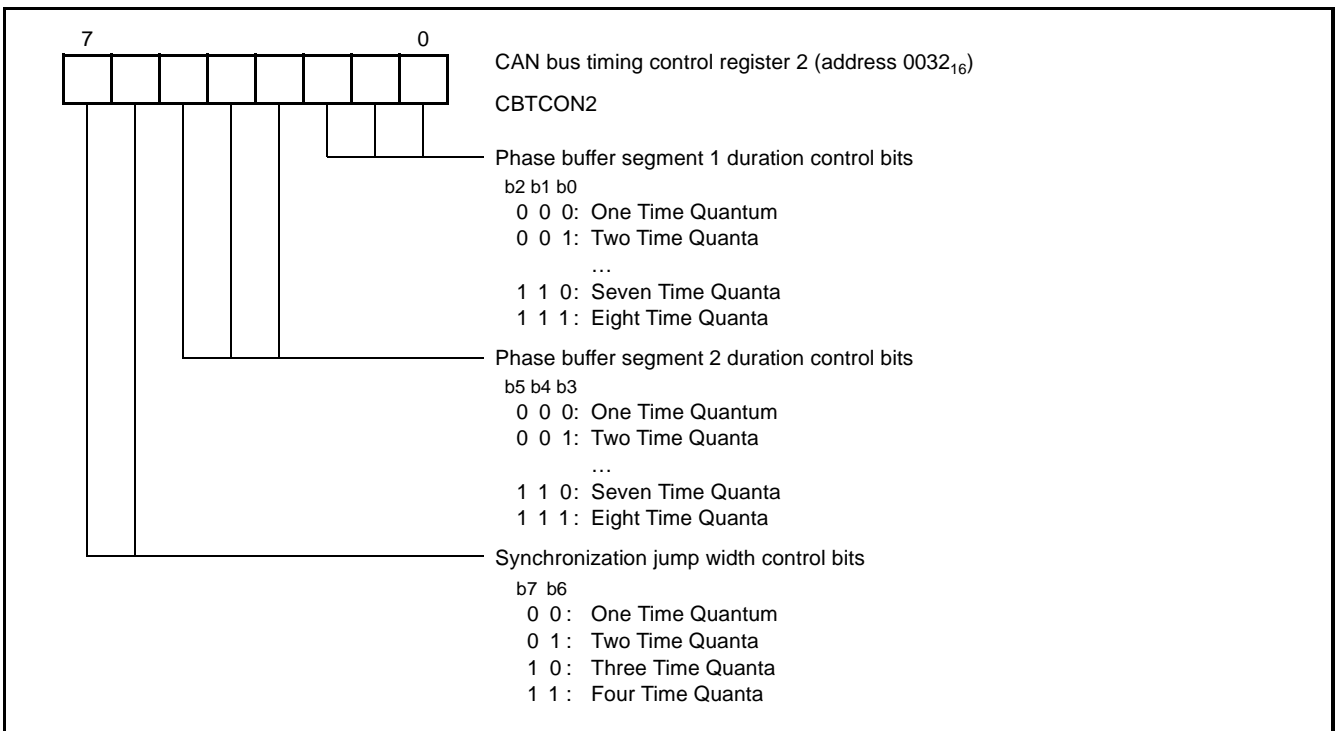


Fig. 36 Structure of CAN bus timing control register 2

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

| | name | 7 | | | | | | | | | 0 | address |
|---|------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--|--------------------|---------|
| Acceptance code registers: | CAC0 | Not used | Not used | Not used | CSID ₁₀ | CSID ₉ | CSID ₈ | CSID ₇ | CSID ₆ | | 0033 ₁₆ | |
| | CAC1 | CSID ₅ | CSID ₄ | CSID ₃ | CSID ₂ | CSID ₁ | CSID ₀ | Not used | Not used | | 0034 ₁₆ | |
| | CAC2 | Not used | Not used | Not used | Not used | CEID ₁₇ | CEID ₁₆ | CEID ₁₅ | CEID ₁₄ | | 0035 ₁₆ | |
| | CAC3 | CEID ₁₃ | CEID ₁₂ | CEID ₁₁ | CEID ₁₀ | CEID ₉ | CEID ₈ | CEID ₇ | CEID ₆ | | 0036 ₁₆ | |
| | CAC4 | CEID ₅ | CEID ₄ | CEID ₃ | CEID ₂ | CEID ₁ | CEID ₀ | Not used | Not used | | 0037 ₁₆ | |
| Select the bit pattern of identifiers which allows to pass acceptance filtering. | | | | | | | | | | | | |
| Acceptance mask registers: | CAM0 | Not used | Not used | Not used | MSID ₁₀ | MSID ₉ | MSID ₈ | MSID ₇ | MSID ₆ | | 0038 ₁₆ | |
| | CAM1 | MSID ₅ | MSID ₄ | MSID ₃ | MSID ₂ | MSID ₁ | MSID ₀ | Not used | Not used | | 0039 ₁₆ | |
| | CAM2 | Not used | Not used | Not used | Not used | MEID ₁₇ | MEID ₁₆ | MEID ₁₅ | MEID ₁₄ | | 003A ₁₆ | |
| | CAM3 | MEID ₁₃ | MEID ₁₂ | MEID ₁₁ | MEID ₁₀ | MEID ₉ | MEID ₈ | MEID ₇ | MEID ₆ | | 003B ₁₆ | |
| | CAM4 | MEID ₅ | MEID ₄ | MEID ₃ | MEID ₂ | MEID ₁ | MEID ₀ | Not used | Not used | | 003C ₁₆ | |
| 0 : Mask identifier bit (do not care) 1 : Compare identifier bit with acceptance code register bit (Not used: write to "0") | | | | | | | | | | | | |

Fig. 37 Structure of CAN mask and code registers

| | name | 7 | | | | | | | | | 0 | offset |
|--|------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--|--------------------|--------|
| | CTB0, CRB0 | Not used | Not used | Not used | SID ₁₀ | SID ₉ | SID ₈ | SID ₇ | SID ₆ | | 0000 ₁₆ | |
| | CTB1, CRB1 | SID ₅ | SID ₄ | SID ₃ | SID ₂ | SID ₁ | SID ₀ | RTR/SRR | IDE | | 0001 ₁₆ | |
| | CTB2, CRB2 | Not used | Not used | Not used | Not used | EID ₁₇ | EID ₁₆ | EID ₁₅ | EID ₁₄ | | 0002 ₁₆ | |
| | CTB3, CRB3 | EID ₁₃ | EID ₁₂ | EID ₁₁ | EID ₁₀ | EID ₉ | EID ₈ | EID ₇ | EID ₆ | | 0003 ₁₆ | |
| | CTB4, CRB4 | EID ₅ | EID ₄ | EID ₃ | EID ₂ | EID ₁ | EID ₀ | RTR | r1 | | 0004 ₁₆ | |
| | CTB5, CRB5 | Not used | Not used | Not used | r ₀ | DLC ₃ | DLC ₂ | DLC ₁ | DLC ₀ | | 0005 ₁₆ | |
| | CTB6, CRB6 | data byte 0 | | | | | | | | | 0006 ₁₆ | |
| | CTB7, CRB7 | data byte 1 | | | | | | | | | 0007 ₁₆ | |
| | CTB8, CRB8 | data byte 2 | | | | | | | | | 0008 ₁₆ | |
| | CTB9, CRB9 | data byte 3 | | | | | | | | | 0009 ₁₆ | |
| | CTBA, CRBA | data byte 4 | | | | | | | | | 000A ₁₆ | |
| | CTBB, CRBB | data byte 5 | | | | | | | | | 000B ₁₆ | |
| | CTBC, CRBC | data byte 6 | | | | | | | | | 000C ₁₆ | |
| | CTBD, CRBD | data byte 7 | | | | | | | | | 000D ₁₆ | |
| Calculate the actual address as follows: TxD buffer address = 0040 ₁₆ + offset RxD buffer address = 0050 ₁₆ + offset (Not used: write to "0") | | | | | | | | | | | | |

Fig. 38 Structure of CAN transmission and reception buffer registers

Note 1: All CAN related SFRs must not be written in "CAN sleep" mode.

A-D CONVERTER

The A-D converter uses the successive approximation method with 8 bit resolution. The functional blocks of the A-D converter are described below. Refer to Block diagram of A-D converter.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} by 256, and outputs the divided voltage.

Channel Selector

The channel selector selects one of ports $P0_0/AN_0$ to $P0_7/AN_7$, and inputs its voltage to the comparator.

A-D conversion register AD

The A-D conversion register is a read-only register that stores the result of an A-D conversion. This register must not be read during an A-D conversion.

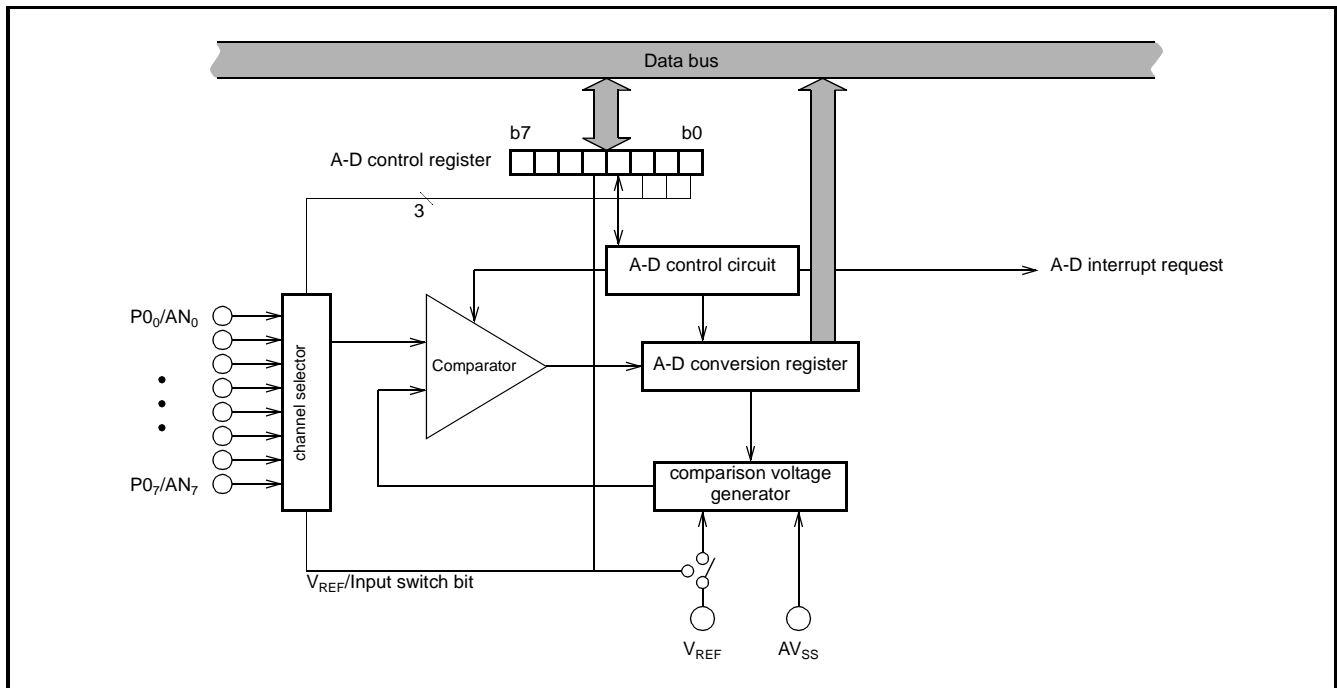


Fig. 39 Block diagram of A-D converter

A-D control register (Structure of A-D control register)

The A-D control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains "0" during an A-

D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion. Bit 4 is the V_{REF} /Input switch bit.

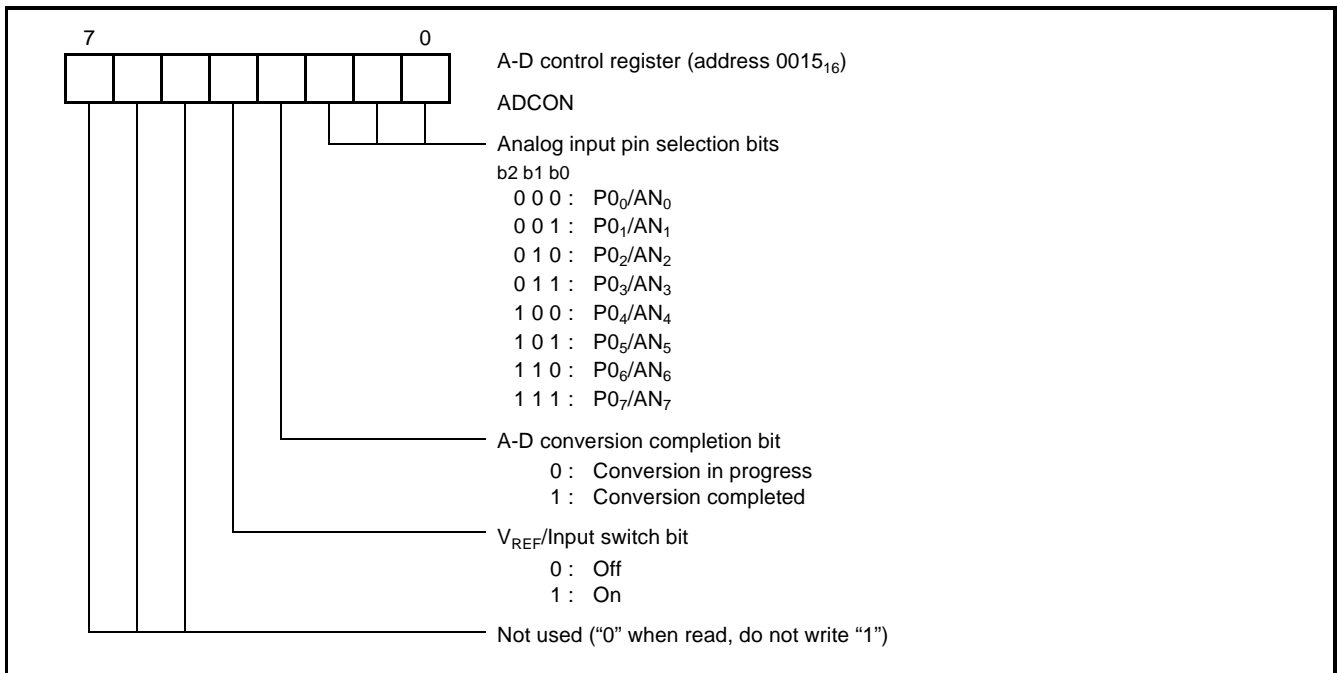


Fig. 40 Structure of A-D control register

A-D Converter Operation

The comparator and control circuit reference an analog input voltage with the reference voltage, then stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D inter-

rupt request bit to "1". The result of A-D conversion can be obtained from the A-D conversion register, AD (address 0014₁₆).

Note that the comparator is linked to a capacitor, so set $f(X_{IN})$ to 500 kHz or higher during A-D conversion.

WATCHDOG TIMER

The watchdog timer consists of two separate counters: one 7-bit counter (WD_H) and one 4-bit counter (WD_L). Cascading both counters or using the high-order counter allows only to select the time-out from either 524288 or 32768 cycles of the internal clock ϕ . Refer to Fig. 41 and Fig. 42. Both counters are addressed by the same watchdog timer register (WDT). When writing to this register, both counters will be set to the following default values:

- the high-order counter will be set to address 7F₁₆
- the low-order counter will be set to address F₁₆

regardless of the data written to the WDT register. Reading the watchdog timer register will return the corresponding control bit status, not the counter contents.

Once the WDT register is written to, the watchdog timer starts counting down and the watchdog timer interrupt is enabled. Once it is running, the watchdog timer cannot be disabled or stopped except by reset. On a watchdog timer underflow, a non-maskable watchdog timer interrupt will be requested.

To prevent the system being stopped by STP instruction, this instruction can be disabled by the STP instruction disable bit of WDT register. Once the STP instruction is disabled, it cannot be enabled again except by RESET.

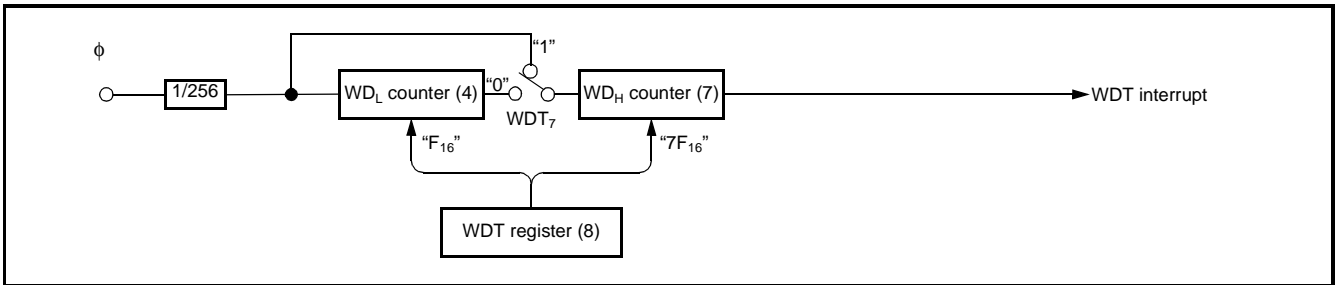


Fig. 41 Block diagram of watchdog timer

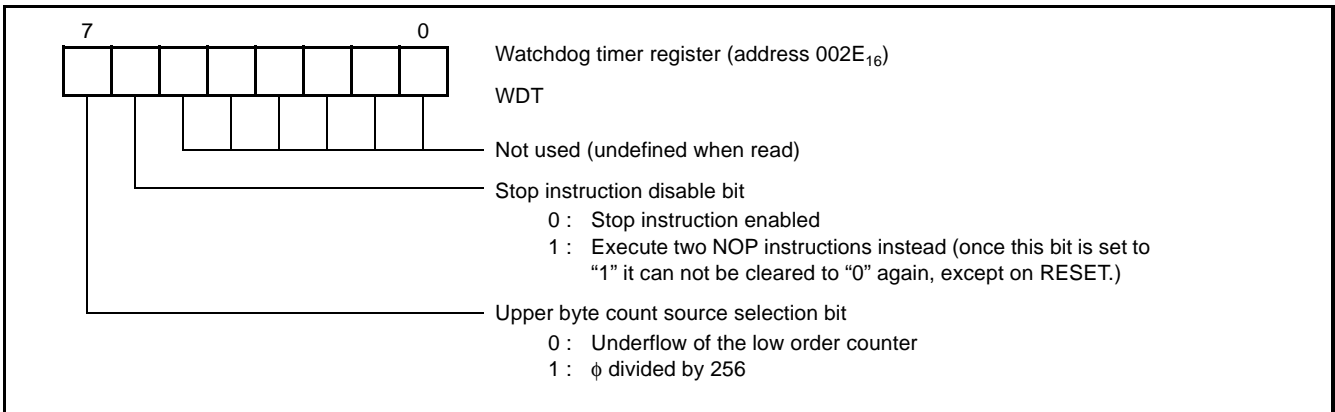


Fig. 42 Structure of watchdog timer register (ϕ is internal clock system)

RESET CIRCUIT

The 7630 group is reset according to the sequence shown in Fig. 44. It starts program execution from the address formed by the contents of the addresses $FFFB_{16}$ and $FFFA_{16}$, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than $2 \mu\text{s}$ while the power supply voltage is

in the recommended operating condition and then returned to "H" level.

Refer to Fig. 43 for an example of the reset circuit.

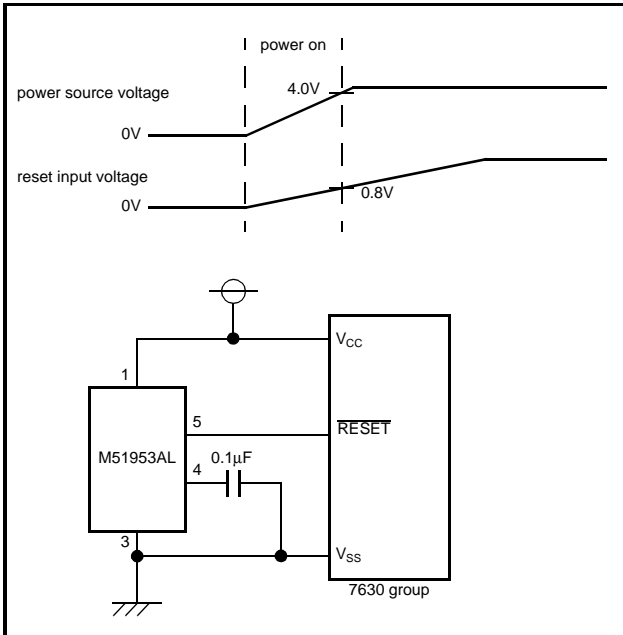


Fig. 43 Example of reset circuit

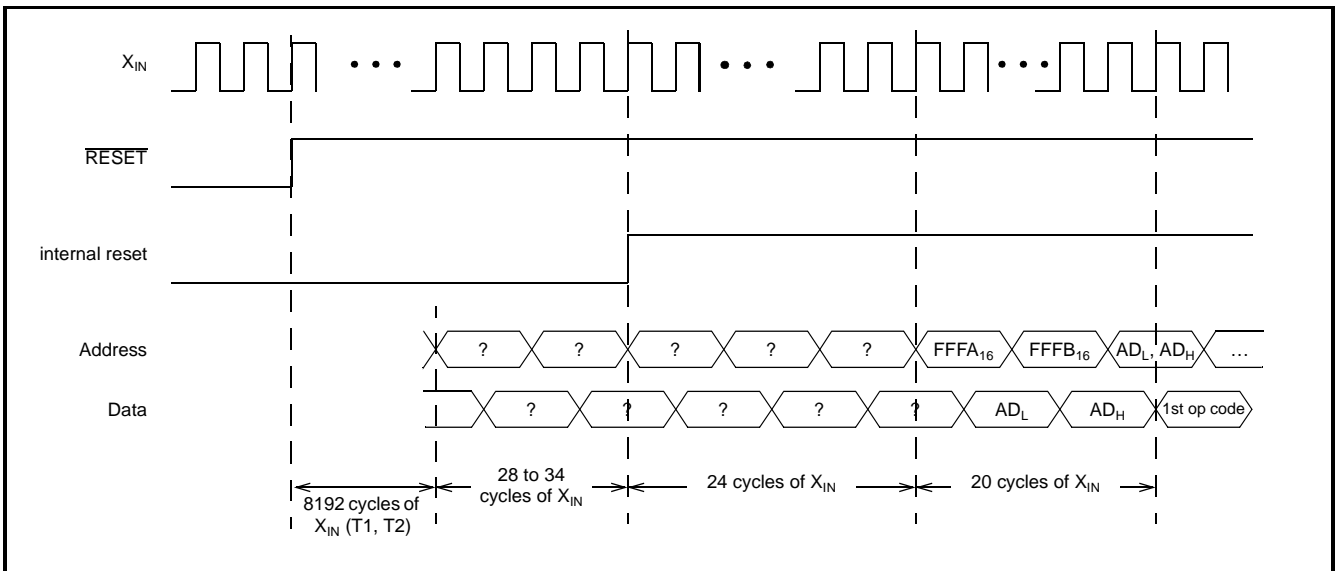


Fig. 44 Reset sequence

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| Register | Address | Register contents | Register | Address | Register contents |
|--------------------------|--------------------|-------------------|-----------------------------------|--------------------|--------------------------------|
| CPU mode reg. | 0000 ₁₆ | 48 ₁₆ | Timer XH | 001B ₁₆ | FF ₁₆ |
| Interrupt request reg. A | 0002 ₁₆ | 00 ₁₆ | Timer YL | 001C ₁₆ | FF ₁₆ |
| Interrupt request reg. B | 0003 ₁₆ | 00 ₁₆ | Timer YH | 001D ₁₆ | FF ₁₆ |
| Interrupt request reg. C | 0004 ₁₆ | 00 ₁₆ | Timer X mode reg. | 001E ₁₆ | 00 ₁₆ |
| Interrupt control reg. A | 0005 ₁₆ | 00 ₁₆ | Timer Y mode reg. | 001F ₁₆ | 00 ₁₆ |
| Interrupt control reg. B | 0006 ₁₆ | 00 ₁₆ | UART mode reg. | 0020 ₁₆ | 00 ₁₀ |
| Interrupt control reg. C | 0007 ₁₆ | 00 ₁₆ | UART control reg. | 0022 ₁₆ | 00 ₁₆ |
| Port P0 reg. | 0008 ₁₆ | 00 ₁₆ | UART status reg. | 0023 ₁₆ | 07 ₁₀ |
| Port P0 direction reg. | 0009 ₁₆ | 00 ₁₆ | Port P0 pull-up control reg. | 0028 ₁₆ | 00 ₁₆ |
| Port P1 reg. | 000A ₁₆ | 00 ₁₆ | Port P1 pull-up control reg. | 0029 ₁₆ | 00 ₁₆ |
| Port P1 direction reg. | 000B ₁₆ | 00 ₁₆ | Port P2 pull-up control reg. | 002A ₁₆ | 00 ₁₆ |
| Port P2 reg. | 000C ₁₆ | 00 ₁₆ | Port P3 pull-up control reg. | 002B ₁₆ | 00 ₁₆ |
| Port P2 direction reg. | 000D ₁₆ | 00 ₁₆ | Port P4 pull-up/down control reg. | 002C ₁₆ | 00 ₁₆ |
| Port P3 reg. | 000E ₁₆ | 00 ₁₆ | Interrupt polarity selection reg. | 002D ₁₆ | 00 ₁₆ |
| Port P3 direction reg. | 000F ₁₆ | 00 ₁₆ | Watchdog timer reg. | 002E ₁₆ | 3F ₁₆ |
| Port P4 reg. | 0010 ₁₆ | 00 ₁₆ | Polarity control reg. | 002F ₁₆ | 00 ₁₆ |
| Port P4 direction reg. | 0011 ₁₆ | 00 ₁₆ | CAN transmit control reg. | 0030 ₁₆ | 02 ₁₆ |
| Serial I/O control reg. | 0013 ₁₆ | 00 ₁₆ | CAN bus timing control reg. 1 | 0031 ₁₆ | 00 ₁₆ |
| A-D control reg. | 0015 ₁₆ | 08 ₁₆ | CAN bus timing control reg. 2 | 0032 ₁₆ | 00 ₁₆ |
| Timer 1 | 0016 ₁₆ | FF ₁₆ | CAN receive control reg. | 003D ₁₆ | 00 ₁₆ |
| Timer 2 | 0017 ₁₆ | 01 ₁₆ | CAN transmit abort reg. | 003E ₁₆ | 00 ₁₆ |
| Timer 3 | 0018 ₁₆ | FF ₁₆ | Processor status reg. | (PS) | 04 ₁₆ |
| Timer 123 mode reg. | 0019 ₁₆ | 40 ₁₆ | Program counter (high-order byte) | (PCH) | contents of FFFB ₁₆ |
| Timer XL | 001A ₁₆ | FF ₁₆ | Program counter (low-order byte) | (PCL) | contents of FFFA ₁₆ |

Note: The contents of RAM and registers other than the above registers are undefined after reset; thus software initialization is required.

Fig. 45 Internal status of microcomputer after reset

CLOCK GENERATING CIRCUIT

The 7630 group is equipped with an internal clock generating circuit.

Please refer to Fig. 46 for a circuit example using a ceramic resonator or quartz crystal oscillator. For the capacitor values, refer to the manufacturers recommended parameters which depend on each oscillators characteristics. When using an external clock, input it to the X_{IN} pin and leave X_{OUT} open.

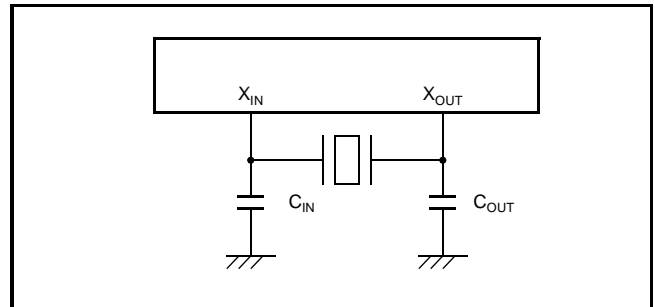


Fig. 46 Ceramic resonator circuit

Oscillation Control

The 7630 group has two low power modes: the stop and the wait mode.

Stop mode

The microcomputer enters the stop mode by executing the STP instruction. The oscillator stops with the internal clock ϕ at "H" level. Timers 1 and 2 will be cascaded and initialized by their reload latches contents. The count source for timer 1 will be set to $f(X_{IN})/16$.

Oscillation is restarted if an external interrupt is accepted or at reset. When using an external interrupt, the internal clock ϕ remains at "H" level until timer 2 underflows allowing a time-out until the

clock oscillation becomes stable. When using reset, a fixed time-out will be generated allowing oscillation to stabilize.

Wait mode

The microcomputer enters the wait mode by executing the WIT instruction. The internal clock ϕ stops at "H" level while the oscillator keeps running.

Recovery from wait mode can be done in the same way as from stop mode. However, the time-out period mentioned above is not required to return from wait-mode, thus no such time-out mechanism has been implemented.

Note: Set the interrupt enable bit of the interrupt source to be used to return from stop or wait mode to "1" before executing STP or WIT instruction.

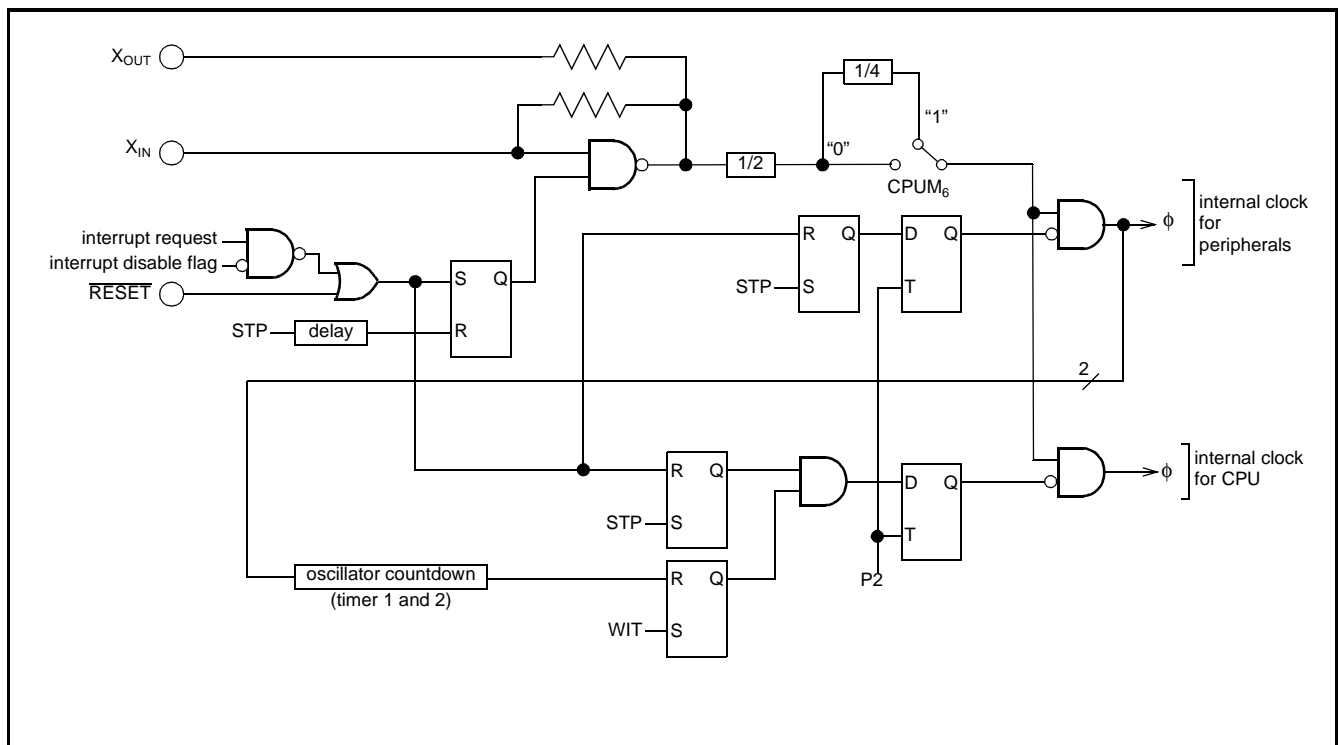


Fig. 47 Block diagram of clock generating circuit

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1 Mask ROM Order Confirmation Form
- 2 Mask Specification Form
- 3 Contents of Mask ROM, in EPROM form (three identical copies)

PROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general purpose PROM programmer using a special programming adapter. Set the address of PROM programmer to the user ROM area.

For the programming adapter type name, please refer to the following table:

Table 6: Programming adapter name

| MCU type | Package | Programming adapter type |
|---------------|---------|--------------------------|
| One Time PROM | 44P6N-A | PCA7430 |
| EPROM | 80D0 | PCA7431 |

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Fig. 48 is recommended to verify programming.

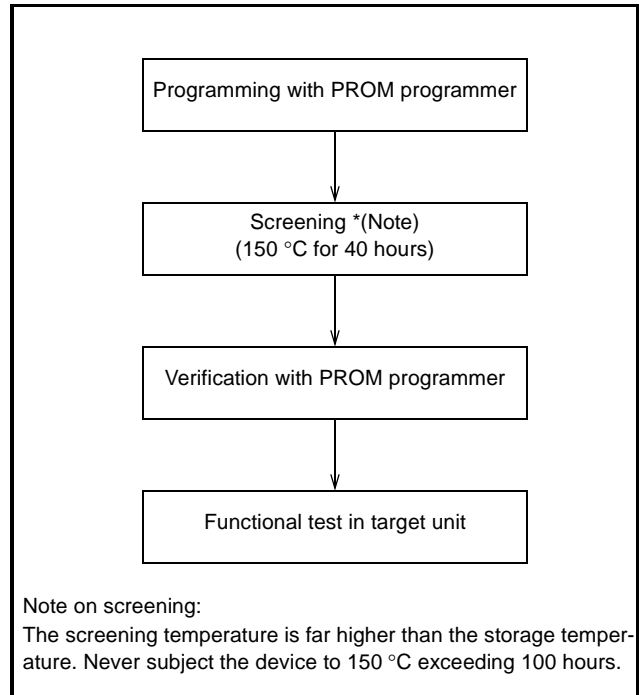


Fig. 48 Programming and testing of One Time PROM version

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Table 7: ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|--|---|------------------------|------|
| V_{CC} | Power source voltage | All voltages with respect to V_{SS} and output transistors are "off". | -0.3 to 7.0 | V |
| V_I | Input voltage P0 ₀ —P0 ₇ , P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , RESET, X _{IN} | | -0.3 to $V_{CC} + 0.3$ | V |
| V_O | Output voltage P0 ₀ —P0 ₇ , P1 ₂ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , X _{OUT} | | -0.3 to $V_{CC} + 0.3$ | V |
| P_d | Power dissipation | T _a = 25 °C | 500 | mW |
| T _{opr} | Operating temperature | | -40 to 85 | °C |
| T _{stg} | Storage temperature | | -60 to 150 | °C |

Table 8: RECOMMENDED OPERATING CONDITIONS

($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, T_a = -40 to 85 °C unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|----------------------------|---|---|------|--------------------|------|
| | | min. | typ. | max. | |
| V_{CC} | Power source voltage | 4.0 | 5.0 | 5.5 | V |
| V_{SS} | | | 0 | | V |
| V_{IH} | "H" Input voltage P0 ₀ —P0 ₇ , P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , RESET, X _{IN} | $0.8 \cdot V_{CC}$ | | V_{CC} | V |
| V_{IL} | "L" Input voltage P0 ₀ —P0 ₇ , P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , RESET, X _{IN} | 0 | | $0.2 \cdot V_{CC}$ | V |
| $\sum I_{OH}(\text{peak})$ | "H" sum peak output current P0 ₀ —P0 ₇ , P1 ₂ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ | | | -80 | mA |
| $\sum I_{OH}(\text{avg})$ | "H" sum average output current | | | -40 | mA |
| $\sum I_{OL}(\text{peak})$ | "L" sum peak output current | | | 80 | mA |
| $\sum I_{OL}(\text{avg})$ | "L" sum average output current | | | 40 | mA |
| $I_{OH}(\text{peak})$ | "H" peak output current | | | -10 | mA |
| $I_{OH}(\text{avg})$ | "H" average output current | | | -5 | mA |
| $I_{OL}(\text{peak})$ | "L" peak output current | | | 10 | mA |
| $I_{OL}(\text{avg})$ | "L" average output current | | | 5 | mA |
| I_{IO} | input current at overvoltage condition ($V_I > V_{CC}$) P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ | | | 1 | mA |
| $\sum I_{IO}$ | total input current at overvoltage condition ($V_I > V_{CC}$) P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ | | | 16 | mA |
| $f(\text{CNTR})$ | Timer input frequency (based on 50 % duty) | P1 ₄ /CNTR ₀ , P1 ₅ /CNTR ₁ (except bi-phase counter mode) | | $f(X_{IN})/16$ | MHz |
| | | P1 ₃ /TX ₀ , P1 ₄ /CNTR ₀ (bi-phase counter mode) | | $f(X_{IN})/32$ | MHz |
| $f(X_{IN})$ | Clock input oscillation frequency | | | 10 | MHz |

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Table 9: ELECTRICAL CHARACTERISTICS

($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, $T_a = -40$ to 85 °C unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-------------------|--|------------------------------------|--------------------|------|------|------|
| | | | min. | typ. | max. | |
| V_{OH} | "H" output voltage P0 ₀ —P0 ₇ , P1 ₂ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ | $I_{OH} = -5$ mA | $0.8 \cdot V_{CC}$ | | | V |
| V_{OL} | "L" output voltage P0 ₀ —P0 ₇ , P1 ₂ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ | $I_{OL} = 5$ mA | | | 2.0 | V |
| $V_{T+} - V_{T-}$ | Hysteresis P1 ₁ /INT ₀ , P1 ₂ /INT ₁ , P1 ₃ /TX ₀ , P1 ₄ /CNTR ₀ , P1 ₅ /CNTR ₁ , P2 ₀ /S _{IN} , P2 ₂ /S _{CLK} , P2 ₆ /U _{RTS} , P2 ₇ /U _{CTS} , P3 ₂ /CRX, RESET | | | 0.5 | | V |
| I_{IH} | "H" input current P0 ₀ —P0 ₇ , P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , RESET | $V_I = V_{CC}$ | | | 5 | μA |
| I_{IH} | "H" input current X _{IN} | $V_I = V_{CC}$ | | 4 | | μA |
| I_{IL} | "L" input current P0 ₀ —P0 ₇ , P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , RESET | $V_I = V_{SS}$ | | | -5 | μA |
| I_{IL} | "L" input current X _{IN} | $V_I = V_{SS}$ | | -4 | | μA |
| I_{IH} | "H" input current P3 ₂ , P4 ₀ —P4 ₇ | $V_I = V_{CC}$ Pull-Down = 'On' | 20 | | 200 | μA |
| I_{IL} | "L" input current P0 ₀ —P0 ₇ , P1 ₁ —P1 ₇ , P2 ₀ —P2 ₇ , P3 ₀ —P3 ₄ , P4 ₀ —P4 ₇ , RESET | $V_I = V_{SS}$ Pull-Up = 'On' | -200 | | -20 | μA |
| V_{RAM} | RAM hold voltage | When clock stopped | 2.0 | | | V |

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| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|----------------------|---|--------|------|------|------|
| | | | min. | typ. | max. | |
| I _{CC} | Power source current | high speed mode, f(X _{IN}) = 8MHz, V _{CC} = 5V, output transistors off, CAN module running, ADC running | | 11.0 | 18.0 | mA |
| | | high speed mode, f(X _{IN}) = 8MHz, V _{CC} = 5V, output transistors off, CAN module stopped, ADC running | | 9.0 | 16.0 | mA |
| | | middle speed mode, f(X _{IN}) = 8MHz, V _{CC} = 5V, output transistors off, CAN module running, ADC running | | 6.0 | 11.0 | mA |
| | | middle speed mode, wait mode, f(X _{IN}) = 8MHz, V _{CC} = 5V, output transis- tors off, CAN module stopped, ADC stopped | | 2.0 | | mA |
| | | stop mode, f(X _{IN}) = 0MHz, V _{CC} = 5V, T _a = 25°C | | 0.1 | 1.0 | μA |
| | | stop mode, f(X _{IN}) = 0MHz, V _{CC} = 5V, T _a = 85°C | | | 10.0 | μA |

Table 10: A-D converter characteristics

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = -40 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------------------|-------------------------|---|--------|------|-----------------|-----------------------------------|
| | | | min. | typ. | max. | |
| — | Resolution | | | | 8 | Bit |
| — | Absolute accuracy | | | ±1.0 | ±2.5 | LSB |
| t _{CONV} | Conversion time | high-speed mode | 106 | | 108 | t _C (X _{IN}) |
| | | middle-speed mode | 424 | | 432 | t _C (X _{IN}) |
| V _{REF} | Reference input voltage | | 2.0 | | V _{CC} | V |
| I _{REF} | Reference input current | V _{CC} = V _{REF} = 5.12 V | | 150 | 200 | μA |
| R _{LADDER} | Ladder resistor value | | | 35 | | kΩ |
| I _{IAN} | Analog input current | V _I = V _{SS} to V _{CC} | | 0.5 | 5.0 | μA |

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Table 11: Timing requirements

($V_{CC}=4.0$ to 5.5 V, $V_{SS}=AV_{SS}=0$ V, $T_a=-40$ to 85 °C unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--|--|-----------------------|------|------|---------------|
| | | min. | typ. | max. | |
| $t_W(\text{RESET})$ | Reset input "L" pulse width | 2 | | | μs |
| $t_C(X_{IN})$ | External clock input cycle time | 100 | | | ns |
| $t_{WH}(X_{IN})$ | External clock input "H" pulse width | 37 | | | ns |
| $t_{WL}(X_{IN})$ | External clock input "L" pulse width | 37 | | | ns |
| $t_C(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input cycle time (except bi-phase counter mode) | 1600 | | | ns |
| | CNTR ₀ input cycle time (bi-phase counter mode) | 2000 | | | ns |
| $t_{WH}(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input "H" pulse width (except bi-phase counter mode) | 800 | | | ns |
| | CNTR ₀ input "H" pulse width (bi-phase counter mode) | 1000 | | | ns |
| $t_{WL}(\text{CNTR})$ | CNTR ₀ , CNTR ₁ input "L" pulse width (except bi-phase counter mode) | 800 | | | ns |
| | CNTR ₀ input "L" pulse width (bi-phase counter mode) | 1000 | | | ns |
| $t_L(\text{CNTR}_0\text{-TX}_0)$ | Lag of CNTR ₀ and TX ₀ input edges (bi-phase counter mode) | 500 | | | ns |
| $t_C(\text{TX}_0)$ | TX ₀ input cycle time (bi-phase counter mode) | 3200 | | | ns |
| $t_{WH}(\text{TX}_0)$ | TX ₀ input "H" pulse width (bi-phase counter mode) | 1600 | | | ns |
| $t_{WL}(\text{TX}_0)$ | TX ₀ input "L" pulse width (bi-phase counter mode) | 1600 | | | ns |
| $t_{WH}(\text{INT})$ | INT ₀ , INT ₁ input "H" pulse width | 460 | | | ns |
| $t_{WL}(\text{INT})$ | INT ₀ , INT ₁ input "L" pulse width | 460 | | | ns |
| $t_C(\text{S}_{CLK})$ | Serial I/O clock input cycle time | $8 \cdot t_C(X_{IN})$ | | | ns |
| $t_{WH}(\text{S}_{CLK})$ | Serial I/O clock input "H" pulse width | $4 \cdot t_C(X_{IN})$ | | | ns |
| $t_{WL}(\text{S}_{CLK})$ | Serial I/O clock input "L" pulse width | $4 \cdot t_C(X_{IN})$ | | | ns |
| $t_{SU}(\text{S}_{IN}\text{-S}_{CLK})$ | Serial I/O input setup time | 200 | | | ns |
| $t_H(\text{S}_{CLK}\text{-S}_{IN})$ | Serial I/O input hold time | 150 | | | ns |

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Table 12: Switching characteristics

($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, $T_a = -40$ to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------------------|---|-------------------------------|------|------|------|
| | | min. | typ. | max. | |
| $t_{WH}(S_{CLK})$ | Serial I/O clock output "H" pulse width | $0.5 \cdot t_C(S_{CLK}) - 50$ | | | ns |
| $t_{WL}(S_{CLK})$ | Serial I/O clock output "L" pulse width | $0.5 \cdot t_C(S_{CLK}) - 50$ | | | ns |
| $t_D(S_{CLK}-S_{OUT})$ | Serial I/O output delay time | | | 50 | ns |
| $t_V(S_{CLK}-S_{OUT})$ | Serial I/O output valid time | 0 | | 50 | ns |
| $t_R(S_{CLK})$ | Serial I/O clock output rise time | | | 50 | ns |
| $t_R(CMOS)$ | CMOS output rise time | | 10 | 50 | ns |
| $t_F(CMOS)$ | CMOS output fall time | | 10 | 50 | ns |

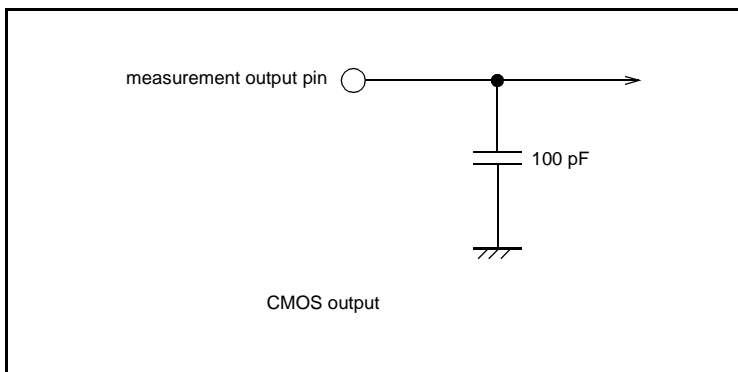


Fig. 49 Circuit for measuring output switching characteristics

TIMING DIAGRAM

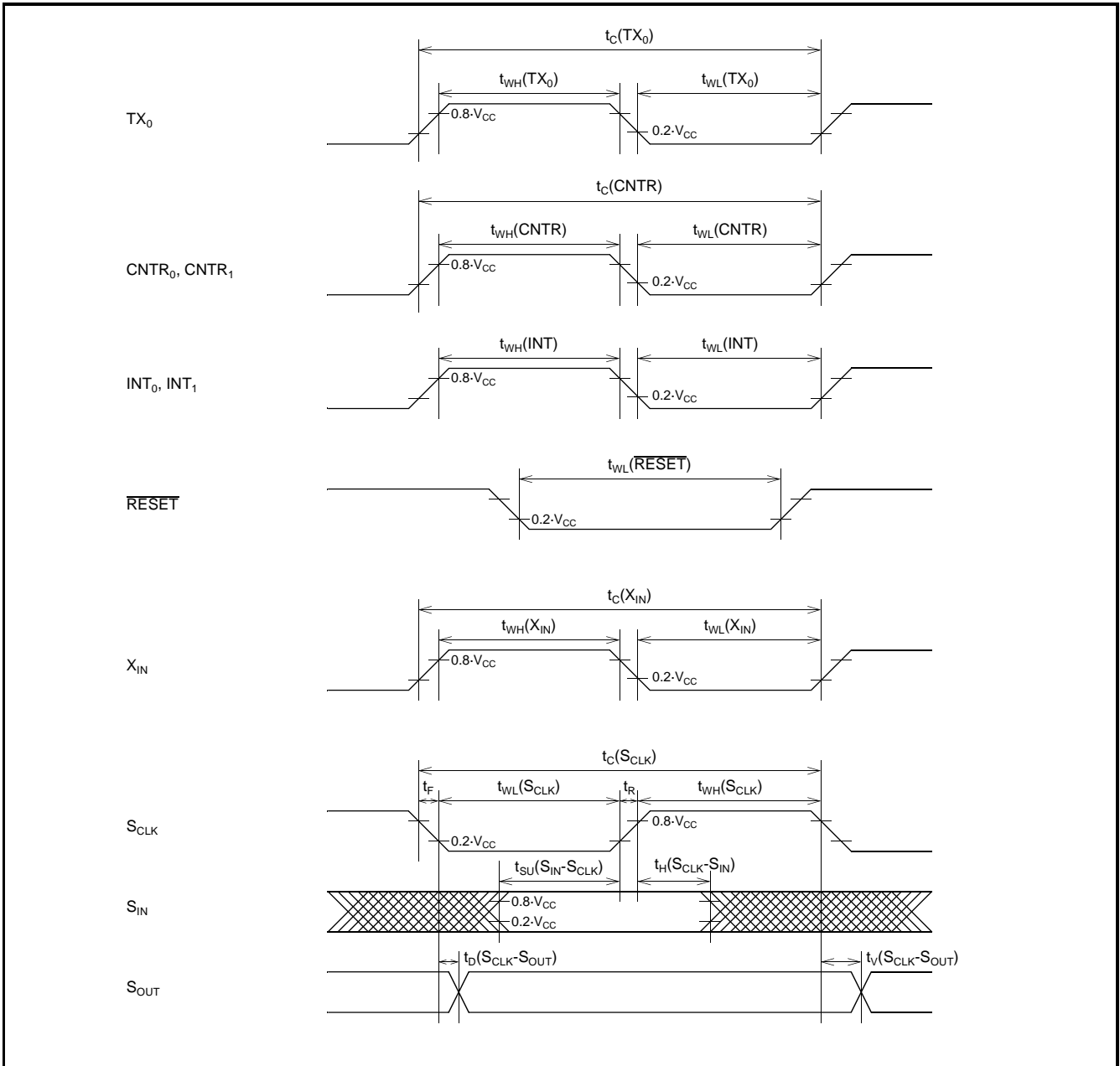


Fig. 50 Timing diagram

| REVISION | DATE | Page | | MODIFICATIONS |
|----------|----------|------|-----|--|
| | | New | Old | |
| 1.1 | 10. 98 | | | <p>“CAN controller” is replaced by “CAN module” in whole document.</p> <p>11 11 Schematics (8) and (11) are corrected.</p> <p>18 18 Replaced: “PUPD_j” with “PUP4_j”</p> <p>26 26 Replaced: “UT_XD” with “SOUT” Replaced: “UR_XD” with “SIN”</p> <p>38 38 Replaced: “FFFB_H” with “FFFB₁₆” Replaced: “FFFA_H” with “FFFA₁₆”</p> <p>41 Replaced: “44P6N” with “44P6N-A)</p> |
| (1.2) | 13.01.99 | 43 | 43 | Values changed:Iih(35, 113) to (20, 200) and Iil(-122, -70) to (-200, -20); typical values are removed. |
| | | 10 | 10 | Schematic (1) is modified. |
| | | 35 | 35 | Fig. 39 is modified. |