38C8 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38C8 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C8 group has a LCD drive control circuit (bias control, time sharing control), a 10-bit A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 38C8 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

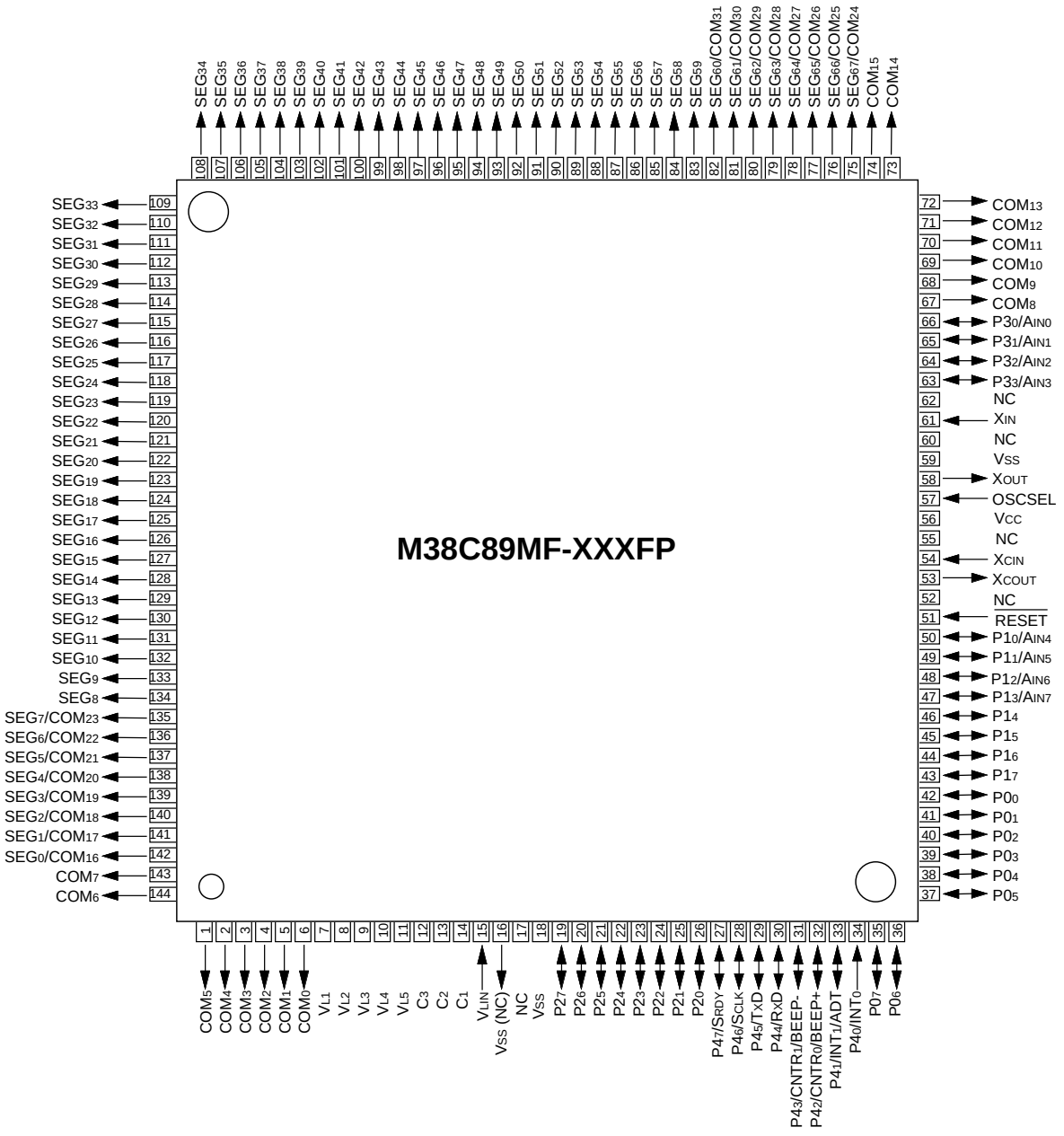
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.5 µs
  (at 8 MHz oscillation frequency)
- Memory size
  - ROM ..... 60 K bytes
  - RAM ..... 2048 bytes
- Programmable input/output ports 35
- Software pull-up resistors
  ..... Ports P0–P3, $P4_1$–$P4_7$
- Interrupts ..... 15 sources, 15 vectors
  (includes key input interrupt)
- Timers ..... 8-bit × 3, 16-bit × 2
- Serial I/O ..... 8-bit × 1 (UART or Clock-synchronized)
- A-D converter (32 kHz operating available) ... 10-bit × 8 channels
- LCD drive control circuit
  - Bias 1/5, 1/7
  - Duty 1/16, 1/32
  - Common output ..... 16 or 32
  - Segment output ..... 52 or 68
- Main clock generating circuit (RC oscillation selectable)
  ..... (connect to external ceramic resonator or resistor)
- Sub-clock generating circuit
  ..... (connect to quartz-crystal oscilaltor)
- Power source voltage
  - In high-speed mode ..... 4.0 to 5.5 V
  - In middle-speed mode ..... 2.2 to 5.5 V
  - In low-speed mode ..... 2.2 to 5.5 V
- Power dissipation
  - In high-speed mode ..... 30 mW
    (at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 60 µW
    (at 32 kHz oscillation frequency, at 3 V power source voltage, at WIT state, at voltage multiplier operating, LCD drive waveform generating state)
- Operating temperature range ..... – 20 to 85°C

APPLICATIONS

Dot-matrix-type displays

PIN CONFIGURATION (TOP VIEW)



Package type : 144P6Q-A

Fig. 1 M38C89MF-XXXFP pin configuration

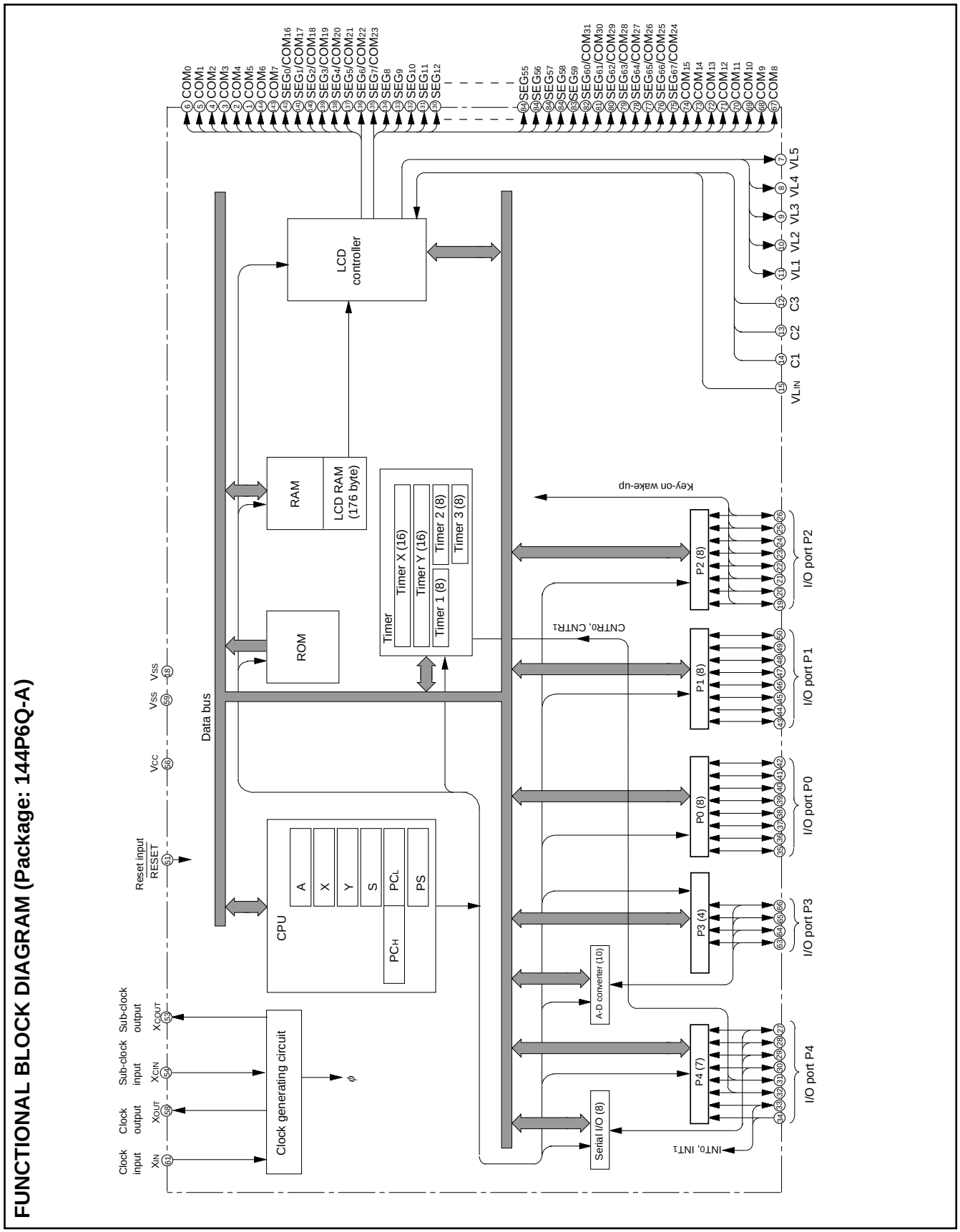


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 4.0–5.5 V to V_{CC}, and 0 V to V_{SS}. (at high-speed mode)	
$\overline{RESET}$	Reset input	• Reset input pin for active "L."	
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. • Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
OSCSEL	RC oscillation select	• This pin determines the oscillation between X_{IN} and X_{OUT}. The oscillation method can be selected from either by an oscillator or by a resistor.	
X_{CIN}	Sub-clock input	• Input and output pins for sub-clock generating circuit. (Connect a quartz-crystal oscillator between the X_{CIN} and X_{COUT} pins to set the oscillation frequency. The clock generated the externals cannot be input directly.)	
X_{COUT}	Sub-clock output		
V_{LIN}	Power source input for LCD	• Reference voltage input pin for LCD. • The input voltage to this pin is boosted threefold by voltage multiplier.	
V_{L1} – V_{L5}	LCD power source	• LCD drive power source pins.	
COM_0 – COM_{32}	Common output	• LCD common output pins.	
SEG_0/COM_{16}– SEG_7/COM_{23}, $SEG_{60}COM_{31}$– SEG_{67}/COM_{24}	Segment output/ Common output	• LCD segment/common output pins.	
SEG_8–SEG_{59}	Segment output	• LCD segment output pins.	
$P0_0$–$P0_7$	I/O port P0	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure.	
$P1_4$–$P1_7$	I/O port P1		
$P1_0/AIN_4$– $P1_3/AIN_7$			• A-D converter analog input pin
$P2_0$–$P2_7$	I/O port P2		• Key-on wake-up interrupt input pin
$P3_0/AIN_0$ – $P3_3/AIN_3$	I/O port P3	• 4-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure.	• A-D converter analog input pin
$P4_0/INT_0$	Input port P4	• 1-bit input port. • CMOS compatible input level.	• External interrupt pin
$P4_1/INT_1$/ADT	I/O port P4	• 7-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure. • I/O direction register allows each pin to be individually programmed as either input or output.	• External interrupt pin • A-D trigger input pin
$P4_2/CNTR_0$/ BEEP+, $P4_3/CNTR_1$/ BEEP-			•Timer function I/O pin
$P4_4/R_xD$, $P4_5/T_xD$, $P4_6/S_{CLK}$, $P4_7/S_{RDY}$			• Serial I/O I/O pin
C_1, C_2, C_3	Voltage multiplier	• External capacitor connect pins for a voltage multiplier of LCD.	
V_{SS} (NC), NC		• Non-function pins. • Leave the V_{SS} (NC) pin open.	

PART NUMBERING

Product M38C8 9 M F –XXX FP

Package type
FP: 144P6Q-A package

ROM number
Omitted in One Time PROM version.

ROM/PROM size

1: 4096 bytes	9: 36864 bytes
2: 8192 bytes	A: 40960 bytes
3: 12288 bytes	B: 45056 bytes
4: 16384 bytes	C: 49152 bytes
5: 20480 bytes	D: 53248 bytes
6: 24576 bytes	E: 57344 bytes
7: 28672 bytes	F: 61440 bytes
8: 32768 bytes	

The first 128 bytes and the last 2 bytes of ROM are reserved areas; they cannot be used.

Memory type
M: Mask ROM version
E: One Time PROM version

RAM size
0: 192 bytes
1: 256 bytes
2: 384 bytes
3: 512 bytes
4: 640 bytes
5: 768 bytes
6: 896 bytes
7: 1024 bytes
8: 1536 bytes
9: 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 38C8 group as follows.

Memory Type

Support for mask ROM and One Time PROM versions

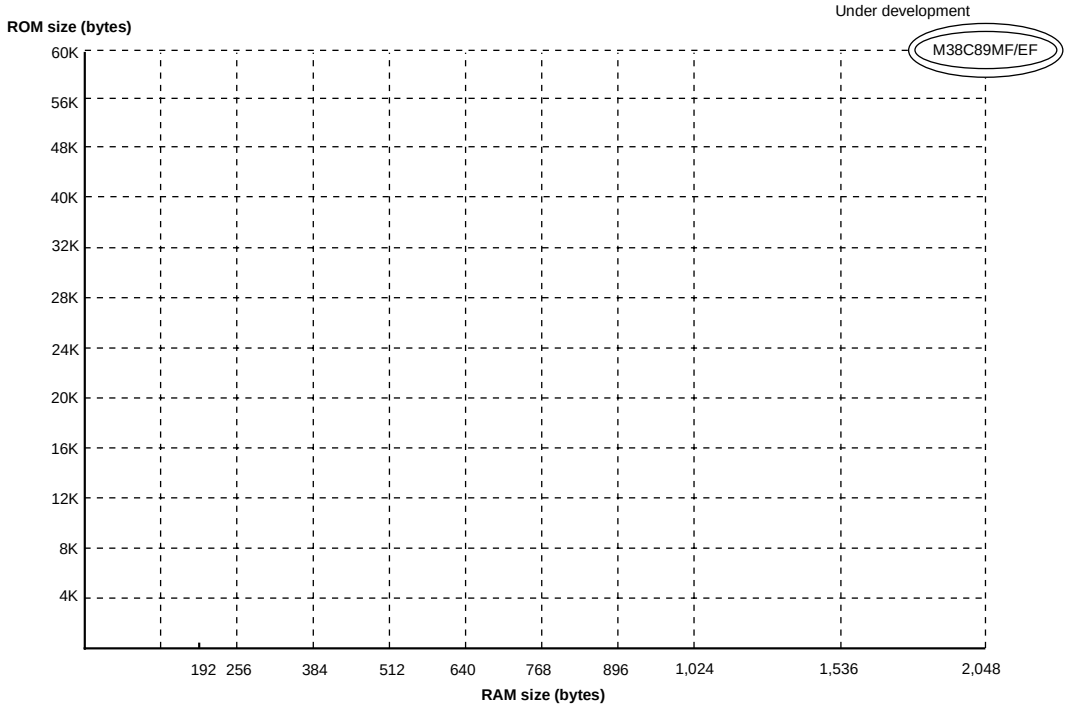
Memory Size

ROM/PROM size ..... 60 K bytes
RAM size ..... 2048 bytes

Packages

144P6Q-A ..... 0.5 mm-pitch plastic molded QFP

Memory Expansion Plan



Products under development or planning: the development schedule and specification may be revised without notice. The development of planning products may be stopped.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 2 Support products

As of Dec. 2000

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38C89MF-XXXFP	61440 (61310)	2048	144P6Q-A	Mask ROM version
M38C89EFFP	61440 (61310)	2048	144P6Q-A	One Time PROM version

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 38C8 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

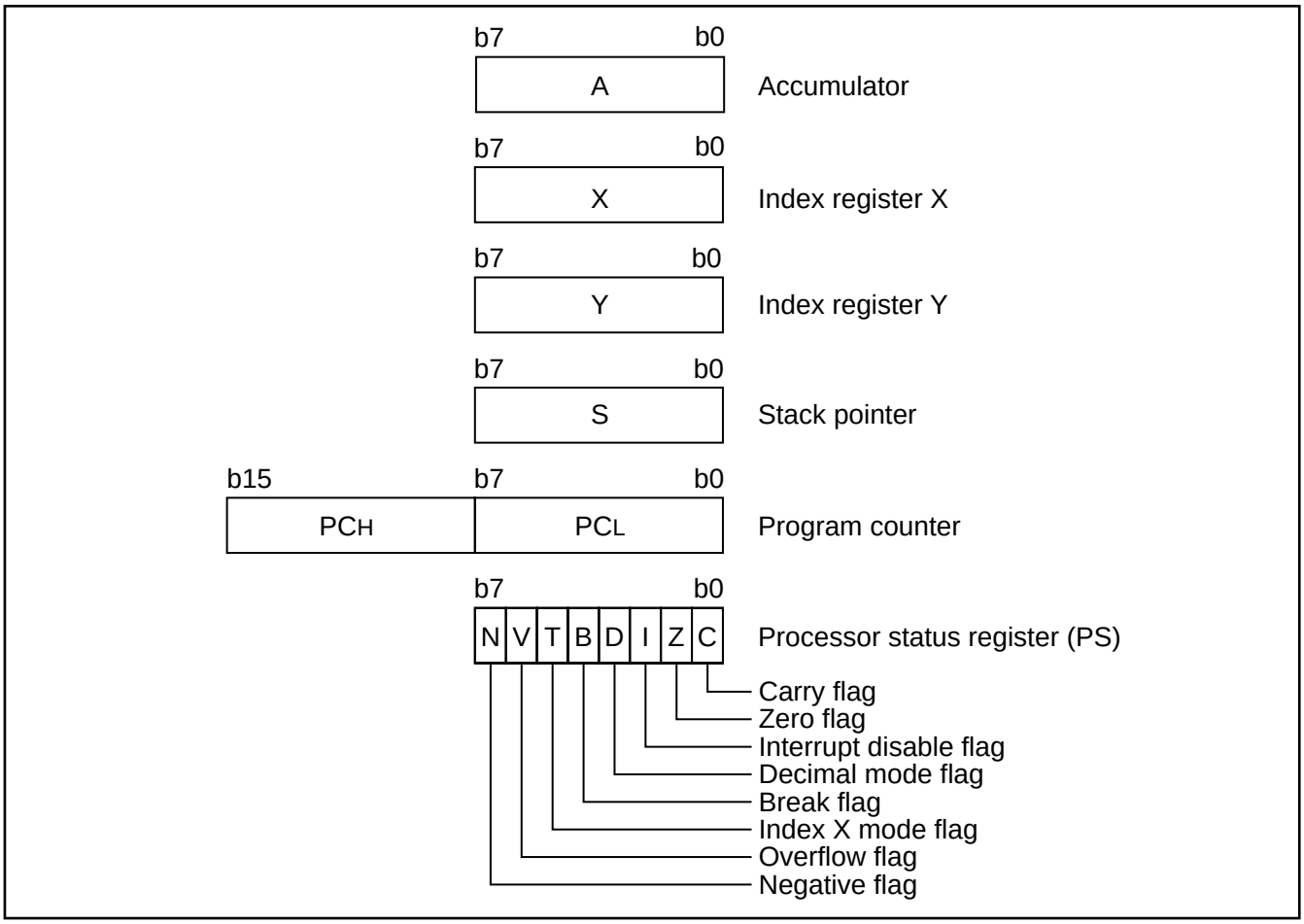


Fig. 5 740 Family CPU register structure

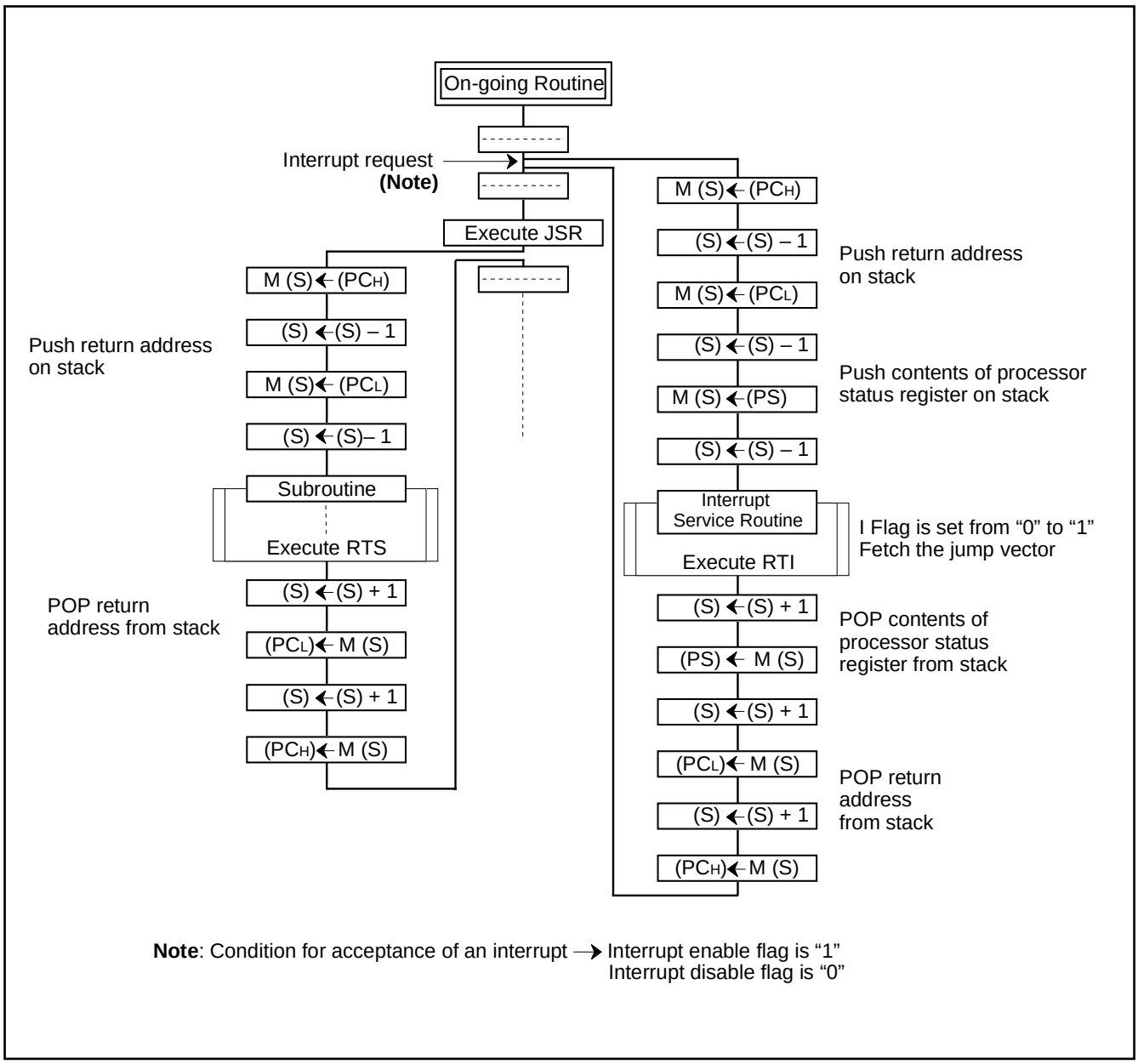


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.
The CPU mode register is allocated at address 003B16.

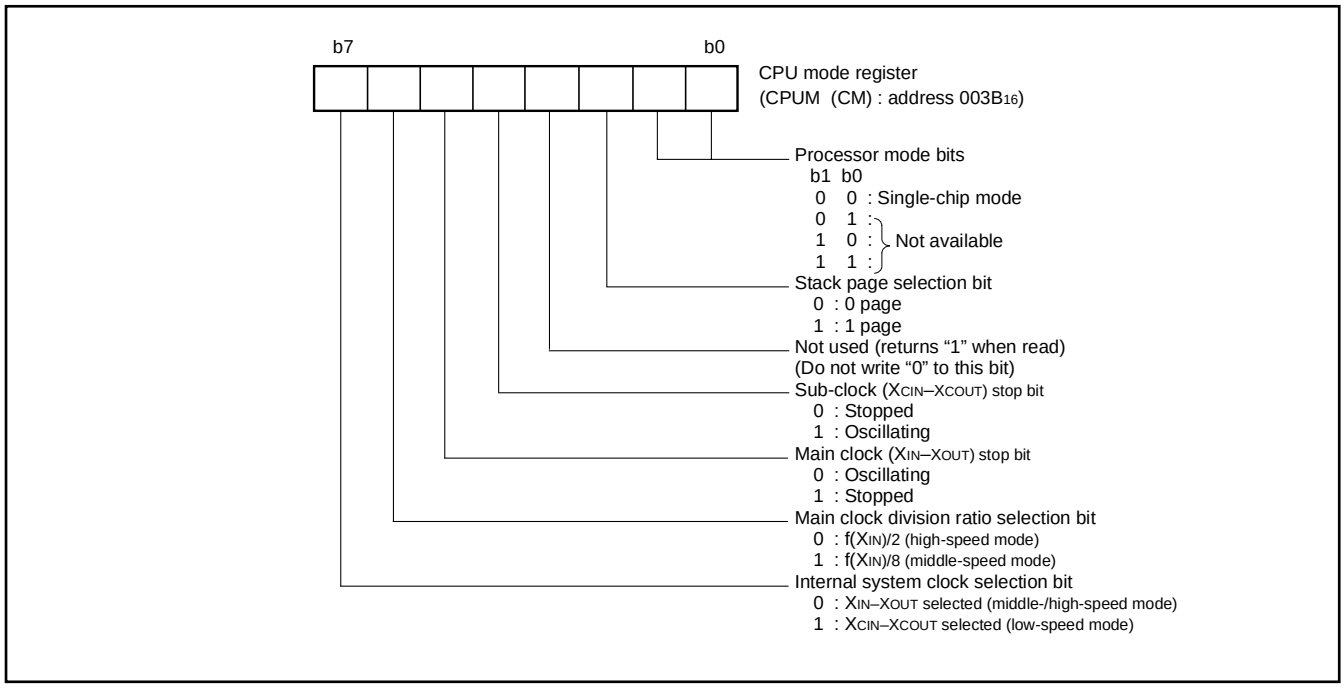


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

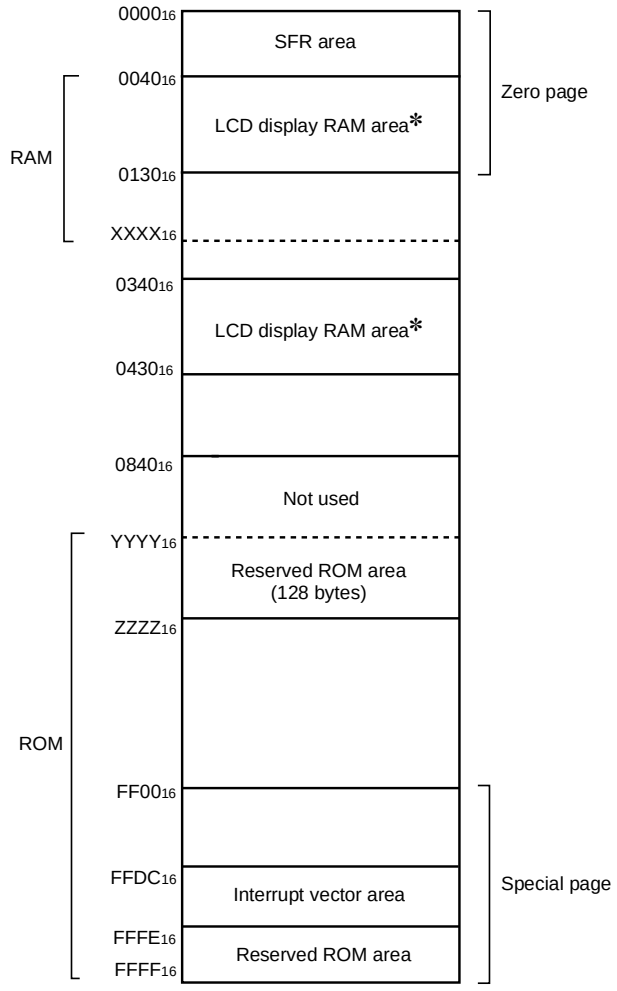
Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}



* The stard address of the LCD display area can be switched either zero page (addresses 0040_{16}–$00EF_{16}$) or 3 page (addresses 0340_{16}–$03EF_{16}$) by software. Immediately after reset released, 3 page is selected.

Fig. 8 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	
$000B_{16}$	
$000C_{16}$	
$000D_{16}$	
$000E_{16}$	
$000F_{16}$	
0010_{16}	
0011_{16}	
0012_{16}	
0013_{16}	
0014_{16}	
0015_{16}	
0016_{16}	PULL register A (PULLA)
0017_{16}	PULL register B (PULLB)
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	
$001E_{16}$	
$001F_{16}$	

0020_{16}	Timer X (low-order) (TXL)
0021_{16}	Timer X (high-order) (TXH)
0022_{16}	Timer Y (low-order) (TYL)
0023_{16}	Timer Y (high-order) (TYH)
0024_{16}	Timer 1 (T1)
0025_{16}	Timer 2 (T2)
0026_{16}	Timer 3 (T3)
0027_{16}	Timer X mode register (TXM)
0028_{16}	Timer Y mode register (TYM)
0029_{16}	Timer 123 mode register (T123M)
$002A_{16}$	
$002B_{16}$	
$002C_{16}$	
$002D_{16}$	
$002E_{16}$	
$002F_{16}$	
0030_{16}	
0031_{16}	A-D control register (ADCON)
0032_{16}	A-D conversion register (low-order) (ADL)
0033_{16}	A-D conversion register (high-order) (ADH)
0034_{16}	
0035_{16}	
0036_{16}	
0037_{16}	LCD control register 1 (LC1)
0038_{16}	LCD control register 2 (LC2)
0039_{16}	LCD mode register (LM)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

Fig. 9 Memory map of special function register (SFR)

I/O PORTS
[Direction Registers]

The I/O ports P0–P3 and P41–P47 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

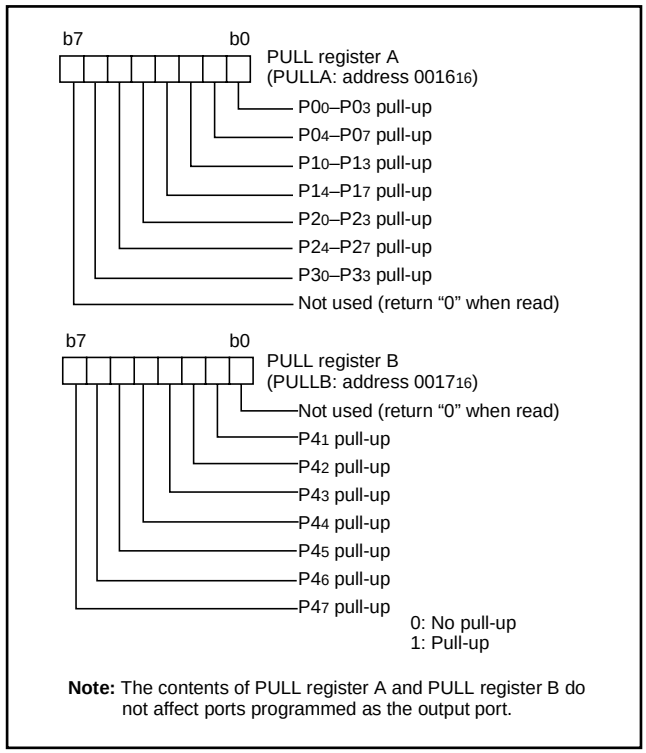
When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pull-up Control

By setting the PULL register A (address 0016_{16}) or the PULL register B (address 0017_{16}), ports P0 to P4 except for port $P4_0$ can control pull-up with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.



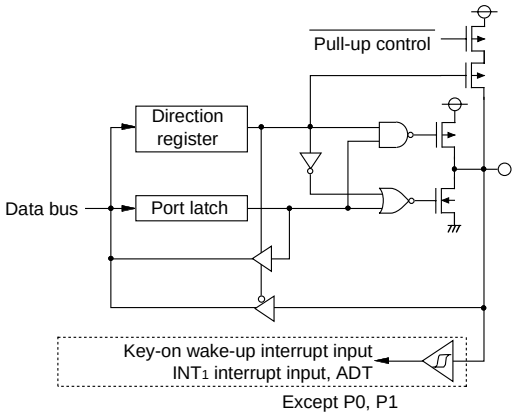
Note: The contents of PULL register A and PULL register B do not affect ports programmed as the output port.

Fig. 10 Structure of PULL register A and PULL register B

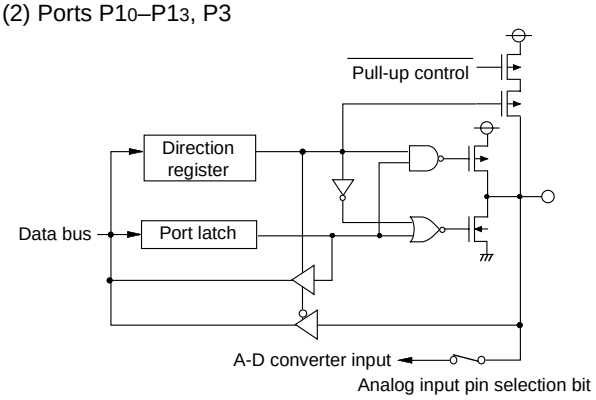
Table 5 List of I/O port function

Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Ref. No.
P0$_0$–P0$_7$	Port P0	Input/Output, individual bits	CMOS 3-state output		PULL register A	(1)
P1$_0$/AN$_4$–P1$_3$/AN$_7$	Port P1				PULL register A A-D control register	(2)
P1$_4$–P1$_7$					PULL register A	(1)
P2$_0$–P2$_7$	Port P2	Input/Output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register 2	(1)
P3$_0$/AN$_0$–P3$_3$/AN$_3$	Port P3	Input/Output, individual bits	CMOS 3-state output	A-D converter input	PULL register A A-D control register	(2)
P4$_0$/INT$_0$	Port P4	Input	CMOS compatible input level	External interrupt input	PULL register B Interrupt edge select register	(3)
P4$_1$/INT$_1$		Input/Output, individual bits	CMOS compatible input level CMOS 3-state output			(1)
P4$_2$/CNTR$_0$/BEEP+				Timer X function I/O	PULL register B Timer X mode register	(4)
P4$_3$/CNTR$_1$/BEEP-				Timer Y function input	PULL register B Timer Y mode register	(5)
P4$_4$/RxD				Serial I/O funtion	PULL register B	(6)
P4$_5$/TxD				I/O	Serial I/O control register	(7)
P4$_6$/S$_{CLK}$					Serial I/O status register	(8)
P4$_7$/$\overline{S_{RDY}}$					UART control register	(9)
COM$_0$–COM$_7$, COM$_8$–COM$_{15}$	Common	Output	LCD common output		LCD mode register	
SEG$_0$/COM$_{16}$–SEG$_7$/COM$_{23}$, SEG$_{60}$/COM$_{31}$–SEG$_{67}$/COM$_{24}$	Segment/ Common		LCD segment output LCD common ouput			
SEG$_8$–SEG$_{59}$	Segment		LCD segment output			

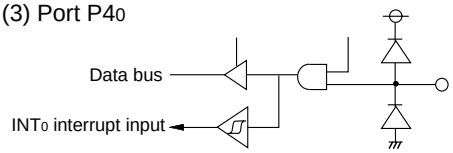
(1) Ports P0, P14–P17, P2, P41



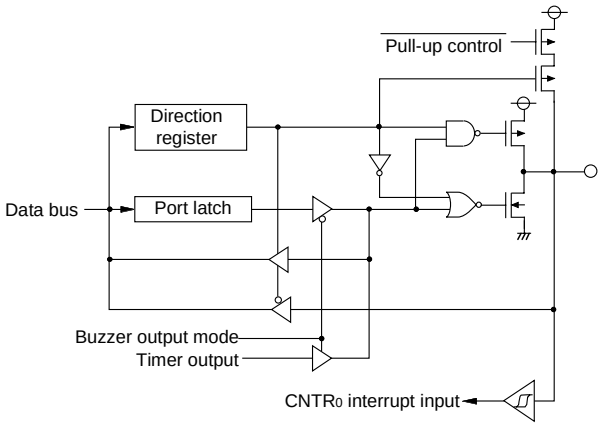
(2) Ports P10–P13, P3



(3) Port P40



(4) Port P42



(5) Port P43

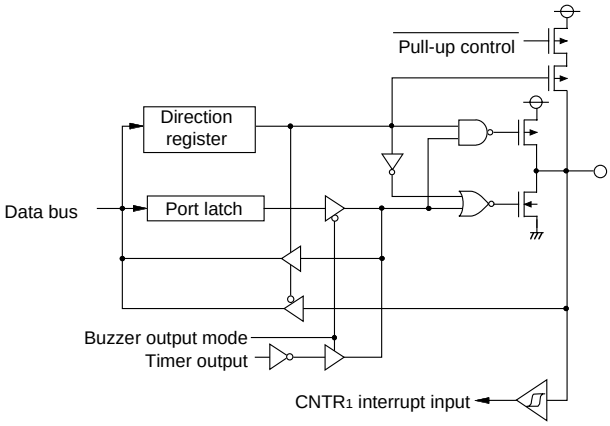
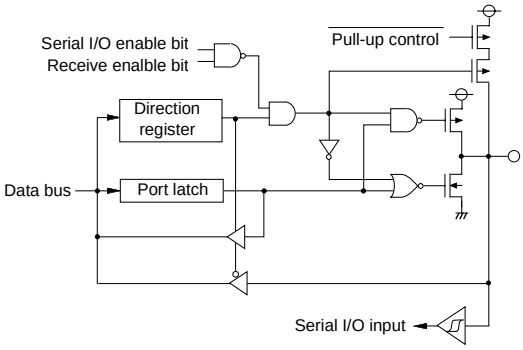
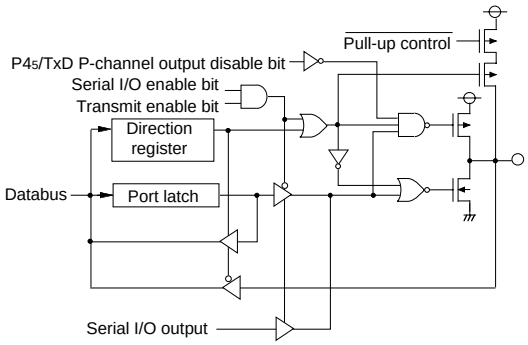


Fig. 11 Port block diagram (1)

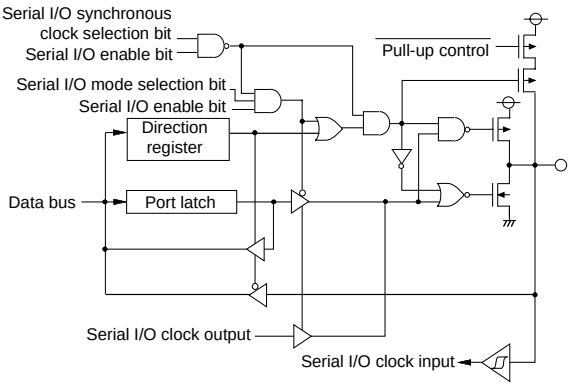
(6) Port P44



(7) Port P45



(8) Port P46



(9) Port P47

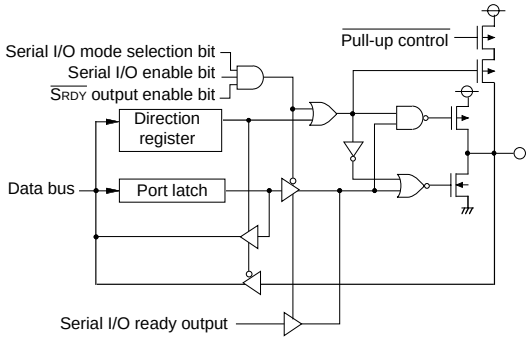


Fig. 12 Port block diagram (2)

INTERRUPTS

Interrupts occur by fifteen sources: six external, eight internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to “1”.

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $3A_{16}$)
Timer X mode register (address 27_{16})
Timer Y mode register (address 28_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: AD control regsiter (address 31_{16})

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to “0” (disabled).
②Set the interrupt edge select bit (active edge switch bit) or the interrupt source select bit to “1”.
③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to “1” (enabled).

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 intput	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O reception	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O transmission shift or when transmission buffer is empty	Valid when serial I/O is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer 1	12	$FFE7_{16}$	$FFE6_{16}$	At timer 1 underflow	
Key input (Key-on wake-up)	13	$FFE1_{16}$	$FFE0_{16}$	At falling of port P2 (at input) input logical level AND	External interrupt (falling valid)
A-D conversion	14	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	Valid when A-D conversion interrupt is selected
BRK instruction	15	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

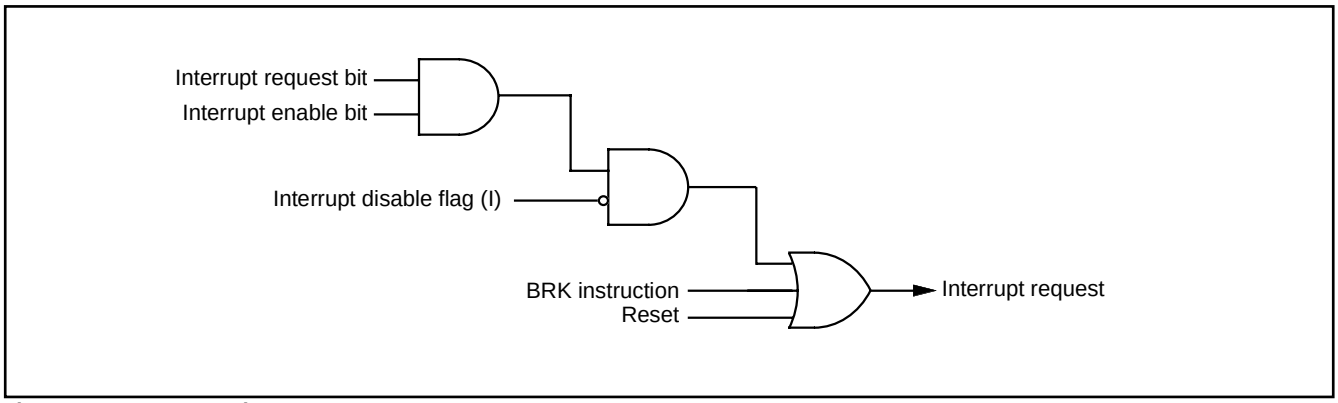


Fig. 13 Interrupt control

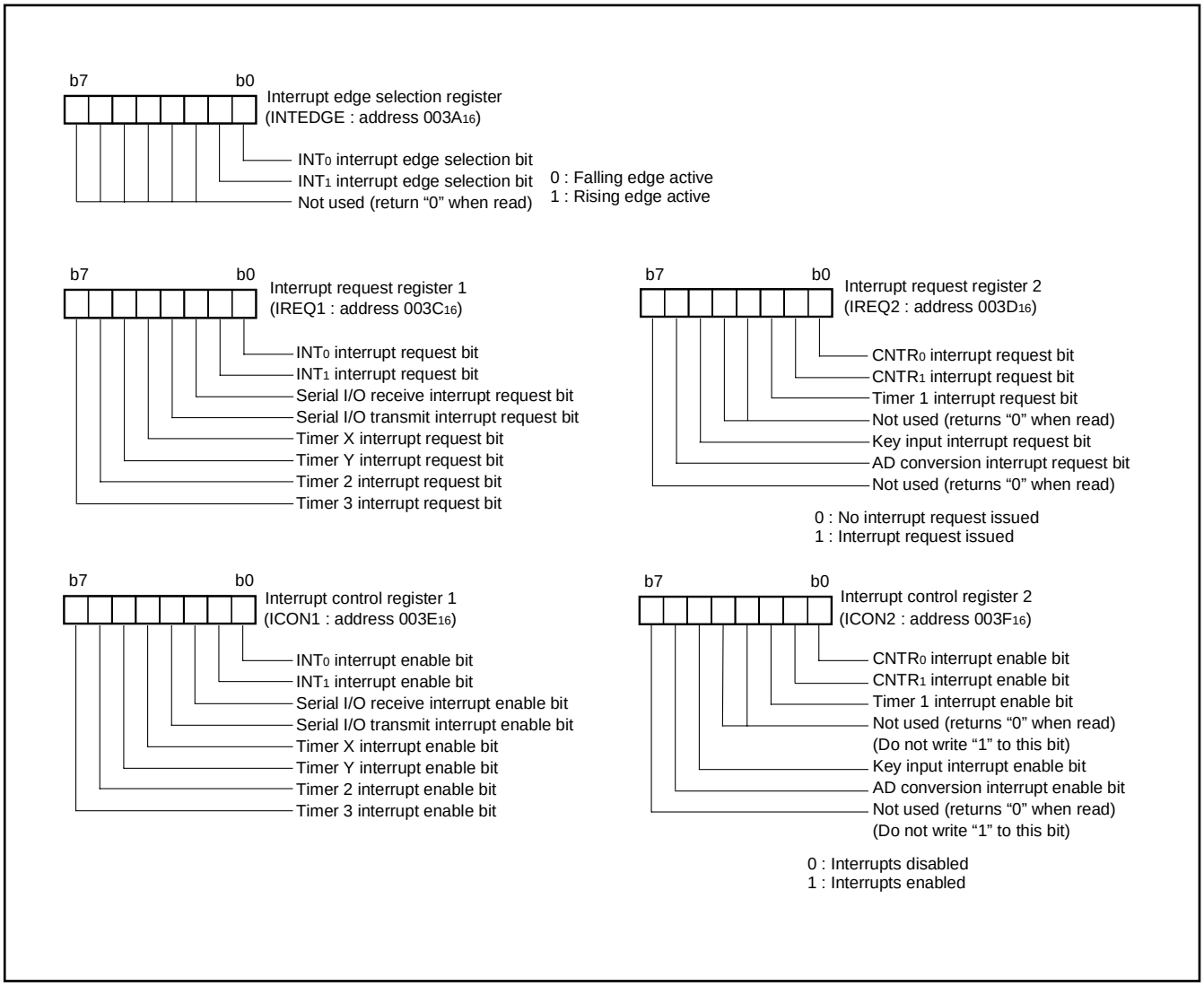


Fig. 14 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake-Up)

A key input interrupt request is generated by applying "L" level to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 15, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports $P2_0$–$P2_3$.

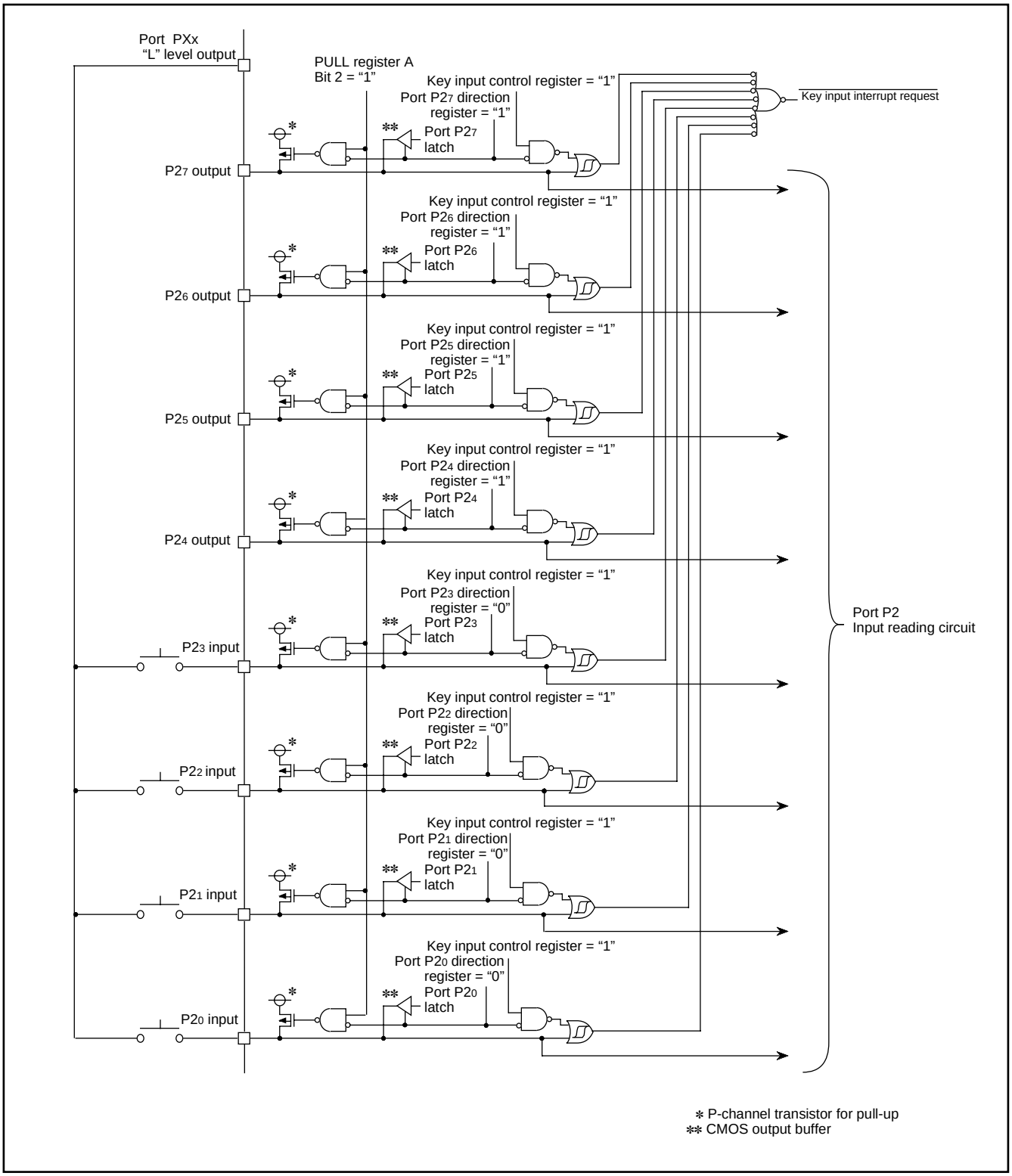


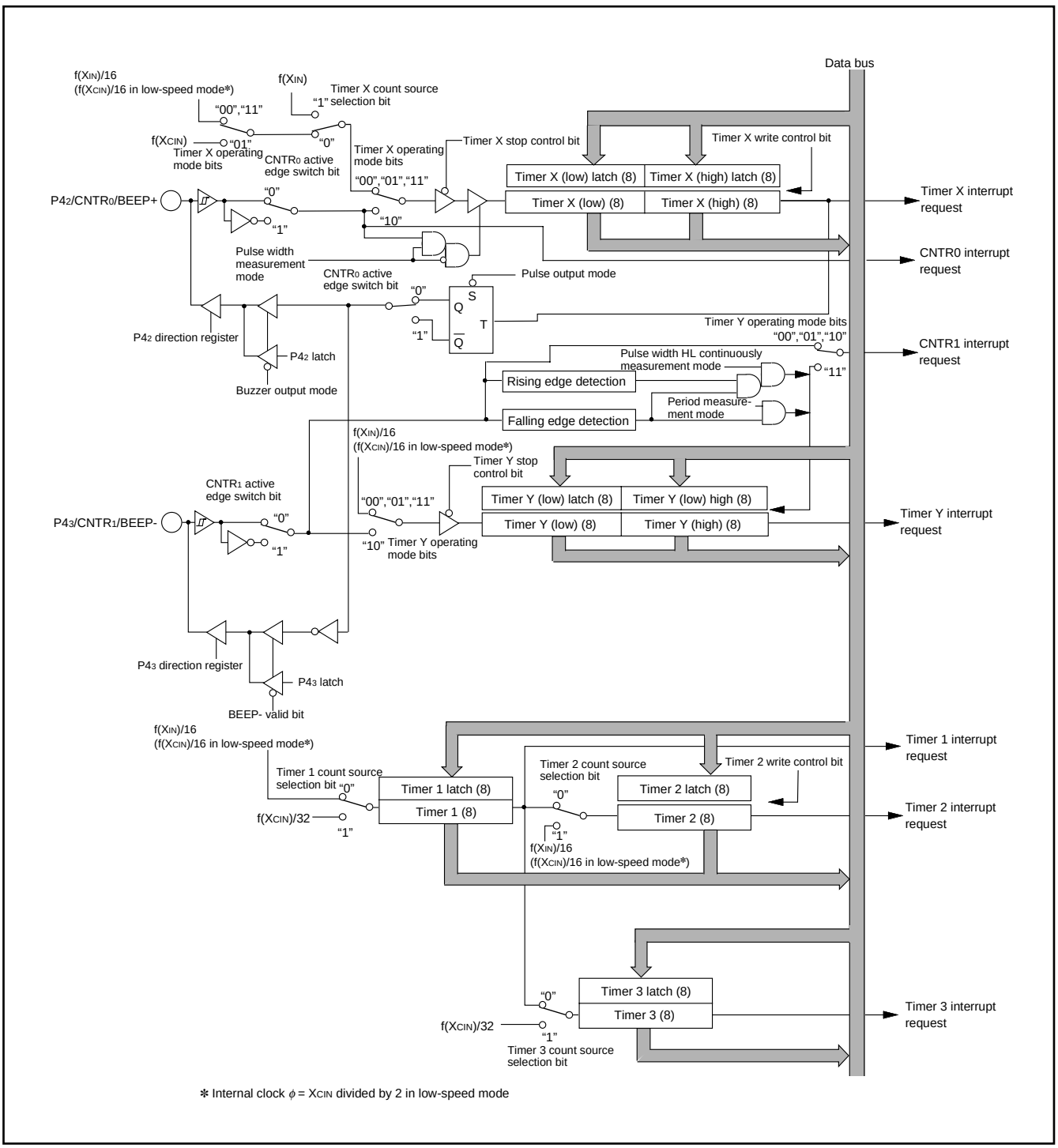
Fig. 15 Connection example when using key input interrupt and port P2 block diagram

TIMERS

The 38C8 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.



✻ Internal clock ϕ = X_{CIN} divided by 2 in low-speed mode

Fig. 16 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write by setting the timer X mode register.

(1) Timer Mode

When the timer X count source selection bit is "0", the timer counts f(XIN)/16 (or f(XCIN)/16 in low-speed mode). When it is "1", the timer counts f(XIN).

(2) Buzzer Output Mode

Each time the timer underflows, a signal output from the BEEP+ pin is inverted. When the BEEP- valid bit is "1", the opposite phase of BEEP+ signal is output from the BEEP- pin. When using the BEEP+ pin and the BEEP- pin, set ports shared with these pins to output.

(3) Event Counter Mode

The timer counts signals input through the CNTR0 pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the CNTR0 pin to input.

(4) Pulse Width Measurement Mode

When the timer X count source selection bit is "0", the count source is f(XIN)/16 (or f(XCIN)/16 in low-speed mode). When it is "1", the count source is f(XIN).
If CNTR0 active edge switch bit is "0", the timer counts while the input signal of CNTR0 pin is at "H". If it is "1", the timer counts while the input signal of CNTR0 pin is at "L". When using a timer in this mode, set the port shared with the CNTR0 pin to input.

●Timer X write control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

■Notes on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

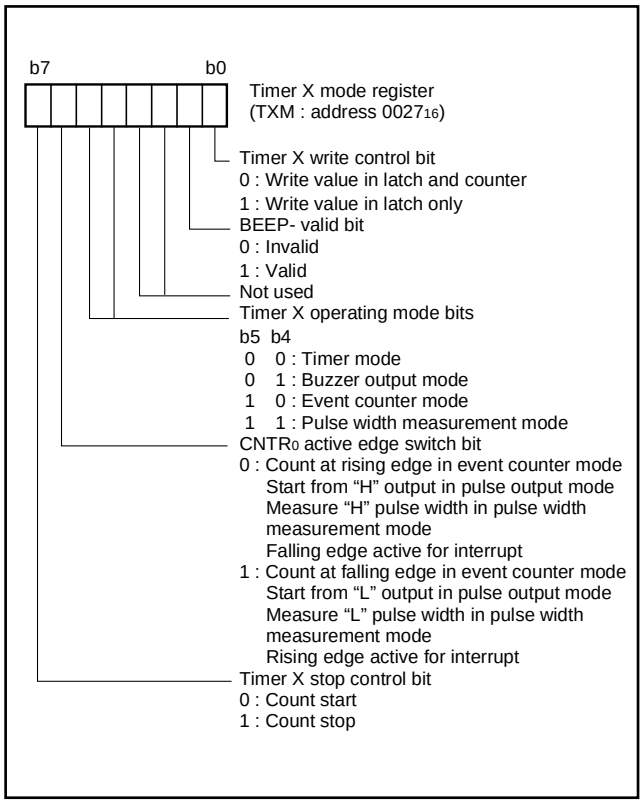


Fig. 17 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer Mode

The timer counts f(XIN)/16 (or f(XCIN)/16 in low-speed mode).

(2) Period Measurement Mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the port shared with the CNTR1 pin to input.

(3) Event Counter Mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the CNTR1 pin to input.

(4) Pulse Width HL Continuously Measurement Mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the port shared with the CNTR1 pin to input.

■Notes on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in the pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

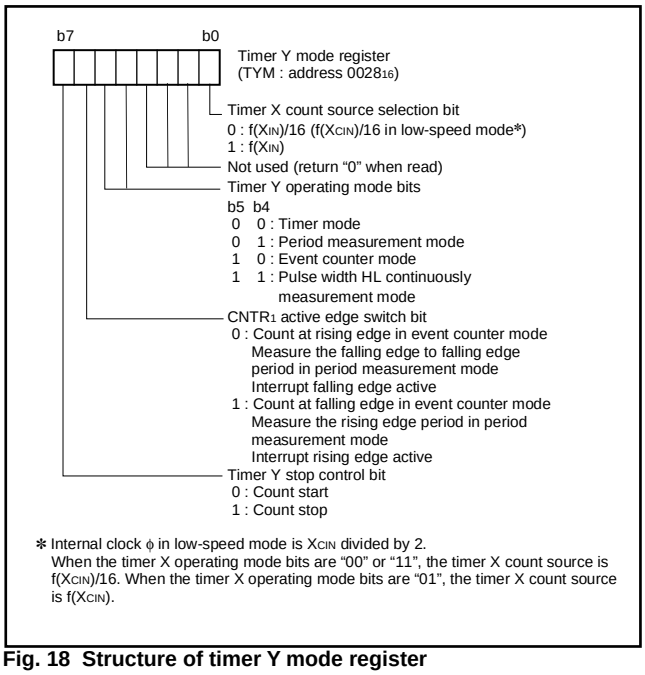


Fig. 18 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by the timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

●Timer 2 write control

If the timer 2 write control bit is “0”, when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is “1”, when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

■Notes on timer 1 to timer 3

When the count source of timer 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

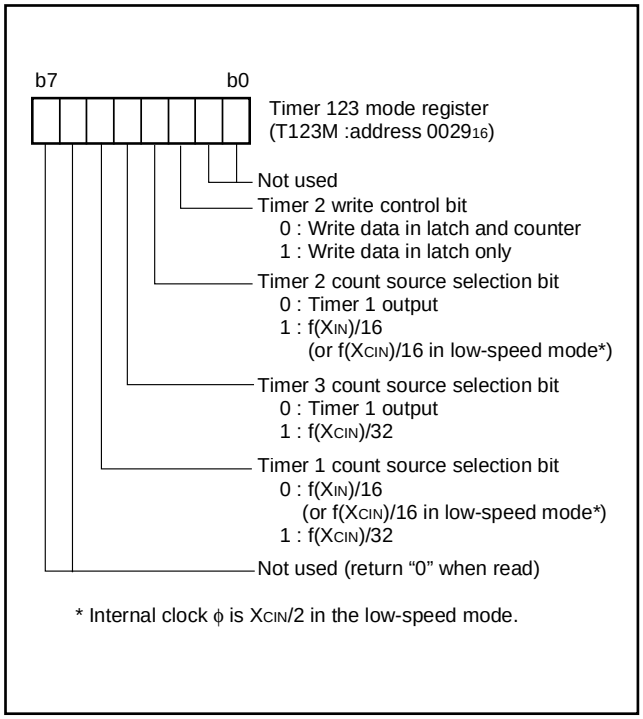


Fig. 19 Structure of timer 123 mode register

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O can be selected by setting the mode selection bit of the serial I/O control register to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer registers.

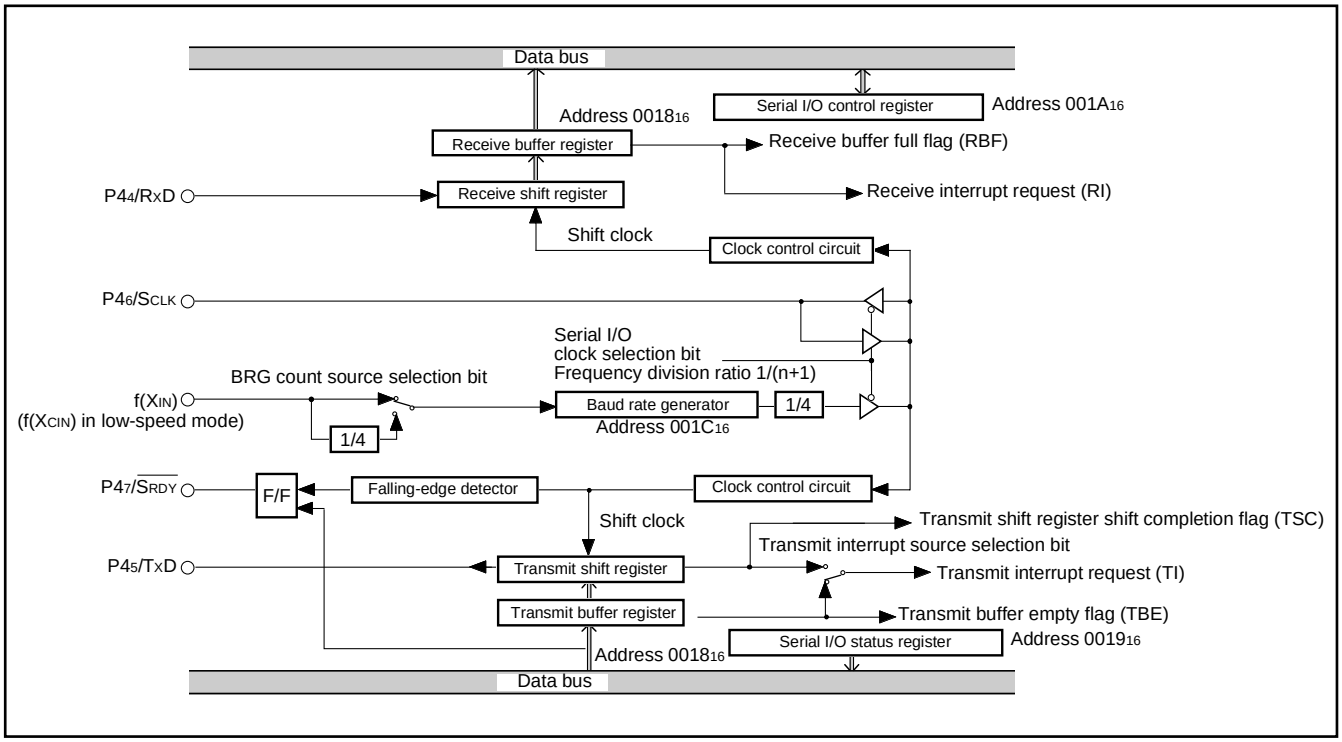
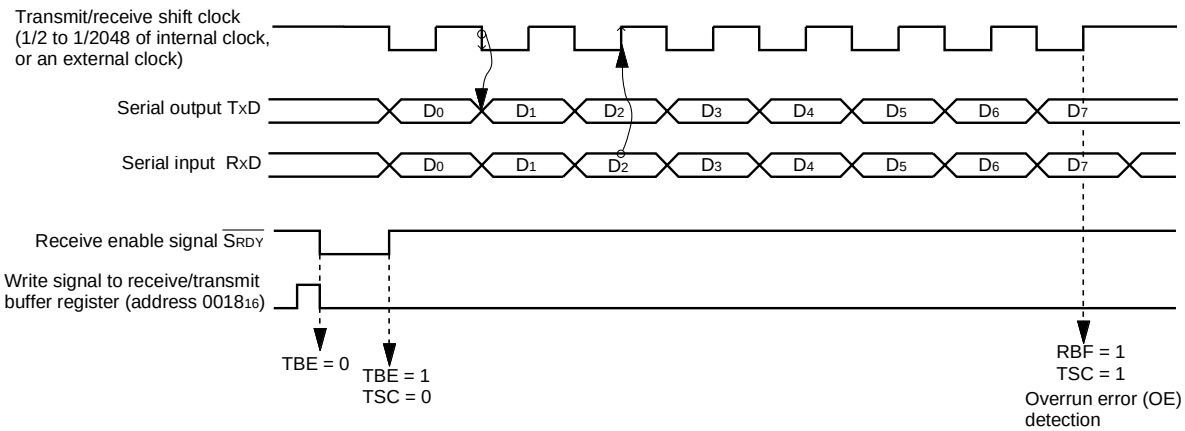


Fig. 20 Block diagram of clock synchronous serial I/O



Notes 1: The transmit interrupt (TI) can be selected to occur either when the transmit buffer register has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 21 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

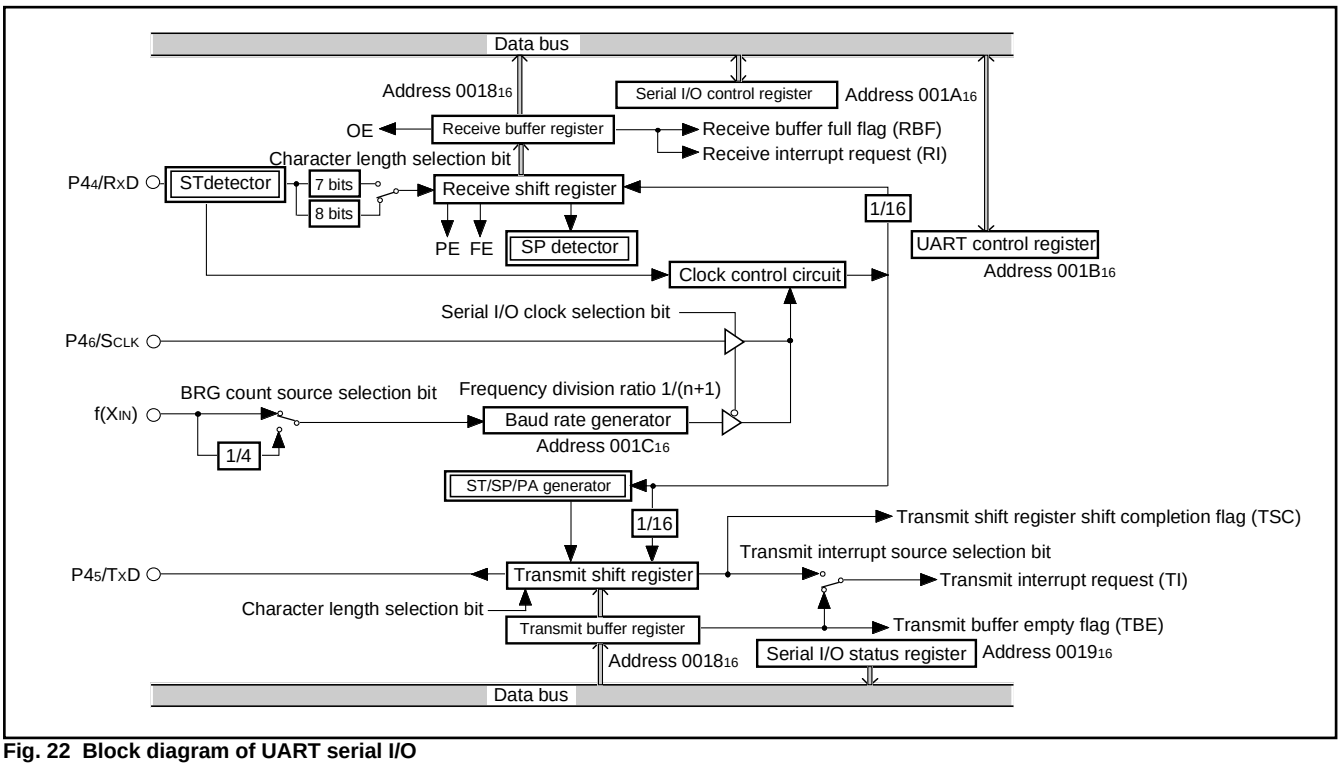
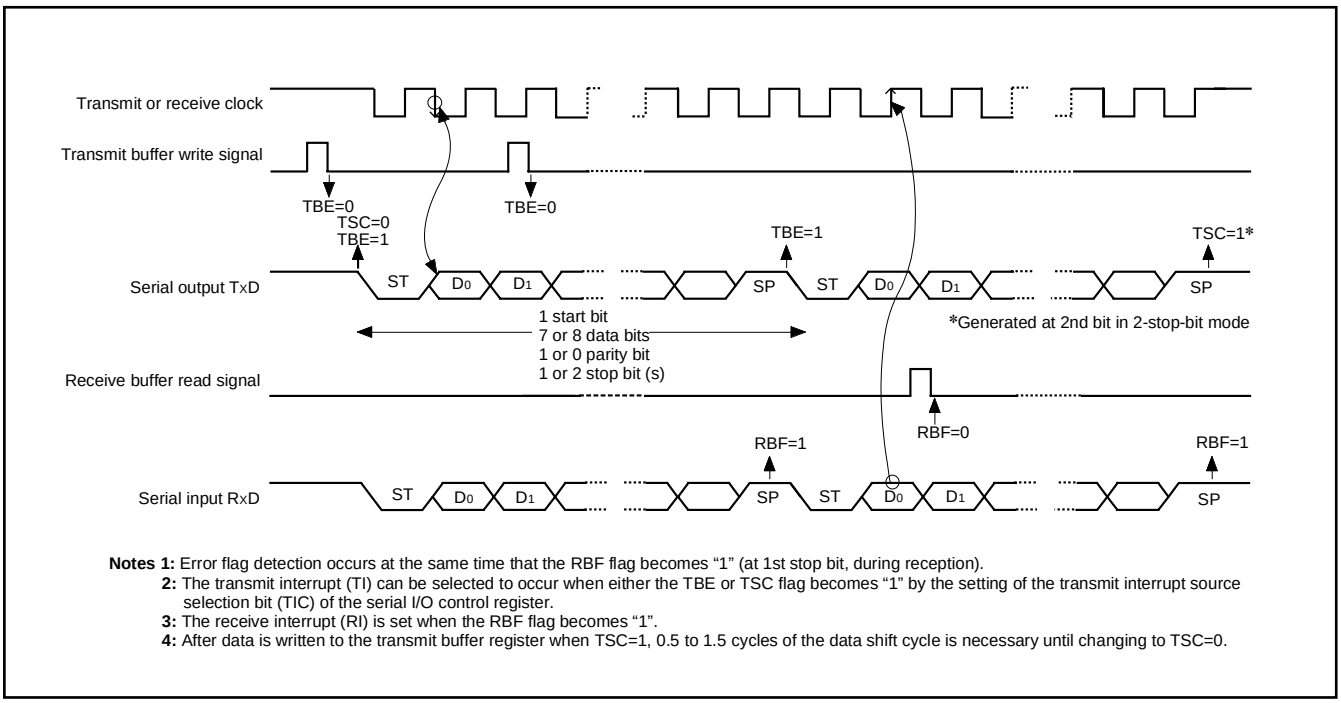


Fig. 22 Block diagram of UART serial I/O



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1" by the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 23 Operation of UART serial I/O function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing “0” to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register contains eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)]001B$_{16}$

This is a 5 bit register containing four control bits, which are valid when UART is selected and set the data format of an data receiver/transfer, and one control bit, which is always valid and sets the output structure of the P4$_5$/TxD pin.

[Baud Rate Generator(BRG)] 0016$_{16}$

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.

①Set the serial I/O transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O transmit interrupt enable bit to “1” (enabled).

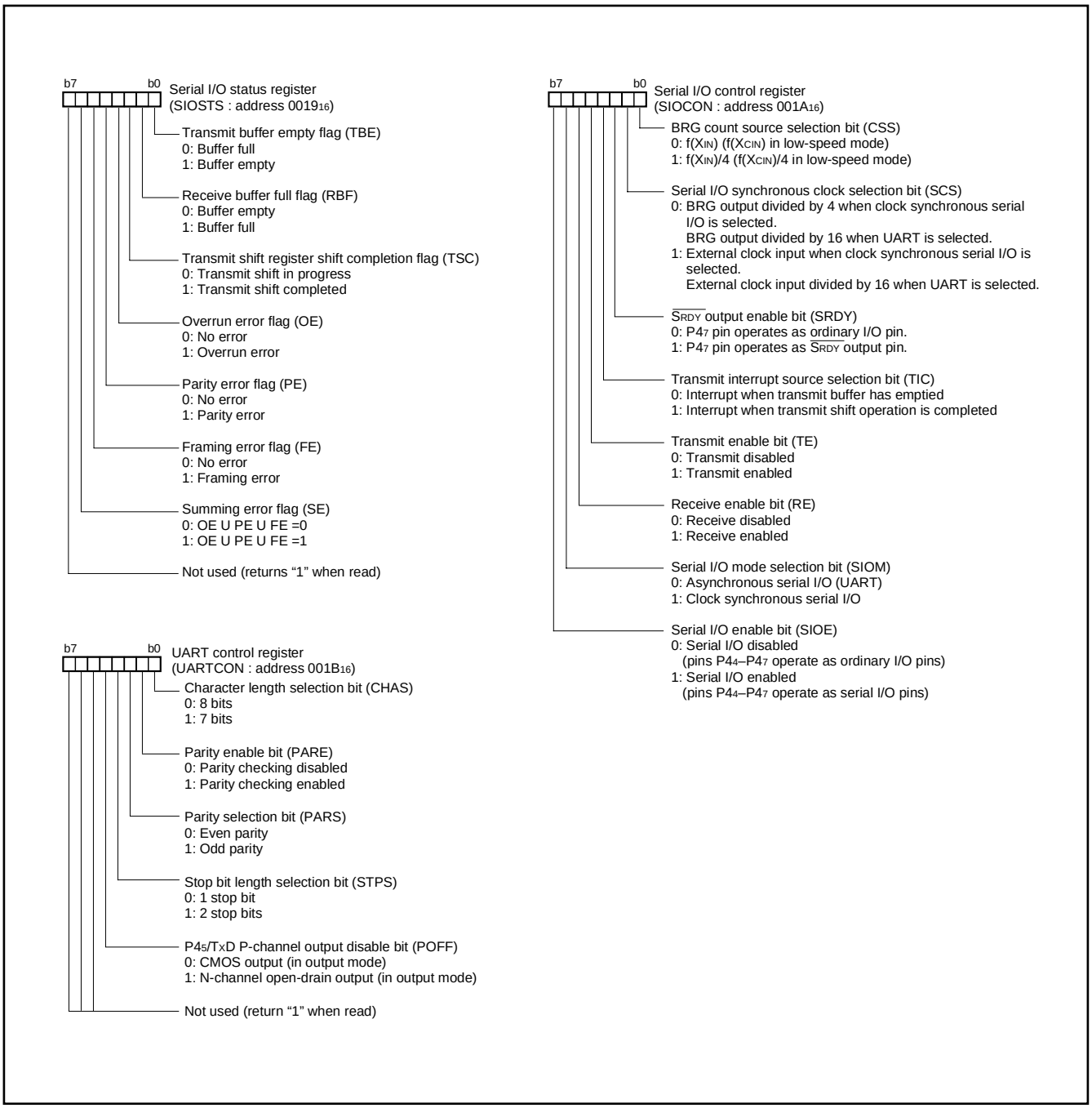


Fig. 24 Structure of serial I/O control registers

A-D CONVERTER

[A-D Conversion Registers (ADL, ADH)] 0032₁₆, 0033₁₆

The A-D conversion registers are read-only registers that contain the result of an A-D conversion. During A-D conversion, do not read these registers.

[A-D Control Register (ADCON)] 0031₁₆

The A-D control register controls the A-D conversion process. Bits 0 to 2 are analog input pin selection bits. Bit 3 is an A-D conversion completion bit and "0" during A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. When bit 5, which is the AD external trigger valid bit, is set to "1", A-D conversion is started even by a rising edge or falling edge of an ADT input.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Because the comparator consists of a capacitor coupling, a deficient conversion speed may cause lack of electric charge and make the conversion accuracy worse. When A-D conversion is performed in the middle-speed mode or the high-speed mode, set f(XIN) to at least 500 kHz.

In the low-speed mode, A-D conversion is performed by using the built-in self-oscillation circuit. Therefore, there is no limitation in the lower bound frequency of f(XIN).

Trigger Start

When using the A-D external trigger, set the port shared with the ADT pin to input. The polarity of INT1 interrupt edge also applies to the A-D external trigger. When the INT1 interrupt edge polarity is switched after an external trigger is validated, an A-D conversion may be started.

Resistor ladder

The resistor ladder outputs the comparison voltage by dividing the voltage between VDD and VSS by resistance.

Channel Selector

The channel selector selects one of the ports P3₃/AIN3–P3₀/AIN0 and ports P1₀/AIN4–P1₃/AIN7, and inputs it to the comparator.

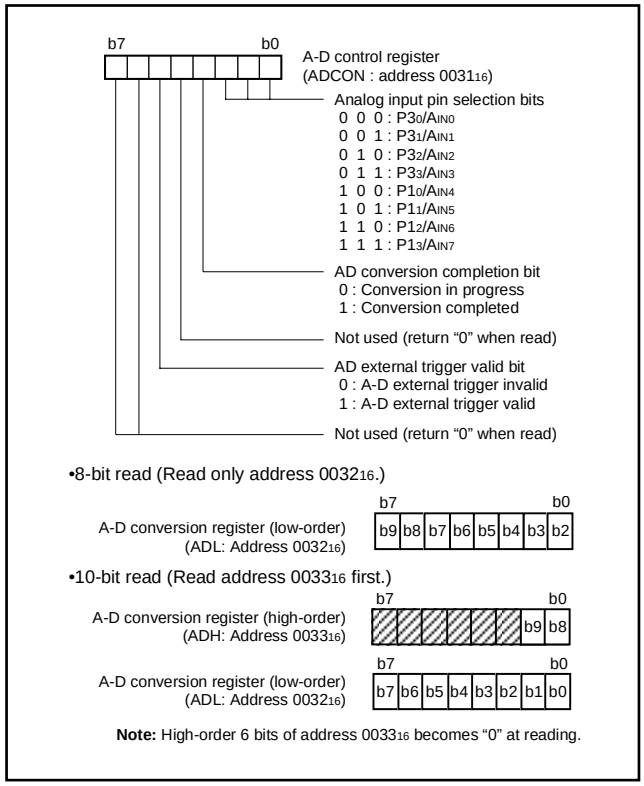


Fig. 25 Structure of A-D control register

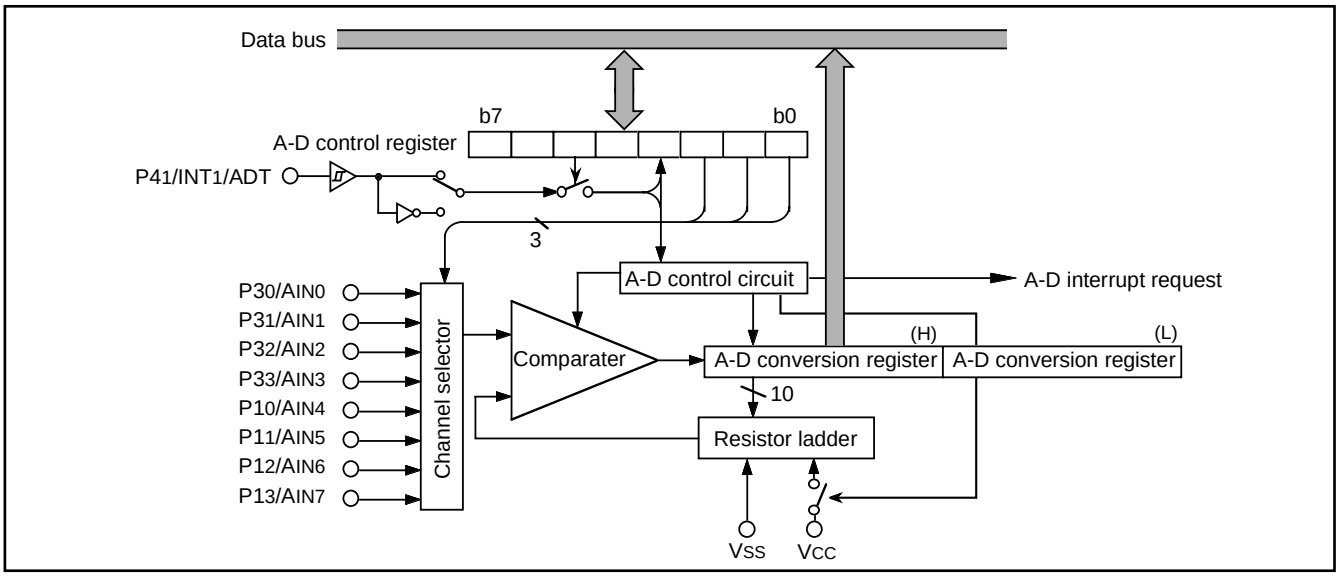


Fig. 26 A-D converter block diagram

LCD CONTROLLER/DRIVER

The 38C8 group has the built-in Liquid Crystal Display (LCD) controller/driver consisting of the following.

- 240-byte LCD display RAM
- 52 or 68 segment driver
- 16 or 32 common driver
- LCD clock generator
- Timing controller
- Bias controller
- Voltage multiplier
- LCD mode register
- LCD control registers 1, 2

A maximum of 68 segment output pins and 32 common output pins can be used for control of external LCD display.

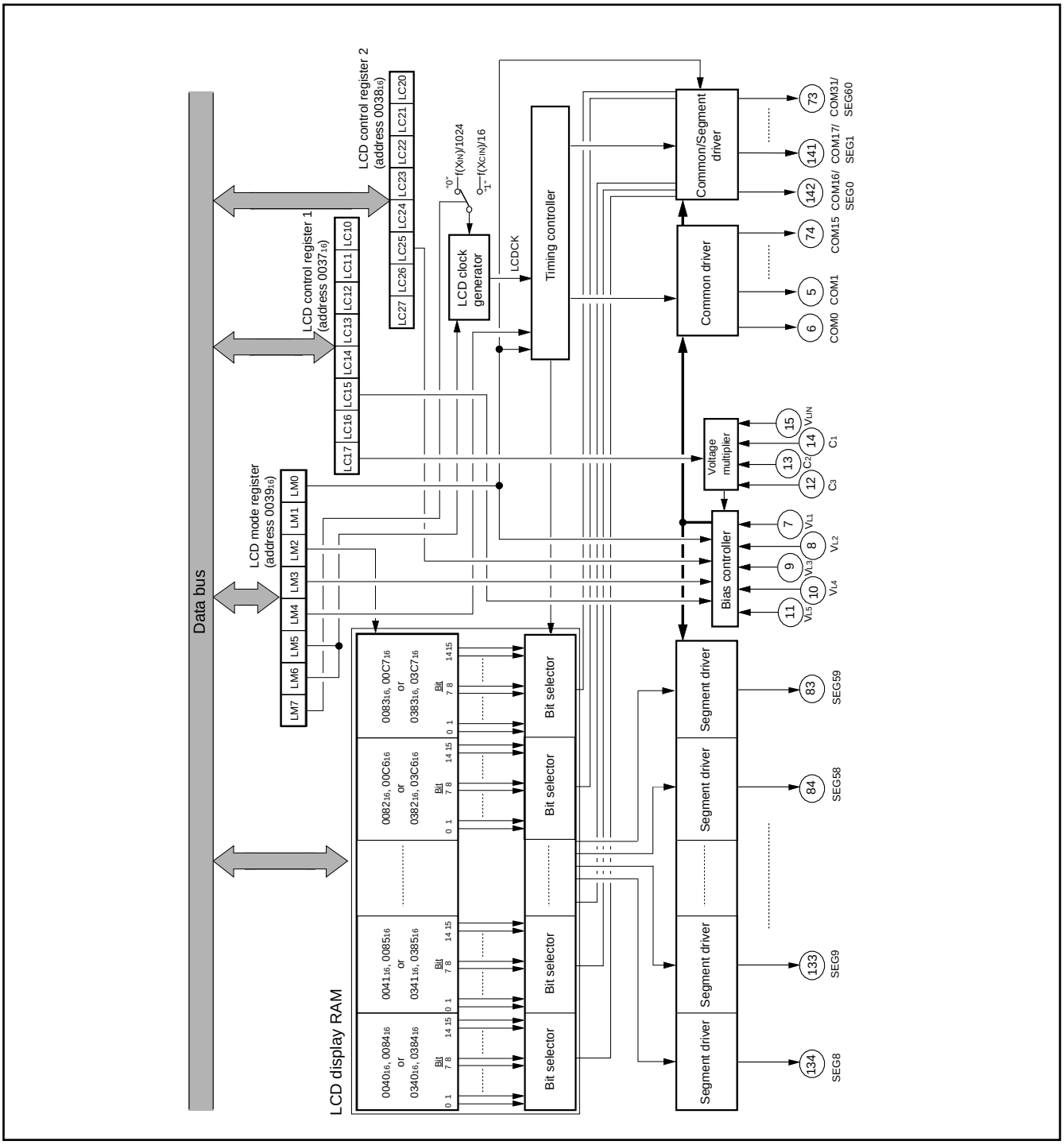


Fig. 27 Block diagram of LCD controller/driver

LCD Controller/Driver Function

The controller/driver performs the bias control and the time sharing control by the LCD control registers 1, 2 (LC1, LC2), and the LCD mode register (LM). The data of corresponding LCDRAM is output from the segment pins according to the output timing of the common pins.

The 38C8 group has the voltage multiplier only for LCD in addition to LCD controller/driver .

[LCD mode register (LM)] 0039$_{16}$

The LCD mode register is used for setting the LCD controller/driver according to the LCD panel used.

[LCD control register 1 (LC1)] 0037$_{16}$

The LCD control register 1 controls the voltage multiplier and built-in resistance.

[LCD control register 2 (LC2)] 0038$_{16}$

The LCD control register 2 is read-only. Setting “1” to bit 5 makes built-in resistance low resistance, and can raise drivability of the segment pins and the common pins.

Table 7 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
16	16 × 68 dots (5 × 7 dots + cursor 2 lines)
32	32 × 52 dots (5 × 7 dots + cursor 4 lines)

Note: When executing the STP instruction while operating LCD, execute the STP instruction after prohibiting LCD (set “0” to bit 3 of the LCD mode regsiter).

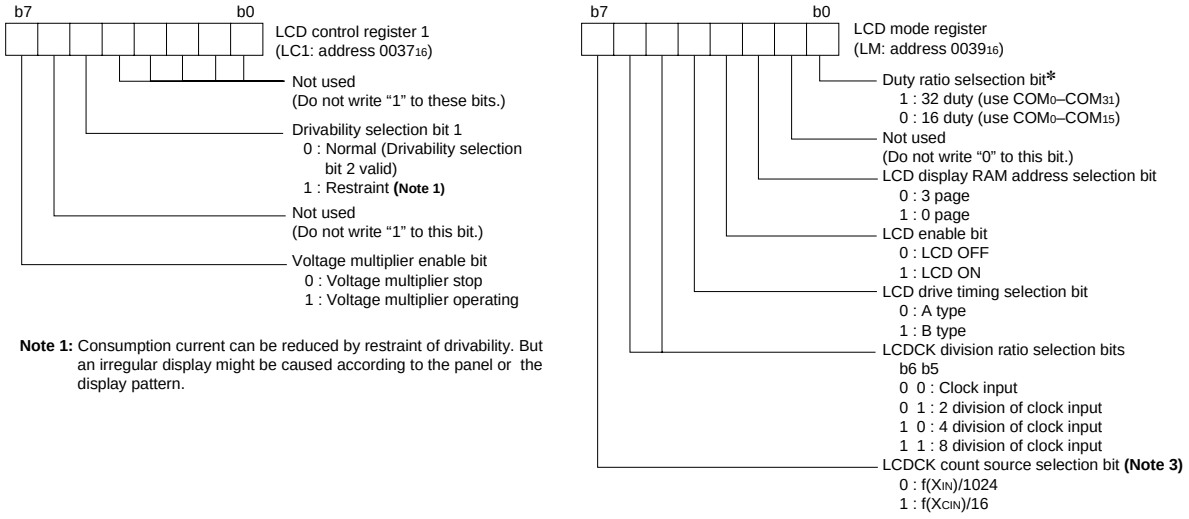


Fig. 28 Structure of LCD control register

Voltage Multiplier

When the voltage multiplier is operated after a reference voltage for boosting is applied to LCD power supply V_{LIN}, a voltage that is three times as large as V_{LIN} pin occurs at the V_{L5} pin. Operate the voltage multiplier after applying a reference voltage for boosting to V_{LIN}.

Bias Control

In the LCD power source pins (V_{L1}–V_{L5}), a proper level is automatically generated in 1/32 and 1/16 duty ratio. The quality of the LCD display can be stabilized by connecting the capacitor for smoothness between Vss and these pins.

Table 8 Bias control and applied voltage to V_{L1}–V_{L5}

Bias value	Voltage value
1/7 bias	V_{L5} = V_{LCD}
	V_{L4} = 6/7 V_{LCD}
	V_{L3} = 5/7 V_{LCD}
	V_{L2} = 2/7 V_{LCD}
	V_{L1} = 1/7 V_{LCD}
1/5 bias	V_{L5} = V_{LCD}
	V_{L4} = 4/5 V_{LCD}
	V_{L3} = 3/5 V_{LCD}
	V_{L2} = 2/5 V_{LCD}
	V_{L1} = 1/5 V_{LCD}

Note: V_{LCD} is a value which can be supplied to the LCD panel. Set value which is less than maximum ratings to V_{LCD}.

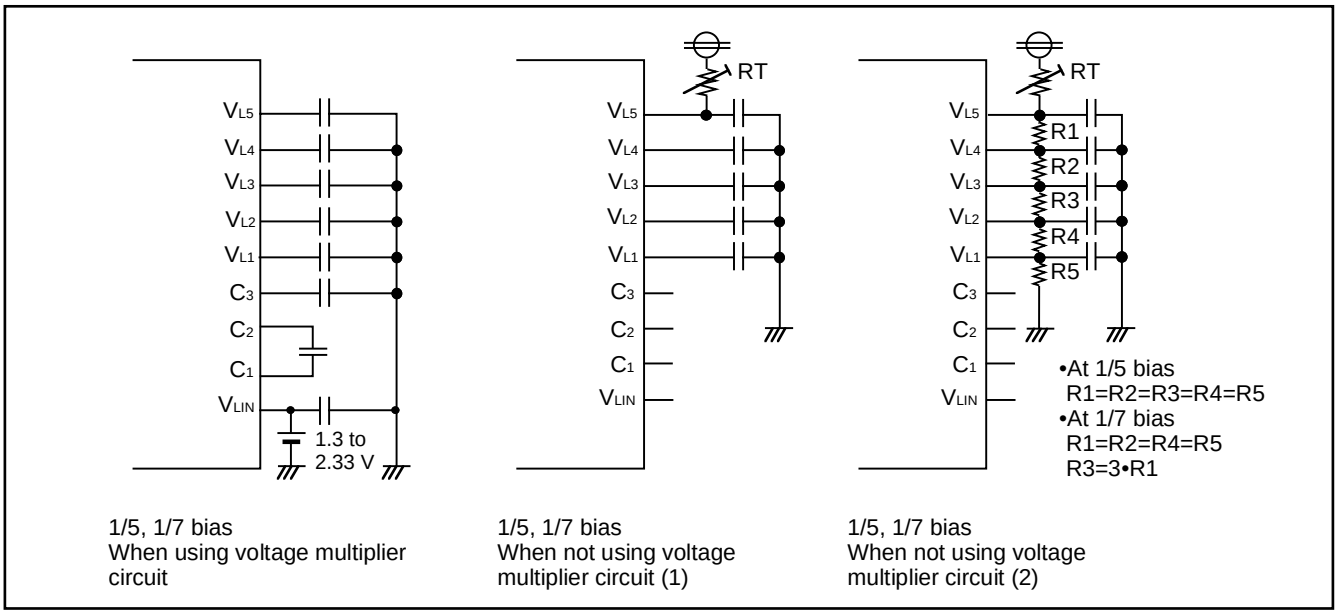


Fig. 29 Example of circuit at each bias

Common Pin and Duty Ratio Control

The common pins (COM0–COM31) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bit (bit 0 of the LCD mode register).

Table 9 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit	Common pins used
16	0	COM0–COM15 **(Note)**
32	1	COM0–COM31

Note: The SEG0/COM16–SEG7/COM23 pins are used as the SEG0–SEG7.
The SEG67/COM24–SEG60/COM31 pins are used as the SEG67–SEG60.

LCD Display RAM

Addresses 0040$_{16}$ to 012F$_{16}$ is the designated RAM for the LCD display. When “1” are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{(\text{frequency of count source for LCDCK})}{(\text{divider division ratio for LCD})}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{(\text{duty ratio})}$$

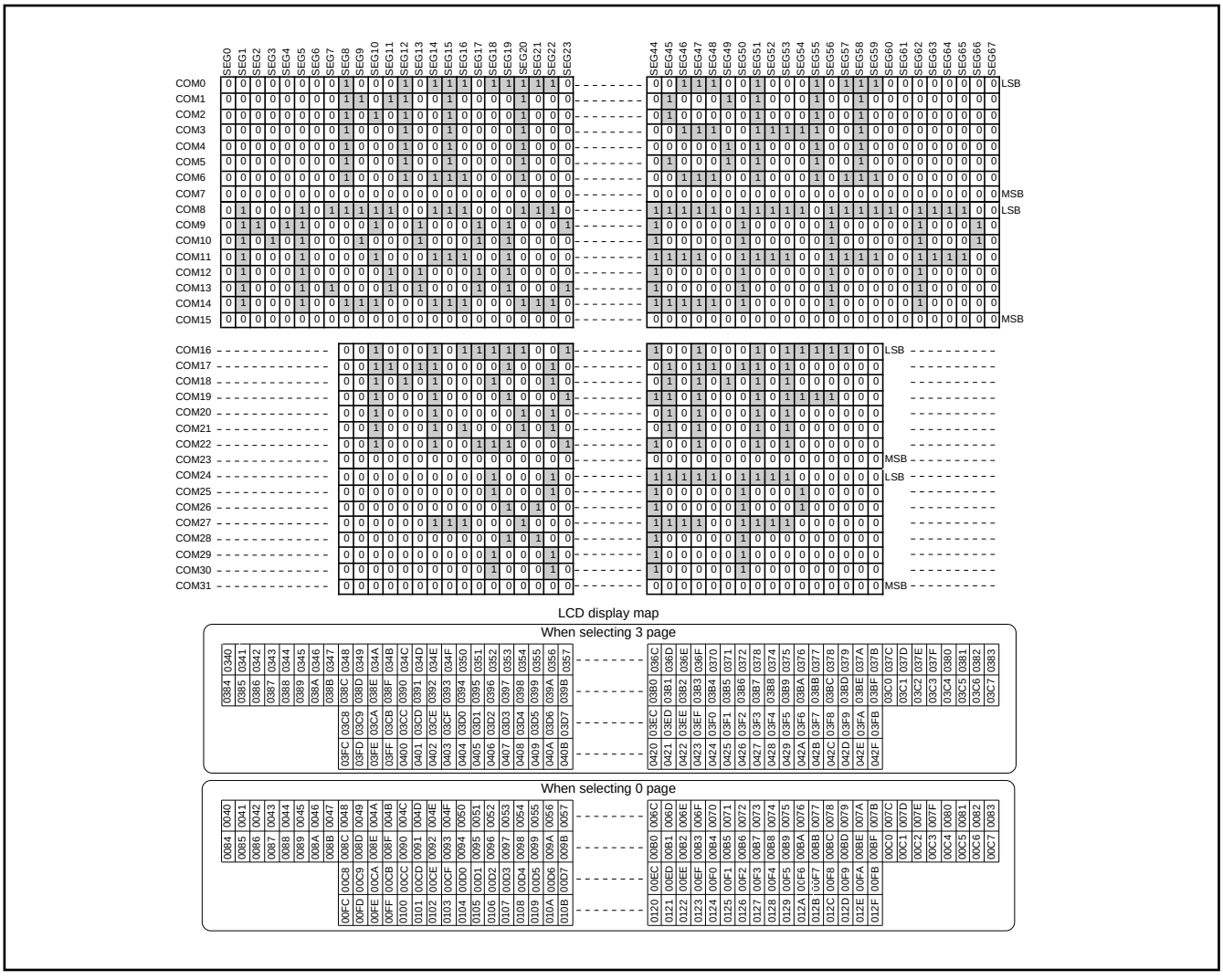


Fig. 30 LCD display RAM map

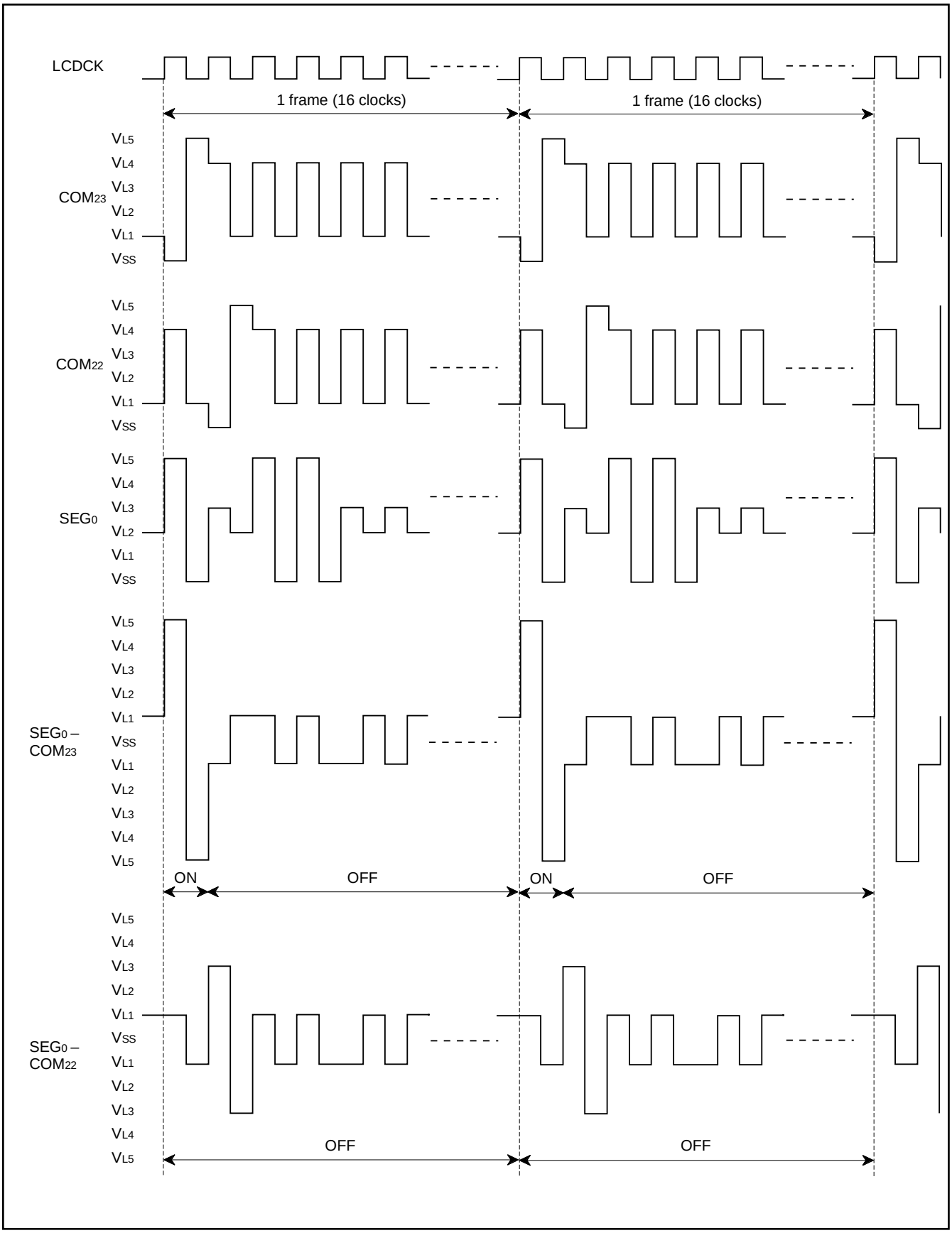


Fig. 31 LCD drive waveform (1/16 duty ratio, 1/5 bias, A type)

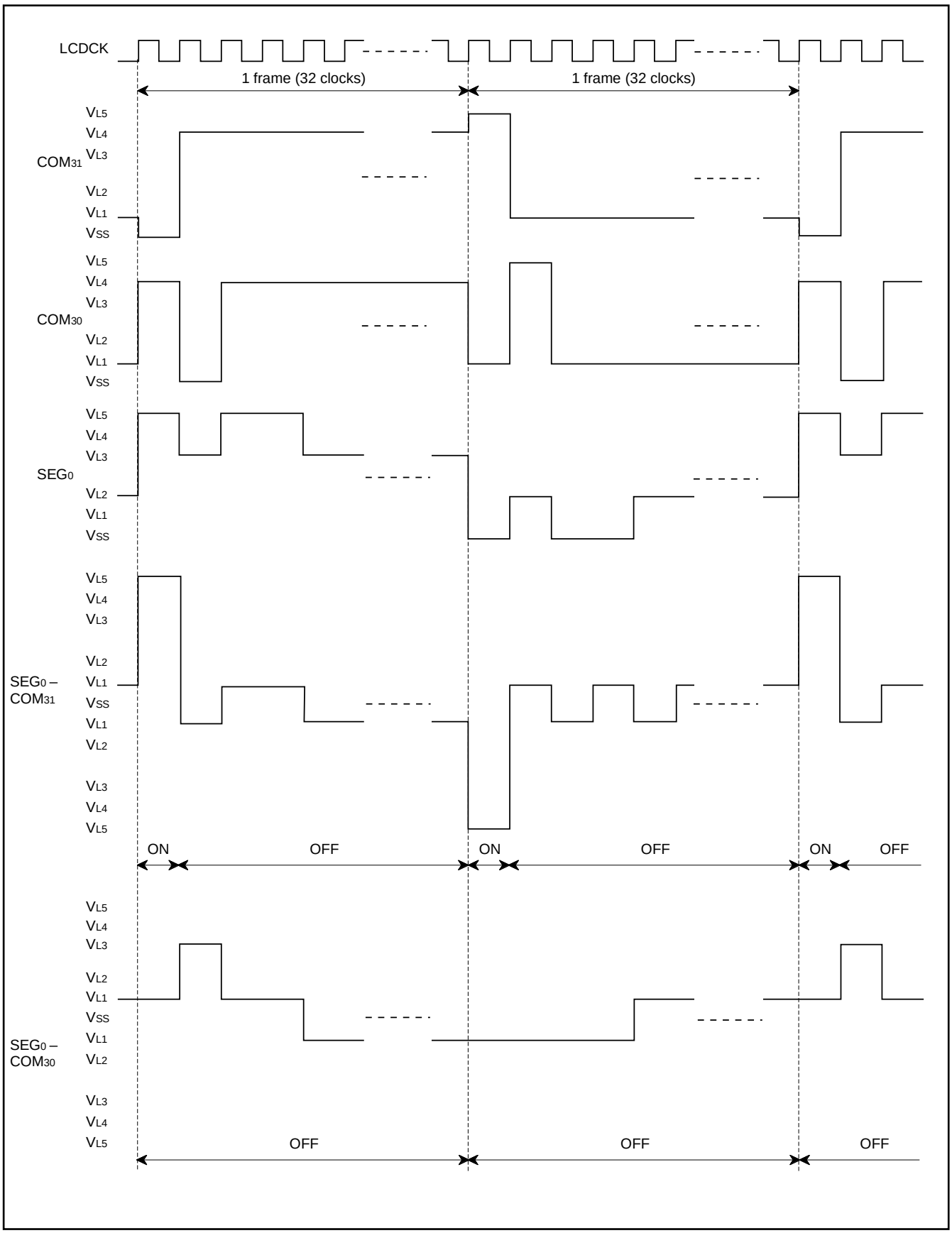


Fig. 32 LCD drive waveform (1/32 duty ratio, 1/7 bias, B type)

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between V_{CC} (min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.2Vcc when a power source voltage passes V_{CC} (min.).

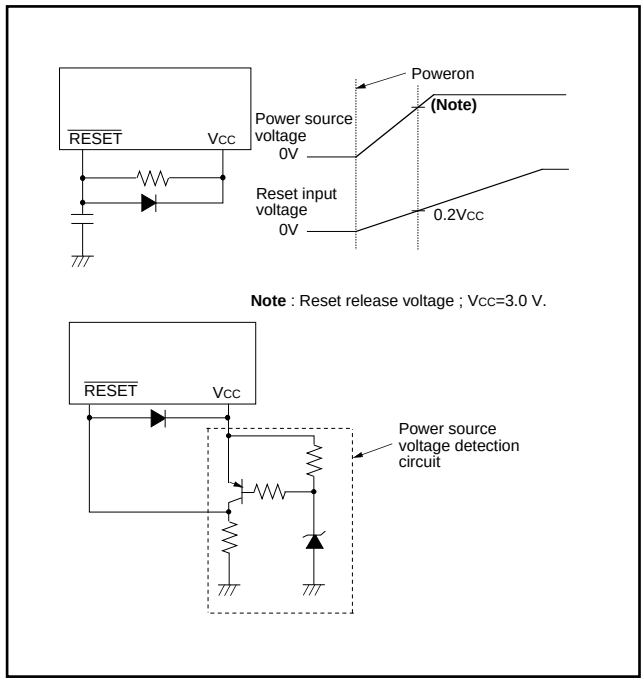
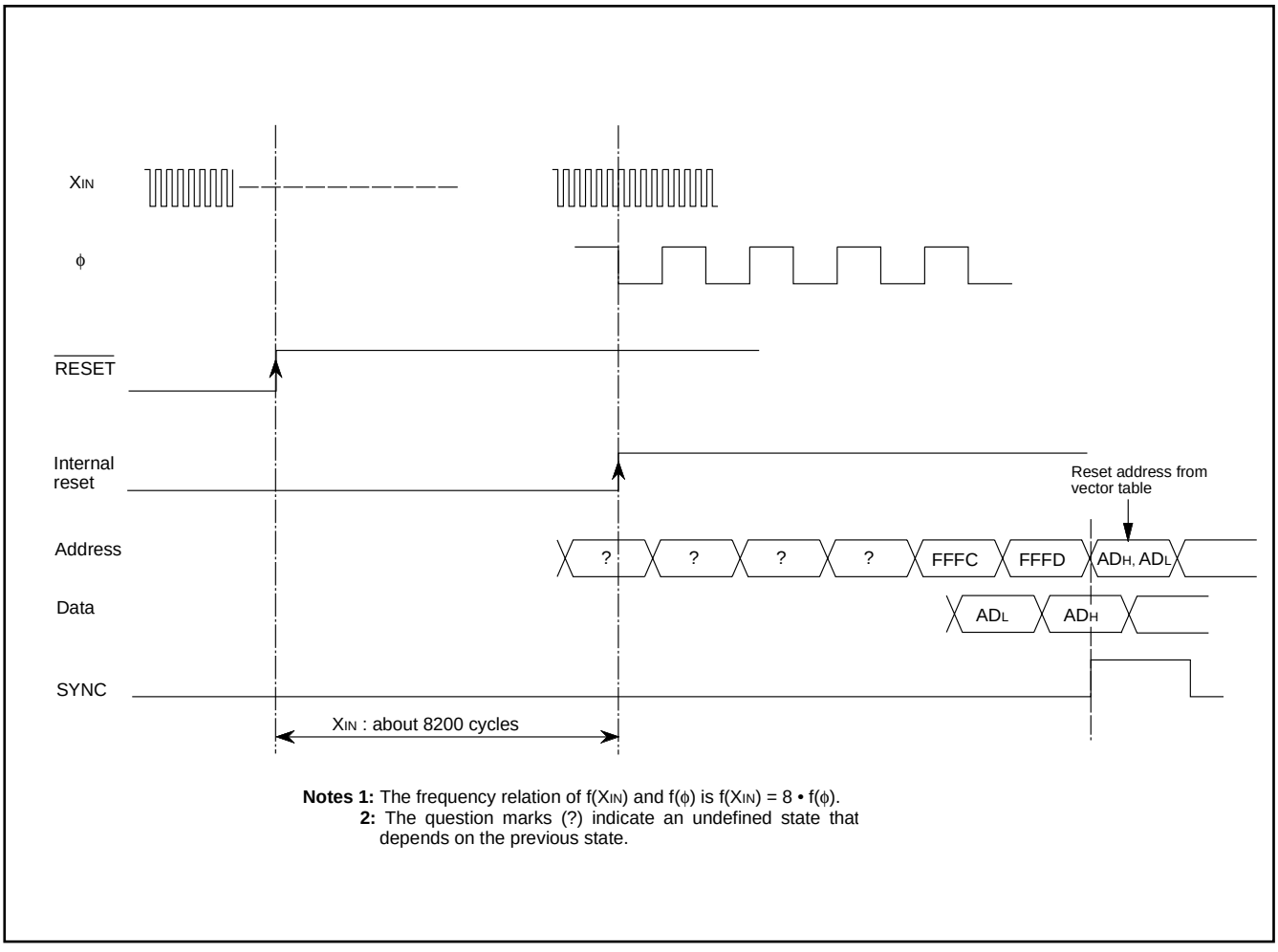


Fig. 33 Reset circuit example



Notes 1: The frequency relation of $f(X_{IN})$ and $f(\phi)$ is $f(X_{IN}) = 8 \cdot f(\phi)$.
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig. 34 Reset sequence

	Address	Register contents
(1) Port P0 direction register	0001_{16}	00_{16}
(2) Port P1 direction register	0003_{16}	00_{16}
(3) Port P2 direction register	0005_{16}	00_{16}
(4) Port P3 direction register	0007_{16}	00_{16}
(5) Port P4 direction register	0009_{16}	00_{16}
(6) PULL register A	0016_{16}	00_{16}
(7) PULL register B	0017_{16}	00_{16}
(8) Serial I/O status register	0019_{16}	80_{16}
(9) Serial I/O control register	$001A_{16}$	00_{16}
(10) UART control register	$001B_{16}$	$E0_{16}$
(11) Timer X (low-order)	0020_{16}	FF_{16}
(12) Timer X (high-order)	0021_{16}	FF_{16}
(13) Timer Y (low-order)	0022_{16}	FF_{16}
(14) Timer Y (high-order)	0023_{16}	FF_{16}
(15) Timer 1	0024_{16}	FF_{16}
(16) Timer 2	0025_{16}	01_{16}
(17) Timer 3	0026_{16}	FF_{16}
(18) Timer X mode register	0027_{16}	00_{16}
(19) Timer Y mode register	0028_{16}	00_{16}
(20) Timer 123 mode register	0029_{16}	00_{16}

	Address	Register contents
(21) A-D control register	0031_{16}	08_{16}
(22) A-D conversion register (low-order)	0032_{16}	XX_{16}
(23) A-D conversion register (high-order)	0033_{16}	XX_{16}
(24) LCD control register 1	0037_{16}	00_{16}
(25) LCD control register 2	0038_{16}	00_{16}
(26) LCD mode register	0039_{16}	03_{16}
(27) Interrupt edge selection register	$003A_{16}$	00_{16}
(28) CPU mode register	$003B_{16}$	$4C_{16}$
(29) Interrupt request register 1	$003C_{16}$	00_{16}
(30) Interrupt request register 2	$003D_{16}$	00_{16}
(31) Interrupt control register 1	$003E_{16}$	00_{16}
(32) Interrupt control register 2	$003F_{16}$	00_{16}
(33) Processor status register	(PS)	× × × × × 1 × ×
(34) Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$

Note: The contents of all other register and RAM are undefined after reset, so they must be initialized by software.
× : Undefined

Fig. 35 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38C8 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). RC oscillation is available for XIN-XOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins go to high impedance state.

Main Clock

An oscillation circuit by a resonator can be formed by setting the OSCSEL pin is set to "L" level and connecting a resonator between XIN and XOUT. Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. To supply a clock signal externally, make the XOUT pin open in the "L" level state of the OSCSEL pin, and supply the clock from the XIN pin. The RC oscillation circuit can be formed by setting the OSCSEL pin to "H" level and connecting a resistor between the XIN pin and the XOUT pin. At this time, the feed-back resistor is cut off. The frequency of the RC oscillation changes owing to a parasitic capacitance or the wiring length etc. of the printed circuit board. Do not use the RC oscillation in the usage which the frequency accuracy of the main clock is needed.

Sub-clock

Connect a resonator between XCIN and XCOUT. An external feed-back resistor is needed between XCIN and XCOUT since a feed-back resistor does not exist on-chip. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Frequency Control
(1) Middle-speed Mode

The internal clock ϕ is the frequency of XIN divided by 8. At reset, this mode is selected.

(2) High-speed Mode

The internal clock ϕ is the frequency of XIN divided by 2.

(3) Low-speed Mode

The internal clock ϕ is the frequency of XCIN divided by 2.
A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

■Notes on clock generating circuit

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3•f(XCIN).

Oscillation Control
(1) Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116."
Either XIN divided by 16 or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits except bit 4 of the timer 123 mode register are cleared to "0." Set the interrupt enable bits of timer 1 and timer 2 to disabled ("0") before executing the STP instruction.
Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

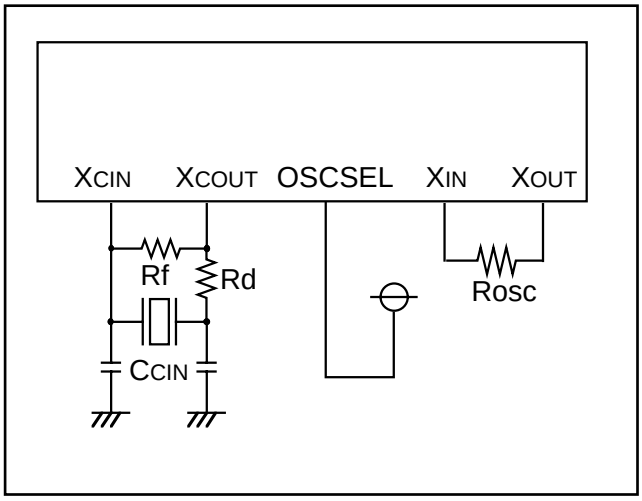


Fig. 36 RC oscillation circuit

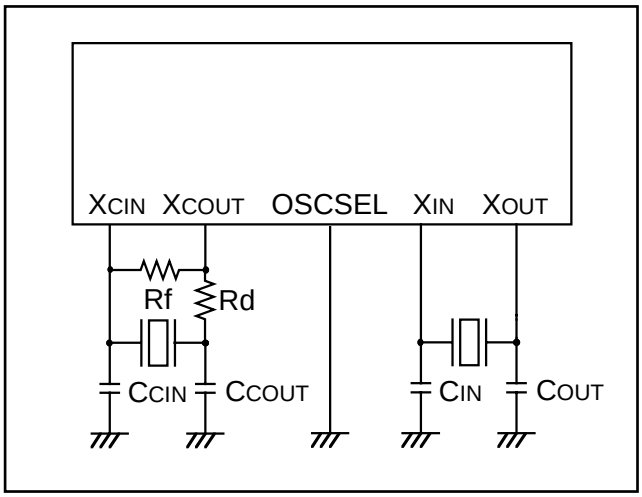
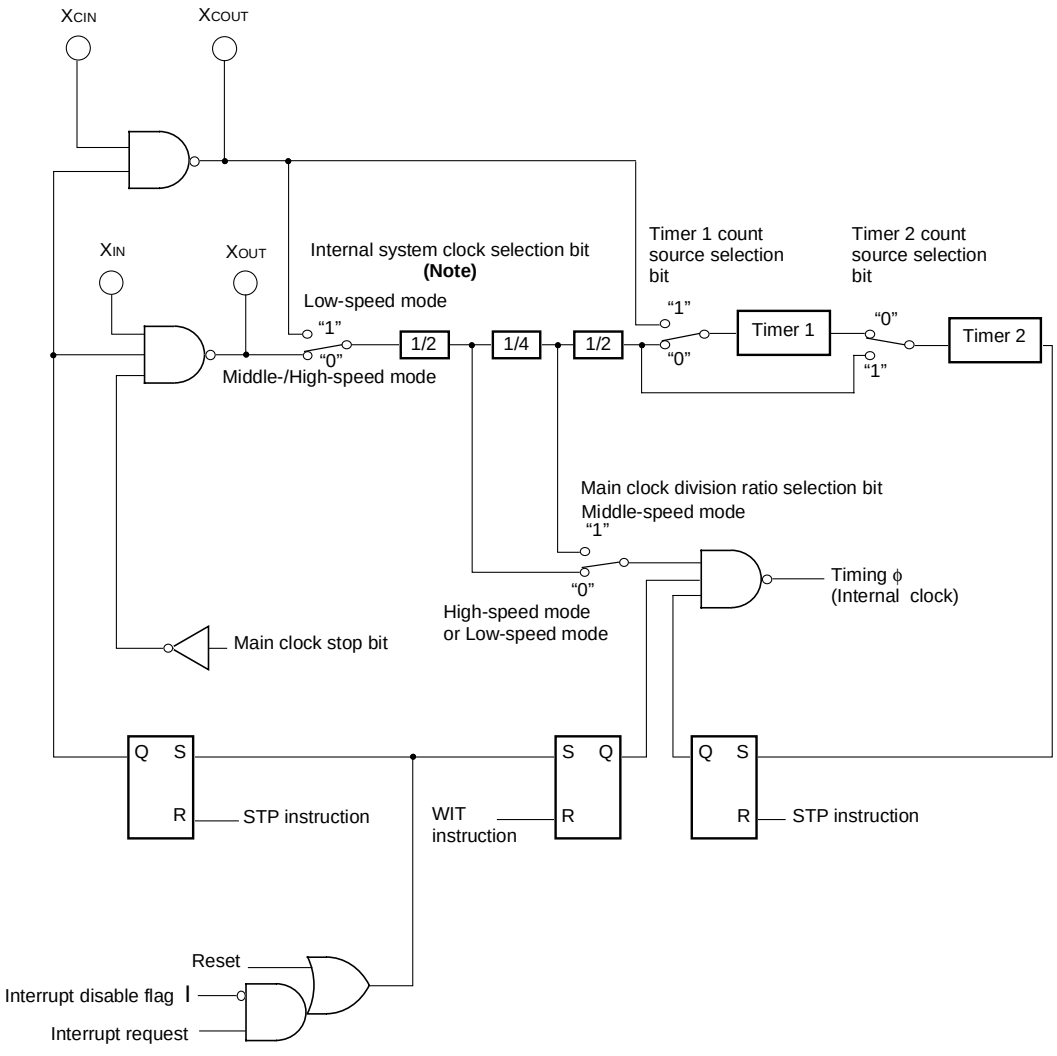
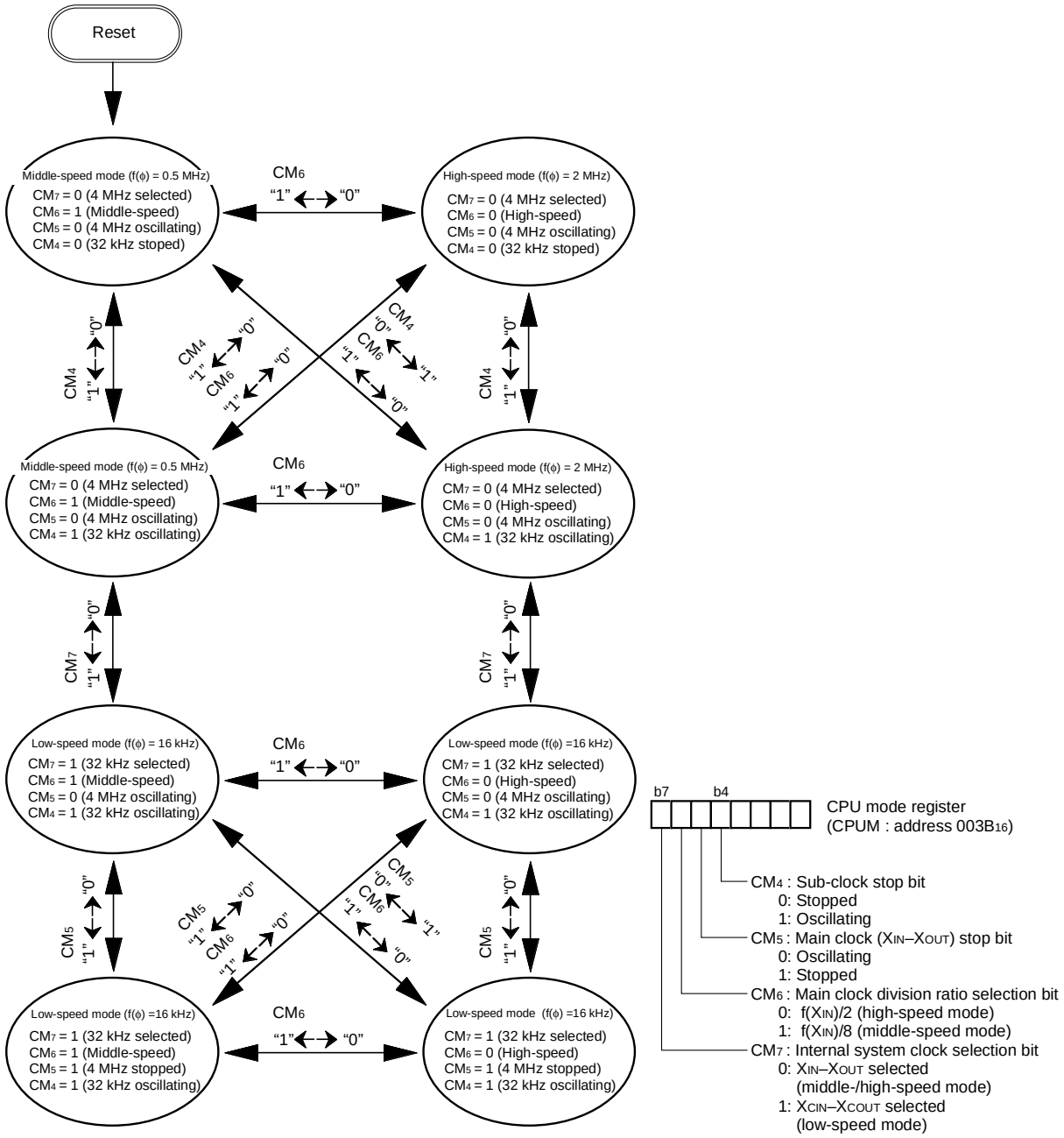


Fig. 37 Resonator circuit



Note: When selecting the XC oscillation, set the port XC switch bit to "1" .

Fig. 38 Clock generating circuit block diagram



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.
3 : Timer and LCD operate in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs automatically by timer 1 and timer 2 in middle-/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs automatically by timer 1 and timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle-/high-speed mode.
7 : The example assumes that 4 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. ϕ indicates the internal clock.

Fig. 39 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A-D Converter

The comparator is constructed linked to a capacitor. When the conversion speed is not enough, the conversion accuracy might be ruined by the disappearance of the charge. When A-D conversion is performed in the middle-speed mode or the high-speed mode, set f(XIN) to at least 500 kHz.
Do not execute the STP or WIT instruction during an A-D conversion because a normal conversion result is not obtained.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the XIN frequency.

At STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

LCD Control

When using the voltage multiplier, apply prescribed voltage to the VLIN pin in the state in which the LCD enable bit is "0", and set the voltage multiplier enable bit to "1".

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*1
2. Mark Specification Form*2
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

For the mask ROM confirmation and the mark specifications, refer to the “Mitsubishi MCU Technical Information” Homepage.

✻1 Mask ROM Confirmation Forms
http://www.infomicom.mesc.co.jp/38000/38ordere.htm

✻2 Mark Specification Forms
http://www.infomicom.mesc.co.jp/mela/markform.htm

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter (PCA7447FP).

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 40 is recommended to verify programming.

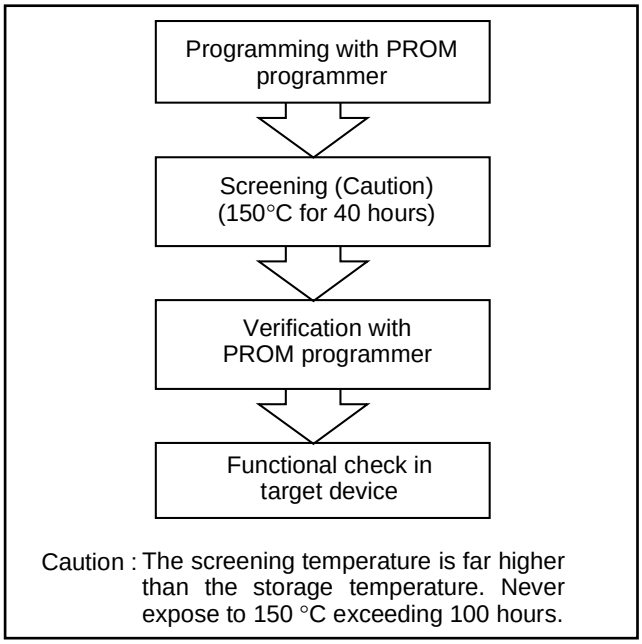


Fig. 40 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 10 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on Vss. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$		–0.3 to V_{CC}+0.3	V
V_I	Input voltage C_1, C_2		–0.3 to 7.0	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		–0.3 to V_{CC}+0.3	V
V_I	Input voltage V_{LIN}	When voltage multiplier is not operated.	–0.3 to 7.0	V
V_I	Input voltage V_{L1}, V_{L2}, V_{L3}, V_{L4}, V_{L5}	$V_{L1} \le V_{L2} \le V_{L3} \le V_{L4} \le V_{L5}$	–0.3 to 7.0	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_1$–$P4_7$		–0.3 to V_{CC}+0.3	V
V_O	Output voltage C_1, C_2, C_3		–0.3 to 7.0	V
V_O	Output voltage COM_0–COM_{31}, SEG_0–SEG_{67}		–0.3 to V_{L5}+0.3	V
V_O	Output voltage X_{OUT}, X_{COUT}		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Ta = 25°C	300	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Table 11 Recommended operating conditions (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) ≤ 8 MHz	4.0	5.0	5.5	V
		High-speed mode f(X_{IN}) ≤ 4 MHz	3.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) ≤ 8 MHz	2.7	5.0	5.5	V
		Middle-speed mode (mask ROM version) f(X_{IN}) ≤ 4 MHz	2.2	5.0	5.5	V
		Middle-speed mode (One Time PROM version) f(X_{IN}) ≤ 4 MHz	2.5	5.0	5.5	V
		Low-speed mode (mask ROM version)	2.2	5.0	5.5	V
		Low-speed mode (One Time PROM version)	2.5	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{LIN}	Power source voltage	V_{LIN}			2.33	V
V_{L5}	Power source voltage	V_{L5}			7.0	V
V_{IA}	Analog input voltage	AN_0–AN_7	V_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$	0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_1$, $P4_2$, $P4_4$, $P4_6$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$	V_{SS}		0.3V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_1$, $P4_2$, $P4_4$, $P4_6$	V_{SS}		0.2V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$	V_{SS}		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	V_{SS}		0.2V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current	All ports **(Note 1)**			–60.0	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current	All ports **(Note 1)**			60.0	mA
$\Sigma I_{OH(avg)}$	“H” total average output current	All ports **(Note 2)**			–30.0	mA
$\Sigma I_{OL(avg)}$	“L” total average output current	All ports **(Note 2)**			30.0	mA
$I_{OH(peak)}$	“H” peak output current	All ports **(Note 3)**			–5.0	mA
$I_{OL(peak)}$	“L” peak output current	All ports **(Note 3)**			10.0	mA
$I_{OH(avg)}$	“H” average output current	All ports **(Note 4)**			–2.5	mA
$I_{OL(avg)}$	“L” average output current	All ports **(Note 4)**			5.0	mA
R_{OSC}	Oscillation resistor at selecting RC oscillation		5	8.2	10	kΩ

Notes 1: The total peak output current is the peak value of the peak currents flowing through all the applicable ports.
2: The total average output current is the average value measured over 100 ms flowing through all the applicable ports.
3: The peak output current is the peak current flowing in each port.
4: The average output current is an average value measured over 100 ms.

Table 12 Recommended operating conditions (mask ROM version) (Vcc = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X, timer Y input frequency (duty cycle 50%)				f(XIN)/2	MHz
f(XIN)	Main clock input oscillation frequency **(Note 1)**	High-speed mode (4.0 V ≤ VCC ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.2 V ≤ VCC < 4.0 V)			(20×VCC–8)/13	MHz
		Middle-speed mode (2.7 V ≤ VCC ≤ 5.5 V)			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency **(Notes 1, 2)**			32.768	50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50 %.
2: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Table 13 Recommended operating conditions (PROM version) (Vcc = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X, timer Y input frequency (duty cycle 50%)				f(XIN)/2	MHz
f(XIN)	Main clock input oscillation frequency **(Note 1)**	High-speed mode (4.0 V ≤ VCC ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.5 V ≤ VCC < 4.0 V)			4×VCC–8	MHz
		Middle-speed mode (2.7 V ≤ VCC ≤ 5.5 V)			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency **(Notes 1, 2)**			32.768	50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50 %.
2: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Table 14 Electrical characteristics (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$	I_{OH} = –5.0 mA V_{CC} = 5.0 V	V_{CC}–2.0			V
		I_{OH} = –1.5 mA V_{CC} = 5.0 V	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.2 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$	I_{OH} = –5.0 mA V_{CC} = 5.0 V	V_{CC}–2.0			V
		I_{OH} = –1.5 mA V_{CC} = 5.0 V	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.2 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$	I_{OL} = 5.0 mA V_{CC} = 5.0 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 5.0 V			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.2 V			1.0	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$	I_{OL} = 5.0 mA V_{CC} = 5.0 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 5.0 V			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.2 V			1.0	V
V_{T+}–V_{T-}	Hysteresis INT_0, INT_1, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+}–V_{T-}	Hysteresis S_{CLK}, RxD			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current All ports				5.0	µA
I_{IH}	"H" input current $\overline{RESET}$				5.0	µA
I_{IH}	"H" input current X_{IN}			4.0		µA
I_{IL}	"L" input current All ports	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5.0 V, V_I = V_{CC} Pull-ups "on"	–60.0	–120.0	–240.0	µA
		V_{CC} = 2.2 V, V_I = V_{CC} Pull-ups "on"	–5.0	–20.0	–40.0	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Table 15 Electrical characteristics (Vcc = 2.2 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{RAM}	RAM hold voltage	When clock is stopped	2.0	5.0	5.5	V
I_{CC}	Power source current	High-speed mode, Vcc = 5.0 V f(X_{IN}) = 8.0 MHz f(X_{CIN}) = 32.768 kHz		5.5	11.0	mA
		Middle-speed mode, Vcc = 5.0 V f(X_{IN}) = 8.0 MHz f(X_{CIN}) = 32.768 kHz		3.0	6.0	mA
		Middle-speed mode, Vcc = 3.0 V f(X_{IN}) = 8.0 MHz f(X_{CIN}) = 32.768 kHz		1.0	2.0	mA
		Low-speed mode, V_{CC} = 3.0 V, f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz		20.0	40.0	µA
		High-/Middle-speed mode, V_{CC} = 5.0 V, f(X_{IN}) = 8.0 MHz (in WIT state) f(X_{CIN}) = 32.768 kHz		0.9	1.8	mA
		Middle-speed mode, Vcc = 3.0 V f(X_{IN}) = 8.0 MHz (in WIT state) f(X_{CIN}) = 32.768 kHz		0.3	0.6	mA
		Low-speed mode, V_{CC} = 3.0 V, f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state)		4.5	9.0	µA
		All oscillation stopped Ta = 25 °C, Output transistors “off” (in STP state)		0.1	1.0	µA
		All oscillation stopped Ta = 85 °C, Output transistors “off” (in STP state)			10.0	µA
I_{AD}	A-D converter current dissipation	Current increase at A-D converter operated, f(X_{IN}) = 8.0 MHz		0.8	1.6	mA
I_{L5}	V_{L5} input current **(Note)**	V_{L5} = 6.0 V, Ta = 25 °C		3	6	µA
F_{ROSC}	RC oscillation frequency	R_{OSC} = 8.2 kΩ	1.5	2.5	3.5	MHz

Note: When normal drivability (drivability selection bit 1 = “0”, drivability selection bit 2 = “0”) is selected.

Table 16 A-D converter characteristics

(Vcc = 2.2 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, f(XIN) ≤ 4 MHz, in middle-speed/high-speed mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy	VCC = 2.7–5.5 V			±4	LSB
	(excluding quantization error)	VCC = 2.5–2.7 V (Ta = –10 to 50 °C)			±6	LSB
tconv	Conversion time	f(XIN) = 4 MHz **(Note)**	30.5		34	µs
IIA	Analog port input current			0.5	5.0	µA

Note: When main clock is selected as system clock.

Table 17 Timing requirements 1 (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tw($\overline{\text{RESET}}$)	Reset input “L” pulse width		2			µs
tc(XIN)	Main clock input cycle time (XIN input)		125			ns
twH(XIN)	Main clock input “H” pulse width		45			ns
twL(XIN)	Main clock input “L” pulse width		40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time		250			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width		105			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width		105			ns
twH(INT)	INT0, INT1 input “H” pulse width		80			ns
twL(INT)	INT0, INT1 input “L” pulse width		80			ns
tc(SCLK)	Serial I/O clock input cycle time	**(Note)**	800			ns
twH(SCLK)	Serial I/O clock input “H” pulse width	**(Note)**	370			ns
twL(SCLK)	Serial I/O clock input “L” pulse width	**(Note)**	370			ns
tsu(RxD-SCLK)	Serial I/O input setup time		220			ns
th(SCLK-RxD)	Serial I/O input hold time		100			ns

Note: When bit 6 of address 001A16 is “1”.
Divide this value by four when bit 6 of address 001A16 is “0”.

Table 18 Timing requirements 2 (Vcc = 2.2 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
tw($\overline{\text{RESET}}$)	Reset input “L” pulse width		2			µs
tc(XIN)	Main clock input cycle time (XIN input)		125			ns
twH(XIN)	Main clock input “H” pulse width		45			ns
twL(XIN)	Main clock input “L” pulse width		40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time		900/(VCC–0.4)			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width		tc(CNTR)/2–20			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width		tc(CNTR)/2–20			ns
twH(INT)	NT0, INT1 input “H” pulse width		230			ns
twL(INT)	NT0, INT1 input “L” pulse width		230			ns
tc(SCLK)	Serial I/O clock input cycle time	**(Note)**	2000			ns
twH(SCLK)	Serial I/O clock input “H” pulse width	**(Note)**	950			ns
twL(SCLK)	Serial I/O clock input “L” pulse width	**(Note)**	950			ns
tsu(RxD-SCLK)	Serial I/O input setup time		400			ns
th(SCLK-RxD)	Serial I/O input hold time		200			ns

Note: When bit 6 of address 001A16 is “1”.
Divide this value by four when bit 6 of address 001A16 is “0”.

Table 19 Switching characteristics 1 (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O clock output “H” pulse width		t_C(SCLK)/2–30			ns
t_{WL}(SCLK)	Serial I/O clock output “L” pulse width		t_C(SCLK)/2–30			ns
t_d(SCLK-TxD)	Serial I/O output delay time	**(Note 1)**			140	ns
t_V(SCLK-TxD)	Serial I/O output valid time	**(Note 1)**	–30			ns
t_r(SCLK)	Serial I/O clock output rising time				30	ns
t_f(SCLK)	Serial I/O clock output falling time				30	ns
t_r(CMOS)	CMOS output rising time	**(Note 2)**		10	30	ns
t_f(CMOS)	CMOS output falling time	**(Note 2)**		10	30	ns

Notes 1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: The XOUT and XCOUT pins are excluded.

Table 20 Switching characteristics 2 (Vcc = 2.2 to 4.0 V, Vss = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
t_{WH}(SCLK)	Serial I/O clock output “H” pulse width		t_C(SCLK)/2–50			ns
t_{WL}(SCLK)	Serial I/O clock output “L” pulse width		t_C(SCLK)/2–50			ns
t_d(SCLK-TxD)	Serial I/O output delay time	**(Note 1)**			350	ns
t_V(SCLK-TxD)	Serial I/O output valid time	**(Note 1)**	–30			ns
t_r(SCLK)	Serial I/O clock output rising time				50	ns
t_f(SCLK)	Serial I/O clock output falling time				50	ns
t_r(CMOS)	CMOS output rising time	**(Note 2)**		20	50	ns
t_f(CMOS)	CMOS output falling time	**(Note 2)**		20	50	ns

Notes 1: When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is “0”.
2: The XOUT and XCOUT pins are excluded.

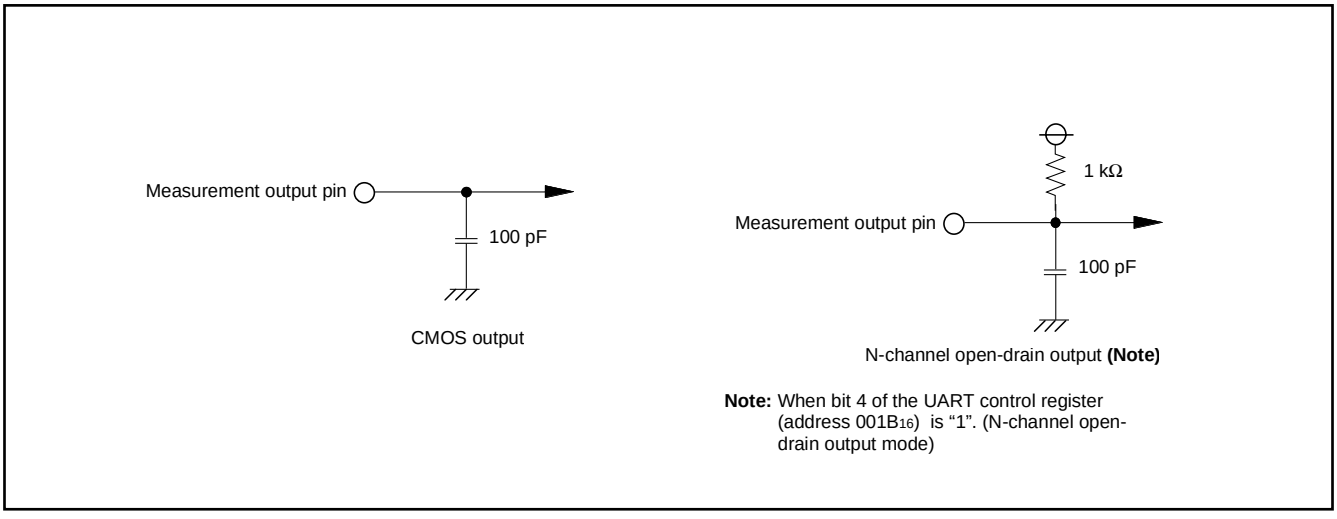


Fig. 41 Circuit for measuring output switching characteristics

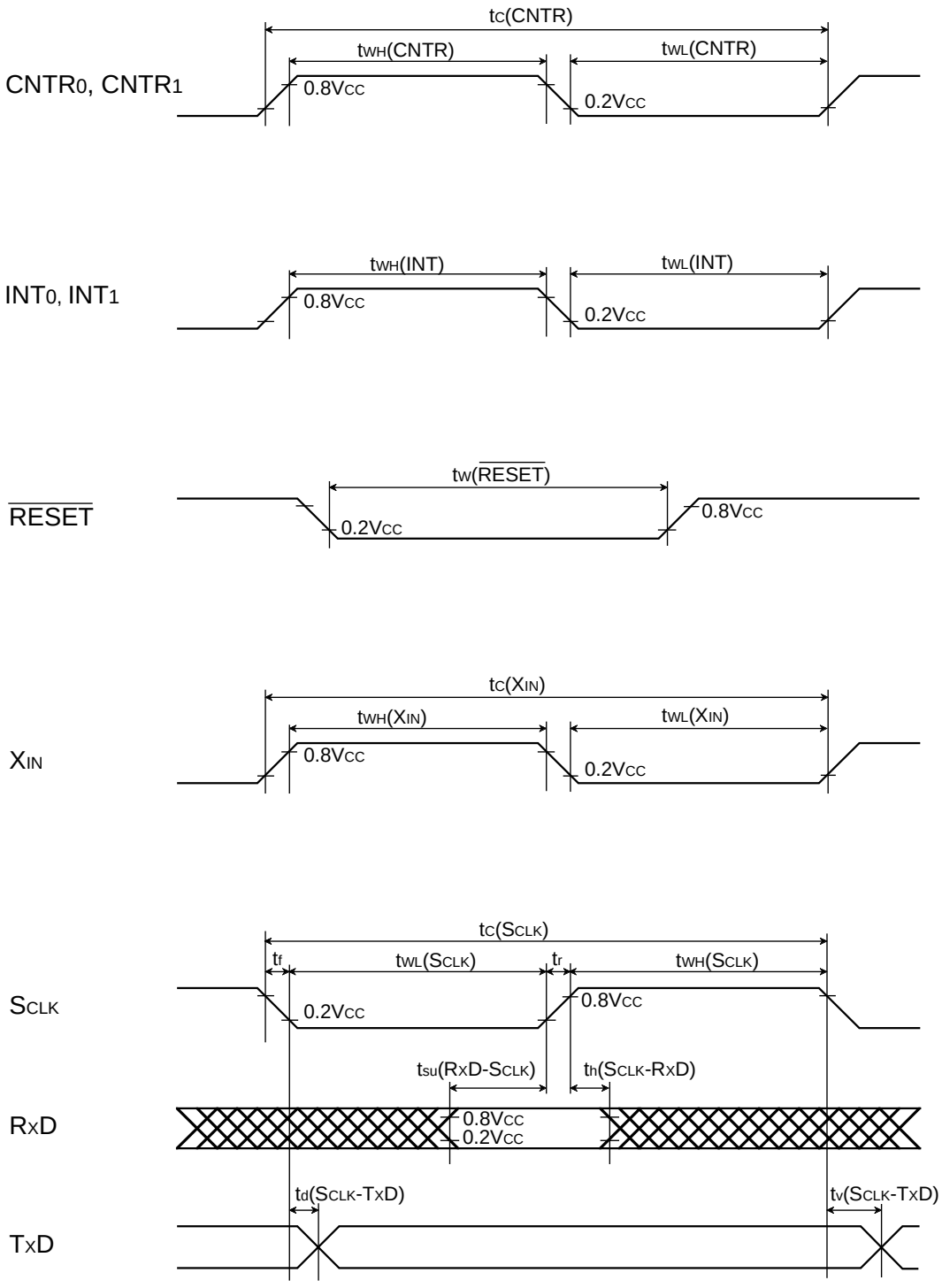


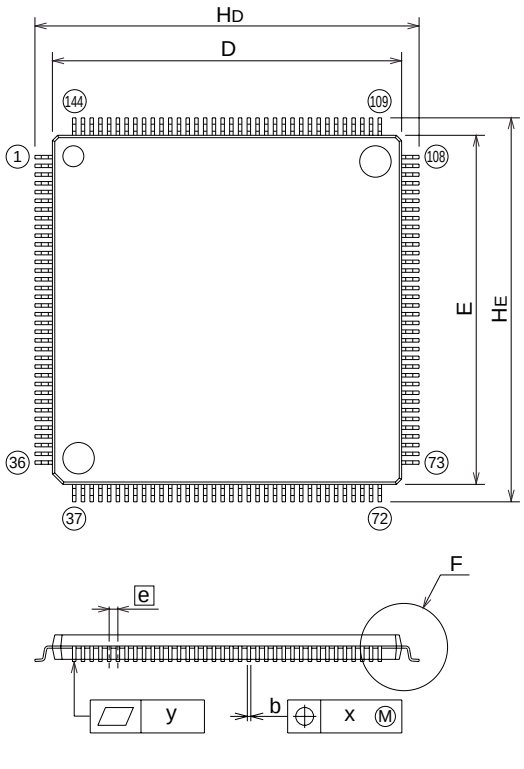
Fig. 42 Timing diagram

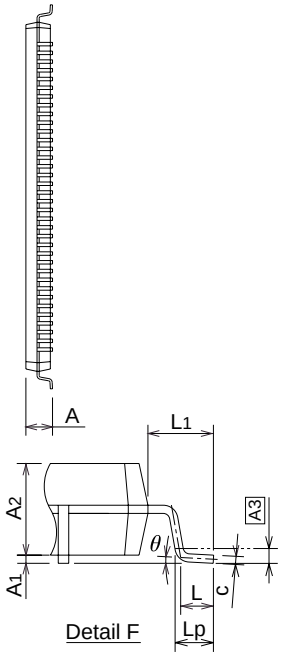
PACKAGE OUTLINE

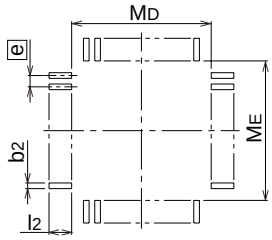
144P6Q-A (MMP)

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–	1.23	Cu Alloy







Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0.05	0.125	0.2
A_2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
L	0.35	0.5	0.65
L_1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.225	–
l_2	0.95	–	–
M_D	–	20.4	–
M_E	–	20.4	–

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

First publication, effective Jan. 2001.
Specifications subject to change without notice.

MITSUBISHI ELECTRIC

REVISION HISTORY	38C8 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.0	01/18/01		First Edition