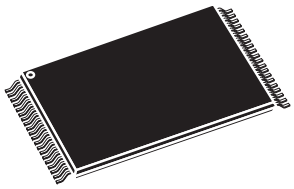
M39432

Single Chip 4 Mbit Flash Memory and 256 Kbit Parallel EEPROM

- Multiple Memories on a Single Chip:
  - 4 Mbit Flash Memory (organised as 8 sectors)
  - 256 Kbit EEPROM
  - 64 Byte One Time Programmable Memory
- CONCURRENT Mode (Read Flash while writing to EEPROM)
- WRITE, PROGRAM and ERASE Status Bits
- 2.7V to 3.6V Single Supply Voltage for PROGRAM, ERASE and READ Operations
- 100 ns Access Time (Flash and EEPROM blocks)
- Low Power Consumption
  - 60 µA Stand-by mode (maximum)
  - Deep Power Down mode: 6 µA (maximum), 200 nA (typical)
- Standard Flash Memory Package
- 100,000 Erase/Write Cycles (minimum)
- 10 Year Data Retention (minimum)



TSOP40 (NC)
10 x 20 mm

DESCRIPTION

The M39432 is a single supply voltage memory device combining Flash memory and EEPROM on a single chip. The memory is mapped in two

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{EE}$	EEPROM Block Enable
$\overline{EF}$	Flash Block Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
R/$\overline{B}$	Ready/$\overline{Busy}$ Output
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

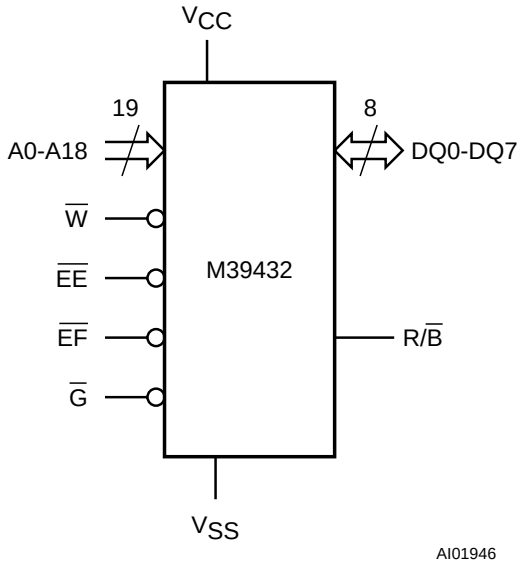
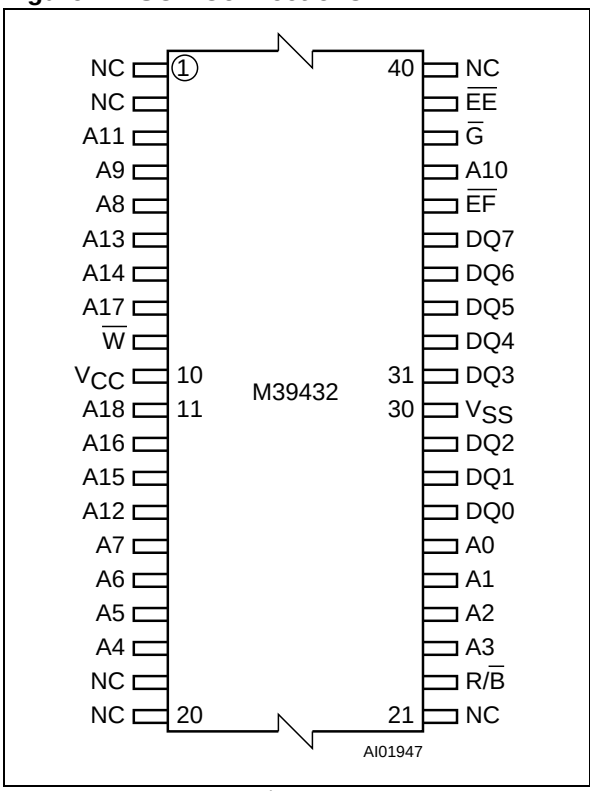


Figure 2. TSOP Connections



Note: 1. NC = Not Connected.

blocks: 4 Mbit of Flash memory and 256 Kbit of EEPROM. Each block operates independently during a Write cycle: in concurrent mode, the Flash Memory can be read while the EEPROM is being written.

There is also a 64 byte row of OTP (one time programmable) EPROM.

The M39432 EEPROM block may be written bytewise or by a page at a time (up to 64 bytes). The integrity of the data can be secured with the help of the Software Data Protection (SDP).

The M39432 Flash Memory block offers 8 sectors, each one 64 KByte in size. Each sector may be erased individually, and programmed a byte at a time. Each sector can be separately protected and unprotected against Program and Erase. Sector erasure may be suspended, while data is read from other sectors of the Flash memory block (or from the EEPROM block), and then resumed. The Flash memory block is functionally compatible with the M29W040 (4 Mbit Single Voltage Flash Memory).

During a Program or Erase cycle in the Flash memory or during a Write cycle in the EEPROM, the status of the M39432 internal logic can be read on the Data Output pins DQ7, DQ6, DQ5 and DQ3.

SIGNAL DESCRIPTION

Address Inputs (A0-A18)

The address inputs for the memory array are latched during a write operation. The EEPROM block is selected by the $\overline{E}$ input, and the Flash memory block the $\overline{F}$ input. A0-A14 access locations in the EEPROM block; A0-A18 access locations in the Flash memory block.

When V_{ID} (as specified in Table 11) is applied on the A9 address input, additional device-specific information can be accessed:

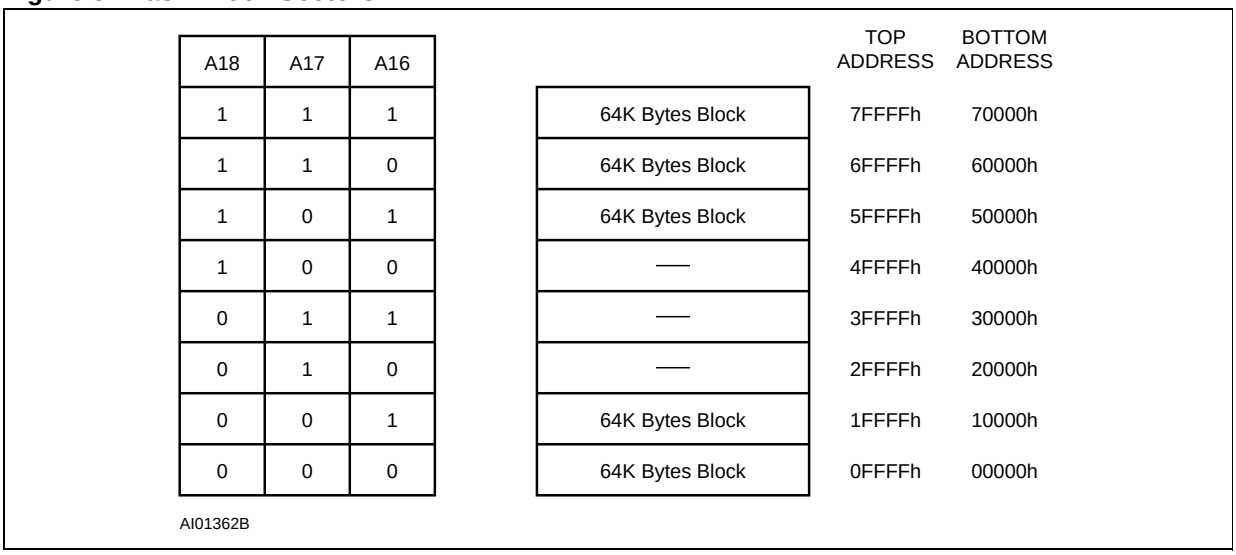
– Read the Manufacturer identifier
– Read the Flash block identifier
– Read/Write the EEPROM block identifier
– Verify the Flash Sector Protection Status.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS} [1]	Temperature Under Bias	–50 to 125	°C
T_{STG} [1]	Storage Temperature	–65 to 150	°C
V_{IO} [1,2]	Input or Output Voltage (except A9)	–0.6 to 7	V
V_{CC} [1]	Supply Voltage	–0.6 to 7	V
V_{A9}, V_G, V_{EF} [1,2]	A9, $\overline{G}$ and $\overline{EF}$ Voltage	–0.6 to 13.5	V

Note: 1. Stresses above those listed may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Please see the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum voltage may undershoot to –2 V, during transition and for less than 20 ns.

Figure 3. Flash Block Sectors



Data Input/Output (DQ0-DQ7)

During a Write operation, one data byte is latched into the device when Write Enable ($\overline{W}$) and one Chip Enable ($\overline{EF}$ or $\overline{EE}$) are driven low.

During a Read operation, the output presented on these pins is valid when Output Enable ($\overline{G}$) and one Chip Enable ($\overline{EF}$ or $\overline{EE}$) are driven low. The output is high impedance when the chip is deselected (both $\overline{EE}$ and $\overline{EF}$ driven high) or the outputs are disabled ($\overline{G}$ driven high).

Read operations are used to output:

– bytes in the Flash memory block
– bytes in the EEPROM block
– the Manufacturer Identifier
– the Flash Sector Protection Status
– the Flash Block Identifier
– the EEPROM Identifier
– the OTP row.

Chip Enable ($\overline{EE}$ and $\overline{EF}$)

Each Chip Enable ($\overline{EE}$ or $\overline{EF}$) causes the memory control logic, input buffers, decoders and sense amplifiers to be activated. When the $\overline{EE}$ input is driven high, the EEPROM memory block is not selected; when the $\overline{EF}$ input is driven high, the Flash memory block is not selected. Attempts to access both EEPROM and Flash blocks ($\overline{EE}$ low and $\overline{EF}$ low) are forbidden. Switching between the two chip enables ($\overline{EE}$ and $\overline{EF}$) must not be made on the same clock cycle, a delay of greater than t_{EHFL} must occur.

The M39432 is in stand-by mode when both $\overline{EF}$ and $\overline{EE}$ are high (when no internal Erase or programming cycle is running). The power consumption is reduced to the stand-by level and the outputs are held in the high state, independent of the Output Enable ($\overline{G}$) or Write Enable ($\overline{W}$) inputs.

After 150 ns of inactivity, and when the addresses are driven at CMOS levels, the chip automatically enters a pseudo-stand-by mode. Power consumption is reduced to the CMOS stand-by level, while the outputs continue to drive the bus.

Output Enable ($\overline{G}$)

The Output Enable gates the outputs through the data buffers during a Read operation. The data outputs are left floating in their high impedance state when the Output Enable ($\overline{G}$) is high.

During Sector Protect (Figure 8) and Sector Unprotect (Figure 9) operations (for the Flash memory block only), the $\overline{G}$ input must be held at V_{ID} (as specified in Table 11).

Write Enable ($\overline{W}$)

Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

Ready/$\overline{Busy}$ (R/$\overline{B}$)

When the EEPROM block is engaged in an internal Write cycle, the Ready/Busy output shows the status of the device:

– R/$\overline{B}$ is 0 when a Write cycle is in progress
– R/$\overline{B}$ is Hi-Z when no Write cycle is in progress

The Ready/$\overline{Busy}$ pin does not show the status of a Program or Erase cycle in the Flash memory.

This pin can be used to show the status of the EEPROM block, even when reading data (or fetching instructions) from the Flash memory block.

Table 3. Operations

Operation	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read from Flash Block
	V_{IH}	V_{IL}			Read from EEPROM Block
Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Write to Flash Block
	V_{IH}	V_{IL}			Write to EEPROM Block
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
	V_{IH}	V_{IL}			
Stand-by	V_{IH}	V_{IH}	X	X	Hi-Z

Note: 1. X = V_{IH} or V_{IL}.

This open drain output can be wire-ORed, using an external pull-up resistor, when several M39xxx devices are used together.

V_{CC} Supply Voltage

The V_{CC} Supply Voltage supplies the power for the device. The M39432 cannot be written when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and during power surges.

A 100 nF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin, to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

V_{SS} Ground

The V_{SS} Ground is the reference for all voltage measurements.

DEVICE OPERATION

The M39432 memory device is addressed via 19 inputs (A0-A18) and carries data on 8 Data Inputs/ Outputs (DQ0-DQ7). There are four other control inputs: Chip Enable EEPROM ($\overline{EE}$), Chip Enable Flash Memory ($\overline{EF}$), Output Enable ($\overline{E}$) and Write Enable ($\overline{W}$).

The Chip Enable inputs ($\overline{EF}$ or $\overline{EE}$) are used mainly for power control (turning the chip on and off) and for block selection (selecting the EEPROM block or the Flash memory block). The gating of data to the DQ0-DQ7 pins should be controlled using the Output Enable input ($\overline{G}$).

The permitted operating modes of the device are listed in Table 3.

Read

For a Read operation, the Output Enable ($\overline{G}$) and one Chip Enable ($\overline{EF}$ or $\overline{EE}$) must be driven low.

As noted on the previous page, Read operations are used to read the contents of:

– bytes in the Flash memory block
– bytes in the EEPROM block
– the Manufacturer Identifier
– the Flash Sector Protection Status
– the Flash Block Identifier
– the EEPROM Identifier
– the OTP row.

The instruction sequences for selecting between these areas is summarized in Table 4.

Write

Writing data requires:

– a Chip Enable (either $\overline{EE}$ or $\overline{EF}$) to be low
– the Write Enable ($\overline{W}$) to be low and the Output Enable ($\overline{G}$) to be high.

Addresses in the Flash memory block (or the EEPROM block) are latched on the falling edge of $\overline{W}$ or $\overline{EF}$ (or $\overline{EE}$) whichever occurs the later. The data to be written to the Flash memory block (or EEPROM block) is latched on the rising edge of $\overline{W}$ or $\overline{EF}$ (or $\overline{EE}$) whichever occurs first.

The Write operation is used in two contexts:

– to write data to the EEPROM memory block
– to enter the sequence of bytes that makes up one of the instructions shown in Table 4.

The programming of a byte of Flash memory involves one of these instructions (as described in the section entitled “Instructions” on this page).

Specific Read and Write Operations

Device specific information includes the following:

– Read the Manufacturer Identifier
– Read the Device Identifier
– Define the Flash Sector Protection
– Read the EEPROM Identifier
– Write the EEPROM Identifier

Table 4. Instructions [1]

Instruction	$\overline{EE}$	$\overline{EF}$	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
Read Manufacturer Identifier [2]	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) set to (0,0,0)			
Read Flash Identifier [2]	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) set to (1,0,0)			
Read OTP Row	0	1	AAh @5555h	55h @2AAAh	90h @5555h	Read Byte 1	Read Byte 2		Read Byte N
Read Sector Protection Status[2]	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) set to (0,1,0)			
Program a Byte of Flash Memory	1	0	AAh @5555h	55h @2AAAh	A0h @5555h	Data @ Address			
Erase a Sector of Flash Memory	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	30h @ Sector address	30h @ Sector address[3]
Erase the Whole of Flash Memory	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	10h @5555h	
Suspend Sector Erase	1	0	B0h @any address						
Resume Sector Erase	1	0	30h @any address						
EEPROM Power Down	0	1	AAh @5555h	55h @2AAAh	30h @5555h				
Deep Power Down	1	0	20h @5555h						
SDP Enable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	A0h @5555h	Write Byte 1	Write Byte 2		Write Byte N
SDP Disable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	20h @5555h	
Write OTP Row	0	1	AAh @5555h	55h @2AAAh	B0h @5555h	Write Byte 1	Write Byte 2		Write Byte N
Return (from OTP Read or EEPROM Power Down)	0	1	F0h @any address						
Reset	1	0	AAh @5555h	55h @2AAAh	F0h @any address				
Reset (short instruction)	1	0	F0h @any address						

Note: 1. AAh @ 5555h means “Write the value AAh at the address 5555h”.
2. This instruction can also be performed as a Verify operation with A9=V_{ID} (please see the section entitled “Flash Sector Protection and Unprotection” on page 18).
3. Addresses of additional sectors to be erased must be entered within a time-out of 80 µs of each other.

Table 5. Device Identifier Operations

Instruction	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Address Lines	DQ0 - DQ7
Read Manufacturer Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Read Flash Block Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	0E3h
Read EEPROM Block Identifier	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	V_{ID}	Don't Care	64 user-defined bytes

Note: 1. X = Don't Care.

To access these, A9 is held at V_{ID} (as specified in Table 11) and the specific logic levels, shown in Table 5, are applied to the address inputs A0, A1 and A6.

The OTP row is accessed with a specific software sequence, as described in the section entitled "Writing the OTP Row" on page 11.

Instructions

Instructions consist of a sequence of specific Write operations, as summarized in Table 4. The time between two consecutive bytes must be shorter than the time-out value (t_{WLWL}).

Each received byte is decoded sequentially, and not executed as a standard Write operation. The overall instruction is executed when the correct number of bytes have been properly received.

The sequence must be followed exactly. If an invalid combination of instruction bytes occurs, or time-out between two consecutive bytes, the device logic resets itself to the Read state, when addressing the Flash block, or is directly decoded as a single operation, when addressing the EEPROM block.

The M39432 instructions set, as summarized in Table 4, includes:

- Program a byte in the Flash memory block
- Read the Protection Status of a Flash Sector
- Erase instructions:
  - Flash Sector Erase
  - Flash Block Erase
  - Flash Sector Erase Suspend
  - Flash Sector Erase Resume
- EEPROM Power Down
- Deep Power Down
- Change the EEPROM software write protection:
  - Enable SDP
  - Disable SDP
- OTP row access:
  - Write the whole OTP row (once)
  - Read from the OTP row
- Reset and Return
- Read identifiers:
  - Read the Manufacturer Identifier
  - Read the Flash Block Identifier

For efficiency, each instruction consists of a two-byte escape sequence, followed by a command byte or a confirmation byte. The escape sequence consists of writing the value AAh at address 5555h, in the first cycle, and the value 55h at address 2AAAh, in the second cycle.

In the case of the Erase instructions, an additional escape sequence is required, for final confirmation that the instruction is the intended one.

POWER SUPPLY AND CURRENT CONSUMPTION

Power Up

The M39432 internal logic is reset, to Read mode, upon a power-up event. All Write operations to the EEPROM are inhibited for the first 5 ms.

No new Write cycles can be started when V_{CC} is below V_{LKO} (as specified in Table 11). However, for maximum security of the contents of the memory, and to remove the possibility of a byte being written on the first rising edge of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$, at least one of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$ should be tied to V_{IH} during the power-up process.

Stand-by

When both $\overline{EE}$ and $\overline{EF}$ are high, the memory enters Stand-by mode, and the Data Input/Output pins are placed in the high-impedance state. To reduce the Supply Current to the Stand-by Supply Current, $\overline{EE}$ and $\overline{EF}$ should be held within V_{CC}±0.2V.

If the Stand-by mode is set during a Program or Erase cycle, the memory continues to use the Supply Current until the cycle is complete.

Table 6. Status Bits

	$\overline{EF}$	$\overline{EE}$	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash	V_{IL}	V_{IH}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-Out	X	X	X
EEPROM	V_{IH}	V_{IL}	Data Polling	Toggle Flag	X	X	X	X	X	X

Note: 1. X = Not a guaranteed value, can be read either as '1' or '0'.

Automatic Stand-by

If CMOS levels (V_{CC}±0.2V) are used to drive the bus, and the bus is inactive for more than 150 ns, the memory enters the Automatic Stand-by state. The internal supply current is reduced to the Stand-by Supply Current, I_{CC3}.

Deep Power Down

The I_{CC} consumption mode can be reduced to a minimum using the Deep Power Down instruction (as shown in Table 4). The device is set in a sleep mode until the next Reset instruction is executed.

EEPROM Power Down

The M39432 can power-down the EEPROM block using the specific instruction shown in Table 4. Once in this state, the EEPROM block is no longer accessible, until a Return instruction is executed.

READ

Read operations and instructions can be used:

– to read the contents of the memory array (Flash memory block or EEPROM block)

– to read the memory array status and identifiers (Flash memory block or EEPROM block).

Read Data (from Flash Memory or EEPROM)

For a Read operation, the Output Enable ($\overline{G}$) and one Chip Enable ($\overline{EF}$ or $\overline{EE}$) must be driven low.

Read the Manufacturer Identifier

There are two alternative methods for reading the Manufacturer Identifier: using a Read operation or using a Read instruction.

Read Operation. The Manufacturer Identifier can be read with a Read operation by applying V_{ID} (as specified in Table 11) on A9, and the logic levels specified in Table 5 applied to A0, A1, A6.

Read Instruction. The Manufacturer Identifier can also be read using an instruction composed of four operations: three specific Write operations (as specified in Table 4) and a Read operation. This either accesses the Manufacturer Identifier, the Flash Block Identifier or the Flash Sector Protection Status, depending on the levels that are being applied to A0, A1, A6, A16, A17 and A18.

Read the Flash Block Identifier

Similarly, there are two alternative methods for reading the Flash Block Identifier (E3h): using a Read operation or using a Read instruction. Please see the previous section, entitled "Read the Manufacturer Identifier", and Table 5 and Table 4 for details.

Read the EEPROM Block Identifier

The EEPROM Block Identifier (64 bytes, user defined) can be read with a single Read operation by holding A6 low and A9 at V_{ID} (see Table 5).

Read the OTP Row

The OTP row is mapped in the EEPROM block. With $\overline{EE}$ held low, and $\overline{EF}$ held high, an EEPROM Read instruction is composed, as specified in

Figure 4. Data Polling Flowchart

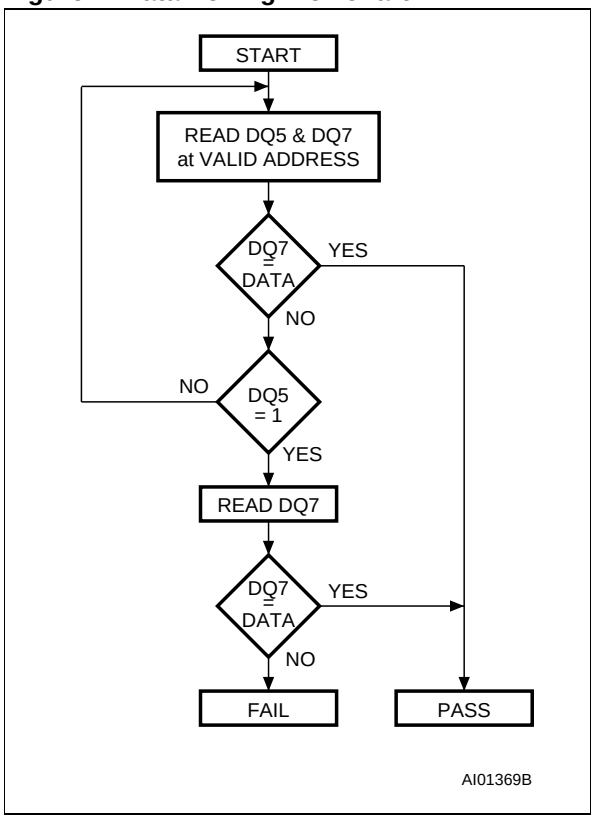


Table 4. This consists of the writing of three specific data bytes at three specific memory locations (each location on a different page) as a prefix to reading the OTP row content.

When accessing the OTP row, only the least significant bits of the address bus (A0 to A6) are decoded (of which A6 must be low).

Each Read of the OTP row has to be followed by the Return instruction (as shown in Table 4).

Read the Flash Sector Protection Status

There are two alternative methods for reading the Flash Sector Protection Status: using a Verify operation with A9=V_{ID} (as described on page 18) or using a Read instruction as described in the section entitled “Read the Manufacturer Identifier”, starting on page 7.

Using the Read instruction, the logic levels on A0, A1, A6 select the correct instruction, while A16, A17 and A18 specify which sector is being addressed. This returns the value 01h if the Flash sector is protected, and the value 00h if the Flash sector is not protected.

Read the Status Bits

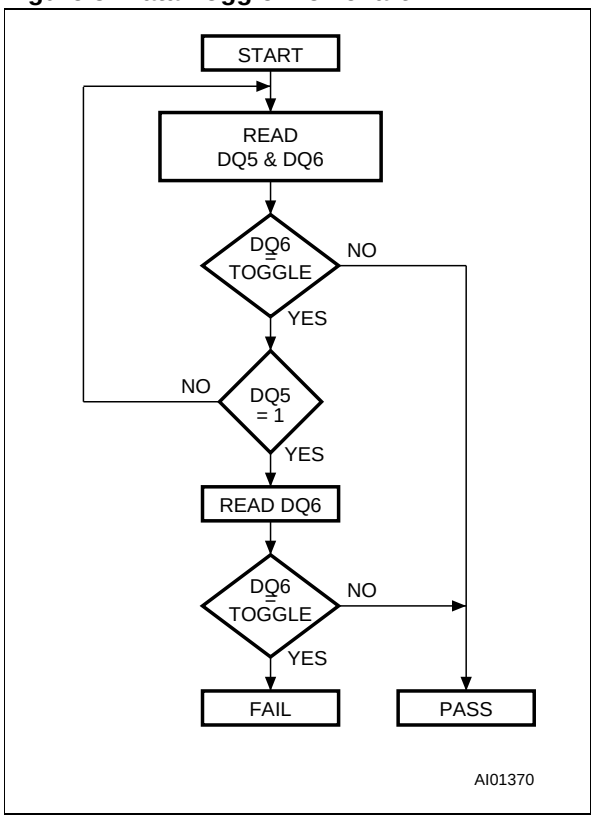
The latency period of Write, Erase and Program cycles can be monitored by the application software, by using the M39432 status bits. The Ready/Busy pin provides the status information during a write cycle to the EEPROM block (though not to the Flash memory block). An internal status register carries the status information during a programming or erase cycle. A Read operation, during the program or write cycle, causes the contents of this register to be presented to the I/O ports (DQ0-DQ7), as summarized in Table 6.

Data Polling flag, DQ7. The I/O lines (DQ0-DQ7) are first used as inputs, carrying the data that is to be written to the EEPROM or programmed in the Flash memory. Once the Write or Program cycle is underway, these lines become outputs (and can be read using a normal Read operation). The value presented on DQ7 is the inverse of the data bit that was presented by the user. When the cycle is complete, the lines remain as outputs, and the value that is presented on DQ7 is the non-inverted value that was originally specified for writing.

The suitable algorithm for using this method of polling is shown in Figure 4. When a Write or Program cycle is in progress, data bit DQ7 is set to the complement of the original data bit 7 (or to ‘0’ in the case of an Erase cycle in the Flash memory block). When DQ7 is identical to the old data (or to ‘1’ in the case of an Erase cycle in the Flash memory block) and the Error bit (DQ5) is still ’0’, the cycle is complete.

For the flash memory block, data Polling is effective after the fourth pulse on the $\overline{W}$ line for Program cycles, and after the sixth pulse on the $\overline{W}$ line for Erase cycles. The Data Polling Read instruction must address the same location as the byte that is being programmed, or within the same Flash sector as the one that is being erased.

Figure 5. Data Toggle Flowchart



Toggle flag, DQ6. During an internal Write, Program or Erase cycle, DQ6 toggles between ’0’ and ’1’, on successive Read accesses to any byte of the memory (when either $\overline{G}$, $\overline{EE}$ or $\overline{EF}$ is held low).

When the internal cycle is complete, the toggling is stopped, and the data read on DQ0-DQ7 is that of the addressed memory byte. A subsequent Reading at the same address will result in the same data being read.

This alternative method for detecting when the internal Write, Program or Erase cycle has completed, is shown in the flowchart in Figure 5. When an internal cycle is in progress, data bit DQ6 toggles between ‘1’ and ‘0’ for successive Read operations. When DQ6 no longer toggles and the Error bit DQ5 is ’0’, the operation is complete. To determine if DQ6 has toggled, each poll requires two consecutive Read operations to see if the data read is the same each time.

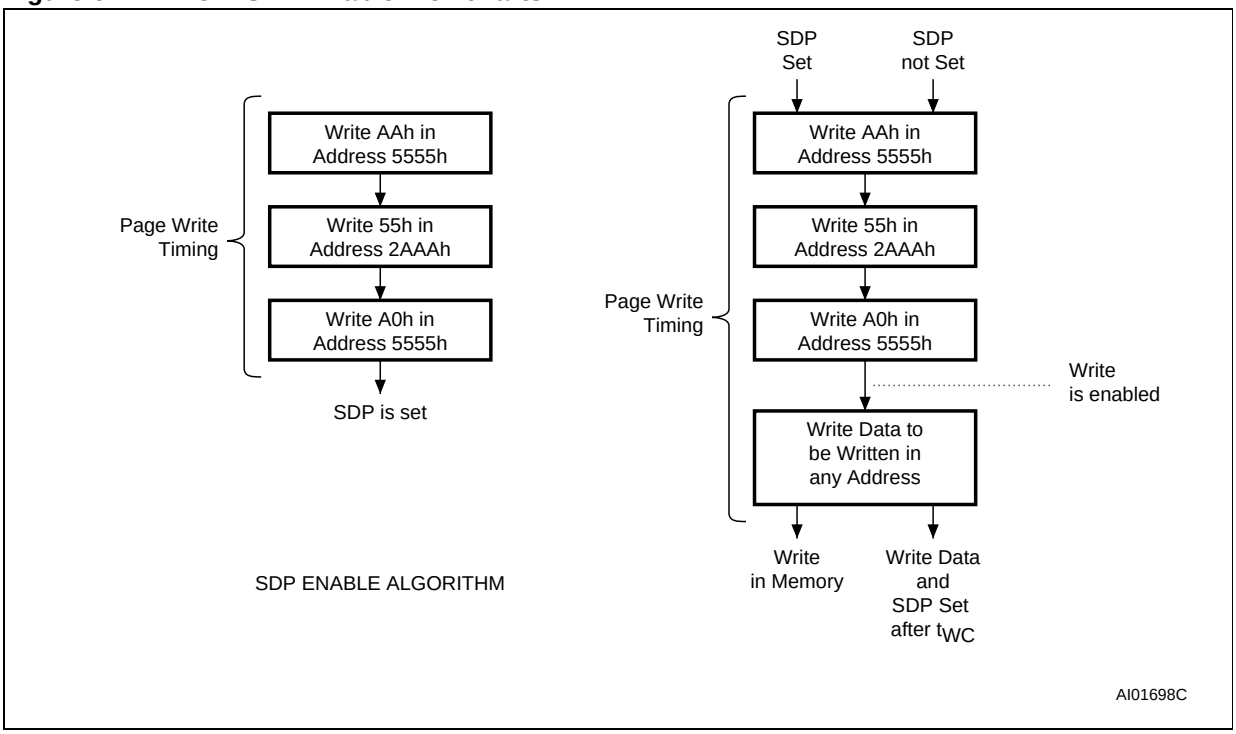
For the flash memory block, data Toggling is effective after the fourth pulse on the $\overline{W}$ line for

Table 7. Summary of the Use of Status Bits

Operation	Address	DQ7 (Data Polling Bit)	DQ6 (Toggle Bit)	DQ5 (Program Error Bit)	DQ3 (Erase Time-Out Bit)
Program (Flash) or Erase (EEPROM)	Any address	$\overline{DQ7}$	Toggling	0	X
Program Error (Flash)	Any address in the Flash block	$\overline{DQ7}$	Toggling	1	X
Flash Block Erase	Any address in the Flash block	0 [1]	Toggling [2]	0	1
Sector Erase	Sector address to be erased	0 [1]	Toggling [2]	0	1
Sector Erase before Time-Out	Sector address to be erased	0 [1]	Toggling [2]	0	0
Erase Suspend	Any byte in the sector in erase mode	Invalid data on DQ7-DQ0			
	Other sector addresses	DQ6 toggles for 15 µs, then behaves as for a standard Read operaion			
Erase Error	Sector address	0 [1]	Toggling [2]	1	1

Note: 1. If all the sectors to be erased are protected, DQ7 is reset to 0 for about 100 µs, then returns to the state it was in for the previously addressed byte. No erasure is performed.
2. If all the sectors to be erased are protected, DQ6 is reset to 0 for about 100 µs, then returns to the state it was in for the previously addressed byte. No erasure is performed.

Figure 6. EEPROM SDP-Enable Flowcharts



Program cycles, and after the sixth pulse on the $\overline{W}$ line for Erase cycles.

Error flag, DQ5 (Flash memory block only). This bit is set to '1' when there is a failure during a Program, Sector Erase, or the Bulk Erase instruction in the Flash memory block. Otherwise, the bit is held at '0'.

If an error occurs during a Program or Sector Erase instruction, the sector in which the error occurred, must not be used any more. Other sectors may still be used, though. The Error bit is reset after a Reset instruction.

If DQ5 becomes set to '1' during either of the polling algorithm, shown in Figure 4 and Figure 5, DQ7 (DQ6) should be checked again in case it had changed simultaneously with DQ5. If DQ7 shows the original data bit (after a Program cycle) or if DQ7 is set to '1' (after an Erase cycle), or if DQ6 has ceased to toggle, the operation is successful and the calling routine can resume normal execution. It is recommended, as a final check, that a second Read be performed, and that the read value be compared against the original data (in the case of a Write or Program cycle) or against the value FFh (in the case of an Erase cycle). If the comparison shows false, this should be flagged as an error.

Erase Time-Out Bit (DQ3). The Erase Time-Out Bit can be used to identify the start of the internal controller operation during a Sector Erase cycle. While the sector addresses (after cycle 5 in Table 4) are being supplied at a faster rate than one every 80 µs between two sector addresses, the M39432 holds the DQ3 bit at 0. This indicates that additional sectors can still be added to the list of sectors that are to be erased. Once the internal controller starts erasing, the Erase Timer Bit is set to '1'.

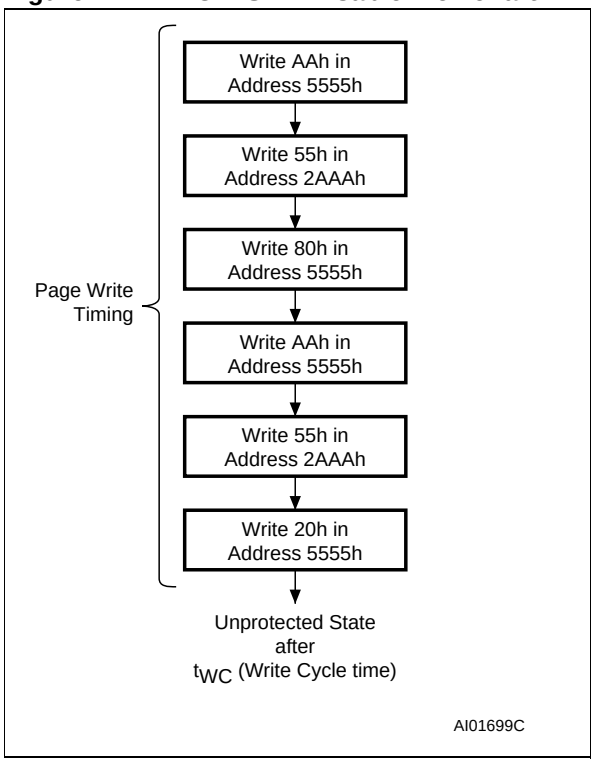
BYTE WRITE (OR PAGE WRITE) IN EEPROM

Writing a byte, or a page of bytes, to the EEPROM block is performed as an operation (see Table 3). This is as opposed to Programming a byte in the Flash memory, which is performed as an instruction (see Table 4).

Byte Write in the EEPROM Block

A write operation is initiated when $\overline{EE}$ is taken low, while $\overline{EF}$ is kept high, the Write Enable ($\overline{W}$) is taken low, and the output enable ($\overline{G}$) is held high. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{EE}$ (whichever occurs the later).

Figure 7. EEPROM SDP-Disable Flowchart



Once initiated, the Write operation continues under internal timing, until it is completed. This period (t_{WHRH}) is specified in Table 16.

The status of the Write operation is indicated on the Data Polling and Toggle bits (as described on the previous page), and on the Ready/Busy output (which is driven low for the duration of the internal Write cycle).

Page Write in the EEPROM Block

The Page Write mode allows up to 64 bytes to be written on a single page in a single go. This is achieved through a series of successive Write operations, no two of which are separated by more than the t_{WLWL} value (as specified in Table 16).

The page write is initiated as a byte write operation: following the first Byte Write instruction, the host may send another address and data with a minimum data transfer rate of: $1/t_{WLWL}$. The internal write cycle can start at any instant after t_{WLWL}. Once initiated, the write operation is internally timed, and continues, uninterrupted, until completion.

Table 8. Write the EEPROM Block Identifier

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A6	A9	Other Address Lines	DQ0 - DQ7
V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	64 user-defined bytes

All bytes must be located on the same page address (A6-A18 must be the same for all bytes). Otherwise, the Page Write operation is not executed.

As with the single byte Write operation, described above, the DQ6 and DQ7 lines can be used to detect the beginning and end of the internally controlled phase of the Page Write cycle.

EEPROM Block Software Data Protection

The Software Data Protection (SDP) instruction protects the EEPROM block from inadvertent Write operations, for example that might be caused under uncontrolled bus conditions.

By default, the M39432 is shipped in the unprotected state: the EEPROM memory can be written to normally. After the SDP Enable instruction, the device enters the Protected Mode, and further write operations have no effect on the EEPROM contents.

The device remains in this mode until a valid SDP Disable instruction has been received. The device then returns to its unprotected state.

To enable the Software Data Protection, the device has to be written (under Page Write timing conditions) with three specific data bytes at three specific memory locations (each location on a different page) as shown in Table 4 and Figure 6.

Figure 6 shows that there are three ways to use the SDP-Enable instruction. Firstly, as shown in the flow-chart on the left, it can be used as a three-byte instruction that sets the SDP. Secondly, it can be used as a way of writing data to the EEPROM even when the SDP is set. Only if the data to be written is preceeded by the correct three byte instruction, and all the bytes are written with the correct Page Write timing, will the request be accepted, and acted on. Lastly, if the SDP is currently not set, the instruction can be used as a means of performing a Page Write, and setting the SDP at the same time.

To disable the Software Data Protection the user has to write specific data bytes into six different locations (under Page Write timing conditions) with different bytes being written on different pages, as shown in Figure 7.

The Software Data Protection state is held internally in a non-volatile latch (and so the state is remembered across power-on and power-off events. Access to this latch, through the SDP Enable and Disable instructions, require the same write time (t_{WC}) as for the non-volatile memory. This Write operation can be monitored on the Toggle bit (status bit DQ6) and the Ready/Busy pin, but not on DQ7. The Ready/Busy output is driven low from the first written byte (the first Write AAh,@5555h of the SDP sequence) until the completion of the internal Page Write sequence.

Writing the OTP Row

Writing in the OTP row is enabled by an instruction composed of three specific Write operations, under Page Write timing conditions, as shown in Table 4. These instructions write data bytes at three specific memory locations, each location on a different page, followed by the data (between 1 and 64 bytes) that is to be stored in the OTP row.

This action can only be performed once. Even by writing fewer than all 64 bytes on the first write to the OTP row, none of the bytes, including any that have not yet been changed, can be modified at a later time.

When accessing the OTP row, the only least significant address bits (A0 to A6) are decoded. Of these, A6 must be held at 0.

Writing the EEPROM Block Identifier

The EEPROM Block Identifier (64 bytes) can be written with a single Write operation with V_{ID} applied on A9, and A6 is driven low, as shown in Table 8.

Programming the Flash Block

Programming a byte in the Flash memory block is performed using the instruction shown in Table 4. This is different to writing data to the EEPROM block, which is performed as an operation (as shown in Table 3). Similarly, an instruction is needed when erasing a sector of Flash memory.

The Program instruction is a sequence of three specific Write operations, followed by a Write operation bearing the address and data that is to be written (as shown in Table 4). The M39432 automatically starts and performs the programming after the fourth write operation. In this way, the Flash memory block can be programmed a byte at a time.

The Flash memory block rejects any further instructions that arrive during the execution of the Program instruction. During programming, the memory status may be checked by reading the status bits DQ7, DQ6 and DQ5, as described on page 8.

Data Polling using DQ7. Please see the description on page 8.

Data Toggling using DQ6. Please see the description on page 8.

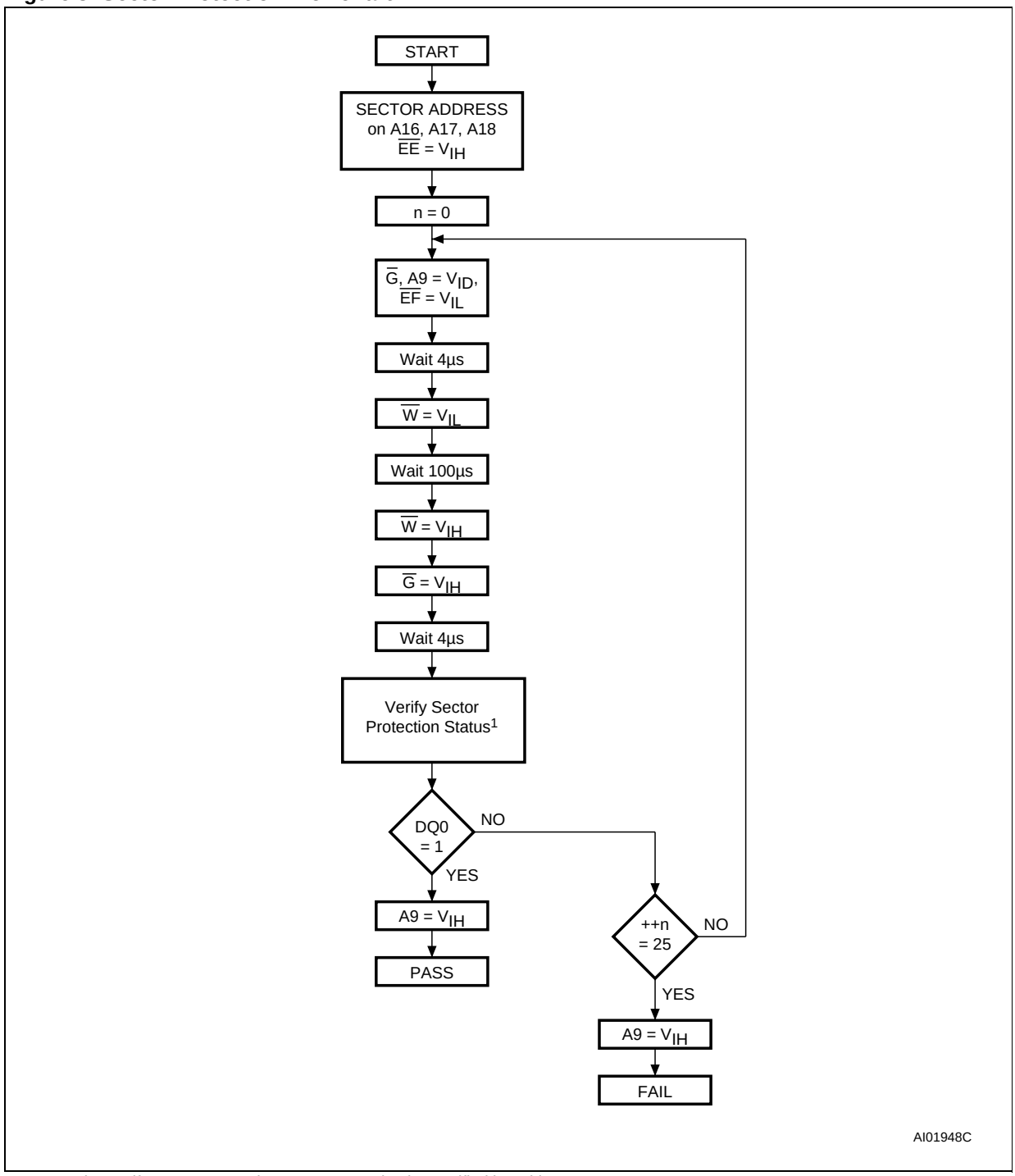
Flash Block Erase

A Write to the EEPROM block is an operation that triggers an automatic, internal sequence of Byte Erase followed by Byte Write.

The Flash memory block, though, is different. Writing to the Flash memory block first requires an explicit Erase operation.

The Flash memory Erase instruction cannot be addressed to a byte at a time. The Erase can only

Figure 8. Sector Protection Flowchart



Note: 1. The Verify Sector Protection Status operation is specified in Table 9.

Table 9. Flash Sector Protection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	A18	DQ0 - DQ7
V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	X	SA	SA	SA	Protection Activation
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	X	SA	SA	SA	Verify Sector Protection Status: when DQ0=1, the sector is protected

Note: 1. X = Don't Care
2. SA = Sector address

be addressed to a whole sector. Either one sector (or more) can be explicitly selected for erasure, or the Bulk Erase instruction can be used to erase all the sectors in the Flash memory block.

During an Erase cycle, the memory status may be checked by reading the status bits DQ7, DQ6 and DQ5, as described on page 8. The Error bit (DQ5) returns a '1' if there has been an Erase Failure (if the maximum number of Erase cycles has been exceeded).

The Program instruction to a byte in the Flash memory block is ignored if it is in a protected sector. Similarly, the Bulk Erase instruction is ignored if all the Flash memory sectors are protected.

If all the addressed sectors, for an Erase instruction, are protected, nothing is erased. DQ7 and DQ6 are set to '0' for about 100 µs, and then are returned to their values from the previously addressed byte.

Bulk Erase Instruction. The Bulk Erase instruction uses six Write operations followed by a number of Read operations, to read the status register bits. This is summarized in Table 4. If any part of the Bulk Erase instruction sequence is wrong, the device reverts to being in its Read mode for the Flash memory, and does not execute the erase instruction.

The M39432 rejects any further instructions that arrive during the execution of the Bulk Erase instruction.

Sector Erase Instruction. The Sector Erase instruction uses six Write operations to specify the first sector that is to be erased, and an additional Write operation for each additional sector that is to be erased in parallel with the first. This is summarized in Table 4. These Write operations are transmitted under normal Page Write timing conditions.

The status of the internal timer can be monitored on DQ3 (Erase Time-Out bit) as described on page 10. If DQ3 is '0' the Sector Erase instruction has been received and the timer is counting. If DQ3 is '1', the time-out has expired, and the M39432 is either in the process of erasing, or has finished (as indicated on DQ7 and DQ6).

Any instruction arriving before the expiration of the Erase Time-Out period, other than Erase Suspend or Erase Resume instruction, aborts the Erase instruction, and resets the device in its read Flash memory mode.

During the execution of the Erase instruction, the Flash memory block accepts only Reset and Erase Suspend instructions.

Erase Suspend Instruction. When a Sector Erase cycle is in progress, the Erase Suspend instruction can be used to suspend the cycle. This allows the reading of data from another Flash sector while the Sector Erase instruction is on hold.

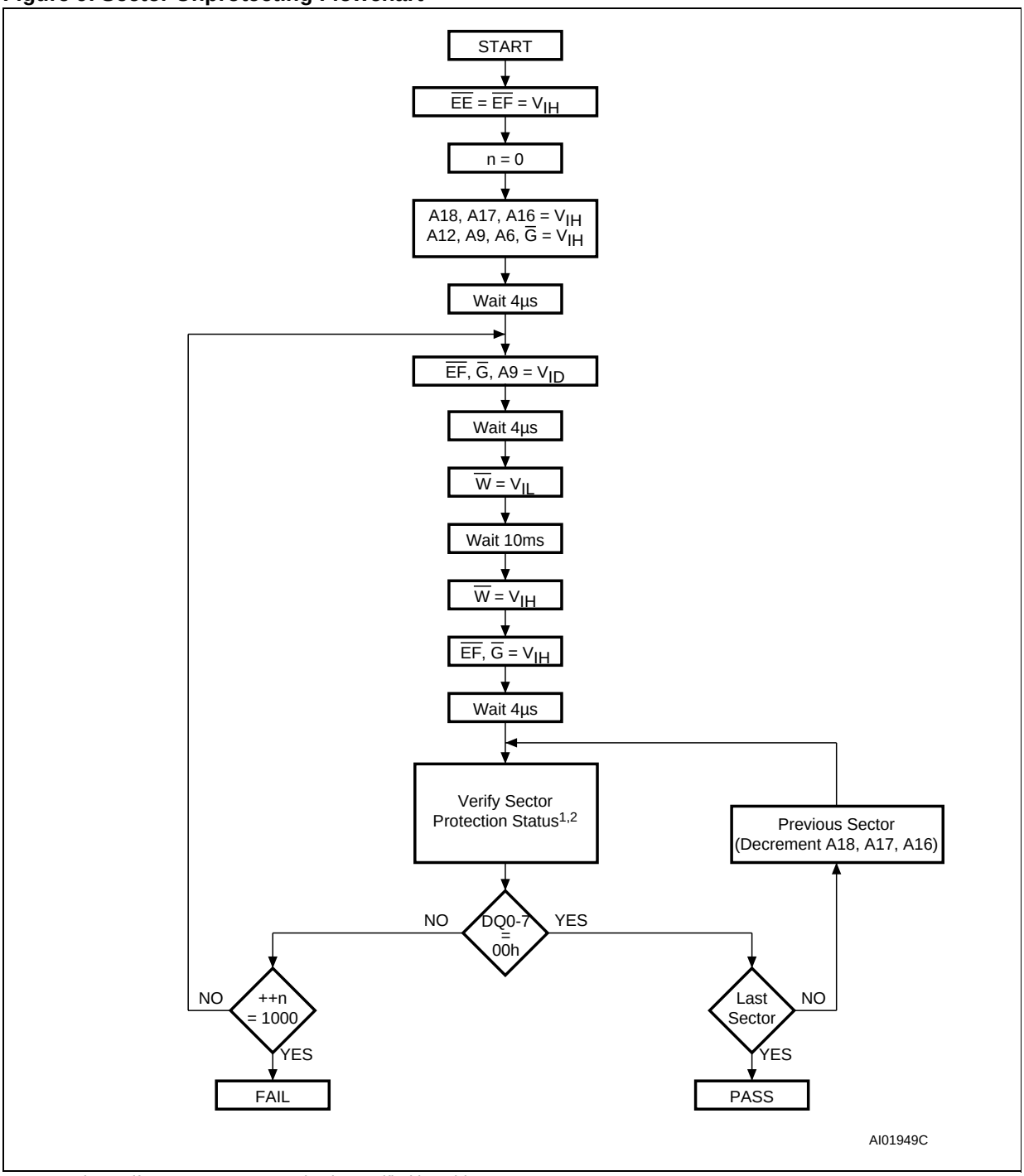
This instruction involves writing B0h at any address (as shown in Table 4). Erase Suspend is accepted only during the Sector Erase instruction execution, and defaults to the Read Flash memory mode, otherwise. An Erase Suspend instruction executed during an Erase Time-Out will, in addition to suspending the Erase, terminate the time-out period.

Table 10. Flash Unprotection (all sectors)

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	A18	DQ0 - DQ7
V_{ID}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	Activation of Unprotected mode
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	X	SA	SA	SA	Verify Sector Protection Status: when 00h, the sector is unprotected

Note: 1. X = Don't Care
2. SA = Sector address

Figure 9. Sector Unprotecting Flowchart



Note: 1. The Verify Sector Status operation is specified in Table 10.
2. A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

Table 11. DC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 2.7 V to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Mean[2] (Typ.)	Max.	Unit
I_{LI}	Input Leakage Current	0 V ≤ V_{IN} ≤ V_{CC}			± 1	µA
I_{LO}	Output Leakage Current	0 V ≤ V_{OUT} ≤ V_{CC}			± 1	µA
I_{CC1}[1]	Supply Current (Read Flash) TTL	($\overline{EE}$,$\overline{EF}$,$\overline{G}$) = (V_{IH},V_{IL},V_{IH}), f = 6 MHz		3	15	mA
I_{CC2}	Supply Current (Read EEPROM) TTL	($\overline{EE}$,$\overline{EF}$,$\overline{G}$) = (V_{IL},V_{IH},V_{IH}), f = 6 MHz		3	15	mA
I_{CC3}	Supply Current (Stand-by) CMOS	$\overline{EF}$ = $\overline{EE}$ = V_{CC} ± 0.2 V			60	µA
I_{CC4}	Supply Current (Flash block Program or Erase)	Byte program, Sector or Chip Erase in progress		3	20	mA
I_{CC5}	Supply Current (EEPROM Write)	During t_{WC}		3	20	mA
I_{CC6}	Supply Current in Deep Power Down Mode	After a Deep Power Down instruction (see Table 4)		0.2	6	µA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC} – 0.4			V
V_{ID}	A9 High Voltage		11.5		12.5	V
I_{ID}	V_{ID} Current	A9 = V_{ID}			50	µA
V_{LKO}	V_{CC} minimum for Write, Erase and Program		1.9		2.2	V

Note: 1. When reading the Flash block and an EEPROM write cycle is already underway, the supply current is I_{CC1} + I_{CC5}.
2. Averaged (over time) typical value.

Table 12. AC Measurement Conditions

Input Rise and Fall Times	≤ 10 ns
Input Pulse Voltages	0.45 V to 2.4 V
Input Timing Reference Voltages	0.8 V and 2 V
Output Timing Reference Voltages	1.5 V

Figure 10. AC Testing Input Output Waveforms

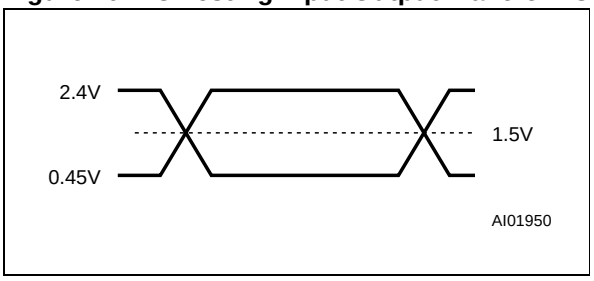


Figure 11. Output AC Testing Load Circuit

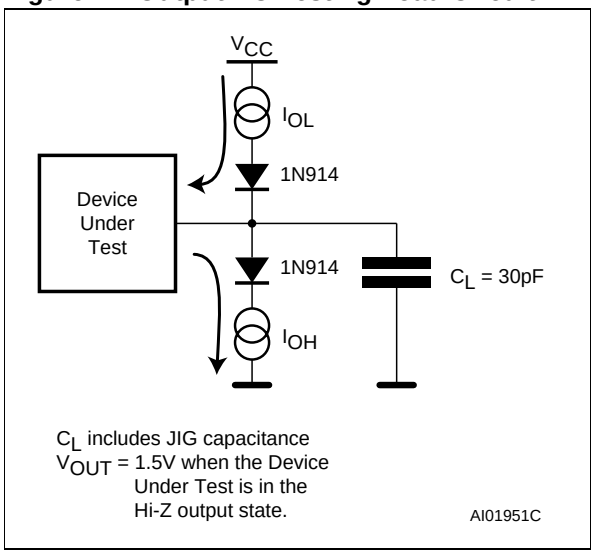


Table 13. Read Mode AC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 2.7 V to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M39432						Unit
				-100		-120		-150		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	($\overline{E}$,$\overline{EF}$,$\overline{G}$) = (V_{IL},V_{IH},V_{IL}) or ($\overline{E}$,$\overline{EF}$,$\overline{G}$) = (V_{IH},V_{IL},V_{IL})	100		120		150		ns
t_{AVQV}	t_{ACC}	Access Time: Address Valid to Output Valid	($\overline{E}$,$\overline{EF}$,$\overline{G}$) = (V_{IL},V_{IH},V_{IL}) or ($\overline{E}$,$\overline{EF}$,$\overline{G}$) = (V_{IH},V_{IL},V_{IL})		100		120		150	ns
t_{ELQX}[1]	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV}[2]	t_{CE}	Access Time: Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX}[1]	t_{OLZ}	Output Enable Low to Output Transition	($\overline{E}$,$\overline{EF}$) = (V_{IL},V_{IH}) or ($\overline{E}$,$\overline{EF}$) = (V_{IH},V_{IL})	0		0		0		ns
t_{GLQV}[2]	t_{OE}	Output Enable Low to Output Valid	($\overline{E}$,$\overline{EF}$) = (V_{IL},V_{IH}) or ($\overline{E}$,$\overline{EF}$) = (V_{IH},V_{IL})		40		55		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ}[1]	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		40		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	($\overline{E}$,$\overline{EF}$) = (V_{IL},V_{IH}) or ($\overline{E}$,$\overline{EF}$) = (V_{IH},V_{IL})	0		0		0		ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	($\overline{E}$,$\overline{EF}$) = (V_{IL},V_{IH}) or ($\overline{E}$,$\overline{EF}$) = (V_{IH},V_{IL})		30		40		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	($\overline{E}$,$\overline{EF}$,$\overline{G}$) = (V_{IL},V_{IH},V_{IL}) or ($\overline{E}$,$\overline{EF}$,$\overline{G}$) = (V_{IH},V_{IL},V_{IL})	0		0		0		ns
t_{EHFL}	t_{CED}	$\overline{E}$ Active to $\overline{EF}$ Active or $\overline{EF}$ Active to $\overline{E}$ Active		100		100		100		ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Table 14. Input and Output Parameters[1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 12. Read Mode AC Waveforms (with Write Enable, $\overline{W}$, high)

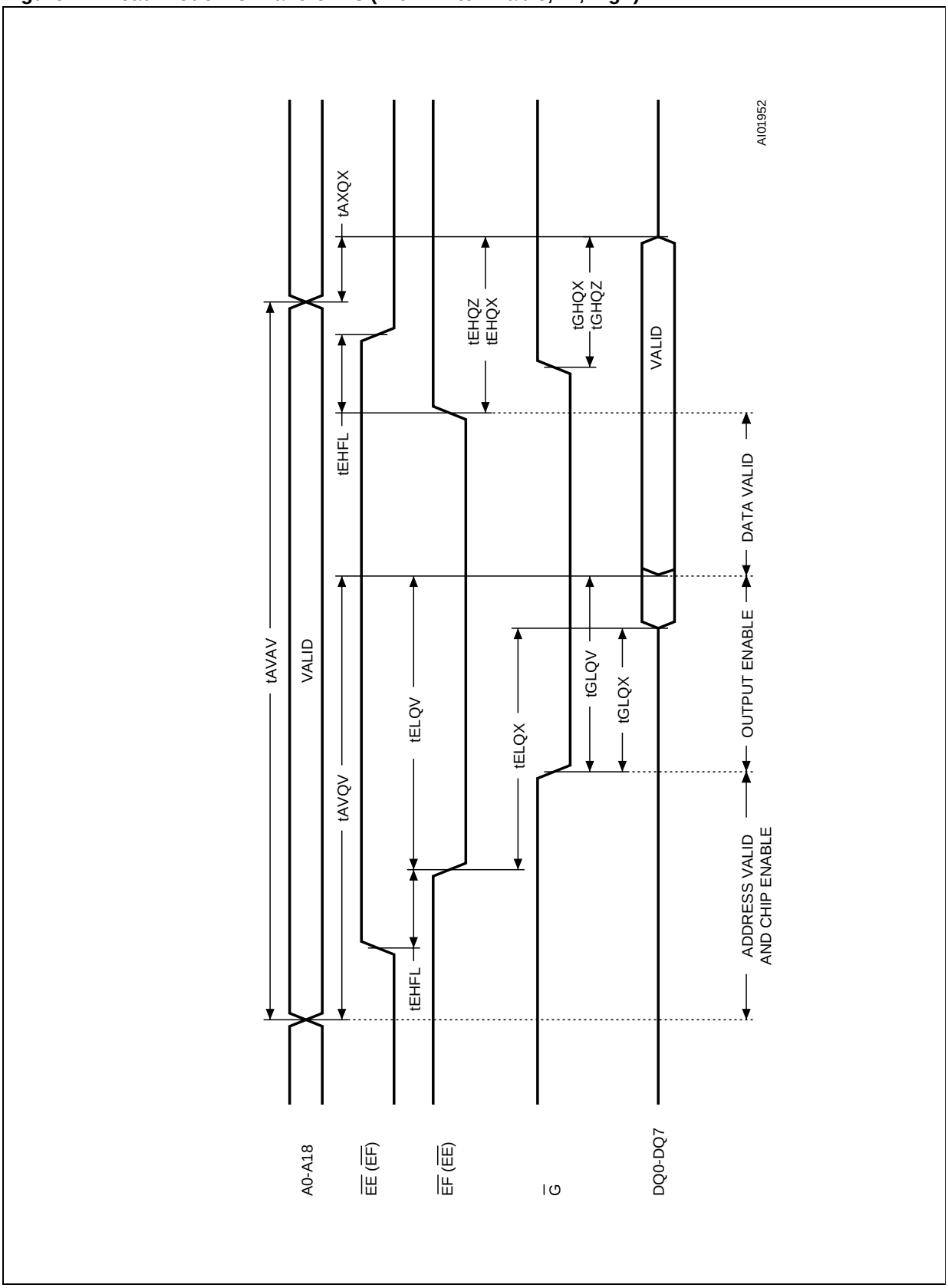
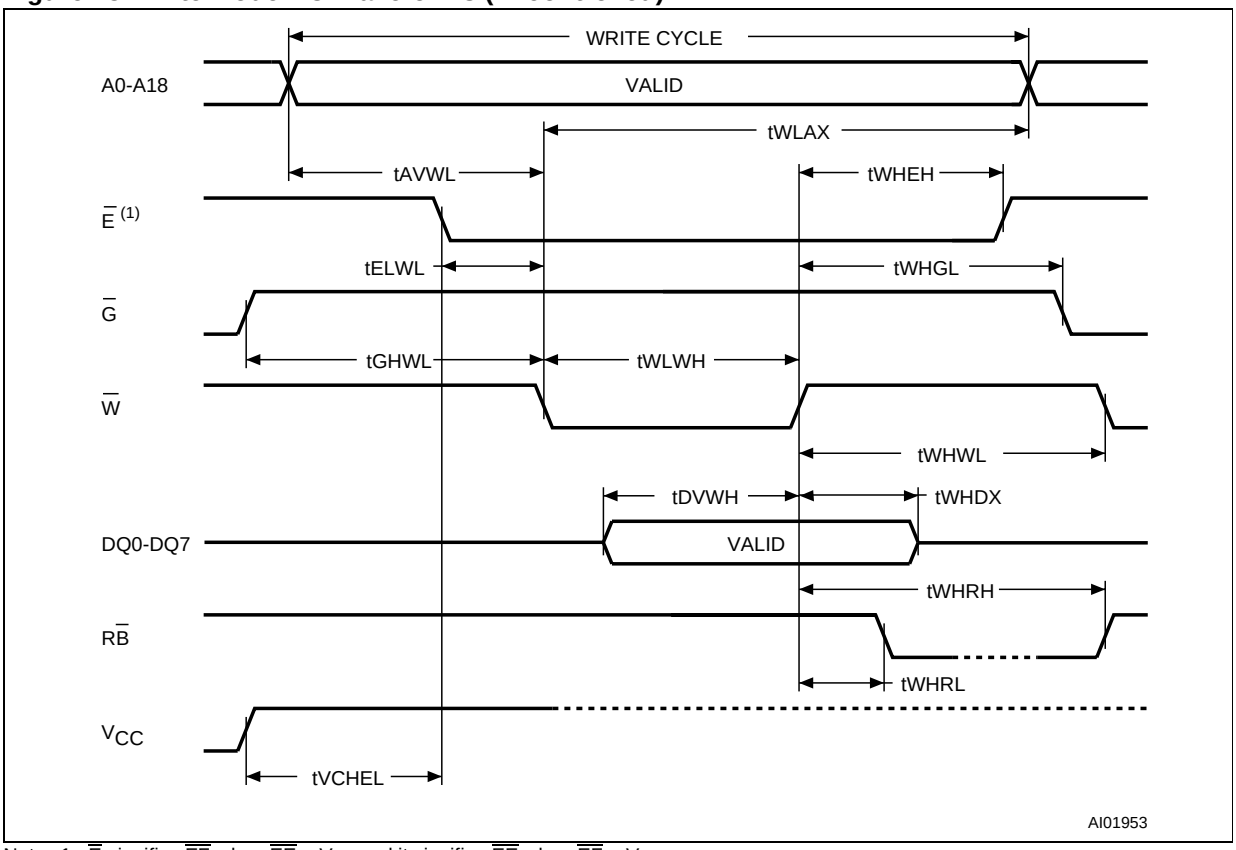


Figure 13. Write Mode AC Waveforms ($\overline{W}$ controlled)



Note: 1. $\overline{E}$ signifies $\overline{EF}$ when $\overline{EE}$ = V_{IH}, and it signifies $\overline{EE}$ when $\overline{EF}$ = V_{IH}.
2. Addresses are latched on the falling edge of $\overline{W}$, Data are latched on the rising edge of $\overline{W}$.

The Toggle bit (DQ6) stops toggling when the Erase cycle is suspended. The Toggle bit status must be monitored using an address that is not in the Flash sector being erased. DQ6 will stop toggling within 15 µs of the Erase Suspend instruction having been sent. The M39432 will then be set automatically into Read Flash Memory mode.

When an Erase cycle is suspended, reading from the Flash sectors that were being erased will return invalid data. Reading is valid from any Flash sectors that are not being erased. During an Erase Suspend cycle, the Flash memory responds only to Erase Resume and Reset instructions.

A Reset instruction will definitively abort the erase cycle, and can leave invalid data in the Flash sectors that was being erased.

Erase Resume Instruction. If an Erase Suspend instruction was the last to have been executed, this instruction allows the Erase cycle to be resumed. The Erase Resume instruction involves writing 30h to any address (as shown in Table 4).

Flash Sector Protection and Unprotection

Each Flash sector can be individually protected against Program or Erase instructions. This mode is activated when both A9 and G are set to V_{ID} (specified in Table 11) and the Flash sector address is applied on A16, A17 and A18, as shown in Figure 8 and Table 9.

Flash Sector Protection is programmed with the help of a specific sequence of levels applied on the $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A16, A17 and A18 lines, as shown in Table 9.

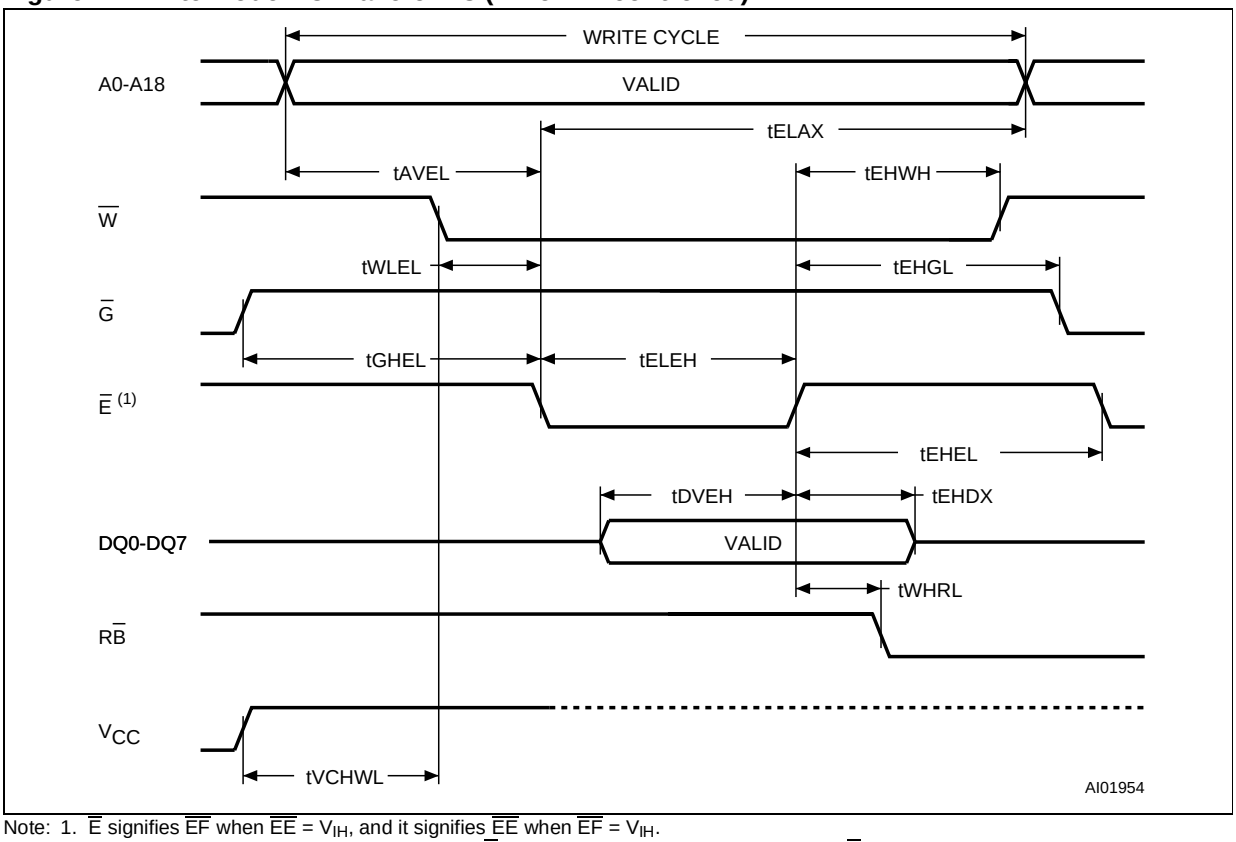
Any attempt to Program or Erase a protected Flash sector is ignored by the device.

Flash sectors can be unprotected, to allow the subsequent updating of their contents. The Sector Unprotection operation unprotects all sectors together (from sector 0 up to sector 7).

The Flash Sector Unprotection operation is invoked by applying the specific levels on the $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A12, A16, A17 and A18 lines, as shown in Table 10.

Verification of the protection status can be obtained after each new sector has been protected, or after all sectors have been

Figure 14. Write Mode AC Waveforms ($\overline{EE}$ or $\overline{EF}$ controlled)



Note: 1. $\overline{E}$ signifies $\overline{EF}$ when $\overline{EE}$ = V_{IH}, and it signifies $\overline{EE}$ when $\overline{EF}$ = V_{IH}.
2. Addresses are latched on the falling edge of $\overline{E}$, Data are latched on the rising edge of $\overline{E}$.

unprotected. Following the protection of a new sector, the status is found on DQ0 as shown by the sequence in Figure 8. Following the unprotection of all sectors, the status is found on DQ0-DQ7 as shown by the sequence in Figure 9.

These two Verify Sector Protection Status operations are implemented like Read operations, but provide a more severe test of the correct functioning of the device than does a Read Sector Protection instruction (as shown in Table 4).

Reset Instruction

Reset is an instruction involving either one write operation or three write operations (as shown in Table 4).

The Reset instruction returns the memory to its Read mode, and resets any errors in the Status Register. If the Reset instruction is issued during a Sector Erase cycle, or during a Programming cycle, then the internal logic will take up to 10 µs to abort. During the abort period, no valid data can be read from the memory. Issuing a Reset command during a sector Erase cycle will leave invalid data in the memory.

GLOSSARY

Block: Flash memory block (4 Mbit) or EEPROM block (256 Kbit)

Bulk: the whole Flash memory block (4 Mbit)

Sector: 64 KByte of Flash memory

Page: 64 Bytes of EEPROM

Program and Write: Programming (in the Flash memory block) and Writing (to the EEPROM block) and are not the same:

- Flash memory bytes are programmed using the Program instruction (as shown in Table 4). This is used to change any bit values from ‘1’s to ‘0’s, where appropriate. As it is impossible to program bits from ‘0’s to ‘1’s, it is necessary to run a Sector Erase instruction before any byte overwriting can be performed.
- EEPROM bytes are written using a simple operation (Table 3).

SDP: Software Data Protection. This is used for protecting the EEPROM block against inadvertent Write operations (for example, in noisy environments).

Table 15. Write Mode AC Characteristics ($\overline{W}$ controlled)
(T_A = –40 to 85 °C; V_{CC} = 2.7 V to 3.6 V)

Symbol	Alt.	Parameter	M39432						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}		Address Valid to Next Address Valid	100		120		150		ns
t_{ELWL}[3]	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		65		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		65		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}[3]	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		35		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		65		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		ns
t_{VCHEL}[4]	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		50		µs
t_{WHQV1}[1]		Write Enable High to Output Valid (Program)	15		15		15		µs
t_{WHQV2}[1]		Write Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	2.0	30	s
t_{WHWL0}		Time-Out between two consecutive Sector Erase		80		80		80	µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		0		ns
t_{WHRL}[2,4]	t_{DB}	Write Enable High to Ready/$\overline{Busy}$ Output Low		150		150		150	ns

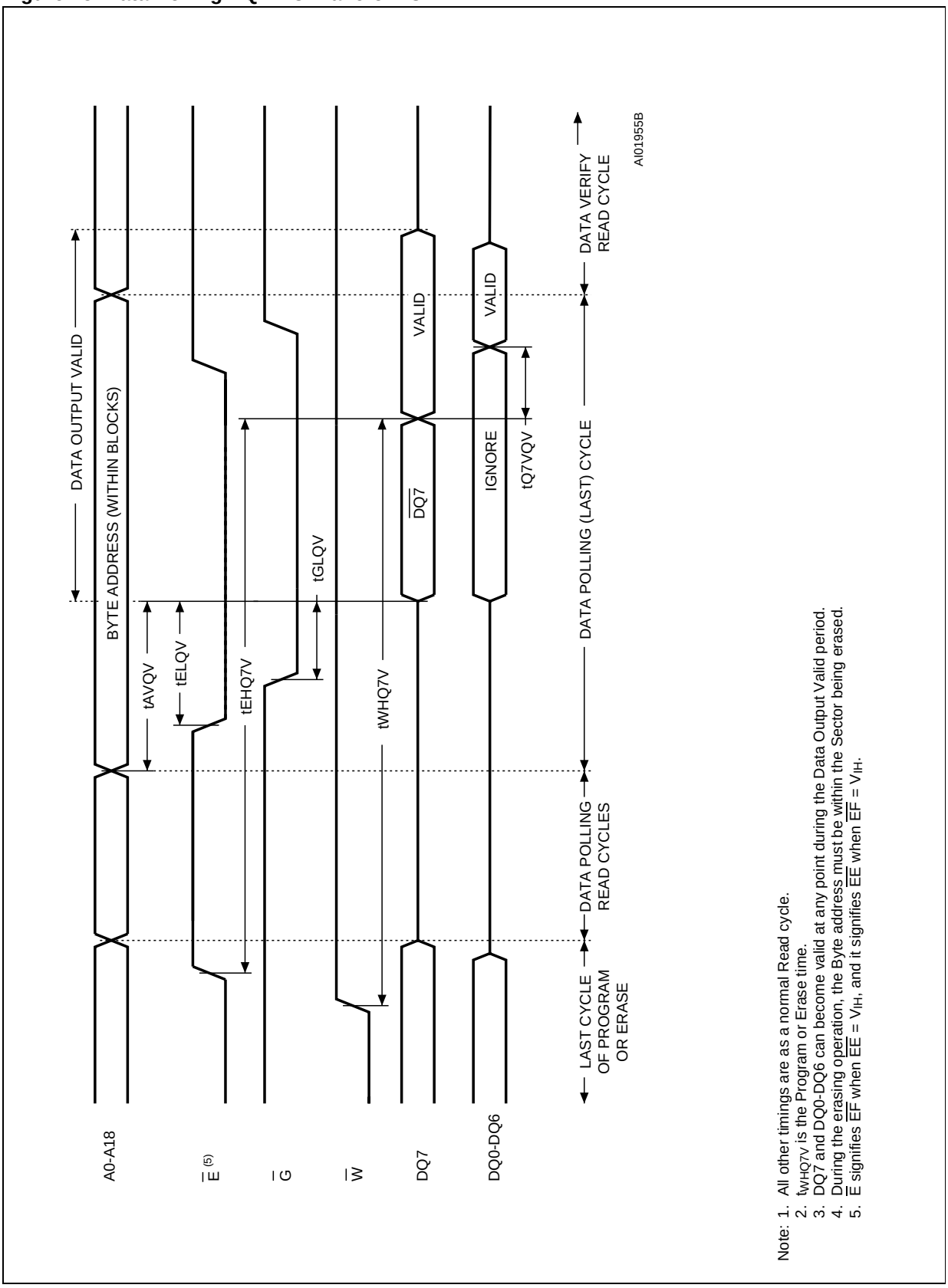
Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. With a 3.3 kΩ pull-up resistor.
3. Chip Enable means ($\overline{EE}$,$\overline{EF}$) = (V_{IL},V_{IH}) or ($\overline{EE}$,$\overline{EF}$) = (V_{IH},V_{IL}).
4. Sampled only, not 100% tested.

Table 16. Write Mode AC Characteristics ($\overline{EE}$ or $\overline{EF}$ controlled)
(T_A = –40 to 85 °C; V_{CC} = 2.7 V to 3.6 V)

Symbol	Alt.	Parameter	M39432						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{WLWL}	t_{BLC}	Time-out after the last byte write (EEPROM)	150		150		150		µs
t_{WHRH}	t_{WC}	Write Cycle Time (EEPROM)		10		10		10	ms
t_{AVAV}		Address Valid to Next Address Valid	100		120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Memory Block Enable Low	0		0		0		ns
t_{ELEH}	t_{CP}	Memory Block Enable Low to Memory Block Enable High	50		50		65		ns
t_{DVEH}	t_{DS}	Input Valid to Memory Block Enable High	50		50		65		ns
t_{EHDX}	t_{DH}	Memory Block Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{WH}	Memory Block Enable High to Write Enable High	0		0		0		ns
t_{EHEL}	t_{CPH}	Memory Block Enable High to Memory Block Enable Low	30		30		35		ns
t_{AVEL}	t_{AS}	Address Valid to Memory Block Enable Low	0		0		0		ns
t_{ELAX}	t_{AH}	Memory Block Enable Low to Address Transition	50		50		65		ns
t_{GHEL}		Output Enable High to Memory Block Enable Low	0		0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		50		µs
t_{EHQV1}[1]		Memory Block Enable High to Output Valid (Program)	15		15		15		µs
t_{EHQV2}[1]		Memory Block Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	2.0	30	s
t_{EHGL}	t_{OEH}	Memory Block Enable High to Output Enable Low	0		0		0		ns
t_{EHRL}[2]	t_{DB}	EEPROM Block Enable High to Ready/ $\overline{Busy}$ Output Low		150		150		150	ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. With a 3.3 kΩ pull-up resistor.

Figure 15. Data Polling DQ7 AC Waveforms



Note: 1. All other timings are as a normal Read cycle.
2. t_{WHQ7V} is the Program or Erase time.
3. DQ7 and DQ0-DQ6 can become valid at any point during the Data Output Valid period.
4. During the erasing operation, the Byte address must be within the Sector being erased.
5. $\overline{E}$ signifies $\overline{EF}$ when $\overline{EE}$ = V_{IH}, and it signifies $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Table 17. Data Polling and Toggle Bit AC Characteristics [1]
(T_A = –40 to 85 °C; V_{CC} = 2.7 V to 3.6 V)

Symbol	Alt.	Parameter	M39432						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{WHQ7V1} [2]		Write Enable High to DQ7 Valid (Program, $\overline{W}$ controlled)	10		10		10		µs
t_{WHQ7V2} [2]		Write Enable High to DQ7 Valid (Sector Erase, $\overline{W}$ controlled)	1.5	30	1.5	30	1.5	30	s
t_{EHQ7V1} [2]		Flash Block Enable High to DQ7 Valid (Program, $\overline{EF}$ controlled)	10		10		10		µs
t_{EHQ7V2} [2]		Flash Block Enable High to DQ7 Valid (Sector Erase, $\overline{EF}$ controlled)	1.5	30	1.5	30	1.5	30	s
t_{Q7VQV}		DQ7 Valid to Output Valid (Data Polling)		40		50		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)	10		10		10		µs
t_{WHQV2}		Write Enable High to Output Valid (Sector Erase)	1.5	30	1.5	30	1.5	30	s
t_{EHQV1}		Flash Block Enable High to Output Valid (Program)	10		10		10		µs
t_{EHQV2}		Flash Block Enable High to Output Valid (Sector Erase)	1.5	30	1.5	30	1.5	30	s

Note: 1. All other timings are defined in Table 13.
2. t_{WHQ7V} is the Program or Erase time.

Table 18. Program, Erase Times and Program, Erase Endurance Cycles (Flash Block)
(T_A = –40 to 85 °C; V_{CC} = 2.7 V to 3.6 V)

Parameter	M39432			Unit
	Min.	Typ.	Max.	
Chip Program (Byte)		8		s
Chip Erase (Pre-programmed)		3	30	s
Chip Erase		10		s
Sector Erase (Pre-programmed)		1	30	s
Sector Erase		2		s
Byte Program		10		µs
Program/Erase Cycles (per Sector)	100,000			cycles

Figure 16. Data Toggle DQ6 AC Waveforms

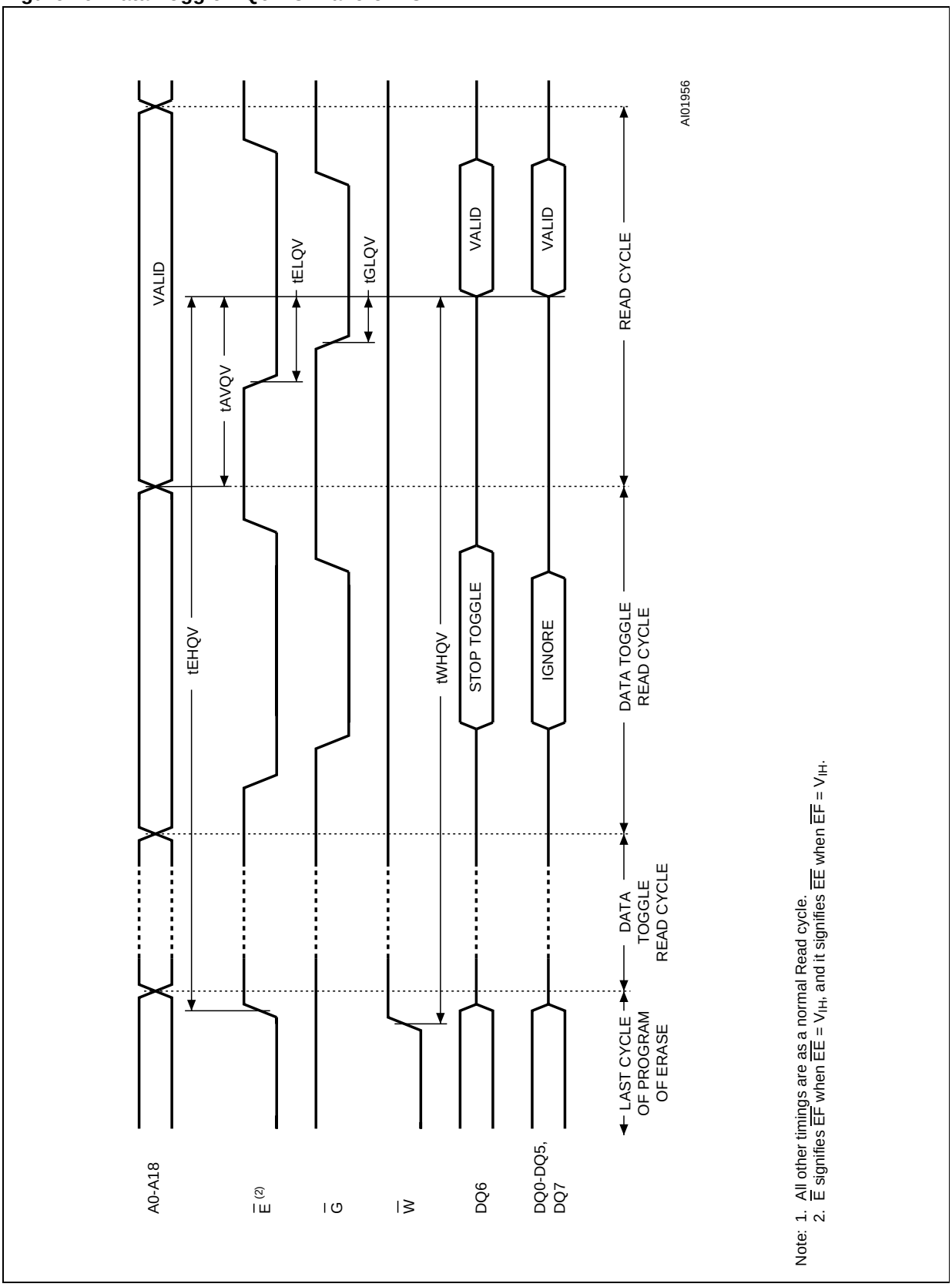
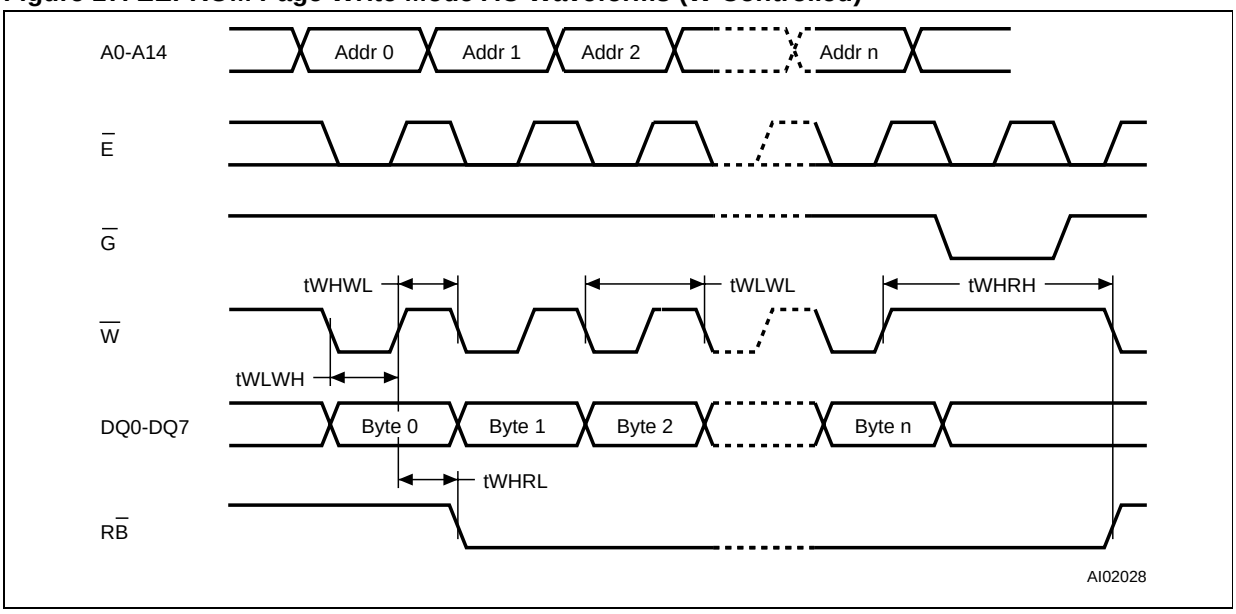


Figure 17. EEPROM Page Write Mode AC Waveforms ($\overline{W}$ Controlled)



ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 19. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 19. Ordering Information Scheme

Example: M39432 -15 W NC 1 T

Speed

-10	100 ns
-12	120 ns
-15	150 ns

Operating Voltage

W	2.7 V to 3.6 V
V[1]	3.0 V to 3.6 V

Option

T	Tape & Reel Packing

Temperature Range

6	–40 to 85 °C

Package

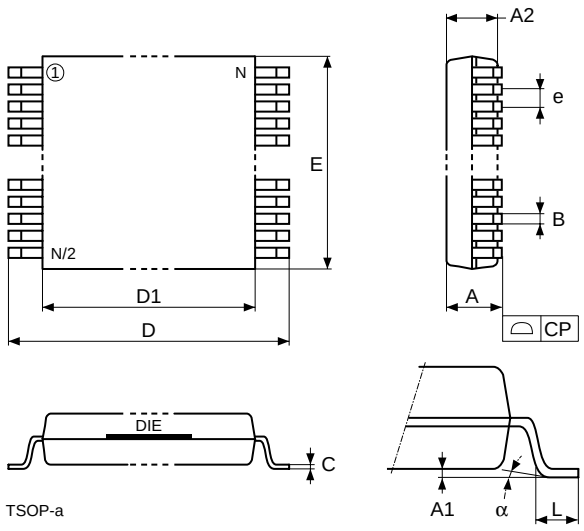
NC	TSOP40: 10 x 20 mm

Note: 1. The –V voltage range is no longer offered, since the –W range also covers these voltages. Similarly, products are no longer offered with a –20 or –25 marking (200 ns or 250 ns) since these are covered by the –15 (150 ns) part; and products are no longer offered with the 1 or 5 temperature ranges (0 to 70°C or –20 to 85°C) since these are covered by the 6 temperature range.

Table 20. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20 mm

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

Figure 18. TSOP40 (NC)



Note: 1. Drawing is not to scale.

Table 21. Revision History

Date	Description of Revision
09-Oct-1998	Document written
25-Nov-1999	Wider -W voltage range added, old -V range removed. Faster -10 speed range added, slowest -20 and -25 ranges removed. Narrowest temperature ranges 1 and 5 removed.