

M4003 & M4004 Series

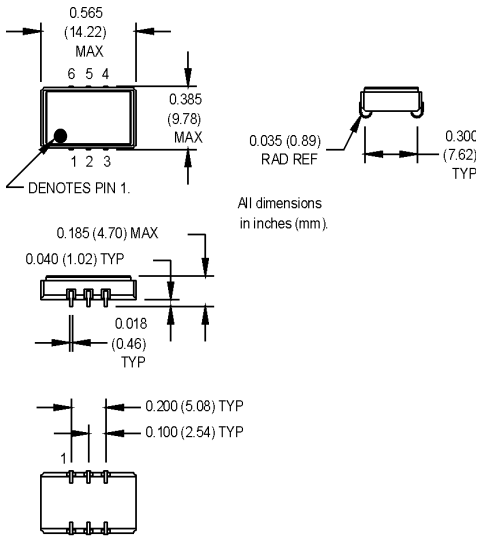
9x14 mm, 5.0 or 3.3 Volt, PECL, VCSO



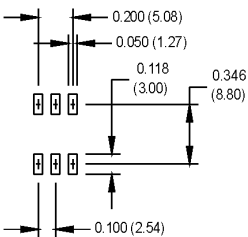
- Integrated phase jitter of less than 0.5 ps from 12 kHz to 20 MHz
- Ideal for SONET and 10 and 40 Gigabit Ethernet applications

Ordering Information		M4003/M4004		1	0	B	1	P	J	-R	00.0000
Product Series	M4003= 3.3 V M4004 = 5.0 V										
Temperature Range	1: 0°C to +70°C 2: -40°C to +85°C *										
Stability	0: Nominal per APR selection 1: ±50 ppm 2: ±100 ppm										
Output Type	B: Complementary, Enable (Enable High) S: Complementary, Enable (Enable Low) U: Complementary, Fixed										
Absolute Pull Range	1: ±50 ppm 2: ±100 ppm										
Symmetry/Output Logic Type	P: 45/55% PECL										
Package/Lead Configurations	J: J-lead K: FR-4										
RoHS Compliance	Blank: non-RoHS compliant part -R: RoHS compliant part										
Frequency (customer specified)											

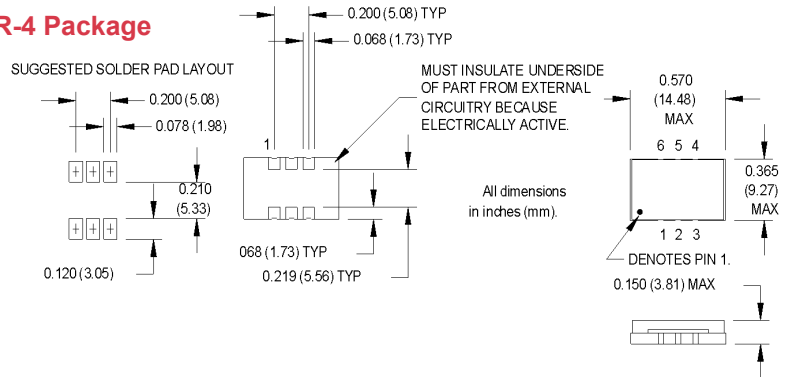
J-Lead Package



SUGGESTED SOLDER PAD LAYOUT



FR-4 Package



PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	500		1300	MHz	See Note 1
Operating Temperature	T _A	(See Ordering Information)				
Storage Temperature	T _s	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						
1st Year						
Thereafter (per year)						
Pullability/APR					ppm	See Note 2
Control Voltage	V _c	0		3.3	V	M4003
		0		5.0	V	M4004
Linearity			±3	±10	%	Positive Monotonic Slope
Modulation Bandwidth	f _m	500			kHz	-3 dB bandwidth
Input Impedance	Z _{in}	50k			Ohms	
Input Voltage	V _{cc}	3.135	3.3	3.465	V	M4003
		4.5	5.0	5.5	V	M4004
Input Current	I _{cc}		80	90	mA	M4003
			73	85	mA	M4004
Output Type						PECL
Load		50Ω to V _{cc} -2V or Thevenin Equivalent				
Symmetry (Duty Cycle)		45	50	55	%	V _{cc} -1.3
Output Skew						
Logic "1" Level	V _{oh}	V _{cc} -0.98			V	
Logic "0" Level	V _{ol}			V _{cc} -1.63	V	
Output Current				20	mA	
Rise/Fall Time	T _r /T _f			0.4	ns	@ 20/80%
Enable Function		PECL high or V _{cc} : output active				Output Option B
		PECL low or GND: output disables				
		PECL low, GND, or N/C: output active				Output Option S
		PECL high: output disables				
Start up Time						
Phase Jitter	φ _J					
@ 622.08 MHz			0.15	0.30	ps RMS	12 kHz - 20 MHz
			0.25	0.40	ps RMS	50 kHz - 80 MHz
Phase Noise (Typical)		10 Hz	100 Hz	1 kHz	10 kHz	100 kHz
@ 622.08 MHz		-40	-70	-100	-120	-140
						Offset from carrier dBc/Hz

1. Consult factory for extended temperature operation and exact frequency availability.
2. APR specification inclusive of initial calibration, deviation over temperature, shock, vibration, supply voltage, and aging.

Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Output Enable or N/C
3	Ground/Case
4	Output Q
5	Output Q or N/C
6	+V _{cc}

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