M46

Baseband Processor for GSM Applications

Conexant's M46 Baseband Processor (BP) is a highly integrated, dual core processor optimized for use in Global System for Mobile Communications (GSM) cellular handset applications. With its companion devices, the 20420 Integrated Analog (IA) device (refer to Conexant document number 100773) and the 20436 Power Management Integrated Circuit (PMIC) device (refer to Conexant document number 100772), the BP forms Conexant's baseband device set for GSM single-band or multi-band handsets.

The BP integrates the industry standard ARM 7 THUMB™ core, Conexant's high performance Digital Signal Processor (DSP) core, a Viterbi co-processor, and auxiliary digital support circuitry. Both the DSP core and the ARM7 THUMB™ Reduced Instruction Set Computer (RISC) architecture are well suited to meet the needs of low power, high performance embedded systems such as cellular phones. The BP operates over a range of 2.7 V to 3.6 V making it ideal for low power applications.

The baseband processing tasks are divided between the two processor cores. The DSP core executes the physical layer processing functions and the microcontroller core executes the Layer 2 and Layer 3 protocol software and the Man-Machine Interface (MMI) functions. The two cores communicate through a dedicated block of dual port memory. Each of the functional blocks in the device can be individually powered down to ensure minimum current consumption in the idle or standby mode. A block diagram of the device is provided in Figure 1.

The BP is packaged in a 160-pin micro Ball Grid Array (μBGA) with a 16-bit data bus and a 22-bit address bus. The package and pin configuration of the BP are shown in Figure 2. The signal pin assignments and functional pin descriptions are provided in Table 1.

Features

- Execution of GSM protocol stack software (Layers 1, 2, and 3)
- Execution of MMI software
- Interface to handset MMI peripherals (e.g., keypad, LCD, buzzer, etc.)
- Interface to data terminals
- Functional interface to a Subscriber Identity Module (SIM)
- Interface to handset memory components (Flash, SRAM, etc.)
- Integrated Real-Time Clock (RTC)
- Supports full rate and enhanced full rate speech coders
- Encryption/decryption
- Automatic Frequency Control (AFC)
- Automatic Gain Control (AGC)
- Digital Audio Interface (DAI)
- Interfaces to Conexant IA and PMIC devices
- Low power operation (2.7 V to 3.6 V)
- Optional voice features: voice recognition, voice prompts, conversation record, and voice memo
- Optional 14.4 kbps data/fax support

Applications

- GSM 900/1800/1900 handsets or modules
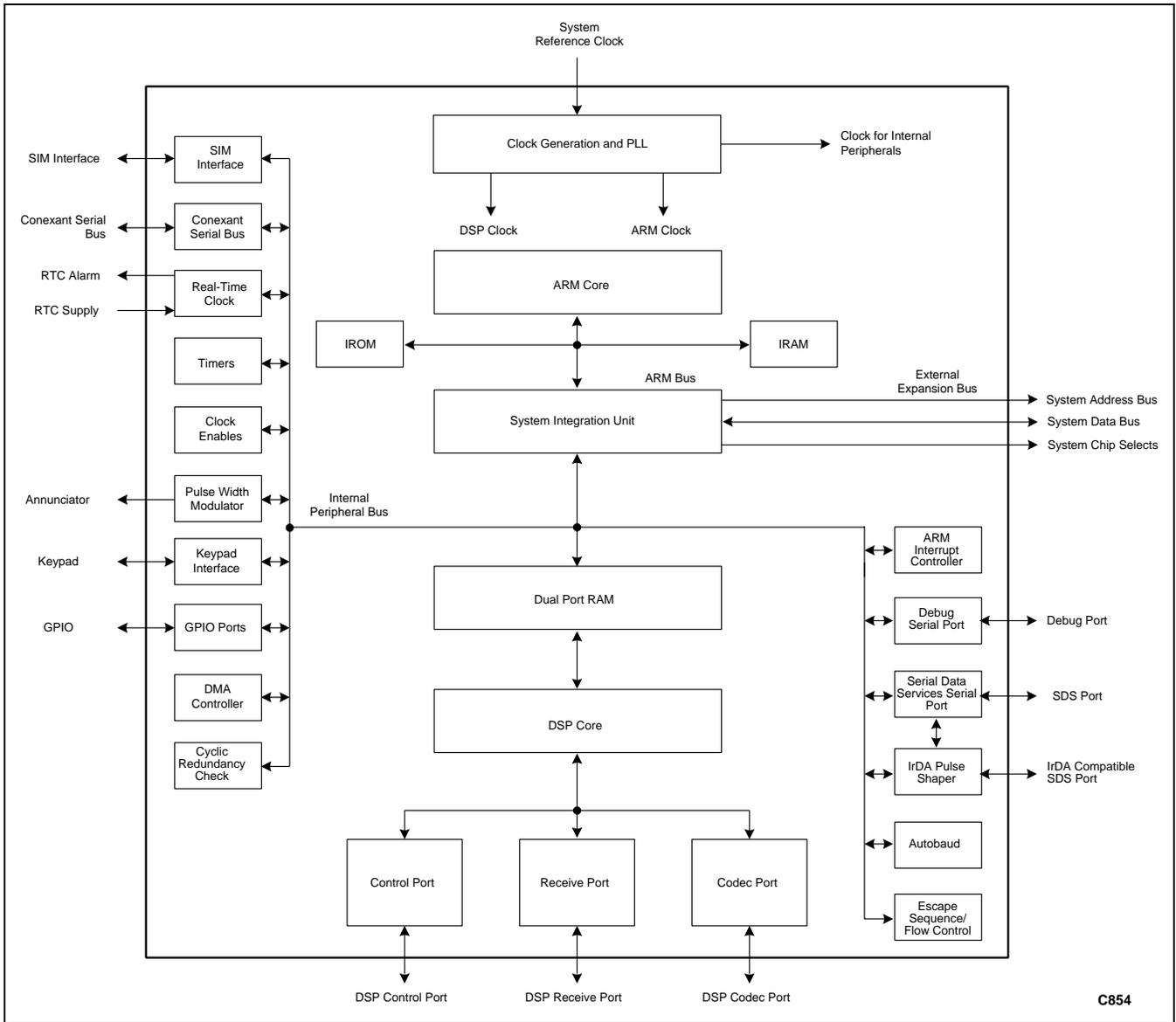
Figure 1. BP Block Diagram

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	N/C	GPIO_C[4]	GPIO_B[3]	GPIO_B[4]	N/C	GPIO_A[1]	DSPVSS	N/C	KPDSTB[3]	KPDSTB[0]	KPDRTN[1]	N/C	N/C	VRTC
B	DSPTEST	RESET	STROBE	GPIO_C[7]	GPIO_B[6]	GPIO_A[2]	IOVDD	KPDSTB[6]	KPDSTB[4]	KPDRTN[3]	KPDRTN[0]	IOVDD	XTLI	IOVSS
C	N/C	GPIO_B[7]	SYS_CLK	YCLK	GPIO_A[7]	IOVDD	DSPVDD	KPDSTB[7]	KPDSTB[2]	KPDRTN[2]	XTLO	PLLVDD	ALARM	GPIO_A[6]
D	N/C	RX_RATE	RX_DATA	CLK_REQ	GPIO_B[5]	GPIO_A[0]	IOVSS	KPDSTB[5]	KPDSTB[1]	CVSS	GPIO_B[0]	PLLVSS	CVDD	N/C
E	CNTRLCLK	DSPVDD	RX_CLOCK	DSPVSS							GPIO_B[2]	DSPVSS	DSPVDD	IOVSS
F	CNTRLRT	CDCCLK	RSPNSDAT	CNTRLDAT							GPIO_C[5]	SDS_TX	SDS_RX	SRLDATA
G	N/C	GPIO_A[4]	ENCDRDAT	CDCRATE							GPIO_A[3]	GPIO_C[6]	SRLCLK	N/C
H	DCDRDAT	D[15]	DSPVSS	DSPVDD							A[2]	A[0]	A[1]	A[5]
J	N/C	D[12]	D[14]	D[13]							A[6]	A[3]	A[4]	IOVDD
K	N/C	IOVSS	IOVDD	GPIO_C[0]							D[0]	A[7]	IOVSS	D[1]
L	N/C	GPIO_C[2]	GPIO_C[3]	D[11]	BS[1]	CS[1]	CVSS	A[17]	D[9]	A[11]	DSPVDD	D[2]	D[3]	D[4]
M	N/C	GPIO_C[1]	SIM_DATA	TCLK	TDI	BS[0]	CVDD	A[18]	IOVDD	D[8]	A[8]	D[6]	DSPVSS	D[5]
N	GPIO_B[1]	D[10]	SIM_CLK	TDO	IROMEN	READ	A[21]	A[19]	A[16]	A[15]	A[13]	A[10]	GPIO_D[2]	GPIO_D[1]
P	GPIO_A[5]	TRES	TMS	TESTP	WRITE	GPIO_D[0]	CS[0]	A[20]	N/C	IOVSS	A[14]	A[12]	A[9]	D[7]

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Figure 2. BP Device 160-Pin µBGA Pinout (Top View)

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Table 1. BP Pinout Assignments (1 of 2)

Pin #	Pin Name	Description	Pin#	Pin Name	Description
Power Supply					
M7, D13	CVDD	Microcontroller supply	E4, H3, M13, E12, A7	DSPVSS	DSP ground
L7, D10	CVSS	Microcontroller ground	C12	PLLVDD	PLL supply
K3, M9, J14, B12, B7, C6	IOVDD	I/O pins supply	D12	PLLVSS	PLL ground
K2, P10, K13, E14, B14, D7	IOVSS	I/O pins ground	A14	VRTC	Supply pin for Real-Time Clock circuitry
E2, H4, L11, E13, C7	DSPVDD	DSP supply			
Test/JTAG					
P4	TESTP	Test	M4	TCLK	JTAG clock
M5	TDI	JTAG data In	P2	TRES	JTAG reset
N4	TDO	JTAG data Out	N5	IROMEN	Enable Internal ROM
P3	TMS	JTAG mode select			
System					
B2	RESET	Power-on reset	B3	STROBE	Test
D4	CLK_REQ	Clock request signal	C13	ALARM	RTC alarm
C3	SYS_CLK	System clock	B13	XTLI	32 kHz crystal input
C4	YCLK	Test	C11	XTLO	32 kHz crystal output
B1	DSPTST	Test			
External Bus					
H12	A[0]		K11	D[0]	
H13	A[1]		K14	D[1]	
H11	A[2]		L12	D[2]	
J12	A[3]		L13	D[3]	
J13	A[4]		L14	D[4]	
H14	A[5]		M14	D[5]	
J11	A[6]		M12	D[6]	
K12	A[7]		P14	D[7]	Data bus 0 to 15
M11	A[8]		M10	D[8]	
P13	A[9]		L9	D[9]	
N12	A[10]	Address bus 0 to 21	N2	D[10]	
L10	A[11]		L4	D[11]	
P12	A[12]		J2	D[12]	
N11	A[13]		J4	D[13]	
P11	A[14]		J3	D[14]	
N10	A[15]		H2	D[15]	
N9	A[16]		N6	READ	Read strobe
L8	A[17]		P5	WRITE	Write strobe
M8	A[18]		P7	CS[0]	Flash select, chip select 0
N8	A[19]		L6	CS[1]	RAM select, chip select 1
P8	A[20]		M6	BS[0]	Byte select for 16-bit SRAM (lower byte)
N7	A[21]		L5	BS[1]	Byte select for 16-bit SRAM (upper byte)

Table 1. BP Pinout Assignments (2 of 2)

Pin #	Pin Name	Description	Pin#	Pin Name	Description
Keypad Control					
A10	KPDSTB[0]		B8	KPDSTB[6]	Keypad strobe lines 0 to 7
D9	KPDSTB[1]		C8	KPDSTB[7]	
C9	KPDSTB[2]	Keypad strobe lines 0 to 7	B11	KPDRTN[0]	
A9	KPDSTB[3]		A11	KPDRTN[1]	Keypad return lines 0 to 3
B9	KPDSTB[4]		C10	KPDRTN[2]	
D8	KPDSTB[5]		B10	KPDRTN[3]	
GPIO					
D6	GPIO_A[0]	GPIO signal port A[0] (I/O select bit = 0) Keyboard return 4 (I/O select bit = 1)	B5	GPIO_B[6]	GPIO signal port B[0] to B[7]
A6	GPIO_A[1]		C2	GPIO_B[7]	
B6	GPIO_A[2]		A2	GPIO_C[4]	GPIO signal port C[4] (I/O select bit = 0)
G11	GPIO_A[3]		F11	GPIO_C[5]	GPIO signal port C[5] (I/O select bit = 0) DEBUG_TX (I/O select bit = 1)
G2	GPIO_A[4]	GPIO signal port A[1] to A[7]	G12	GPIO_C[6]	GPIO signal port C[6] (I/O select bit = 0) DEBUG_RX (I/O select bit = 1)
P1	GPIO_A[5]		B4	GPIO_C[7]	GPIO signal port C[7]
C14	GPIO_A[6]		P6	GPIO_D[0]	GPIO signal port D[0] (I/O select bit = 0) CS[2] (I/O select bit = 1)
C5	GPIO_A[7]		N14	GPIO_D[1]	GPIO signal port D [1] (I/O select bit = 0) CS[3] (I/O select bit = 1)
D11	GPIO_B[0]		N13	GPIO_D[2]	GPIO signal port D[2] (I/O select bit = 0) CS[4] (I/O select bit = 1)
N1	GPIO_B[1]		K4	GPIO_C[0]	GPIO port C[0] (I/O select bit = 0) SIM_5V_3V (I/O select bit = 1)
E11	GPIO_B[2]	GPIO signal port B[0] to B[7]	M2	GPIO_C[1]	GPIO port C[1] (I/O select bit = 0) SIM_ENABLE (I/O select bit = 1)
A3	GPIO_B[3]		L2	GPIO_C[2]	GPIO port C[2] (I/O select bit = 0) SIM_RW (I/O select bit = 1)
A4	GPIO_B[4]		L3	GPIO_C[3]	GPIO port C[3] (I/O select bit = 0) SIM_RESET (I/O select bit = 1)
D5	GPIO_B[5]				
Serial Data Port					
F13	SDS_RX	SDS port data in	F14	SRLDATA	Conexant serial bus data I/O
F12	SDS_TX	SDS port data out	G13	SRLCLK	Conexant serial bus clock
IA Serial Ports					
D3	RX_DATA	Receive port data	F1	CNTRLRT	Control port rate
E3	RX_CLOCK	Receive port clock	H1	DCDRDAT	Codec port data to IA
D2	RX_RATE	Receive port rate	G3	ENCDRDAT	Codec port data from IA
F4	CNTRLDAT	Control port data to IA	F2	CDCCLK	Codec port clock
F3	RSPNSDAT	Control port data from IA	G4	CDCRATE	Codec port data
E1	CNTRLCLK	Control port clock			
SIM					
N3	SIM_CLK	Clock signal for SIM interface	M3	SIM_DATA	Bi-directional SIM data signal

Technical Description

The BP is a dual-core device consisting of an ARM7 THUMB microcontroller core, a Conexant proprietary DSP core, and all the digital control circuitry required in a GSM handset. The following sections describe the operation and programming of each of the functional blocks in the BP. Table 2 specifies the address and default value for each of the registers in the device. Note that the table specifies the value of each register before the BP IROM code is executed.

ARM7 THUMB™ Core

The ARM7 THUMB™ core is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit microcontrollers that offer high performance with very low power consumption. The ARM architecture is based on RISC principles with a simple yet powerful instruction set. This simplicity enables high instruction throughput and rapid real-time interrupt response.

Pipelining is used extensively to ensure that all parts of the processing and memory systems can operate continuously. While one instruction is being executed, the next instruction is being decoded and a third is being fetched from memory.

For further information on ARM7 THUMB™ please refer to the ARM7TDMI data sheet published by ARM.

Internal Memory

The BP is supported by 12 kB of Internal RAM (IRAM) and 16 kB of Internal ROM (IROM). Both the IRAM and the IROM directly interface to the 32-bit data and address buses from the microcontroller core.

The IROM contains the embedded firmware which is executed on power up. The IRAM is used for data storage during run time.

System Integration Unit (SIU)

The SIU is used to interface the 32-bit ARM bus to 8, 16, or 32-bit memory and peripherals connected to the External Expansion Bus (EXB) and Internal Peripheral Bus (IPB). Since the ARM only interfaces to 32-bit devices, the SIU formats the address and data to and from the ARM to allow 8, 16, or 32-bit data transfers.

The SIU also performs address decoding to generate internal and external chip select signals. These peripherals can be internal to the BP or external. Internal peripherals (such as the pulse width modulator) interface to the IPB while external peripherals (such as system Flash memory) interface to the EXB. The SIU performs the following main functions:

- Generates the required internal or external chip selects
- Formats the address bus and data bus for 8, 16 or 32-bit transfers

Separating the buses minimizes power dissipation since only the required bus lines are driven at any one time.

Internal Peripheral Bus (IPB)

The IPB interfaces to internal peripherals on the BP. The bus supports both 8-bit and 16-bit peripherals. The bus is only active when one of the internal peripherals is being accessed; if a device on the EXB is being accessed, there is no activity on the IPB.

External Expansion Bus (EXB)

The EXB allows external memory devices such as flash and SRAM to be connected to the BP. Internal to the BP, the EXB is connected to the SIU. The device features a 16-bit data bus D[15:0] and a 22-bit address bus A[21:0].

Besides the address and data buses, the EXB also consists of the following control signals:

- READ – active low read strobe that is asserted while data is read from the external peripheral.
- WRITE – active low write strobe that is asserted while data is being written to the external peripheral.
- CS[4:0] – configurable chip select signals.
- BS[1:0] – active low upper byte/lower byte select signals. These are used when the BP is transferring byte wide data to/from 16-bit peripherals. The polarity of these signals is programmable.

Note that the BP always produces a byte address. When word data (32-bit data) is transferred, A[1:0] bits are always low (set to "0"), and when half word data (16-bit data) is transferred, the A[0] bit is always low (set to "0").

The timing diagrams for read and write accesses over the EXB are shown in Figures 3 and 4, respectively. Figure 3 shows a read from a 16-bit external device that requires two wait states. Figure 4 shows a write to a 16-bit external device that requires two wait states.

Note that the ARM clock signal is internal to the device and is not output on any of the device pins.

Table 3 provides the values for all of the timing parameters.

Chip Select Signals_____

The BP has five chip select signals. Two of these ,CS0 and CS1, are on dedicated pins while the other three are multiplexed with General Purpose Input Output (GPIO) signals.

Each of the chip select signals has a configuration register. Each register is 16 bits wide but only the least significant 9 bits are used. The function of each register bit is shown in Table 4.

The address and default values for the Chip Select Signal Registers are specified in Table 2.

Table 2. BP Register Addresses (1 of 6)

Address (Hex)	Block Size (bytes)	Type	Name	Function	Default Value (Hex)
Chip Select Configuration Registers					
0040000	2	R/W	SIU Configuration	Bit [15] controls the polarity of the byte select signals	0002
0040002	2	R/W	CS0 Configuration	Control register for configuration of CS0 signal	0005
0040004	2	R/W	CS1 Configuration	Control register for configuration of CS1 signal	000E
0040006	2	R/W	CS2 Configuration	Control register for configuration of CS2 signal	000E
0040008	2	R/W	CS3 Configuration	Control register for configuration of CS3 signal	000E
004000A	2	R/W	CS4 Configuration	Control register for configuration of CS4 signal	000E
Real-Time Clock					
0040080	2	R/W	RTC Seconds	Real-Time Clock seconds	Undefined
0040082	2	R/W	RTC Minutes	Real-Time Clock minutes	Undefined
0040084	2	R/W	RTC Hours	Real-Time Clock hours	Undefined
0040086	2	R/W	RTC Days	Real-Time Clock days	Undefined
0040088	2	R/W	RTC Months	Real-Time Clock months	Undefined
004008A	2	R/W	RTC Years	Real-Time Clock years	Undefined
004008C	2	R/W	RTC Control	Control of the Real-Time Clock operation	Undefined
004008E	2		Reserved		
0040090	2		Reserved		
0040092	2	R/W	Alarm Minutes	Alarm minutes	Undefined
0040094	2	R/W	Alarm Hours	Alarm hours	Undefined
0040096	2	R/W	Alarm Days	Alarm days	Undefined
0040098	2	R/W	Alarm Months	Alarm months	Undefined
004009A	2	R/W	Alarm Years	Alarm years	Undefined
Interrupt Controller					
0040110	4	R/W	Interrupt Pending	Reading gives interrupts that are pending.	0000 0000
0040114	4	R/W	Interrupt Select	Directs a given interrupt to the IRQ or the FIQ input to the ARM.	0000 0000
0040118	4	R/W	Interrupt Enable	Enables the corresponding interrupt source.	0000 0000
004011C	4	R/W	External Interrupt Polarity	Set the polarity of external interrupts.	0000 0000
0040120	4		Reserved		
0040124	4	R	FIQ Interrupt	Determine if a particular interrupt is generating an FIQ interrupt to the ARM.	0000 0000
0040128	4	R	IRQ Interrupt	Determine if a particular interrupt is generating an IRQ interrupt to the ARM.	0000 0000

Table 2. BP Register Addresses (2 of 6)

Address (Hex)	Block Size (bytes)	Type	Name	Function	Default Value (Hex)
Timers					
0040180	2	R/W	Timer A Mode	Timer A configuration	0808
0040182	2	R/W	Timer A Latch	Timer A latch contents	0000
0040184	2	R/W	Timer A Counter	Timer A	FFFF
0040190	2	R/W	Timer B Mode	Timer B configuration	0808
0040192	2	R/W	Timer B Latch	Timer B latch contents	0000
0040194	2	R/W	Timer B Counter	Timer B	FFFF
Precision Timing Generators (PTGs)					
00401C0	2	R/W	PTG A Mode	PTG A configuration	0000
00401C2	2	R/W	PTG A Latch	PTG A latch contents	0000
00401C4	2	R/W	PTG A Counter		FFFF
00401C8	2	R/W	PTG B Mode	PTG B configuration	0000
00401CA	2	R/W	PTG B Latch	PTG B latch contents	0000
00401CC	2	R/W	PTG B Counter		FFFF
Cyclic Redundancy Check (CRC)					
00401D0	2	R/W	CRC Data	Writing will input 8-bit data to the Shift Register. Reading will read 16-bit results from the Polynomial Register.	FFFF
00401D2	2	W	CRC Reset	Writing to this address will reset polynomial Shift Register to 0xFFFF.	0000
Serial Data Services (SDS) Serial Port					
0040200	2	R/W	SDS Serial Buffer In /Out Buffer	Reading from this address will read the contents of the Serial In buffer. Writing to this address will write to the Serial Out buffer.	0000
0040202	2	R/W	SDS Serial Port Mode	SDS port configuration.	0000
0040204	2	R/W	SDS Serial Port Interrupt	Interrupt enable and flags.	0000
0040206	2	R/W	SDS Serial Port Line	Word length, parity and formatting.	0000
0040208	2	R/W	SDS Serial Port Status	SDS port status.	6060
004020A	2	R/W	SDS Serial Port Form	Vary duration of stop bits.	0000
004020C	2	W	SDS Serial Out Divider Latch	Controls serial out baud rate.	0000
004020E	2	W	SDS Serial In Divider Latch	Controls serial in baud rate.	0000
0040210	2		Reserved		

Table 2. BP Register Addresses (3 of 6)

Address (Hex)	Block Size (bytes)	Type	Name	Function	Default Value (Hex)
Debug Serial Port					
0040220	2	R/W	Debug Serial In / Out Buffer	Reading from this address will read the contents of the Serial In buffer. Writing to this address will write to the Serial Out buffer.	0000
0040222	2	R/W	Debug Serial Port Mode	Debug port configuration.	0000
0040224	2	R/W	Debug Serial Port Interrupt	Interrupt enable and flags.	0000
0040226	2	R/W	Debug Serial Port Line	Word length, parity and formatting.	0000
0040228	2	R/W	Debug Serial Port Status	Debug port status.	6060
004022A	2	R/W	Debug Serial Port Form	Vary duration of stop bits.	0000
004022C	2	W	Debug Serial Out Divider Latch	Controls serial out baud rate.	0000
004022E	2	W	Debug Serial In Divider Latch	Controls serial in baud rate.	0000
0040230	2		Reserved		
GPIO Ports					
0040280	2	R/W	Port A I/O Select	Select special function associated with GPIO signal.	0000
0040282	2	R/W	Port A Data I/O	Port A read/write data.	Undefined
0040284	2	R/W	Port A I/O Configuration	Select port A GPIO signals as inputs or outputs.	00FF
0040288	2	R/W	Port B I/O Select	Select special function associated with GPIO signal.	00FF
004028A	2	R/W	Port B Data I/O	Port B read/write data.	Undefined
004028C	2	R/W	Port B I/O Configuration	Select port B GPIO signals as inputs or outputs.	FFFF
0040290	2	R/W	Port C I/O Select	Select special function associated with GPIO signal.	00FF
0040292	2	R/W	Port C Data I/O	Port C read/write data.	00C0
0040294	2	R/W	Port C I/O Configuration	Select port C GPIO signals as inputs or outputs.	00FF
0040298	2	R/W	Port D I/O Select	Select special function associated with GPIO signal.	0007
004029A	2	R/W	Port D Data I/O	Port D read/write data.	0007
004029C	2	R/W	Port D I/O Configuration	Select port D GPIO signals as inputs or outputs.	00FF
Conexant Serial Bus					
0040300	2	R/W	Serial Bus Data I/O	Bit [0] at this address is connected to the serial data signal.	0003
0040302	2	R/W	Serial Bus Clock	Bit [0] at this address is connected to the serial clock signal.	0003

Table 2. BP Register Addresses (4 of 6)

Address (Hex)	Block Size (bytes)	Type	Name	Function	Default Value (Hex)
Escape Sequence/Flow Control Detection					
0040320	2	R/W	Control	Sets mode of detection circuitry.	0000
0040322	2	R/W	Status	Stores the status of the detection block.	0000
0040324	2	R/W	Escape Sequence Character	Character to detect as escape sequence.	002B
0040326	2	R/W	XON Character	Character to detect as XON.	0011
0040328	2	R/W	XOFF Character	Character to detect as XOFF.	0013
004032A	2	R/W	Escape Sequence Timeout	Number of 20 ms counts for timeout of escape sequence detection.	0000
004032C	2	R/W	Reserved		
IrDA Pulse Shaper					
0040340	2	R/W	Pulse Length	Sets transmit pulse duration and expected receive pulse duration.	0000
0040342	2	R/W	Divider Ratio	Sets number of PTG A pulses per bit period.	000F
DMA Controller					
0040500	4	R/W	DMA0 Address	Address of DMA channel 0 transfers (channel 0 is used for SDS_RX transfers).	0000 0000
0040504	4	R/W	DMA0 Threshold	Threshold address of DMA channel 0.	0000 0000
0040508	2	R/W	DMA0 Control	DMA channel 0 control.	0000
0040510	4	R/W	DMA1 Address	Address of DMA channel 1 transfers (channel 1 is used for DEBUG_RX transfers).	0000 0000
0040514	4	R/W	DMA1 Threshold	Threshold address of DMA channel 1.	0000 0000
0040518	2	R/W	DMA1 Control	DMA channel 1 control.	0000
0040520	4	R/W	DMA2 Address	Address of DMA channel 2 transfers (channel 2 is used for SDS_TX transfers).	0000 0000
0040524	4	R/W	DMA2 Threshold	Threshold address of DMA channel 2.	0000 0000
0040528	2	R/W	DMA2 Control	DMA channel 2 control.	0000
0040530	4	R/W	DMA3 Address	Address of DMA channel 3 transfers (channel 3 is used for DEBUG_TX transfers).	0000 0000
0040534	4	R/W	DMA3 Threshold	Threshold address of DMA channel 3.	0000 0000
0040538	2	R/W	DMA3 Control	DMA channel 3 control.	0000
0040540	4	R/W	DMA4 Address	Address of DMA channel 4 transfers (channel 4 is used for SIM transfers)	0000 0000
0040544	4	R/W	DMA4 Threshold	Threshold address of DMA channel 4.	0000 0000
0040548	2	R/W	DMA4 Control	DMA channel 4 control.	0000
0040550	2		Reserved		

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Table 2. BP Register Addresses (5 of 6)

Address (Hex)	Block Size (bytes)	Type	Name	Function	Default Value (Hex)
Autobaud					
0040740	16	R/W	Decision Values	Thresholds for baudrate decision.	Undefined
0040750	16	R/W	Timer Values	Values to load into PTG B.	Undefined
0040760	2	R/W	Control	Configures operation of Autobaud block.	0000
0040762	2	R	Status	Stores status of Autobaud block.	0000
0040764	2	R	Status Failure	If Autobaud detection fails, this register indicates the cause of the failure.	0000
0040766	2	R	First/Second Character	Stores the first and second characters received during the last autobaud attempt.	0000
0040768	2	R	Autobaud Count	Count value for start bit.	0000
004076A	2	R	Temporary Character	Temporary character value.	0000
Keypad					
0040800	2	R/W	Keypad I/O Configuration	Configure the keypad strobe lines as inputs or outputs (as the strobe lines as GPIO type signals).	0000
0040802	2	R/W	Keypad Strobe	Data written to this register will appear on the keypad strobe lines.	0000
0040804	2	R/W	Keypad Return Lines	Status of keypad return lines are stored in this register.	001F
Clock Generation and Phase Locked Loop					
0040902	2	R/W	Clock Enables	Turn on / off the clock to each block.	4003
0040B00	2	R/W	Reserved		
0040B02	2	R/W	Reserved		
Annunciator					
0040A00	2	R/W	PWM 1 Control	PWM 1 configuration.	0000
0040A02	2	R/W	PWM 1 Duty Cycle	PWM 1 duty cycle.	0000
0040A04	2	R/W	PWM 1 Divider Ratio	PWM 1 divider ratio.	0000
0040A06	2	R/W	PWM 1 Counter Register	PWM 1 counter register.	0064
0040A08	4	R/W	PWM 1 Data Pattern	PWM 1 data pattern.	0000
0040A10	2	R/W	PWM 2 Control	PWM 2 configuration.	0000
0040A12	2	R/W	PWM 2 Duty Cycle	PWM 2 duty cycle.	0000
0040A14	2	R/W	PWM 2 Divider Ratio	PWM 2 divider ratio.	0000
0040A16	4	R/W	PWM 2 Counter Register	PWM 2 counter register.	0064
0040A18	4	R/W	PWM 2 Data Pattern	PWM 2 data pattern.	0000

Table 2. BP Register Addresses (6 of 6)

Address (Hex)	Block Size (bytes)	Type	Name	Function	Default Value (Hex)
SIM Interface					
0040A80	4	R/W	SIM Control	SIM configuration	20D1 7420
0040A84	2	R/W	SIM Status	Stores the current status of the SIM Interface.	0000
0040A86	2	R/W	SIM Interrupt Enable	Enable/disable SIM Interrupt sources.	0000
0040A88	2	R/W	SIM Output Buffer	Data to be transmitted over the SIM interface is written to this buffer.	0000
0040A8A	2	R/W	SIM Input Buffer	Data received over the SIM interface is stored in this buffer.	0000

Byte Select Signals _____

The byte select signals, BS[1:0], are used to transfer byte wide data to and from 16-bit peripherals. When BS[0] is asserted, it indicates that data is on bits D[7:0]; if BS[1] is asserted, data is on bits D[15:8]. Both of these signals are active low.

During write operations to 16-bit peripherals, the byte select signals must be connected to the corresponding pins on the peripheral. These signals allow each 8-bit half of the 16-bit peripheral register to be written to independently. This is required since the ARM compiler may generate two byte transactions when accessing a 16-bit peripheral instead of a single half word (16-bit) transfer.

The polarity of the byte select signals is programmable. Bit [15] of the SIU Configuration Register controls the polarity of these signals. If this bit is set to "0," the signals are active low. If this bit is set to "1," the bits are active high.

Clock Generation and Phase Locked Loop

The BP clock generation circuitry takes a 3.9 MHz square wave system clock input, buffers it, and routes it to the internal peripherals. Each of the peripherals has a dedicated clock enable signal so that the clock signal can be turned off when the peripheral is not in use.

The 3.9 MHz signal is also routed to the Phase Locked Loop (PLL) circuitry which generates both the ARM and DSP clock signals.

Clock Enables _____

Each of the device circuitry blocks has a dedicated clock enable signal. This allows the clock signal to the circuitry block to be turned off when it is not in use. The clock enable signals are controlled by the contents of the Clock Control Register. If a particular bit is set to "1," the clock to the associated block is turned on; if the bit is set to "0," the clock is turned off. Table 5 describes the function of each bit in this register.

If a "0" is written to a specific bit, the associated clock will go low at the next high-to-low transition of the system clock and stay low until it is enabled again.

If a "1" is written to a specific bit, the associated clock will be turned on at the next low-to-high transition of the system clock.

The address and default settings for the Clock Control Register are specified in Table 2.

PLL Operation _____

A functional block diagram of the PLL is shown in Figure 5.

The system clock input (3.9 MHz) is divided down by the division factor, P. This factor is a 2-bit number with a value of 2. The output from this divider is input to the PLL block, which generates an output at N times the input frequency, where N is the multiplying factor (the value of N is 20). The PLL output is input to the DSP core. The PLL output is also divided down by a factor, M, to generate the ARM clock. The value of M is 2.

ARM Interrupt Controller

The ARM core can handle two interrupts:

- Fast Interrupt Request (FIQ)
- Interrupt Request (IRQ)

The FIQ has a higher priority than the IRQ. The IRQ is masked when an FIQ sequence is entered. In the case of an FIQ interrupt, fewer registers are required to be saved to memory. Therefore, switching into the interrupt handler is slightly faster.

All possible interrupt sources (internal and external) are routed to the Interrupt Controller, which generates either the FIQ or IRQ interrupt.

Interrupt Controller Registers _____

The address and default settings for the Interrupt Controller Registers are specified in Table 2.
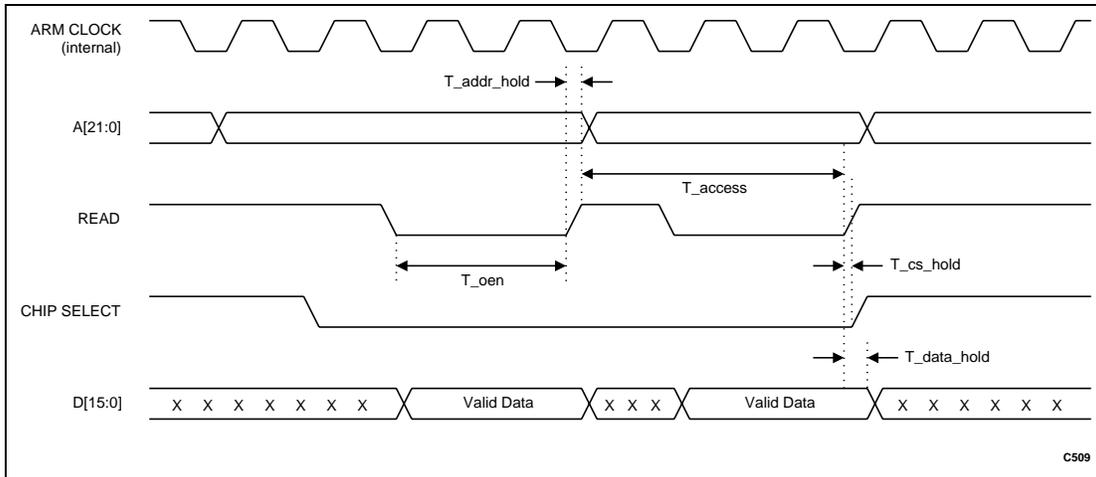
Figure 3. EXB Read Timing Diagram
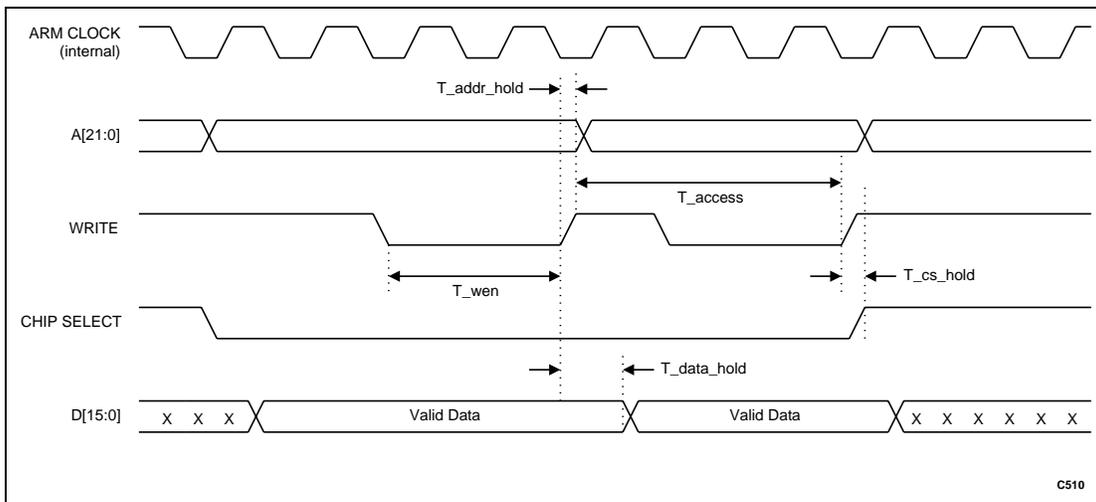
Figure 4. EXB Write Timing Diagram

Proprietary Information and Specifications are Subject to Change

Table 3. EXB Timing Specifications

Parameter	Symbol	Min	Max (Note 1)	Units
Read Timing for 0 Wait States				
Access time	T_access		45	ns
Address bus hold time after read strobe	T_addr_hold		6	ns
Chip select hold time after read strobe	T_cs_hold		6	ns
Duration of read strobe	T_oen		20	ns
Data bus hold time after write strobe	T_data_hold	0		ns
Write Timing for 0 Wait States				
Access time	T_access		43	ns
Address bus hold time after read strobe	T_addr_hold		4	ns
Chip select hold time after read strobe	T_cs_hold		5	ns
Duration of write strobe	T_wen		20	ns
Data bus hold time after write strobe	T_data_hold		34	ns
Read Timing for 1 or More Wait States				
Access time	T_access		$WS \times 51 + 25$	ns
Address bus hold time after read strobe	T_addr_hold		24	ns
Chip select hold time after read strobe	T_cs_hold		2	ns
Duration of read strobe	T_oen		$WS \times 51$	ns
Data bus hold time after write strobe	T_data_hold	0		ns
Write Timing for 1 or More Wait States				
Access time	T_access		$WS \times 51 + 25$	ns
Address bus hold time after read strobe	T_addr_hold		4	ns
Chip select hold time after read strobe	T_cs_hold		1	ns
Duration of write strobe	T_wen		$WS \times 51 - 1$	ns
Data bus hold time after write strobe	T_data_hold		30	ns
Note 1: WS is the number of wait states.				

Table 4. Chip Select Configuration Register

Bit	Name	Function
15:9	Reserved	N/A
8:7	DELAY	Assertion of the chip select will be asserted this many cycles after the address is stable. This allows for peripherals that require extra address bus settling time.
6	POLARITY	Chip select polarity: 1 = active high 0 = active low
5:4	SIZE[1:0]	Data bus width: 00 = byte 01 = half word 10 = word 11 = undefined
3:1	WAIT[2:0]	Number of wait states. Maximum is seven.
0	ENABLE	Chip select enable: 0 = disabled 1 = enabled

Table 5. Clock Control Register Functions

Bit	Block Controlled	Bit	Block Controlled
15	IrDA / Escape Sequence	7	PTGA
14	DSP	6	CRC
13	Reserved	5	Timer B
12	DMA Controlled	4	PWM
11	Autobaud	3	SIM
10	SDS Port	2	Reserved
9	Debug Port	1	SIU
8	PTGB	0	ARM Core
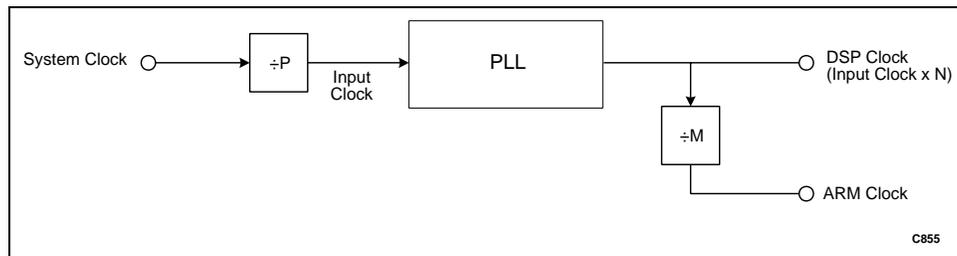
Figure 5. PLL Functional Block Diagram

Interrupt Pending Register. All interrupt sources are latched into the Interrupt Pending Register. When an interrupt is latched into this register the bit will remain set to "1" until the interrupt source has disappeared and the bit is cleared by the ARM. The source of each of the bits in the register is specified in Table 6.

Interrupt Select Register. Every enabled interrupt source can generate either an FIQ or IRQ interrupt to the ARM core. The Interrupt Select Register contains a bit for each possible interrupt source. If the associated bit is set to "1," an FIQ interrupt is generated when an interrupt occurs and the interrupt is enabled. Conversely, if the bit is set to "0," an IRQ interrupt is generated when an interrupt occurs and the interrupt is enabled.

The Interrupt Select Register bits have the same mapping to the interrupt sources as the Interrupt Pending Register (see Table 6).

Interrupt Enable Register. The Interrupt Enable Register contains a corresponding bit for each possible interrupt source. If the bit is set to "1," and an interrupt occurs, an interrupt is sent to the ARM. Either an FIQ or IRQ interrupt is generated depending on the status of the associated interrupt bit in the Interrupt Select Register. If the bit is set to "0," the interrupt is disabled.

The Interrupt Enable Register bits have the same mapping to the interrupt sources as the Interrupt Pending Register (see Table 6).

External Interrupt Polarity Register. The polarity of all external interrupts is selected by writing to the appropriate bit in the Interrupt Polarity Register. If the bit is set to "1," an interrupt is generated on the falling edge of the signal. If the bit is set to "0," the rising edge of the signal is the interrupting edge.

Care must be taken since the act of altering the bit could result in the generation of an interrupt edge. This potential hazard can be avoided by using software to disable the interrupt source when the polarity bit is changed.

The External Interrupt Polarity Register bits have the same mapping to the interrupt sources as the Interrupt Pending Register (see Table 6). For internally generated interrupts, the associated bits in this register are unused.

FIQ Interrupt Register. The FIQ Interrupt Register contains bits for all the possible interrupt sources. The FIQ Interrupt Register bits have the same mapping to the interrupt sources as the Interrupt Pending Register (see Table 6). If a bit for a particular interrupt is set to 1, the following conditions apply to that interrupt:

- The interrupt has occurred
- The interrupt is enabled
- The interrupt is set to generate an FIQ interrupt

If the bit is set to 0, at least one of the conditions listed above is not met.

Table 6. Interrupt Pending Register Sources

Bit	Source	Internal/External	Bit	Source	Internal/External
29:31	Reserved		14	SDS port transmit	Internal
28	GPIO port B[6]	External	13	DSP	Internal
27	GPIO port B[1]	External	12	DMA channel 4, SIM Rx and Tx	Internal
26	GPIO port B[7]	External	11	DMA channel 3, debug Tx	Internal
25	Reserved		10	DMA channel 2, SDS Tx	Internal
24	Keypad (key pressed)	Internal	9	DMA channel 1, debug Rx	Internal
23	GPIO port B[4]	External	8	DMA channel 0, SDS Rx	Internal
22	GPIO port B[5]	External	7	GPIO port B[2]	External
21	GPIO port B[3]	External	6	Reserved	
20	Debug port Rx	Internal	5	SIM interrupt	Internal
19	Autobaud interrupt	Internal	4	RTC alarm	Internal
18	Debug port Tx	Internal	3	PTGB (generates baud rate for debug port)	Internal
17	GPIO port B[0]	External	2	PTGA (generates baud rate for SDS port)	Internal
16	SDS port Rx	Internal	1	Timer B (used for general timing)	Internal
15	SDS_Rx (start bit received)	Internal	0	Timer A (used for SIM timing)	Internal

IRQ Interrupt Register. The IRQ Interrupt Register contains bits for all the possible interrupt sources. The IRQ Interrupt Register bits have the same mapping to the interrupt sources as the Interrupt Pending Register (see Table 6). If a bit for a particular interrupt is set to 1, the following conditions apply to that interrupt:

- The interrupt has occurred
- The interrupt is enabled
- The interrupt is set to generate an IRQ interrupt

If the bit is set to 0, at least one of the conditions listed above is not met.

Timers

The BP timer block contains the following timers:

- Two general purpose timers (Timer A and Timer B)
- Two precision timing generators (PTG A and PTG B)

General Purpose Timers _____

There are two 16-bit general purpose counters/timers used to generate time related interrupts to the ARM. Timer A is used to generate timeouts related to the SIM interface (required by the ETSI GSM specifications). Timer A uses either the SIM system clock or the SIM Elementary Time Unit (ETU) clock as an input clock. The output from Timer A is input to the Interrupt Controller.

Timer B is used for general purpose timing. Its input clock can be either the system clock (3.9 MHz) or the ARM clock (19.5 MHz). The output from Timer A is input to the Interrupt Controller as timb_irq.

Each of the timers consists of a Latch Register and a Counter Register. The Counter Register is loaded from the Latch Register and the timer counts down the contents of the Counter Register. When the Counter Register contents reach 0, the interrupt is generated.

Registers for General Purpose Timers. The address and default values for the General Purpose Timers Registers are specified in Table 2.

Timer Mode Register. Each of the timers has a dedicated Timer Mode Register. The contents of this register determine the configuration of the timer. The function of each bit in the register is provided in Table 7.

Latch Register. Each of the timers has a dedicated Latch Register. The contents of this register are loaded into the counter.

Counter Register. Each of the timers has a dedicated Counter Register. Writing to this register also writes the data to the Latch Register.

Table 7. Timer Mode Register Functions

Bit	Function
7	Enable/disable serial shifting in of data to the Serial In Buffer Register: 0 = disabled 1 = enabled
6	Enable/disable serial shifting out of data from the Serial Out Buffer Register: 0 = disabled 1 = enabled
5	Reserved. Set to "0" for normal operation
4:0	N/A (reserved)

Precision Timing Generators (PTGs)_____

PTG A generates symbol timing for the Serial Data Services (SDS) port. PTG B generates symbol timing for the Debug Port. Both timers can also generate an interrupt to the device Interrupt Controller. The timers use the 3.9 MHz system clock as an input clock. The output from either PTG is a clock signal at a frequency that is calculated as follows:

$$Clock\ Frequency = Input\ Clock\ Frequency \times \frac{Latch\ Value}{65536}$$

The input clock frequency is 3.9 MHz and the latch value is a 16-bit word that is individually programmable for each PTG.

For example, if a serial port baud rate of 230.4 kbps is required, the port needs to be clocked at 16 times this rate which is 3.6864 MHz. Setting the latch value to 0xF1FA results in a PTG output frequency of 3.686421 MHz, which is the closest to the required frequency that the PTG can generate.

PTG Registers. The address and default values for the Precision Timing Generator (PTG) Registers are specified in Table 2. The PTG Registers each contain a Mode Register and a Latch Register.

Mode Register. Each PTG has a dedicated Mode Register. The Mode Register configures the operation of the PTG. The function of each bit in the register is described in Table 8.

Latch Register. Each PTG has a dedicated Latch Register. The latch value is programmed by writing to the Latch Register. The latch value sets the PTG clock frequency.

Serial Ports

The BP device provides two asynchronous, full duplex serial ports:

- Debug Port. This port is used to output protocol stack signaling information and for remote control of the handset.

- Serial Data Services (SDS) Port. This port is used to communicate with a data terminal or PC.

Both ports can operate at baud rates of up to 230.4 kbps. Timing for the port is generated by two precision timers which, in turn, derive their timing from the 3.9 MHz system clock.

The timing of both ports is RS-232-compatible. Since the BP is a 2.8 V device, the logic levels are not RS-232 compatible. Therefore, external voltage translation circuitry is required to interface either of the ports to an RS-232 interface on a PC.

Debug Port _____

There are two Debug Port signals:

- DEBUG_TX (transmit data output from the device)
- DEBUG_RX (receive data input to the device)

The serial port sends signaling information from the protocol stack to monitor handset operation on a PC. The serial port receives data from a PC to allow remote control of the handset by the PC (e.g., originate a call, terminate a call, etc).

The Serial Port Registers are used to program the operating mode and data rate of the Debug Port.

SDS Port _____

There are two SDS Port signals:

- SDS_TX (transmit data)
- SDS_RX (receive data)

SDS timing is generated by Precision Timing Generator (PTG) A. The clock to the interface circuitry is normally off (to save power). When a start bit is seen on the SDS_RX signal or a byte is written to the port output buffer, the clock is turned on.

The Serial Port Registers are used to program the operating mode and data rate of the SDS Port.

Table 8. Serial Mode Register Functions

Bit	Signal	Function
15:4	N/A	Reserved
3	Counting Disable	Enable/disable timer counting

2	Clock Select	Select the timer counting clock:
		   Timer A (SIM interface):
		      0 = SIM clock selected as the counting clock.
		      1 = SIM ETU clock selected as the counting clock.
		   Timer B (general purpose timing):
		      0 = ARM clock (19.5 MHz) selected as the counting clock.
		      1 = system clock (3.9 MHz) selected as the counting clock.

1:0	N/A	Reserved. "00" must be written to these bits.

Serial Port Registers _____

There are eight serial port registers:

- Serial Buffer Registers (In and Out)
- Serial Mode Register
- Serial Port Interrupt Register
- Serial Port Line Register
- Serial Port Status Register
- Serial Port Form Register
- Serial Out Divider Register
- Serial In Divider Register

All of the Serial Port Registers are eight bits wide. The address and default values for the serial port registers are specified in Table 2.

Serial Buffer Registers. The Serial In and Serial Out Buffer Registers are located at the same address. The Serial In Buffer Register is read only and contains data that is received at the input to the port. The Serial Out Buffer Register is write only and contains data that is transmitted at the output of the port.

Serial Mode Register. The contents of the Serial Mode Register determine the operating mode of the serial port. The function of each bit in this register is described in Table 8.

Serial Port Interrupt Register. The Serial Port Interrupt Register contains the flags for all of the serial port interrupts and the enables for each of these interrupts. The function of each bit in this register is described in Table 9. Bits [4:0] are read/write. Bits [7:5] are read only.

Serial Port Line Register. The contents of the Serial Port Line Register specify the data formatting of input and output serial data. Parity, word length, and start/stop bits are all configured by this register. All bits in the register are read/write. The function of each bit in this register is described in Table 10.

Serial Port Status Register. The Serial Port Status Register provides information on the status of the port. All bits are read only and may be read by the ARM processor or the DMA Controller. The function of each bit in this register is described in Table 11.

Serial Port Form Register. The Serial Port Form Register is used to specify the duration of the last stop bit in the serial transmit data stream and to control the IrDA pulse shaper circuit. Bits [1:0] specify the duration of the last stop bit. Normally, the last stop bit is one bit in length. If it is necessary to use shorter stop bits, the Serial Out Divider Register must be loaded with 0x0F. The stop bit length for each of the possible values of bits [1:0] is specified in Table 12. All bits in the Serial Port Form Register are read/write.

Table 9. Serial Port Interrupt Register Functions

Bit	Function
7	Serial In Status Interrupt flag. This flag is set to "1" if either of the following two conditions occurs: 1. Any of bits [3:1] in the Serial Port Status Register are set to "1." 2. Bit [4] of the Serial Port Status Register changes state.
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Enable/disable generation of the port receive interrupt if bit [7] of this register is set to 1: 0 = disabled 1 = enabled
1	Enable/disable generation of the port transmit interrupt when the output buffer is empty: 0 = disabled 1 = enabled
0	Enable/disable generation of the port receive interrupt when the input buffer is full: 0 = disabled 1 = enabled

Table 10. Serial Port Line Register Functions

Bit	Function
7	Parity stuff. Output as the transmit data parity bit when bit [3] and bit [1] are set to "1."
6	Set break: 1 = break condition is transmitted (i.e., the output data is forced to a logic 0 state. 0 = Normal operation.
5	Parity stuff enable: 1 = Parity stuff enabled (bit [7] inserted in the serial out data in the position of the parity bit). 0 = Parity stuff disabled.
4	Even parity select: 1 = even parity enabled (even parity bit will be inserted in transmit data stream if bit 3 = "1" and bit 5 =" 0." 0 = even parity disabled.
3	Enable parity: 1 = parity bit inserted in serial out data; serial in data checked for parity bit. 0 = parity bit not inserted in serial out data; serial in data not checked for parity bit.
2	Number of stop bits to be inserted into the serial out data stream: 1 = 2 stop bits 0 = 1 stop bit
1:0	Word length. Specifies the number of bits in each serial in and serial data out word: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

Table 11. Serial Port Status Register Functions

Bit	Function
0	Serial in, buffer is full: 　1 = received character has been loaded into the Serial In buffer and can be read. This bit is reset to "0" when the buffer is read.
1	Overrun error: 　1 =　data in the Serial In buffer was not read before the next received character was transferred into the register, 　　　overwriting the previous data. This bit is reset to "0" when the Serial In buffer is read and the next character received can be safely transferred into the buffer.
2	Parity error: 　1 = parity error detected in the serial in data. This bit is reset to "0" when a character with a correct parity bit is received.
3	Framing error: 　1 = received word does not have a valid stop bit. This bit is reset to "0" when a character with a valid stop bit is detected.
4	Break interrupt: 　1 = serial in data is logic 0 from the start bit to the first stop bit. This bit is reset to "0" when a logic 1 is detected on the serial input.
5	Serial Out buffer empty: 　1 =　serial Out buffer is ready to accept a new character for transmission. If bit [1] of the Serial Port Interrupt Register is 　　　also set to 1, the port transmit interrupt will be asserted. This bit is reset to "0" by a write to the Serial Out buffer.
6	Serial out underrun: 　1 =　the Serial Out Register is empty and the Serial Out buffer has not been reloaded. Serial Out data will be set to logic 　　　1 if this occurs. This bit is reset to "0" by a write to the Serial Out buffer.
7	Received data parity bit is copied to this location.

Table 12. Serial Port Form Register Stop Bit Lengths

Bits [1:0]	Duration of Final Stop Bit (5-bit word length, 2 stop bit mode)	Duration of Final Stop Bit For All Other Modes
00	1/2 bit period	1-bit period
01	1/4 bit period	3/4 bit period
10	3/8 bit period	7/8 bit period
11	1/8 bit period	5/8 bit period
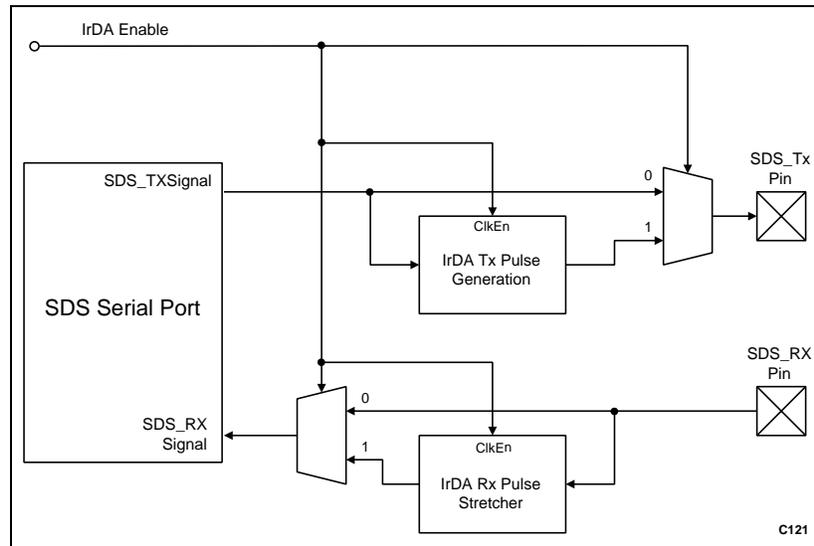
Figure 6. IrDa Pulse Shaper Functional Block Diagram

For the SDS Port Form Register, bit[6] enables/disables the IrDA Pulse Shaper circuit. If this bit is set to "0," the IrDa circuit is disabled. If the bit is set to "1," the circuit is enabled.

Serial Out Divider Register. The Serial Out Divider Register is a write only register that controls the baud rate of the serial port transmit data. The baud rate is calculated as:

$$Po = \frac{Sp}{(So + 1)}$$

where: Po = port output baud rate
              Sp = serial port clock
              So = serial out divider

The serial port clock is the output from the PTG. Note that this register must be loaded with 0x0F if a short stop bit is to be used or if 5-bit word length is selected.

Serial In Divider Register. The Serial In Divider Register is a write only register that determines the baud rate at which the serial port expects to receive data. The baud rate is calculated as:

$$Pi = \frac{Sp}{(So + 1)}$$

where: Pi = port input baud rate
              Sp = serial port clock
              So = serial out divider

The serial port clock is the output from the PTG. The address and default values for the Serial Port Form Register are specified in Table 2.

Infrared Data Adapter (IrDA) Pulse Shaper

The IrDA Pulse Shaper allows an IrDA-compatible transceiver to be connected directly to the SDS pins on the BP. Enabling the Pulse Shaper inserts an IrDA-compliant Pulse Shaper between the SDS signals and the SDS pins. The IrDA block is enabled by setting bit [6] in the SDS Port Serial Form Register.

A functional block diagram for the operation of the Pulse Shaper is provided in Figure 6.

When the IrDA block is enabled, the following occurs:

1. Using the bit stream output from the SDS Serial Port block on the SDS_RX signal, the IrDA Tx Pulse Shaper generates a short positive pulse for every "0" transmitted by the port and a low level pulse for every "1" transmitted by the port. The duration of pulse is programmable. The output of the Tx Pulse Shaper is routed to the SDS_TX pin.
2. If the IrDA RX Pulse Stretcher recognizes a pulse of the expected duration on the SDS_RX pin, a "0" is generated on the SDS_RX signal for one bit period. If no pulse is detected, a "1" is generated for the duration of the bit period. The expected duration of the received pulse is programmable.

IrDA Registers _____

There are two IrDA registers:

- Pulse Length Register
- Divider Ratio Register

IrDA Pulse Length Register. The IrDA Pulse Length Register is used to set the length of the Tx pulse and the expected duration of the Rx pulse. Bits [3:0] set the length of the Tx pulse. The duration of the pulse is calculated as:

$$(Bits\ [3:0]\ +\ 1)\ \times system\ clock\ cycle$$

For example, if the bits are set to 0x0F, the duration of the pulse is:

$$(15 + 1) \times \frac{1}{3.9\ MHz} = 4.1\ \mu sec$$

Bits [7:4] set the expected length of the Rx pulse. A pulse received on the SDS_RX pin must be of this duration for the Pulse Stretcher to generate a "0" on the SDS_RX pin. The expected pulse duration is calculated the same as the Tx pulse duration.

Bits [15:8] of the IrDA Pulse Length Register are reserved.

IrDA Divider Ratio Register. The IrDA Divider Ratio Register is used to set the IrDA baud rate. The IrDA circuit derives the interface bit period from PTG A, which is used to generate timing for the SDS port. Bits [0:3] of this register set the baud rate of the IrDA circuit. The baud rate is calculated as:

$$\frac{PTG\ frequency}{(bits[3:0]+1)}$$

The address and default values for the IrDA Registers are specified in Table 2.

Cyclic Redundancy Check (CRC) Block _____

The CRC block is used to perform error checking on blocks of data. The microcontroller writes a sequence of byte-wide data to the CRC Data Register, which calculates an output polynomial based on the input sequence.

Before writing the data sequence, the output polynomial is reset to 0xFFFF by writing to the CRC Reset Register. The output polynomial can be read at any time and is typically appended to a block of data so that the receiving entity can determine if there were errors in the received data.

Reading from the CRC Data Register gives the output polynomial.

The address and default values for the CRC Registers are specified in Table 2.

DMA Controller

The DMA Controller allows blocks of data to be transferred directly between peripherals and memory. The maximum block size that can be transferred is 2 KB.

When a DMA transfer is required, the ARM sets up the DMA Controller with the block starting address and the block finishing address. If a number of DMA transfers are requested at the same time, the DMA Controller determines which has the highest priority.

There are five DMA channels that are assigned as follows :

- DMA Channel 0 - Transfer data from the SDS serial port to the main memory.
- DMA Channel 1 - Transfer data from the Debug serial port to the main memory.
- DMA Channel 2 - Transfer data from the main memory to the SDS serial port.
- DMA Channel 3 - Transfer data from the main memory to the Debug serial port.
- DMA Channel 4 - Transfer data from the main memory to the SIM interface.

The highest priority is Channel 0 and the lowest priority is Channel 4.

During the DMA transfer, the DMA Controller assumes control of the bus and communicates with the SIU to allow the data to be transferred directly between the memory and the peripheral. After each data transfer, the value in the DMA Address Register (originally loaded with the block starting address) is incremented. When the block finishing address is reached, the DMA Controller ceases data transfer after the current transfer has been completed.

DMA Registers_____

The DMA registers are used to set up the DMA operation. The address and default values for the DMA Registers are specified in Table 2.

DMA Address Register. Each DMA channel has a dedicated Address Register. The Address Register is written to by the ARM to set the starting address of the block to be transferred. After each DMA data transfer, the value in the register is incremented. The ARM writes to bits[0:23] to set up the address but only bits[0:10] are incremented after each DMA data transfer.

Table 13. DMA Control Register Functions

Bit	Function
0:2	Reserved
3	Enable DMA channel: 0 = disabled 1 = enabled
4	Reserved. Should be set to "0" for normal operation.
5	Controls direction of data transfer: 0 = from peripheral to memory 1 = from memory to peripheral
6	Select whether transfers are byte wide of half word (16 bits) wide: 0 = byte wide. Address Register is incremented by 1 after each transfer. 1 = half word wide. Address register is incremented by 2 after each transfer.

DMA Threshold Register. Each DMA channel has a dedicated Threshold Register. The ARM writes to this register to set the finishing address of the block of data to be transferred by the DMA Controller. When bits[10:0] in this register match bits[10:0] in the DMA Address Register, DMA transfer will be suspended after the current transfer has been completed. Bits[23:11] of this register are set equal to bits[23:11] of the DMA Address Register.

DMA Control Register. Each DMA channel has a dedicated Control Register. The DMA Control Register configures the operation of the DMA channel. The function of each of the bits in the register is shown in Table 13.

GPIO Ports

The BP provides 27 General Purpose Input/Output (GPIO) signals which may be used to implement the various functions of a GSM handset design. The GPIO signals are divided into four ports:

- Port A with eight signals (GPIO_A[7] to GPIO_A[0])
- Port B with eight signals (GPIO_B[7] to GPIO_B[0])
- Port C with eight signals (GPIO_C[7] to GPIO_C[0])
- Port D with three signals (GPIO_D[2] to GPIO_D[0])

Each of the ports has three registers that are used to configure the ports and to read/write data from/to the ports.

GPIO Interrupts _____

Each of the Port B GPIO signals can generate an interrupt to the device Interrupt Controller. These interrupts are routed to the Interrupt Controller before being latched and, therefore, are present even if the system clock signal to the circuit is turned off.

GPIO Registers _____

For each of the registers, there is a one to one mapping between the register bit and the GPIO signal it controls. For example bit [0] in the Port A I/O Select Register enables/disables the special function of Port A [0].

The address and default values for the GPIO registers are specified in Table 2.

Port Data I/O Register. Each of the ports has a Port Data I/O Register. The ARM writes to this register to output data on the port pins and reads from this register to read data input on the port pins.

I/O Select Register. Each of the GPIO signals has an associated I/O select bit. Several of the GPIO signals are multiplexed with other special function signals. The alternate function is enabled when a "1" is written to the associated I/O select bit.

For example, GPIO Port C[4] is multiplexed with the output from the BP Pulse Width Modulator (PWM) circuit. If a "1" is written to the Port C[4] I/O select bit, the output of the device PWM circuit is routed to the GPIO pin. If a "0" is written to the Port C[4] I/O select bit, the GPIO pin is configured as a GPIO signal.

Table 14 shows the alternate function associated with each of the GPIO signals.

I/O Configuration Register. Each GPIO signal has a companion configuration bit that selects the GPIO signal as an input or an output. If the bit is set to "0," the signal is configured as an output; if the bit is set to "1," the signal is configured as an input.

Table 15 describes how the GPIO signals are typically used in a handset design.

Table 14. GPIO Alternate Functions

GPIO Signal	I/O Select Bit = 1	GPIO Signal	I/O Select Bit = 1
A0	KPDRTN[4]	B6	N/A
A1	N/A	B7	N/A
A2	N/A	C0	SIM_5V_3V
A3	N/A	C1	SIM_ENABLE
A4	N/A	C2	SIM_RW
A5	N/A	C3	SIM_RESET
A6	N/A	C4	BUZZER
A7	N/A	C5	DEBUG_TX
B0	N/A	C6	DEBUG_RX
B1	N/A	C7	N/A
B2	N/A	D0	CS2
B3	N/A	D1	CS3
B4	N/A	D2	CS4
B5	N/A		

Keypad Interface

The keypad interface consists of eight strobe lines and four return lines. This allows for a keypad matrix of up to 32 keys. The strobe lines are GPIO type signals and the return lines are dedicated signals. Unused strobe lines can be used as extra GPIO signals if required. If a keypad matrix of more than 32 keys is required, one of the GPIO signals (GPIO Port A[0]) can be configured as a return line to give a total matrix of 40 keys. The GPIO is configured as a keypad return line by setting the Port A[0] I/O select bit to "1" (refer to the GPIO section of this Data Sheet for more information).

Figure 7 illustrates a typical keypad interface circuit. The strobe lines are output from the BP and connected to the keypad columns. The return lines are input to the BP and connected to the keypad rows.

Keypad Scan _____

Once every frame (4.6 ms) the BP drives one of the strobe lines low and all of the others high. If a key connected to the strobe line that is driven low is pressed during this time, the return line that is also connected to this key will be pulled low. This triggers an interrupt to the microcontroller to indicate that a key has been pressed. Since the microcontroller knows which strobe line it is driving low and which return line has been driven low by the keypress, it can uniquely identify the key pressed.

A complete scan of the entire keypad requires 4.6 ms multiplied by the number of strobe lines:

Complete keyboard scan time = 4.6 ms × 8 = 36.8 ms

Key debounce is performed by the software.

Keypad Registers _____

There are three keypad registers used to configure and monitor the keypad interface: the Keypad I/O Configuration Register, Keypad Strobe Register, and the Keypad Return Lines Register.

The address and default values for the keypad registers are specified in Table 2.

Keypad I/O Configuration Register. The Keypad I/O Configuration Register is used to set up the strobe lines as either inputs or outputs. Each of the strobe lines has a related bit that sets the direction of the pin. If the bit is set to "0," the pin is configured as an output. If the bit is set to "1." the pin is configured as an input. There is a one-to-one mapping between the bits and the keypad strobes (i.e., bit [0] configures keypad strobe 0, bit[1] configures keypad strobe [1], etc.).

The default value of this is 0xFF, which configures all the keypad strobes as outputs from the BP.

Table 15. Typical GPIO Assignments

GPIO Signal	Function	Type	Description
A[0]	IRDA_ENABLE	Output	Enables the IrDa device.
A[1]	SIM_CLAMP	Output	Clamp the SIM supply to 0 V on handset power down.
A[2]	MOTOR_ENABLE	Output	Enable the handset vibrating anunciator.
A[3]	RED_LED_ENABLE	Output	Enables red status LED.
A[4]	BOOST_ENABLE	Output	Enables the DC/DC boost converter circuit on the PMIC.
A[5]	RMT_CNTL	Output	Enables the audio headset circuit.
A[6]	GREEN_LED_EN	Output	Enables the green status LED.
A[7]	LED_CTL	Output	Enables the backlight LEDs.
B[0]	SEND_END	Input	Detects when the Send/End key on the headset is pressed.
B[1]	BAT_DET_EN	Output	Enables the battery type detection circuit.
B[2]	TA_PRESENT	Input	Indicates if the external DC voltage is connected to the handset (travel charger adapter).
B[3]	DAI_CLOCK	Output	DAI_CLOCK for audio testing.
B[4]	CHARGER_DISABLE	Output	Controls the battery charging circuit. This signal can be used to turn off the charging circuit when the battery has been fully charged.
B[5]	FLIP_SENSE	Input	Indicates if the handset flip is open or closed.
B[6]	HDST_DETECT	Input	Indicates if the audio headset is connected to the handset.
B[7]	F_RT	Input	Frame rate interrupt from the IA to the M46.
C[0]	SIM_DATA_AUX	Output	Drives the SIM_DAT line to the required logic level when the SIM read or write is complete.
C[1]	SIM_ENABLE	Output	Enables SIM circuitry on the PMIC.
C[2]	VSET	Output	Sets up charging voltage for the battery charging circuit (4.1 or 4.2 V).
C[3]	SIM_RESET	Output	Resets the SIM card.
C[4]	BUZZER	Output	Output of the BP circuit. This is used to drive the handset annunciator.
C[5]	DEBUG_TX	Output	Trace Tx data.
C[6]	DEBUG_RX	Input	Trace Rx data.
C[7]	FLASH_PROGRAM	Output	Enable programming of the handset program flash.
D[0]	AUDIO_FLASH_EN	Output	Chip select for audio flash.
D[1]	LCD_SELECT	Output	Chip select used to enable the LCD.
D[2]	AUDIO_FLASH_EN	Output	Chip select for audio flash storage.
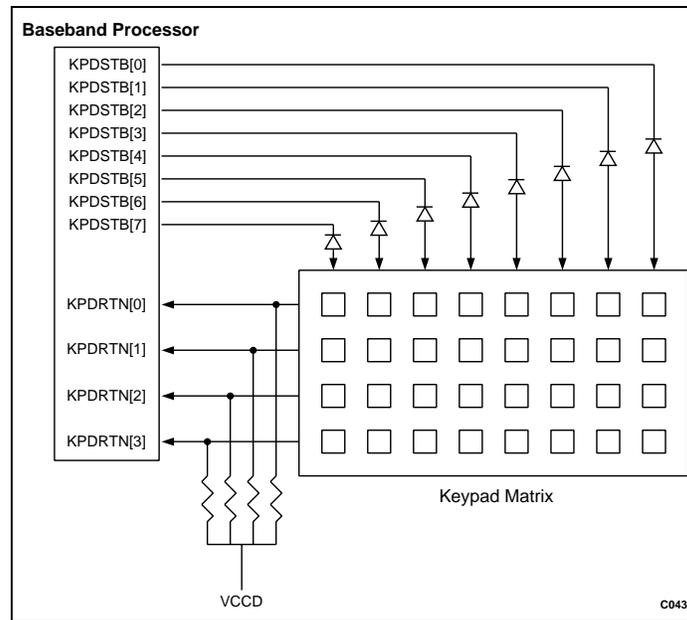
Figure 7. Typical Keypad Interface Circuit

Keypad Strobe Register. The Keypad Strobe Register is used to specify the output level of the strobe lines. Data written to this register will appear on the strobe lines, assuming that the Configuration Register has been written to set up the signals as outputs. There is a one-to-one mapping between the bits and the keypad strobes (i.e., bit [0] drives keypad strobe 0, bit[1] drives keypad strobe [1], etc.).

Keypad Return Lines Register. The Keypad Return Lines Register is used to read the state of each of the keypad return lines. Keypad Return 4 is multiplexed with GPIO Port A[0] so the related GPIO I/O select bit must be set to configure the pin as a keypad return signal.

There is a one-to-one mapping between the bits and the keypad return lines (i.e., bit [0] stores the state of keypad return line 0, bit[1] stores the state of keypad return line [1], etc.).

Annunciator _____

The annunciator circuitry on the BP generates a signal to drive a handset buzzer. Some external circuitry may be required to drive the buzzer depending on its electrical characteristics.

The output from the annunciator circuitry is multiplexed with GPIO Port C[4]. To select the PWM output to the pin, the I/O select bit for GPIO Port C[4] must be set to "1." See the GPIO section of this Data Sheet for more information.

There are two identical but separately programmable PWM circuits on the BP. The outputs from the two circuits are toggled at a rate of 1.95 MHz to generate the annunciator output from the device. The annunciator output circuitry and the buzzer driving circuitry are shown in Figure 8.

PWM Operation _____

The basic operation of each of the PWM circuits is described below.

The PWM uses a reference clock of 1.95 MHz to generate two pulse trains:

- A low frequency pulse train programmable from 200 to 500 Hz. This is the Tone signal.
- A high frequency pulse train at 39 kHz with a variable duty cycle. This is the Mod signal.

The two pulse trains are mixed and filtered to produce the PWM output. The frequency of this output is the frequency of Tone; the volume is dependent on the duty cycle of Mod. The frequency of Tone and the duty cycle of Mod are programmable so that complex annunciator tones can be generated.

A functional block diagram for the PWM is shown in Figure 9.
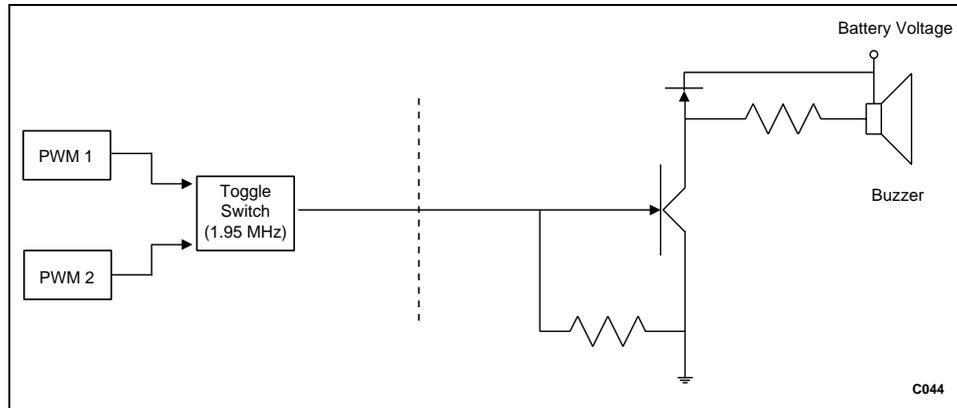
**Figure 8. Annunciator Output Circuitry and Buzzer Driving Circuitry**

Note : The shaded blocks are programmable
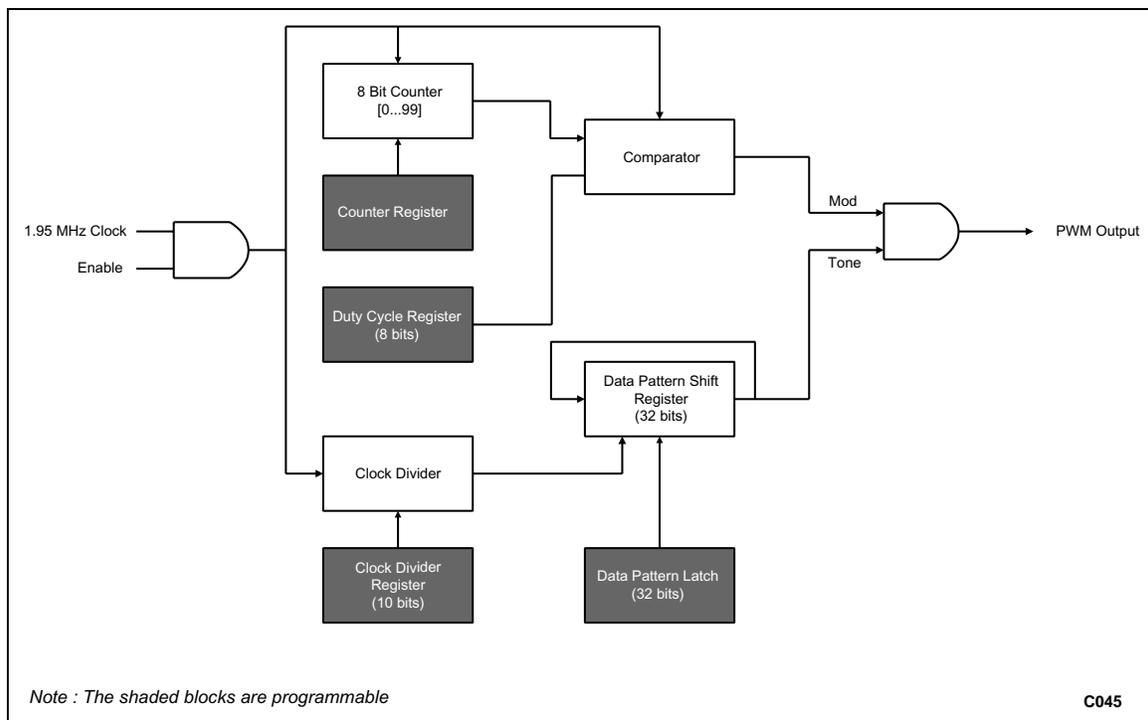
Figure 9. PWM Functional Block Diagram

The counter circuit is an 8-bit counter that is clocked at 3.9 MHz. The counter counts to the value set in the Counter Register and is then reset to 0. The default value of the Counter Register is decimal 100.The Duty Cycle Register is a programmable 8-bit register. The duty cycle for Mod is written to this register. The comparator function compares the counter output with the value of the Duty Cycle Register. The output from the comparator is determined by the following rule:

If Counter Value ≤ Duty Cycle Register, Comparator Output = 1,
Else Comparator Output = 0

The output from the comparator is the Mod signal. The duty cycle of the Mod signal is programmable by writing to the Duty Cycle Register and to the Counter Register. If the Counter Register default value is used (decimal 100) the frequency of the Mod signal is 39 kHz (3.9 MHz/100).

An example of the generation of the Mod signal is shown in Figure 10. In this example the Counter Register default value of 100 is used.

Duty Cycle Register = 40
Counter Register = 100

Counter Output   0   20   40   60   80   0   20   40   60

Tone

In this example the duty cycle of the Tone signal is 60:40 (mark:space).
Regardless of the value of the duty cycle, the frequency of the Tone signal is
3.9 MHz/100 = 39 kHz.

C046
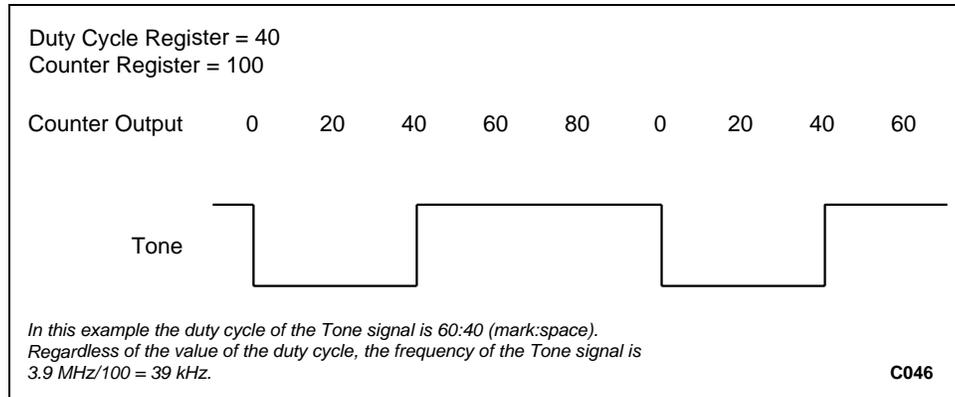
Figure 10. Generation of PWM Mod Pulse Train

Table 16. Example Generation of the Tone Signal

Programmable Parameters :

   Clock Divider Register = 250

   Data Pattern Shift Register = 0xF0F0F0F0F0F0F0F0 (11110000111100001111000011110000b)

Calculation of Tone Frequency :

   Clock Divider Input Clock = 1.95 MHz

   Clock Divider Output = 1.95 MHz/250 = 7800 Hz (F)

   Data Pattern Frequency = F/32 = 7800 Hz/32 = 243.75 Hz

With the above data pattern there are four signal cycles per data pattern cycle. Therefore, the frequency of Tone is:

   $243.75 \text{ Hz} \times 4 = 975 \text{ Hz}$

and the duty cycle of Tone is 50%

The Clock Divider Register is a programmable, 10-bit register. The divider circuit divides down the 1.95 MHz input to the circuit by the value of the register to yield an output signal with frequency F. The output from the divider is used to clock the Data Pattern Shift Register.

The Data Pattern Shift Register is a 32-bit serial shift register. The contents of the programmable Data Pattern Latch Register are downloaded to the Data Pattern Shift Register to set the initial value of the shift register.

The output from the shift register is the tone pulse train, Tone. This output is also fed back to the register input so that the same series of 32 bits are continuously cycled through the register. The data pattern is cycled at a frequency of f2/32.

An example of the generation of the Tone signal is shown in Table 16.

The Mod and Tone pulse trains are ANDed to generate the output from the annunciator circuit.

PWM Control Registers_____

Table 17 shows the address and function of each of the PWM registers. The default value of each of the registers is specified in Table 2.

Autobaud

The Autobaud circuit monitors the SDS_RX input and automatically detects the baud rate of the data received, whether the data is formatted into seven or eight-bit words and whether the parity is odd or even. There are certain restrictions on the baud rate, word length, and characters that can be detected.

When the Autobaud block is enabled, the ARM microcontroller configures all the SDS port parameters except for the baud rate, word length, and parity, which are provided by the Autobaud circuit.

Table 17. PWM Control Registers

Register Address (Hex)	Register Function
0040A00	Control Register for PWM circuit 1: Bit [15:2]: Reserved. Bit [1]: Read the value of the 32-bit Shift Register (0 = read latch, 1 = read Shift Register). Bit [0]: PWM circuit 1 enable (0 = off, 1 = on).
0040A10	Control Register for PWM circuit 2: Bit [15:2]: Reserved. Bit [1]: Read the value of the 32-bit Shift Register (0 = read latch, 1 = read Shift Register). Bit [0]: PWM circuit 2 enable (0 = off, 1 = on).
0040A02	Annunciator Duty Cycle Register for PWM circuit 1: Bit [15:8]: Reserved. Bit [7:0]: Duty cycle.
0040A12	Annunciator Duty Cycle Register for PWM circuit 2: Bit [15:8]: Reserved. Bit [7:0]: Duty cycle.
0040A04	Divider Register for PWM circuit 1: Bit [15:10]: Reserved. Bit [9:0]: Divider ratio.
0040A14	Divider Register for PWM circuit 2: Bit [15:10]: Reserved. Bit [9:0]: Divider ratio.
0040A06	Counter Register for PWM circuit 1: Bit [7:0]: Counter value.
0040A16	Counter Register for PWM circuit 2: Bit [7:0]: Counter value.
0040A08	Data pattern latch for PWM circuit 1: Bit [31:0]: 32-bit data pattern.
0040A18	Data pattern latch for PWM circuit 2: Bit [31:0]: 32-bit data pattern.

After successful derivation of these parameters, the Autobaud circuit programs the SDS port with the information, enables the SDS port, and disables itself. The SDS port will therefore start to receive characters immediately after the "t," "T," or "/" is received as the second character. While the Autobaud block is reprogramming the SDS port, the ARM cannot access the port configuration registers.

After the Autobaud block disables itself, an interrupt is sent to the ARM to indicate that valid data is being received by the SDS port. The values of the characters that were decoded are stored so the ARM can determine which characters were detected.

Autobaud Limitations _____

There are certain limitations on the baud rates, character combinations, and data formats that can be detected by the Autobaud circuit. These limitations are described below.

Baud Rates. The following baud rates can be detected:

- 230.4 kbps
- 115.2 kbps
- 57.6 kbps
- 38.4 kbps
- 19.2 kbps
- 9.6 kbps
- 4.8 kbps
- 2.4 kbps

When a low edge is detected on the SDS_RX signal (indicating a start bit), the Autobaud circuit starts to search for the required set of start characters, determines the baud rate, determines whether the data is formatted into seven bit or eight-bit words, and detects if the parity is odd or even.

Table 18. Autobaud Control Register Functions

Bit	Signal	Function
15:5	N/A	Reserved
4	SDS port loopback enable	Status of this bit indicates whether or not the Autobaud circuit will attempt to disable the hardware loopback in the SDS port on successful detection of an AT sequence. 0 = do not attempt disable of hardware loopback 1 = attempt disable of hardware loopback
3	N/A	Reserved
2	Autobaud detection flag	This bit will be set to "1" whenever a correct Autobaud detection has taken place. The bit can only be cleared by the ARM.
1	Failure interrupt enable	Enable interrupt to the ARM if a failure is detected: 0 = off 1 = on
0	Autobaud enable	Enable the Autobaud function: 0 = off 1 = on

Character Combinations. The following character combinations can be detected:

- at
- AT
- a/
- A/

The detection circuit allows for successive "a" or "A" characters to be received (e.g., "aat" and aAT" are also valid combinations).

Data Formatting. The following data formats can be detected:

- 7-bit data, no parity, 2 stop bits
- 7-bit data, even parity, 1 stop bit
- 7-bit data, odd parity, 1 stop bit
- 8-bit data, no parity, 1 stop bit

Autobaud Registers_____

The Autobaud registers are used to configure and monitor the Autobaud function. The address and default values for the Autobaud registers are specified in Table 2.

Autobaud Control Register. The Autobaud Control Register is used to control the operation of the Autobaud function. The function of each of the bits in this register is described in Table 18.

Autobaud Status Register. The Autobaud Status Register is used to provide the current status of the Autobaud function. The function of each of the bits in this register is described in Table 19. This register is read only.

Failure Register. The Failure Register is used to detect Autobaud failures. If the Autobaud detection fails, one of the bits in the Failure Register will be set to "1." The bit that is set depends on the failure mode. Bits [8:0] in this register are cleared to "0" when the start bit is detected. If the Failure Interrupt Enable bit in the Control Register is set to "1," an interrupt to the ARM is generated when any of these bits is set. The function of each of the bits in this register is described in Table 20.

First Character/Second Character Register. Bits [7:0] store the first character detected during the last Autobaud attempt. Bits [15:8] store the second character detected during the last Autobaud attempt.

Temporary Character Register. When the Autobaud circuit processes an incoming character, the character bits are stored in this register. If the Autobaud function fails, the actual bits received can be read from this register.

Decision Value/Timer Value Registers. The Decision Value/Timer Value Registers are used to determine the baud rate of the incoming data stream by counting the number of 3.9 MHz clock cycles in the start bit. The start bit is a "0" and the first bit of the "A" or "a" character is a "1."

Therefore, the duration of the start bit can be measured by counting the number of clock cycles for which the SDS_RX signal is low. Based on the number of clock cycles counted, the Autobaud circuit decides what the baud rate is and programs the SDS baud rate accordingly.

Table 19. Autobaud Status Register Functions

Bit	Signal	Function
15:7	N/A	Reserved
6	Active	1 = start bit detected and character sequence detection in progress. Bit = 0 at any other time
5	Correct detection	0 = start bit detected 1 = Autobaud detection completed successfully
4:3	Parity	00 = parity detected as no parity 01 = parity detected as even parity 10 = parity detected as odd parity 11 = Invalid
2	Word length	0 = word length successfully detected as seven bits 1 = word length successfully detected as eight bits
1	Second character detected	0 = start bit falling edge detected 1 = second character successfully compared with the set of possible characters ("t," "T," "/")
0	First character detected	0 = start bit falling edge detected 1 = first character successfully compared with the set of possible characters ("a," "A," etc.)

Table 20. Failure Register Functions

Bit	Failure Mode
15:9	Reserved
8	No previous word/parity
7	"At/aT" error
6	Second character stop bit error
5	Second character match error
4	Second character start bit error
3	First character stop bit error
2	First character match error
1	Baud counter overflow
0	Start bit too short

There are eight Decision Value Registers and eight Timer Value Registers. The Decision Value Registers are programmed to set the lower and upper cycle count thresholds for eight different baud rates. There is a threshold overlap in that the upper cycle count threshold for one baud rate is also the lower cycle count threshold for the next higher baud rate. For each baud rate there is a value programmed in one of the Timer Value Registers. The value programmed is the actual value that would be written to the SDS Divider Registers if the Autobaud circuit detected that particular baud rate.

When the Autobaud circuit has counted the number of 3.9 MHz clock cycles in the start bit, it then compares this number of counts with values in the Decision Value Registers. If it detects

that the number of counts lies between two threshold values set by the registers, then the contents of the corresponding Timer Value Register are written to the SDS Port Divider Registers to set the port transmit and receive baud rate.

For the Decision Value Registers, bits[10:0] set the count thresholds. Bits[15:11] are unused. For the Timer Value Registers, bits[15:0] are programmed with the value to be written to the SDS Divider Registers.

Baud Count Register. The Baud Count Register stores the number of 3.9 MHz cycles that the Autobaud circuit has counted in the start bit received on the SDS Rx line.

Table 21. Flow Control/Escape Sequence Detection Control Register Functions

Bit	Signal	Function
15:4	N/A	Reserved
3	Counter enable	Enable/disable the guard time counter used during the escape sequence detection: 0 = counter disabled 1 = counter enabled
2	XOFF enabled	0 = XOFF detection disabled 1 = XOFF detection enabled
1	XON enabled	0 = XON detection disabled 1 = XON detection enabled
0	Escape sequence enable	0 = escape sequence detection disabled 1 = escape sequence detection enabled

Table 22. Flow Control/Escape Sequence Detection Status Register Functions

Bit	Signal	Function
15:3	N/A	Reserved
2	XOFF detected	Set to "1" if the XOFF character has been detected. This bit can be cleared by the ARM.
1	XON detected	Set to "1" if the XON character has been detected. This bit can be cleared by the ARM.
0	Escape sequence detected	Set to "1" if the escape sequence has been detected. This bit can be cleared by the ARM.

Escape Sequence Detection and Flow Control

The function of these blocks is to detect an escape sequence or the XON/XOFF flow control characters on the SDS serial port. The escape sequence is a programmable series of characters (normally "+++") used in some serial communication protocols. The escape sequence is separated from other data by a large guard time.

The detection functions monitor the data bytes received on the SDS_RX line. If the escape character sequence, the XON character, or the XOFF character is detected, the associated flag is set.

Registers for Flow Control/Escape Sequence Detection _____

The Flow Control/Escape Sequence Detection registers include the following:

- Control Register
- Status Register
- Escape Sequence Character Register
- XON Character Register
- XOFF Character Register
- Escape Sequence Timout Register

The address and default values for the Escape Sequence Detection and Flow Control Registers are specified in Table 2.

Flow Control/Escape Sequence Detection Control Register. The Flow Control/Escape Sequence Detection Control Register is used to configure the operation of the Escape Sequence

Detection and Flow Control circuitry. The function of each of the bits in this register is described in Table 21.

Flow Control/Escape Sequence Detection Status Register. The Flow Control/Escape Sequence Detection Status Register is used to indicate the detection status for each of the character sequences (escape sequence, XON, XOFF). The function of each of the bits in this register is described in Table 22.

Escape Sequence Character Register. The Escape Sequence Character Register is used to store the escape sequence character. Bits [7:0] hold the 8-bit character to be compared with the SDS_RX input data to determine if the escape sequence has occurred. The default character is "+." The character must occur three times (e.g., "+++") for the escape sequence to be detected.

XON Character Register. The XON Character Register is used to store the XON character. Bits [7:0] store the 8-bit character that is to be compared with the SDS_Rx input data to determine if the XON character has been received.

XOFF Character Register. The XOFF Character Register is used to store the XOFF character. Bits [7:0] store the 8-bit character that is to be compared with the SDS Rx input data to determine if the XOFF character has been received.

Escape Sequence Timeout Register. The Escape Sequence Timeout Register is used to specify the guard band time. The escape character sequence has a guard band before and after the escape sequence characters. Bits [7:0] of this register set the guard band. The guard band is set as the register contents multiplied by 20 ms. The value of this register should be between 1 and 255.

Bits [15:8] of the Escape Sequence Timeout Register are unused.

Real Time Clock (RTC)

The RTC provides the handset with the current time in seconds, minutes, hours, days, months, and years. The RTC maintains the time information under primary power or battery backup conditions. The real-time information provided by the RTC can be displayed on the handset's Liquid Crystal Display (LCD) or used to calculate call duration.

The RTC also has a programmable alarm which can power down or power up the handset besides providing a time-related alarm to the user. The RTC uses an external 32.768 kHz crystal as a timing reference.

RTC Supply _____

The RTC has a dedicated supply pin, VRTC. Typically, the primary source for the circuit is the handset battery so that the RTC can continue to keep track of real time even when the handset is powered off. A lithium cell can be used as a secondary power source so that the RTC remains powered when the handset battery is removed.

The RTC operates over a voltage range of 2.5 to 3.6 V. The typical current consumption of the RTC is 2 μA.

RTC Crystal. A 32.768 kHz crystal is used as a timing reference by the RTC.

RTC Registers _____

These registers include the following:

- RTC Control Register
- Time Interval Registers
- Alarm Registers

The address and default values for the RTC Registers are specified in Table 2.

RTC Control Register. The RTC Control Register is used to reset the RTC. Writing any data to the register resets all the time and alarm registers. Data written to this register, or read from this register, is "don't care."

The MSB of each of the time interval registers (seconds, minutes, hours, etc) is a "busy" bit which, if set, indicates that a one second edge has occurred and the registers are in the process of being updated. Reading from the RTC Control Register resets the "busy" bit in each of the registers.

Time Interval Registers. The Time Interval registers contain the RTC time values. Six individual registers separately track the time in seconds, minutes, hours, days, months, and years. Each of the registers is eight bits wide. The MSB of each register (bit

7) is a "busy" bit that indicates when a one second edge has occurred and the registers are in the process of being updated. The remaining bits (bits [6:0]) indicate the time.

Reading the contents of each of these registers indicates the current time. Writing to any of the registers increments the value of the register by 1 (e.g., writing to the months register increments the month by 1). The data written to the register is "don't care."

Alarm Registers. The Alarm registers are used to specify the RTC alarm time. When the time indicated by the Time Interval Registers matches the time set in the Alarm Registers, the alarm output from the RTC circuit becomes active. The alarm signal is output from the BP so it can be used to activate or deactivate other parts of the system.

There are separate registers for seconds, minutes, hours, days, months and years. Writing to the registers sets the time at which the next alarm will occur. Reading from the registers returns the time currently programmed for the alarm.

Conexant Serial Bus

The Conexant serial bus is an asynchronous, full duplex serial interface that the BP uses to communicate with other components in the handset system. The Conexant serial bus is used for intra-device communication. The BP acts as bus master and the external component is the bus slave. The maximum data transfer rate is 100 kbits/sec.

The bus uses two signals: SRLDATA and SRLCLK. Both signals are bi-directional and have open drain outputs. The voltages for input and output logic high and logic low levels are specified in Table 23.

Figure 11 and Table 24 show the timing for data transfer using the Conexant serial bus.

Data Transfer Protocol _____

The data on the SRLDATA line must be stable while the SRLCLK signal is high. When the SRLCLK signal is low, the SRLDATA line can change level.

There are exceptions to this rule. When a high to low transition occurs on the SRLDATA line while SRLCLK is high, a start condition is indicated (i.e., the start of the transfer of an undefined number of bytes over the bus). The bus protocol only allows for transfers of byte-wide data. A low to high transition on the data line while the clock line is high indicates a stop condition (i.e., the end of the transfer of one or more bytes of data over the bus).

The bus master (i.e., the BP) always generates the start and stop conditions. The bus is considered to be busy after the start condition and is free again after the stop condition. Figure 12 shows the bit formatting for data transfers over the bus.

Table 23. Serial Bus Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
Input High voltage	V_{IH}		1.5			V
Input low voltage	V_{IL}				0.5	V
Output high voltage	V_{OH}	@ 500 µA I_{OH} (Note 1)	2.4			V
Output low voltage	V_{OL}	@ 3.2 mA I_{OL} (Note 2)			0.4	V
Note 1: I_{OH} is the maximum source current for a "1" output.						
Note 2: I_{OL} is the maximum sink current for a "0" output.						

The bus only allows for byte-wide data transfers. An unrestricted number of bits can be transferred between each start and stop condition. The MSB is transmitted first.

After each byte transfer, the bus master generates an acknowledge-related clock pulse. During this clock pulse, the party that received the data must acknowledge that the data has been received by pulling the SRLDATA line low (the transmitter releases the SRLDATA line during this clock period to allow the receiver to drive the line).

All data transactions between bus master and the bus slave are initiated when the BP issues the Serial Bus Start condition. The BP then sends the device address over the SRLDATA line. The device address consists of seven bits of address and one bit that specifies whether the operation is a read or write (from the perspective of the bus master).

After the device address, the register address is sent by the bus master. Following the register address, the data is placed on the bus by the BP (write operation) or the bus slave (read operation). If more than one byte of data is being transferred, the register address is the starting address and subsequent bytes are read from or written to sequential registers.

Figures 13 through 16 shows the sequence of events for single or multiple byte read and write operations over the Conexant serial bus.

Serial Bus Registers _____

Two registers control the operation of the Conexant serial bus data and clock signals. The address and default values for the Serial Bus Registers are specified in Table 2.

Serial Data Register. The Serial Data Register is used to specify the logic level of the serial data output. Writing to bit [0] of this register places the written logic level on the serial data pin. Reading bit [1] of the register returns the actual logic level of the serial data pin. All other bits in this register are unused.

Serial Clock Register. The Serial Clock Register is used to specify the logic level of the serial clock output. Writing to bit [0] of this register places the written logic level on the serial clock pin. Reading bit [1] of the register returns the actual logic level of serial clock pin. All other bits in this register are unused.

SIM Interface

The BP provides a functional interface to the handset SIM card. Since the BP nominally operates at 2.8 V and produces 2.8 V logic levels, external voltage level translation circuitry is necessary to interface with a 3 V SIM card.

The SIM interface is a half duplex, serial synchronous data link which is fully described in sections 11.11 and 11.12 of the European Telecommunications Standard Institute (ETSI) GSM specifications.

The BP generates a number of SIM interface signals some of which are required by the ETSI definition of the SIM interface (after the external voltage translation circuitry, if required) and some of which implement auxiliary functions required for Conexant's implementation of the SIM Interface. Table 25 provides a summary of these interface signals and their functions.

For the SIM signals that are multiplexed with GPIO signals, the appropriate I/O select bit must be set. See the GPIO section of this Data Sheet for more information.

SIM Interrupts _____

Two different interrupts can be generated by the SIM interface circuitry :

- SIM timer interrupt
- SIM activity interrupt

The SIM timer interrupt is generated when a time out condition occurs. General purpose timer A is used to detect that a time out has occurred. The timer can use the SIM system clock or the SIM Elementary Time Unit (ETU) clock as an input. See the General Purpose Timers section of this Data Sheet for more information.

The SIM activity interrupt is generated when a recognized error has occurred on the SIM interface. Each of these interrupts can be individually enabled or disabled and are described in the section on the SIM Interrupt Enable Register. If the SIM activity interrupt is generated, the ARM can read the SIM Status Register to determine the cause of the interrupt.
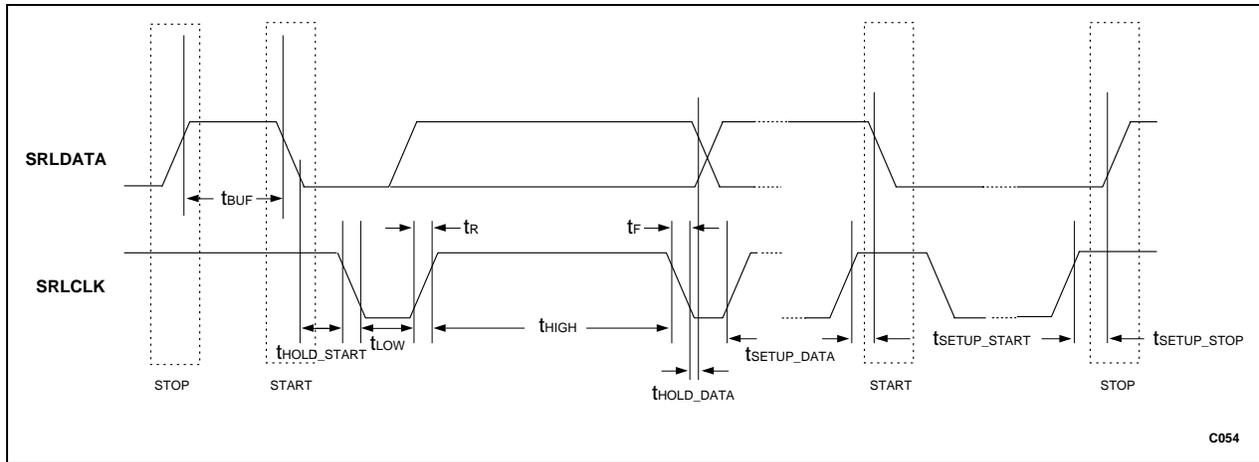
**Figure 11. Timing Data Diagram for the Conexant Serial Bus**

Table 24. BP Timing Requirements for the Conexant Serial Bus

Parameter	Symbol	Min	Max	Units
Serial clock frequency	f_{SERIAL_CLOCK}		100	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7		μs
Hold time start condition. After this period the first clock pulse is generated	t_{HOLD_START}	4		μs
Low period of the clock	t_{LOW}	4.7		μs
High period of the clock	t_{HIGH}	4		μs
Setup time for start condition (only relevant for a repeated start condition)	t_{SETUP_START}	4.7		μs
Hold time SRLDATA	t_{HOLD_DATA}	0 *		μs
Setup time SRLDATA	t_{SETUP_DATA}	250		ns
Rise time of both SRLDATA and SRLCLK lines	t_R		1	μs
Fall time of both SRLDATA and SRLCLK lines	t_F		300	ns
Setup time for stop condition	t_{SETUP_STOP}	4.7		μs
Notes:				
All values referenced to V_{IH} and V_{IL} levels.				
* A transmitter must internally provide a hold time to bridge the undefined region (300 ns maximum) of the falling edge of SRLCLK.				
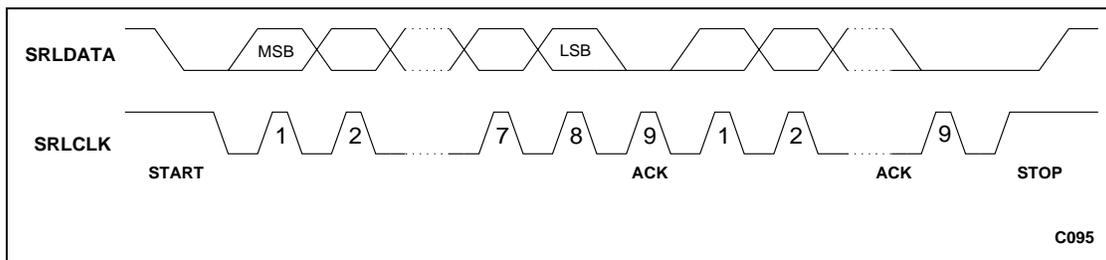
Figure 12. Serial Interface Data Format Diagram

Conexant
Proprietary Information and Specifications are Subject to Change

1	7	1	1	8	1	8	1	1
START	DEVICE ADDRESS	W(0)	A	REGISTER ADDRESS	A	DATA BYTE	A	STOP
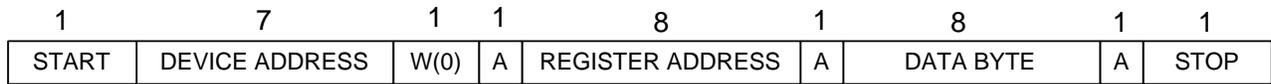
C838

Figure 13. Single Byte Write Operation

1	7	1	1	8	1	8	1	1
START	DEVICE ADDRESS	R(1)	A	REGISTER ADDRESS	A	DATA BYTE	A	STOP

⌐→ From Host CPU

C839a

Figure 14. Single Byte Read Operation

START	DEVICE ADDRESS	W(0)	A	Start Register Address	A	DATA BYTE #1	A	DATA BYTE #2	A	•••	DATA BYTE #n	A	STOP

C840

Figure 15. Sequential or Block Write Operation

START	DEVICE ADDRESS	R(1)	A	Start Register Address	A	DATA BYTE #1	A	DATA BYTE #2	A	•••	DATA BYTE #n	A	STOP

C841

Figure 16. Sequential or Block Read Operation

Table 25. SIM Interface Signals

Signal	Direction	Function	Notes
SIM_DATA	I/O	SIM interface data signal	Required by ETSI specification
SIM_RESET	O	SIM interface reset signal (multiplexed with GPIO Port C[3])	Required by ETSI specification
SIM_CLOCK	O	SIM interface clock signal	Required by ETSI specification
SIM_ENABLE	O	Enable external circuitry to generate SIM supply (multiplexed with GPIO Port C[1])	Required by Conexant implementation
SIM_RW	O	Indicate to external voltage translation circuitry if the SIM transfer is a read or write operation (multiplexed with GPIO Port C[2])	Required by Conexant implementation
SIM_5V_3V	O	Indicate to external voltage translation circuitry if a 3 V SIM card or a 5 V SIM card is being used	Required by Conexant implementation

SIM Interface Registers_____

The following registers are described in this section:

- SIM Control Register
- SIM Status Register
- SIM Interrupt Enable Register
- SIM Interface Registers
- SIM Control Register

The address and default values for the SIM Interface Registers are specified in Table 2.

SIM Control Register. The SIM Control Register controls the operation of the SIM interface. The register is 32 bits wide. The function of each of the bits in this register is described in Table 26.

SIM Status Register. The SIM Status Register provides information on the status of the SIM interface. If a SIM interrupt is received by the ARM, reading this register indicates the source of the interrupt. If the bit is set to a "1," the associated condition has occurred. The register is eight bits wide. The function of each of the bits in this register is described in Table 27.

SIM Interrupt Enable Register. The SIM Interrupt Enable Register is used to mask the SIM interrupts. Each of the SIM interface conditions that can generate a SIM activity interrupt has an associated bit in this register which can be used to enable or disable the generation of the interrupt if the condition occurs. The register is eight bits wide. The function of each of the bits in this register is described in Table 28.

SIM Output Buffer. The SIM Output Buffer is used to store the data to be transmitted over the SIM interface.

SIM Input Buffer. The SIM Input Buffer is used to store the data received over the SIM interface.

DSP Core

The DSP core is a dedicated DSP processor core that implements all the physical layer (Layer 1) signal processing required by a GSM-based handset. The DSP core communicates with the controller core via the Dual Port RAM (DPRAM) memory. The DSP also interfaces to the IA.

Dual Port Memory (DPRAM)

The DSP and ARM cores communicate via the DPRAM. On the ARM side, the DPRAM interfaces to the IPB. Instructions and information are passed between the two cores by writing to and reading from the device DPRAM.

Control Interface

The control interface is a four-wire serial interface that provides an interface between the BP and Conexant's Integrated Analog

(IA) device. The interface is a high speed, synchronous, full duplex, serial communications link. The interface is connected to the DSP of the BP.

The control interface consists of the following signals:

- CNTRLCLK: 3.9 MHz clock signal output from the BP. This is the clock signal for the interface.
- CNTRLRT: indicates the start and end of a communications session. This signal is output from the BP.
- CNTRLDAT: serial output data from the BP.
- RSPNSDAT: serial data input to the BP.

The BP is the bus master for the interface. It initiates all communications over the interface. Using this port, the BP can perform the following functions:

1. Send control information to configure the operation of the IA device.
2. Send bursts of transit data to the IA device for modulation.
3. Read contents of the IA Registers.
4. Figure 17 shows the signal sequence for write and read operations over the control interface.

Codec Interface

The Codec interface is a four-wire serial interface that provides an interface between the BP and the IA device. The interface is a high speed, synchronous, full duplex, serial communications link. The interface is connected to the DSP of the BP.

The Codec interface consists of the following signals:

- CDCCLK: 4 MHz input clock.
- CDCRATE: 8 kHz input framing signal.
- ENCDRDAT: serial data input to the BP. The bit rate is the same as the CDCCLK rate (4 Mbps). The word rate is the same as the CDCRATE signal (8 kwps). Words are 16 bits wide.
- DCDRDAT: serial data output from the BP. The bit rate is the same as the CDCCLK rate (4 Mbps). The word rate is the same as the CDCRATE signal (8 kwps). Words are 16 bits wide.

When a voice call is in progress, the following occurs:

1. In the receive path, digitized audio samples are sent out from the BP using the Codec interface. The digitized samples are converted to an analog signal by the IA and used to drive the handset speaker.
2. In the transmit path, the IA device converts the analog output from the handset microphone into digital samples that are sent to the BP using the Codec interface. The DSP processes the samples for transmission by the handset RF subsystem.

Figure 18 shows the timing diagram for the BP Codec interface.

Table 26. SIM Control Register Functions

Bit	Function
32:30	Reserved
29	Reset all the SIM Registers to their default values: 0 = reset 1 = normal operation
28	SIM_Clock divider ratio: 0 = divide by 1 1 = divide by 2
27:25	Reserved
24:8	Divide ratio to generate SIM ETU from the SIM_Clock signal
7	SIM data transfer convention: 0 = direct convention 1 = inverse convention
6	Enable/disable SIM to ME retransmission: 0 = disabled 1 = enabled
5	Enable/disable ME to SIM retransmission: 0 = disabled 1 = enabled
4	Logic level of SIM_Clock when bit 3 is set to "0": 0 = low 1 = high
3	SIM_CLOCK on/off bit: 0 = off 1 = on
2	SIM_RESET active state: 0 = active low 1 = active high
1	SIM 5V/3V select bit: 0 = 5 V SIM 1 = 3 V SIM
0	SIM enable bit: 0 = off 1 = on

Table 27. SIM Status Register Functions

Bit	Function
7:5	Reserved
4	SIM output buffer empty
3	SIM input buffer full
2	SIM input buffer overrun error
1	SIM to ME receive failure
0	SIM to ME transmit failure

Table 28. SIM Interrupt Enable Register Functions

Bit	Function
7:5	Reserved
4	SIM output buffer empty interrupt enable/disable
3	SIM input buffer full interrupt enable/disable
2	SIM input buffer overrun error interrupt enable/disable
1	SIM to ME receive failure interrupt enable/disable
0	SIM to ME transmit failure interrupt enable/disable

Receive Interface

The receive interface is a three-wire serial interface that provides an interface between the BP and the IA device. The interface is a high speed, synchronous, simplex, serial communications link. The direction of data transfer is from the IA to the BP. The interface is connected to the DSP of the BP. Samples received over the interface are stored in dedicated RAM for processing by the DSP.

The receive interface consists of the following three signals:

- RX_CLOCK: 19.5 MHz clock input.
- RX_RATE: 1.0833 MHz word rate input signal.
- RX_DATA: serial data input to the BP. The data rate is 19.5 Mbps.

Digitized In-Phase and Quadrature (I/Q) samples, recovered from the received RF signal, are sent from the RF subsystem to the BP over this interface. The samples are stored in RAM for further processing by the DSP.

Figure 19 shows the timing diagram for the BP receive interface.

Digital Audio Interface Port

The ETSI specifications for Type Approval testing of a GSM handset (GSM 11.10) require a Digital Audio Interface (DAI) port to verify the handset audio paths and transducers (microphone and speaker). During Type Approval testing, the DAI port interfaces to the System Simulator test equipment.

The DAI Interface is a full duplex serial interface consisting of the following four signals:

- DAI_CLOCK: DAI interface clock output signal
- DAI_RX: DAI interface receive data input signal
- DAI_TX: DAI interface transmit data output signal
- DAI_RESET: DAI interface reset input signal

The DAI signals are multiplexed with GPIO pins on the BP device. To enable the DAI functionality of the pins, a DAI_Enable bit is set to "1" in one of the device registers. Details on the use of the DAI function are described in Conexant's GSM Hardware Designer's Guide (document number 100649).

Table 29 specifies which DAI signals are multiplexed with GPIO pins.

Electrical and Mechanical Specifications _____

The absolute maximum ratings of the BP are provided in Table 30, the recommended operating conditions are specified in Table 31, and the electrical characteristics are specified in Table 32. Note that the BP device has digital outputs with different output drive current capabilities. Table 33 specifies the output drive level of each output pin. Figure 20 shows a block diagram for a typical application of the device. Figure 21 provides the package dimensions for the 160-pin µBGA and Figure 22 provides the shipping tray dimensions.
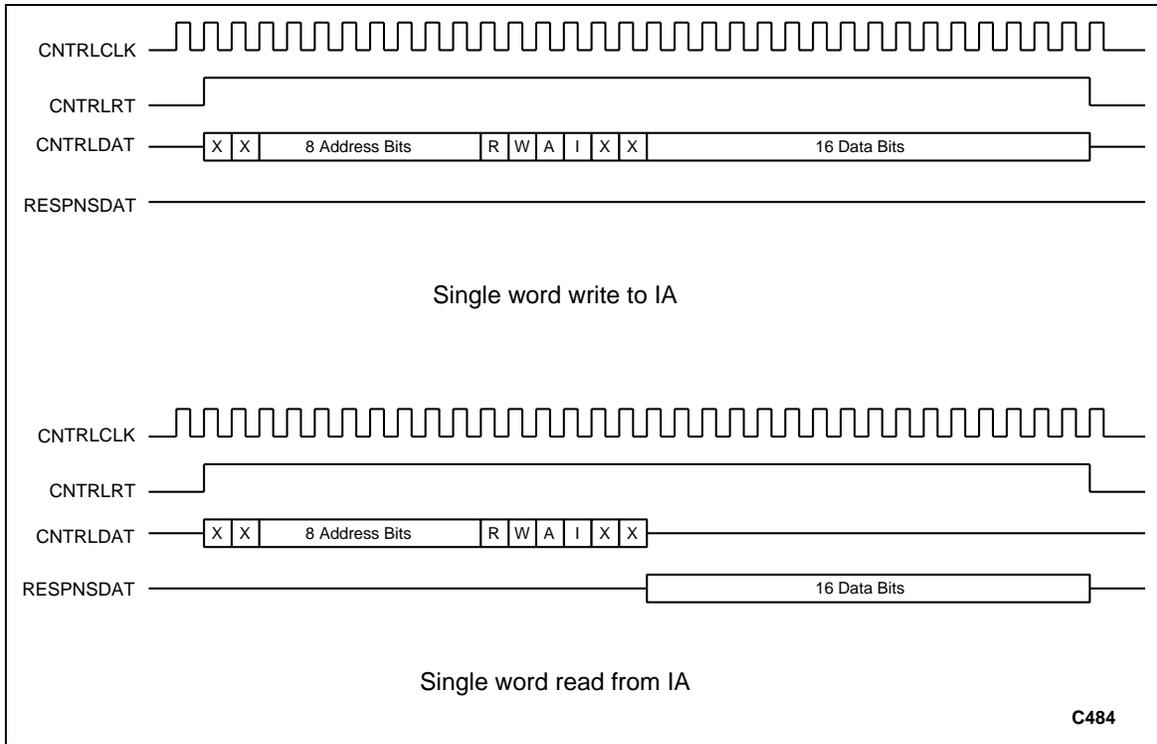
Figure 17. Control Interface Timing Diagram
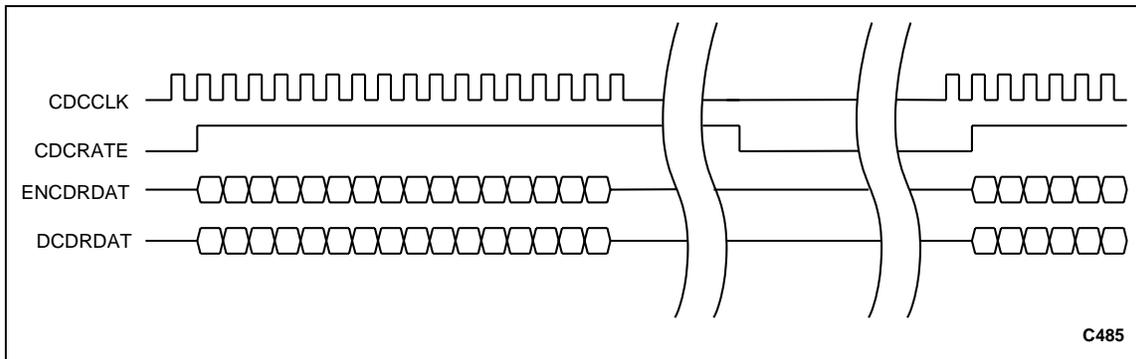
Figure 18. Codec Interface Timing Diagram
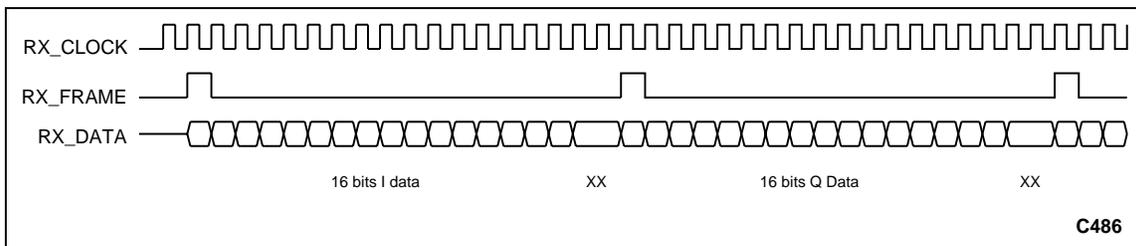
Figure 19. BP Receive Interface Timing Diagram

Table 29. DAI Signal Multiplexing With GPIO Pins

GPIO Pin	DAI Signal
Port B[3]	DAI_CLOCK
Port C[6]	DAI_RX
Port C[5]	DAI_TX
Port B[6]	DAI_RESET

Table 30. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply voltage	V_{dd}	5.6	V
Input voltage	V_{IN}	Vdd + 3.6	V
DC input clamp current	I_{IK}	±10	mA
DC output clamp current	I_{OK}	±10	mA
Static discharge voltage (25 °C)	V_{ESD}	Human Body Model: ±4500 Charged Device Model: ±500	V
Latch-up current (25 °C)	I_{TRIG}	±150	mA
Storage temperature range	T_{STG}	−55 to +150	°C
Notes: Voltages referenced to ground (Vss).			

Table 31. BP Device Recommended Operating Conditions

Parameter	Symbol	Limits	Units
Supply voltage	V_{dd}	+2.7 to +3.6	V
Operating ambient temperature range	TA	−30 to +85	°C
RTC supply voltage	V_{rtc}	+2.5 to +3.6	V

Table 32. BP Device Digital Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Units
Input High voltage (logic 1)	V_{IH}		$0.7 \times$ Vdd		V
Input low voltage (logic 0)	V_{IL}			$0.3 \times$ Vdd	V
Type A output high voltage (logic 1)	V_{OH}	@ 8 mA	2.2		V
Type A output low voltage (logic 0)	V_{OL}	@ 8 mA		0.4	V
Type B output high voltage (logic 1)	V_{OH}	@ 4 mA	2.2		V
Type B output low voltage (logic 0)	V_{OL}	@ 4 mA		0.4	V
Type C output high voltage (logic 1)	V_{OH}	@ 2 mA	2.2		V
Type C output low voltage (logic 0)	V_{OL}	@ 2 mA		0.4	V
Input leakage current	I_{IN}	V_{IN} = 0 V to 5 V		±10	µA
Capacitive load	CL			50	pF
Capacitive drive	CD			50	pF
Note: All voltages referenced to ground (Vss). Currents are positive when flowing into the device.					

Table 33. Digital Output Drive Levels

Pin	Drive Level (mA)
A[21:0]	8
BS[1:0]	8
D[15:0]	8
READ	8
STROBE	8
WRITE	8
GPIO_C[3]	4
SIM_CLK	4
SRLCLK	4
SRLDATA	4
TDO	4
ALARM	2
CLK_REQ	2
CNTRLCLK	2
CNTRLDAT	2
CNTRLRT	2
CS[1:0]	2
DCDRDAT	2
GPIO_A[7:0]	2
GPIO_B[7:0]	2
GPIO_C[2:0]	2
GPIO_C[7:4]	2
GPIO_D[2:0]	2
KPDSTB[7:0]	2
SDS_TX	2
SIM_DATA	2
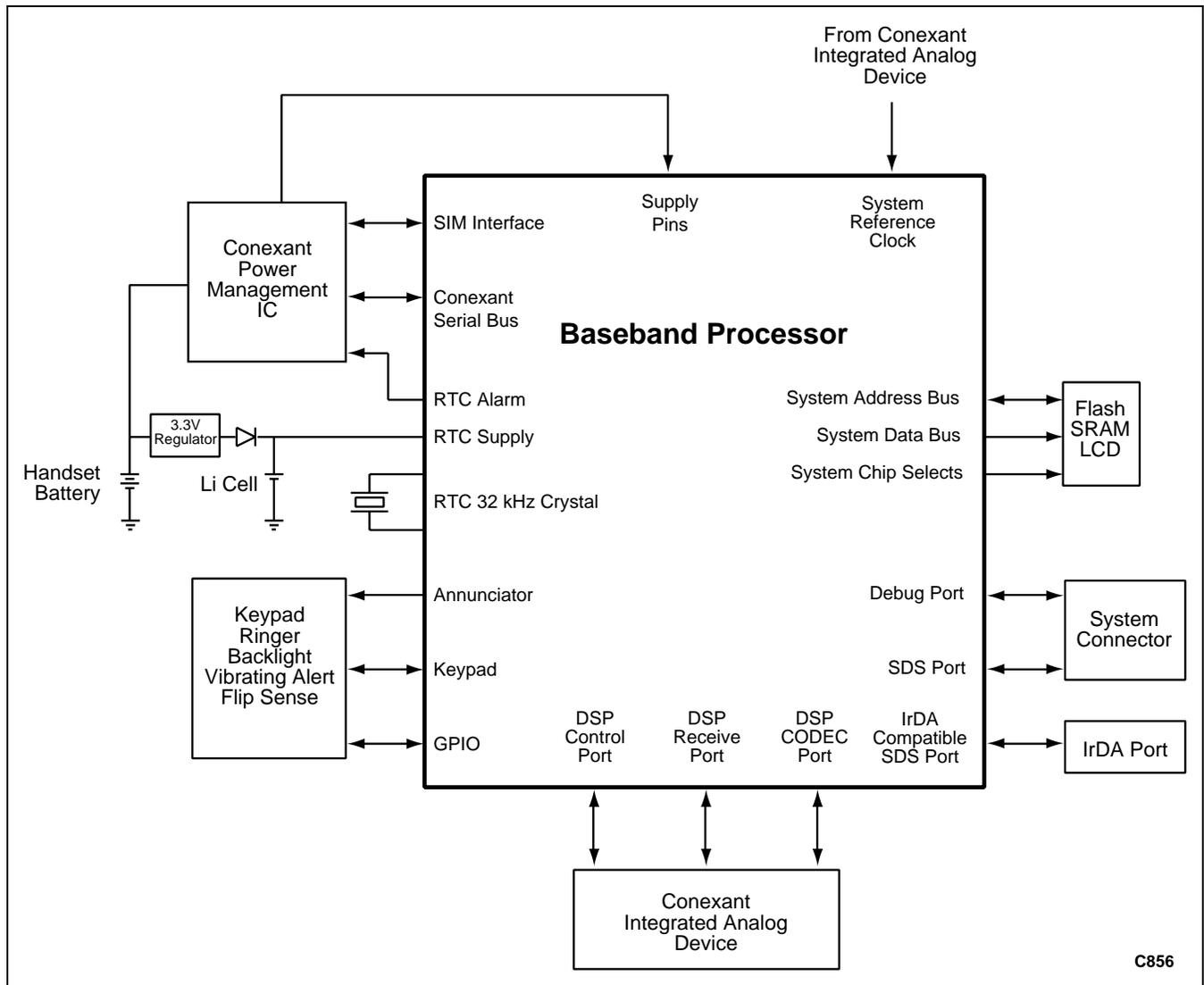
Figure 20. Typical BP Application Block Diagram
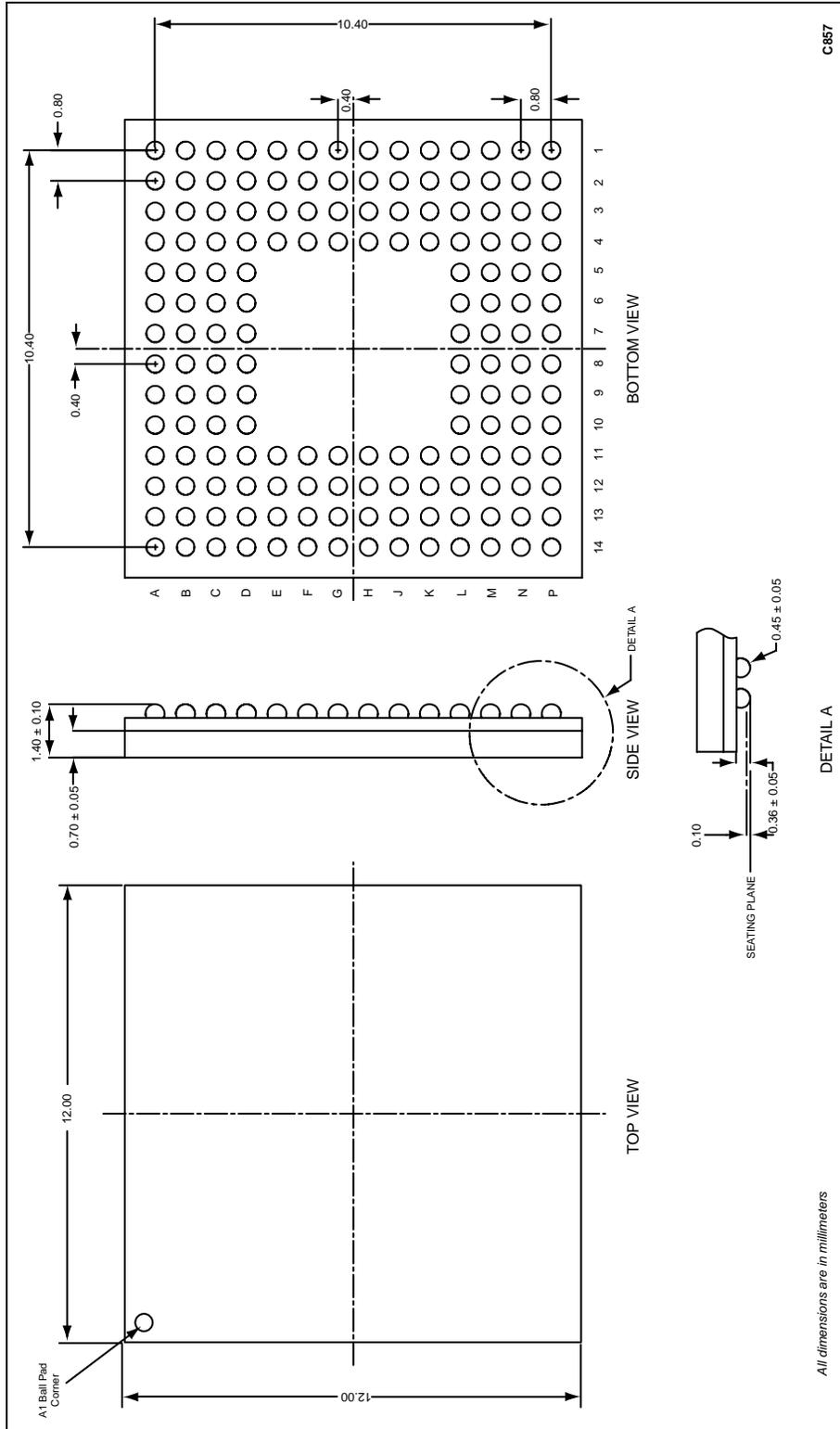
Figure 21. BP 160-Pin μBGA Package Dimensions

Figure 22. BP 160-Pin μBGA Shipping Tray Dimensions
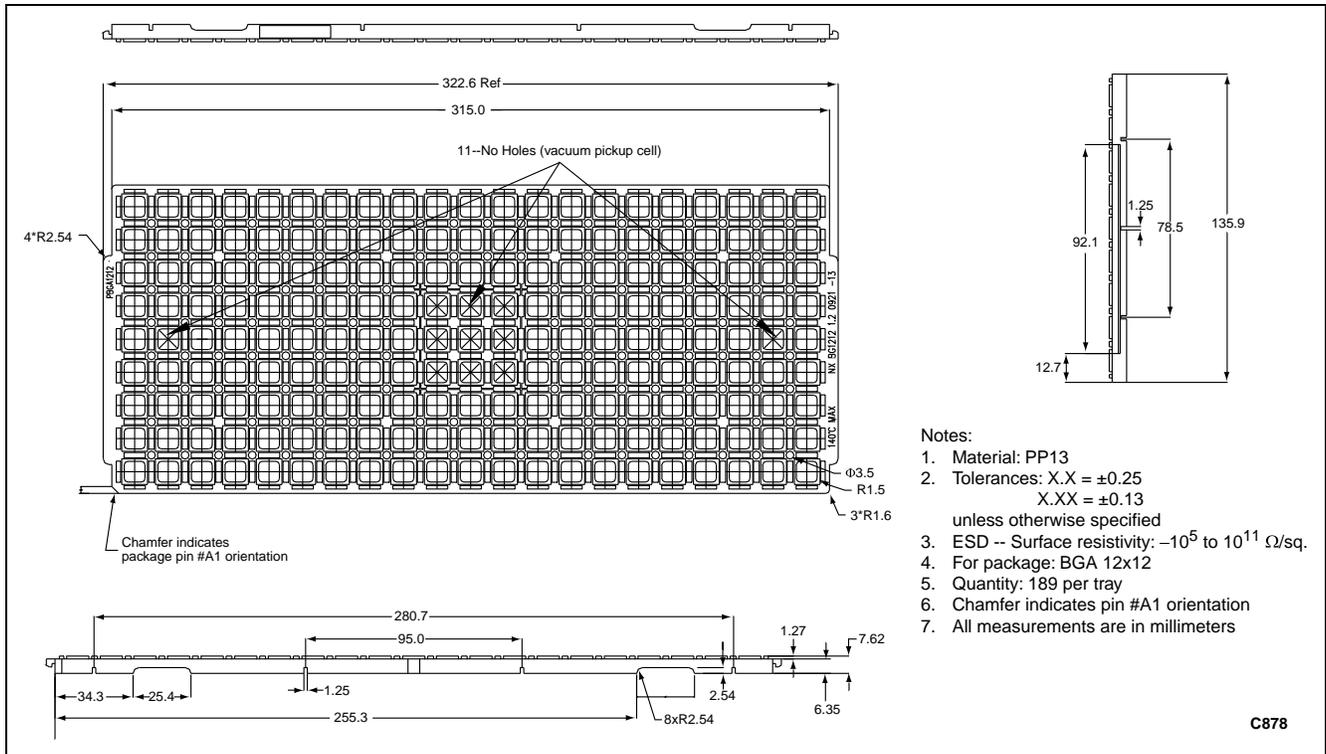
Notes:
1. Material: PP13
2. Tolerances: X.X = ±0.25
                    X.XX = ±0.13
   unless otherwise specified
3. ESD -- Surface resistivity: -10^5 to 10^{11} Ω/sq.
4. For package: BGA 12x12
5. Quantity: 189 per tray
6. Chamfer indicates pin #A1 orientation
7. All measurements are in millimeters

Ordering Information

Model Name	Part Number	DSP Code Version	Comments

Baseband Processor:
        160-pin µBGA package
        160-pin µBGA package
        160-pin µBGA package
	M4640-19
	M4641-19
	M4641-20
		7800
		7A00
		7A00
			Initial production device
			DSP 7A00 required for speech recognition features
			Manufacturing optimization. DSP 7A00 required for speech recognition features

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China – South
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Fax: (852) 2 827-6488

China – South (Satellite)
Phone: (86) 755-518-2495

China – North
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Fax: (86-10) 8529-9778

India
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Fax: (91-11) 692-4712

Korea
Phone: (82-2) 565-2880
Fax: (82-2) 565-1440

Korea (Satellite)
Phone: (82-53) 745-2880
Fax: (82-53) 745-1440

Singapore
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