

MITSUBISHI ICs (TV)
M52042FP

NTSC VIDEO CHROMA SIGNAL PROCESSOR

DESCRIPTION

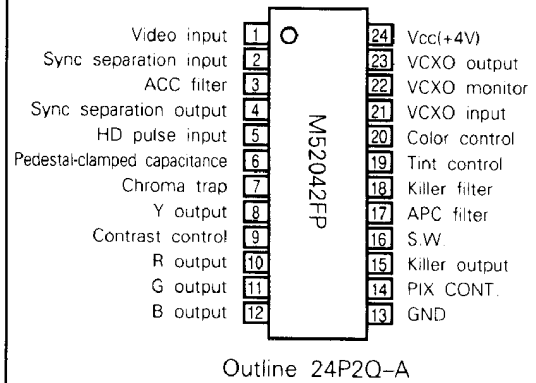
The M52042FP is a semiconductor integrated circuit (IC) for picture signal processing that has been developed for NTSC system LCD color TV.

This IC has a built-in luminance signal processing circuit and color signal processing circuit, which is employed to convert a composite video signal to an RGB signal.

FEATURES

- Low voltage and low power dissipation design
- Built-in Y/C separation circuit and external chroma trap switchable (fc is nearly equal to 1.5MHz.)
- Built-in sync separation circuit
- Provided with Y-signal blanking function by HD pulse
- R.G.B signal output
- Tint, contrast, picture quality and color control linearly adjustable
- 24-pin, shrink pitch, flat package employed
- Same package as in PAL system video chroma IC M52045FP, pin perfectly compatible

PIN CONFIGURATION (TOP VIEW)



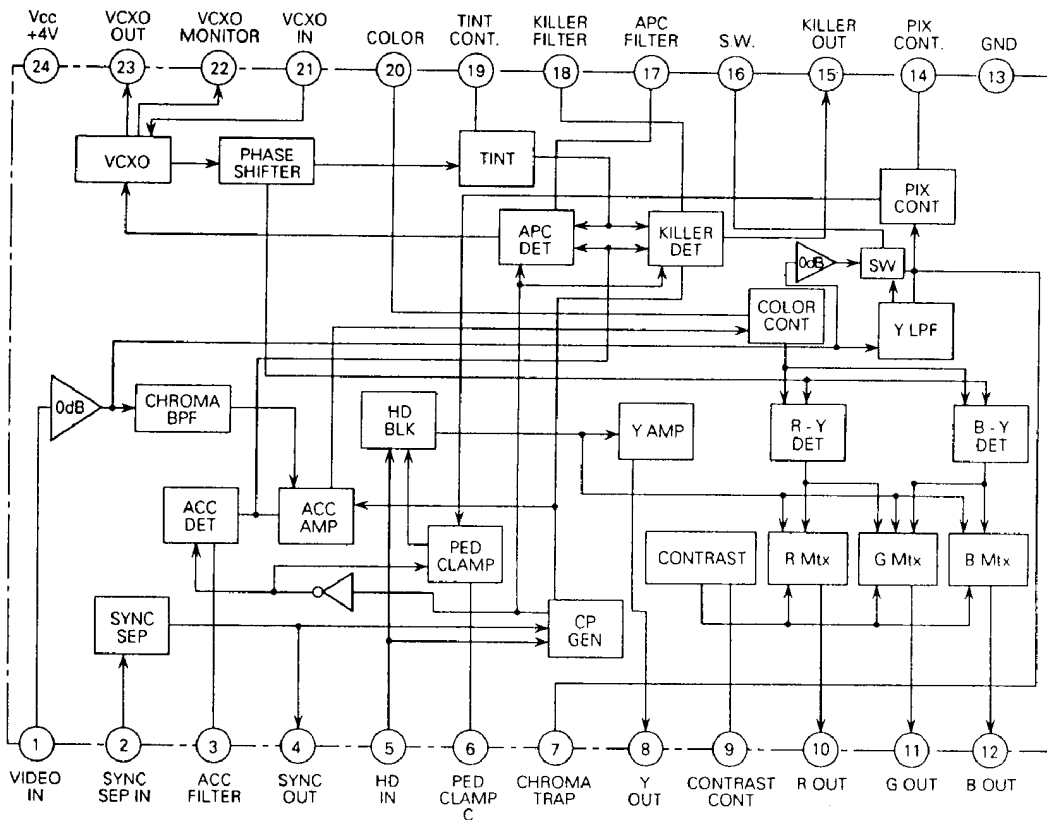
RECOMMENDED OPERATING CONDITION

Supply voltage range 3.7~4.5V
 Rated supply voltage 4.0V

APPLICATION

LCD color TV and LCD color view finder

BLOCK DIAGRAM





NTSC VIDEO CHROMA SIGNAL PROCESSOR

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rated	Unit
V _{CC}	Supply voltage	4.8	V
P _d	Power dissipation	680	mW
T _{opr}	Operating temperature	-10~70	deg
T _{stg}	Storage temperature	-45~120	deg
k _θ	Thermal derating	5.4	mW/deg
V _{max}	Electrostatic capacity	±200 ※	V

※ Charging capacity : 200 pF

ELECTRICAL CHARACTERISTICS (T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test No	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
I _{cc}	Circuit current	1	Input standard color bar signal of V _{CC} =4V.	-	17	21	mA
SYNC SEP Section							
V _{sync 1} V _{sync 7}	SYNC tip voltage	2	Measure each output signal SYNC tip voltage at pins ①, ⑦ when standard color bar signal of 0.7 V _{p-p} is input.	2.20 1.25	2.30 1.40	2.40 1.50	V
V _{sync H} V _{sync L}	SYNC output amplitude	3	Input only SYNC pulse of pulse width 4.7 μ seconds to pin ①. Measure the output amplitude at pin ④ when the input SYNC pulse amplitudes are 0.2 and 0.05 V _{p-p} .	2.7 2.7	3.1 3.1	3.4 3.4	V _{p-p}
T _{sync H} T _{sync L}	SYNC output pulse width	4	Input only SYNC pulse of pulse width 4.7 μ seconds to pin ①. Measure the output amplitude at pin ④ when the input SYNC pulse amplitudes are 0.2 and 0.05 V _{p-p} .	3.7 3.7	4.7 4.7	5.7 5.7	μsec
D _{sync H} D _{sync L}	SYNC output pulse delay	5	Input only SYNC pulse of pulse width 4.7 μ seconds to pin ①. Measure the pulse width + delay time when the input SYNC pulse amplitudes are 0.2 and 0.05 V _{p-p} .	3.7 3.7	4.7 4.7	6.0 6.0	μsec
Video Section							
YLPF(L) YLPF(H)	YLPF frequency characteristics (Pin ⑦)	6	Measure the frequency at which the sine wave output amplitude is -3 dB when the input signal ( 0.2 V _{p-p}) 0.2 V _{p-p} is input. Also measure the output gain at input sine wave 3.58 MHz.	1.45 -30	1.55 -24	- -21	MHz dB
YLPF through	YLPF frequency characteristics (through mode)	7	Measure the frequency at which the sine wave output amplitude is -3dB when the input signal ( 0.2 V _{p-p}) 0.2 V _{p-p} is input, and V16 is 4.0V _{pc} input	5.0	7.0	10.0	MHz
Y _{max}	Maximum output	7	Input standard staircase wave of 0.7 V _{p-p} . Measure the output amplitude at pin ② when V9 is 0 V.	1.1	1.7	1.7	V _{p-p}
GY _{max}	Video amplifier gain	8	Input standard staircase wave of 0.7 V _{p-p} . Calculate the ratio between the output amplitude at pin ② and input amplitude when V9 is 1.7 V.	4.0	6.0	8.0	dB
Y _{ctrast} (1) Y _{ctrast} (2.5) Y _{ctrast} (3.5)	Contrast control characteristics	9	Input standard staircase wave of 0.7 V _{p-p} , and calculate the ratio of the input amplitude to the output amplitude in Test No. 8 above when V9 is changed 1 V, 2.5V and 3.5V.	1.20 -7.3 -	2.45 -5.0 -30	4.50 -2.7 -17	dB
XPIX(4) XPIX(0)	PIX control characteristics	10	Input 1.5 MHz sine wave of 0.2 V _{p-p} to the input. Measure each output amplitude at pin ② when V9 is 1.7 V, and V14 is changed to 2, 4 and 0 V and calculate the ratio between the input amplitude and the output amplitude when V14 = 2 V.	-3.5 10.0	-2.0 12.0	-0.5 14.0	dB dB
GY _{amp}	Y AMP gain	11	Input standard staircase wave of 0.7 V _{p-p} and calculate the ratio between the output amplitude at pin ② and input amplitude.	9.1	11.0	12.6	dB
V _{ped}	PED offset level	12	With input SYNC pulse at 0.2 V _{p-p} , measure pin ③ output pedestal offset, and calculate ratio of the offset to that when 0.7 V _{p-p} standard staircase is input.	0.00	0.05	0.06	

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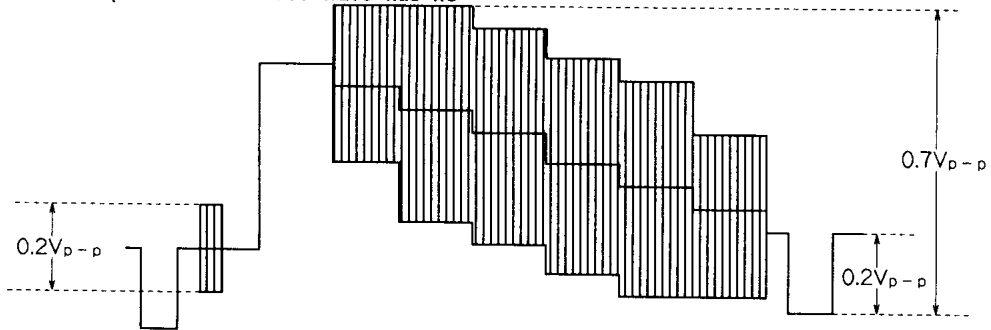
ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test No	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
Chroma Section							
Cacc (+4)	Acc control characteristics	14	Input burst 0.2 V _{p-p} +CW 4.33 MHz shall be 0 dB. Measure the output at pin ⑫ when the input is changed to +4 dB and -20 dB, and calculate the ratio of the measured amplitude to the output amplitude at 0 dB.	0	0.7	1.5	dB
Cacc (-20)				-6.0	-2.0	0	
Ckilor	Killer operation	15	Input a chroma signal of 0.2 V _{p-p} to the input. Reduce the amplitude and measure the amplitude ratio when the voltage at pin ⑮ exceeds 2.5 V.	-53	-49	-43	dB
Cast(4)	Color control characteristics	16	Input burst 0.2 V _{p-p} +CW 4.33 MHz: change V ₂₀ to 2V, 4V, 3V, 1V and 0.5V to measure each output (100kHz beat) amplitude at pin 12, and calculate the ratio between the measured amplitude and the output amplitude at V ₂₀ = 1V.	2	2.2	4.5	dB
Cast(3)				1.5	2.0	4.0	
Cast(1)				-8.5	-6	-4	
Cast(0.5)				-17	-13	-10	
Δ fapc	APC pull-in range	17	Input only SYNC, and after adjusting free run, input 0.2 V _{p-p} CW (0.2 V _{p-p}), then change the frequency. Measure the frequency when VCXO oscillator is placed in a locked condition from the free-run condition.	+400	+600	-	Hz
				-	-300	-200	
DB	B demodulator sensitivity	18	Input CW 4.33 MHz of 0.2 V _{p-p} to the input, and measure the output amplitude at pin ⑫ when V ₂₀ =1 V.	0.8	1.2	1.6	V _{p-p}
R(R/B)	Demodulated output voltage ratio	19	Input CW 4.33 MHz of 0.2 V _{p-p} to the input, measure the output amplitude at pins ⑩, ⑪ when V ₂₀ = 1 V, and calculate the ratio of the measured amplitude to the output amplitude in Test No. 18 above.	0.46	0.52	0.60	-
R(G/B)				0.20	0.30	0.40	
Vkiller H	Killer output voltage H	21	Measure DC voltage at pin ⑮ when 0V and 4V are applied to pin ⑯.	2.5	3.2	-	V
Vkiller L	Killer output voltage L			-	0.20	0.40	
T	TINT control variance	22	Input a chroma signal of 0.4 V _{p-p} to the input, and measure the phase variance at pin ⑫ when 0 V and 4 V are applied to V ₁₉ .	75	85	100	deg
Topen	TINT control characteristics	23	Apply B monochromatic wave(variable phase) 0.4 V _{p-p} and burst 0.2 V _{p-p} to the input. Measure the input phase in which the output at pin ⑫ becomes maximum with V ₁₉ open as burst phase -180 degrees.	-5	+5	+15	deg
Tmin				-55	40	-25	deg
Tmax				+30	-40	+60	
Dhd	HD for chroma delay	24	Apply B monochromatic wave 0.4 V _{p-p} and burst 0.2 V _{p-p} to the input. Measure the delay time from HD pulse rise to thr chroma rise of pin ⑫ output.	-	2.0	2.2	μsec

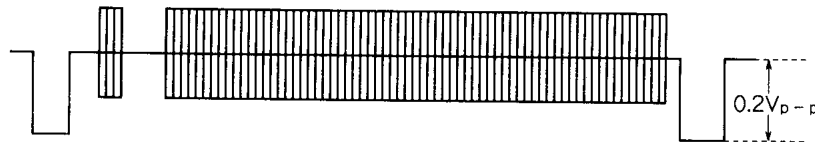
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INPUT SIGNAL

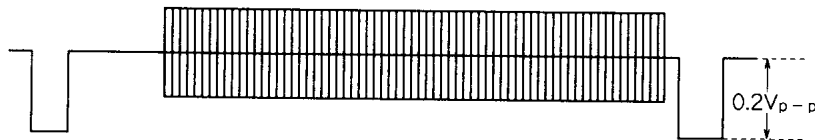
Standard Color Bar-PAL (Standard staircase wave has no chroma signal)



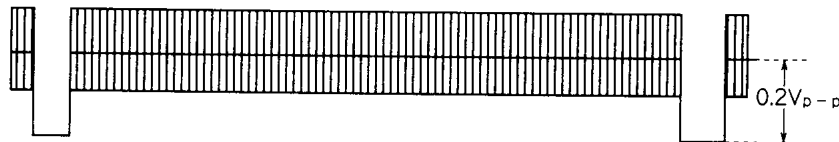
Burst+CW (B monochromatic wave, etc.) PAL



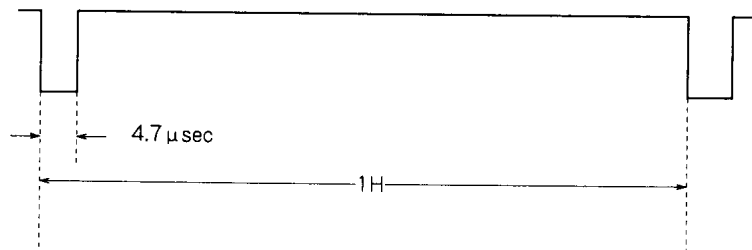
Sine wave



Continuous sine wave (CW)



SYNC pulse



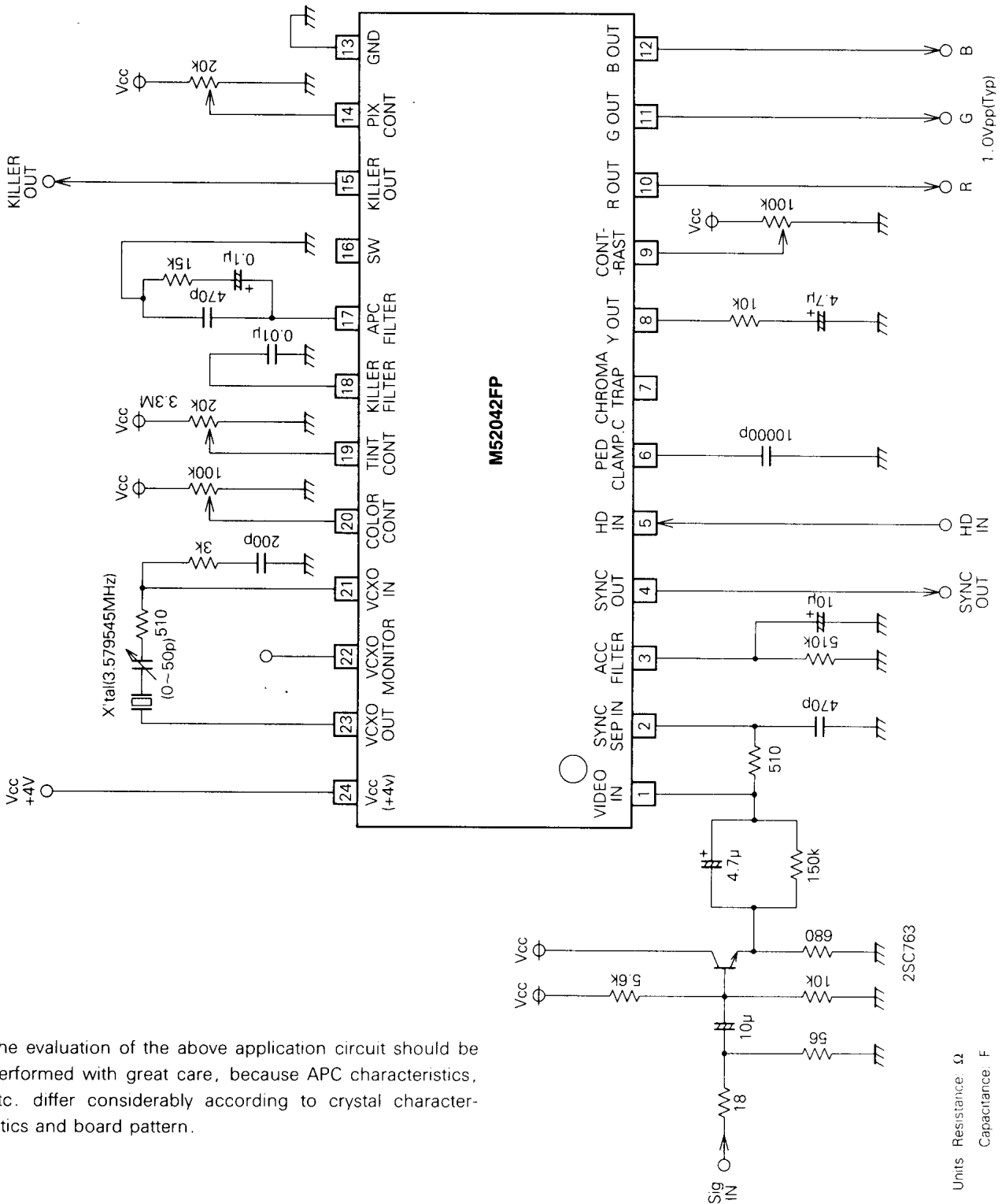
Standard HD signal



M52042FP

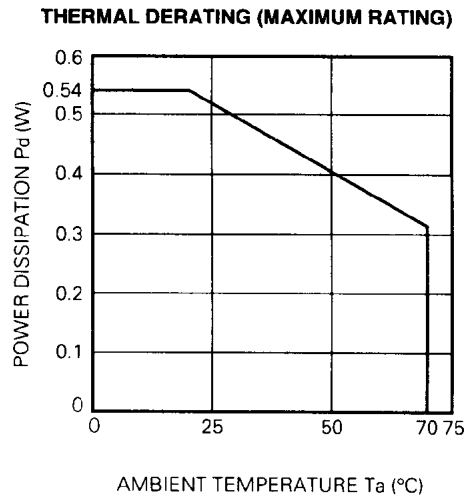
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TEST CIRCUIT



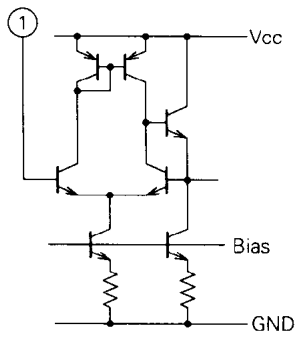
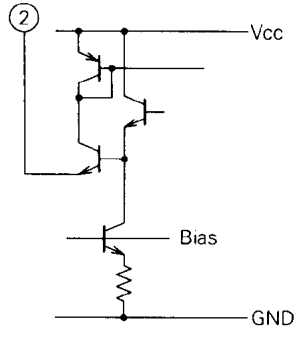
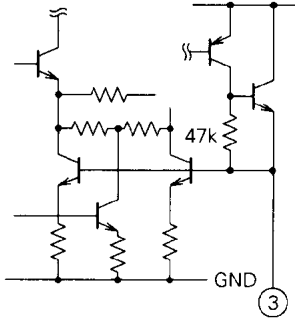
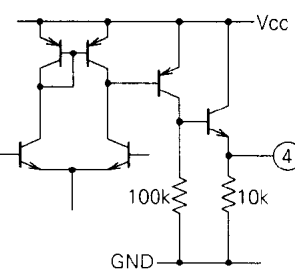
The evaluation of the above application circuit should be performed with great care, because APC characteristics, etc. differ considerably according to crystal characteristics and board pattern.

TYPICAL CHARACTERISTICS



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DESCRIPTION OF PIN

Pin No.	Name	Peripheral circuit of pins
①	VIDEO IN (Video input)	
②	SYNC SEP IN (SYNC separation input)	
③	ACC FILTER	
④	SYNC OUT (SYNC separation output)	

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins
⑤	HD IN (HD pulse input)	
⑥	PED CLAMP C (Pedestal-clamped capacitance)	
⑦	CHROMA TRAP	
⑧	Y OUT (Y output)	

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins
⑨	CONTRAST CONT. (Contrast control)	
⑩	R OUT (R output)	
⑪	G OUT (G output)	
⑫	B OUT (B output)	
⑬	GND (Grounding)	—
⑭	Vcc + 4V (Power supply)	—
⑮	S.W. (Selector switch)	
⑳	VCXO MONITOR	

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins
⑭	PIX CONT. (Picture quality control)	<p>The diagram shows a multi-emitter transistor circuit. The base is connected to Vcc through a resistor. There are three emitters, each connected to a 36k resistor which is in turn connected to GND. The collector is connected to Vcc through a 100k resistor. Pin 14 is connected to the collector.</p>
⑮	KILLER OUT (Killer output)	<p>The diagram shows a multi-emitter transistor circuit. The base is connected to Vcc through a 100k resistor. There are two emitters, each connected to a 100k resistor which is in turn connected to GND. The collector is connected to Vcc through a 150k resistor. Pin 15 is connected to the collector.</p>
⑰	APC FILTER	<p>The diagram shows a multi-emitter transistor circuit. The base is connected to Vcc through a resistor. There are three emitters, each connected to a 10k resistor which is in turn connected to GND. The collector is connected to Vcc through a resistor. Pin 17 is connected to the collector.</p>
⑱	KILLER FILTER	<p>The diagram shows a multi-emitter transistor circuit. The base is connected to Vcc through a resistor. There are three emitters, each connected to a 41k resistor which is in turn connected to GND. The collector is connected to Vcc through a resistor. Pin 18 is connected to the collector.</p>

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DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins
⑲	TINT CONT. (Tint control)	<p>The circuit for Pin 19 is a differential amplifier. It features two input transistors. The base of the upper transistor is connected to Vcc through a 15k resistor. The base of the lower transistor is connected to a Bias input through a resistor. The emitters of both transistors are connected to GND through resistors. The collector of the upper transistor is connected to Vcc through a 2k4 resistor. The collector of the lower transistor is connected to Pin 19 through a 160k resistor. A 15k resistor is also connected between the two bases.</p>
⑳	COLOR (Color control)	<p>The circuit for Pin 20 is a differential amplifier. It features two input transistors. The emitters of both transistors are connected to GND through resistors. The collector of the upper transistor is connected to Vcc through a resistor. The collector of the lower transistor is connected to Pin 20 through a resistor. A diode is connected between the two collectors.</p>
㉑	VCXO IN (VCXO input)	<p>The circuit for Pin 21 is a differential amplifier. It features two input transistors. The base of the upper transistor is connected to Pin 21 through a 22k resistor. The base of the lower transistor is connected to a Bias input through a resistor. The emitters of both transistors are connected to GND through resistors. The collector of the upper transistor is connected to Vcc through a 30k resistor. The collector of the lower transistor is connected to GND through a 2k resistor.</p>
㉓	VCXO OUT (VCXO output)	<p>The circuit for Pin 23 is a differential amplifier. It features two input transistors. The base of the upper transistor is connected to Vcc through a 500 resistor. The base of the lower transistor is connected to a Bias input through a resistor. The emitters of both transistors are connected to GND through resistors. The collector of the upper transistor is connected to Vcc through a 1k resistor. The collector of the lower transistor is connected to Pin 23 through a 15k resistor. A 180 resistor is connected between the two bases.</p>