

M52390FP

NTSC/PAL ENCODER

DESCRIPTION

The M52390FP is a single-chip semiconductor integrated circuit which has a function to convert R/G/B signal to NTSC/PAL composite video signal and the superimpose function.

FEATURES

RGB encode

- LPF for chroma difference signal is built-in. Cutoff frequency control is possible by connecting a resistor externally.
- Because VCA circuit is built-in, gain control at chroma block is possible.
- Carrier leak is on a low level because of built-in high-precision modulation circuit and clamp circuit.
- Burst signal and sync signal are generated within the IC.

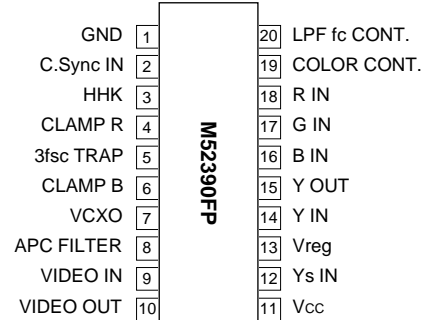
Superimpose function

- Ys IN (control input) is used for switching 2 input signals, VIDEO IN and RGB IN.
- Because high-speed analog switch is built-in, even microscopic characters can be inserted.
- Built-in an APC circuit to adjust tint of the parent picture (VIDEO IN) and the RGB encode signal automatically.

Overall functions

- A drive circuit (75Ω) can be configured with one transistor by outputting the video output signal at 2VP-P.
- This device can be used for both NTSC system and PAL system.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2N-A
(Lead pitch:1.27mm)

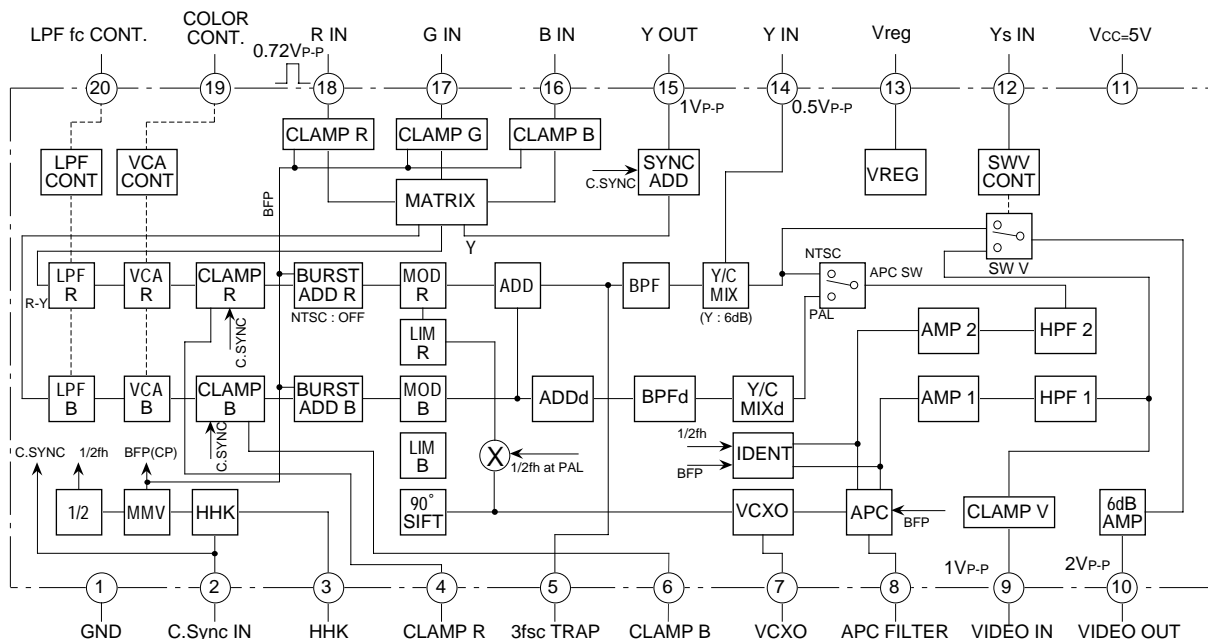
APPLICATION

TV, VCR, monitor, and other AV equipments

RECOMMENDED OPERATING CONDITION

Supply voltage range 4.7 to 5.3V
Rated supply voltage 5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	7	V
Pd	Power dissipation	620 (900)	mW
Topr	Operating temperature	-20 to 75	°C
Tstg	Storage temperature	-40 to 125	°C
K θ	Thermal derating (Ta≥25°C)	6.2 (9.0)	mW/°C

Values in parentheses are those measured when the IC is mounted on a standard board.

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=5V, Sa2=sync input, unless otherwise noted)

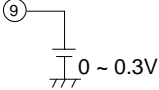
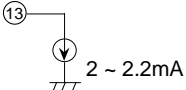

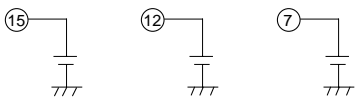
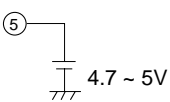
Test No.	Symbol	Parameter	Test conditions	Test point	Limits			Unit
					Min.	Typ.	Max.	
1	Icc1	Current dissipation 1	NTSC MODE ⑫ 5V	⑪	35	50	65	mA
2	Icc2	Current dissipation 2	PAL MODE (SW13 : ON) ⑫ 5V	⑪	37	52	67	mA
RGB IN → Y OUT								
3	ER	Matrix ratio R	SG18 : 1VP-P	⑮	0.27	0.30	0.33	VP-P
4	EG	Matrix ratio G	SG17 : 1VP-P	⑮	0.53	0.59	0.65	VP-P
5	EB	Matrix ratio B	SG16 : 1VP-P	⑮	0.09	0.11	0.13	VP-P
6	EY	Y level at RGB 100%	SG16, SG17, SG18 : 0.71VP-P	⑮	0.63	0.71	0.79	VP-P
7	FR	R IN - Y OUT frequency characteristics	SG18 : 500kHz/5MHz, 0.5VP-P CW SW16, 17, 18 : ON ② 0V (SG2 : OFF)	⑮	-1.5	0	1.5	dB
8	FG	G IN - Y OUT frequency characteristics	SG17 : 500kHz/5MHz, 0.5VP-P CW SW16, 17, 18 : ON ② 0V (SG2 : OFF)	⑮	-1.5	0	1.5	dB
9	FB	B IN - Y OUT frequency characteristics	SG16 : 500kHz/5MHz, 0.5VP-P CW SW16, 17, 18 : ON ② 0V (SG2 : OFF)	⑮	-1.5	0	1.5	dB
10	Vs1	Sync level 1	NTSC MODE	⑮	257	286	315	mVP-P
11	Vs2	Sync level 2	PAL MODE (SW13 : ON)	⑮	270	300	330	mVP-P
Y IN → VIDEO OUT								
12	GY	Y IN - VIDEO OUT Gain	SG14 : 500kHz, 0.5VP-P CW ⑫ 5V	⑩	10.5	12	13.5	dB
13	FY	Y IN - VIDEO OUT frequency characteristics	SG14 : 5MHz, 0.5VP-P CW ⑫ 5V	⑩	-1.5	0	1.5	dB
RGB IN → TRAP								
14	DL(R-Y)	Delay (R-Y)	SG18 : 1VP-P ⑮ 5V, ⑫ 5V, ⑦ 0V	⑤	210	310	410	ns
15	DL(B-Y)	Delay (B-Y)	SG16 : 1VP-P ⑮ 5V, ⑫ 0V, ⑦ 0V	⑤	210	310	410	ns
16	GH(R-Y)	Gain (R-Y) VCA:Hi	SG18 : 500kHz, 0.5VP-P CW SW4, 6, 16, 17, 18 : ON ⑮ 5V, ⑫ 5V, ⑦ 0V, ⑰ 5V/2.5V ② 0V (SG2 : OFF)	⑤	1	2	3.5	dB
17	GH(B-Y)	Gain (B-Y) VCA:Hi	SG16 : 500kHz, 0.5VP-P CW SW4, 6, 16, 17, 18 : ON ⑮ 5V, ⑫ 0V, ⑦ 0V, ⑰ 5V/2.5V ② 0V (SG2 : OFF)	⑤	1	2	3.5	dB
18	GL(R-Y)	Gain (R-Y) VCA:Lo	SG18 : 500kHz, 0.5VP-P CW SW4, 6, 16, 17, 18 : ON ⑮ 5V, ⑫ 5V, ⑦ 0V, ⑰ 0V/2.5V ② 0V (SG2 : OFF)	⑤	-4.5	-3	-2	dB

ELECTRICAL CHARACTERISTICS (cont.)

Test No.	Symbol	Parameter	Test conditions	Test point	Limits			Unit
					Min.	Typ.	Max.	
19	GL(B-Y)	Gain (B-Y) VCA:Lo	SG16 : 500kHz, 0.5V _{P-P} CW SW4, 6, 16, 17, 18 : ON ⑮ 5V, ⑫ 0V, ⑦ 0V, ⑰ 0V/2.5V ② 0V (SG2 : OFF)	⑤	-4.5	-3	-2	dB
RGB IN → VIDEO OUT								
20	VB1	NTSC burst level	NTSC MODE ⑫ 5V	⑩B	243	286	329	mV _{P-P}
21	VB2	PAL burst level	PAL MODE (SW13 : ON) ⑫ 5V	⑩B	255	300	345	mV _{P-P}
22	VB3	PAL burst level difference	PAL MODE (SW13 : ON) ⑫ 5V	⑩B	-30	0	30	mV _{P-P}
23	PPB	PAL burst phase difference	PAL MODE (SW13 : ON) ⑫ 5V	⑩B	82	90	98	deg
24	VR/B	R/burst level ratio	SG18 : 0.71V _{P-P} ⑫ 5V	⑩B	2.68	3.15	3.62	
25	VG/B	G/burst level ratio	SG17 : 0.71V _{P-P} ⑫ 5V	⑩B	2.51	2.95	3.39	
26	VB/B	B/burst level ratio	SG16 : 0.71V _{P-P} ⑫ 5V	⑩B	1.91	2.25	2.59	
27	VC/B	Carrier leak in NTSC mode	NTSC MODE ⑫ 5V	⑩B	-	-40	-28	dB
28	PR/B	R/burst phase difference	SG18 : 0.71V _{P-P} ⑫ 5V	⑩B	96	104	112	deg
29	PG/B	G/burst phase difference	SG17 : 0.71V _{P-P} ⑫ 5V	⑩B	233	241	249	deg
30	PB/B	B/burst phase difference	SG16 : 0.71V _{P-P} ⑫ 5V	⑩B	339	347	355	deg
VIDEO IN → VIDEO OUT								
31	G _{VIO}	VIDEO IN → VIDEO OUT Gain	SG9 : 500kHz, 0.5V _{P-P} CW SW9 : ON ⑫ 0V, ② 0V (SG2 : OFF)	⑩	5	6	7	dB
32	F _{VIO}	VIDEO IN → VIDEO OUT frequency characteristics	SG9 : 5MHz, 0.5V _{P-P} CW SW9 : ON ⑫ 0V, ② 0V (SG2 : OFF)	⑩	-1.5	0	1.5	dB
SUPER IMPOSE								
33	PSI	RGB/VIDEO IN burst phase difference	SG9 : 3.58MHz, 286mV _{P-P} CW SG12 : 1V _{P-P}	⑩B	-5	0	5	deg
34	Vos	DC offset	SG9 : burst, 286mV _{P-P} SG12 : 1V _{P-P}	⑩	-20	0	20	mV
MMV								
35	HHK	HHK width	PAL MODE (SW13 : ON) ⑤ 5V	② ⑮	40	47	54	μs
36	BFPP	BFP point (burst point)	⑤ 5V	② ⑮	4.5	5.6	6.7	μs
37	BFPW	BFP width (burst width)	⑤ 5V	⑮	2.0	2.5	3.0	μs

ELECTRICAL CHARACTERISTICS TEST METHOD

Mode table (common to each test)

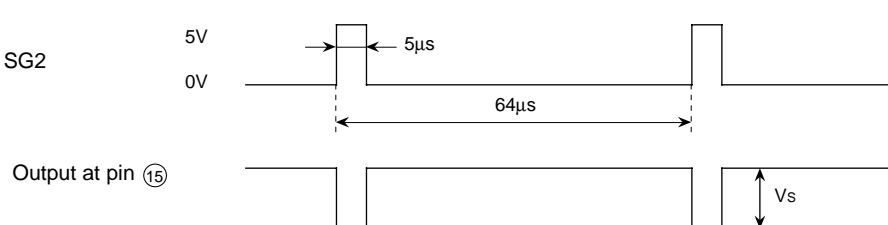
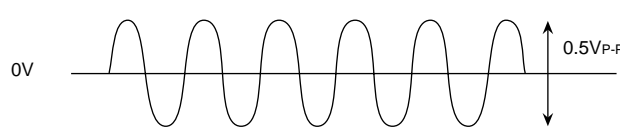
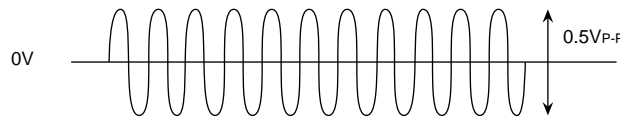
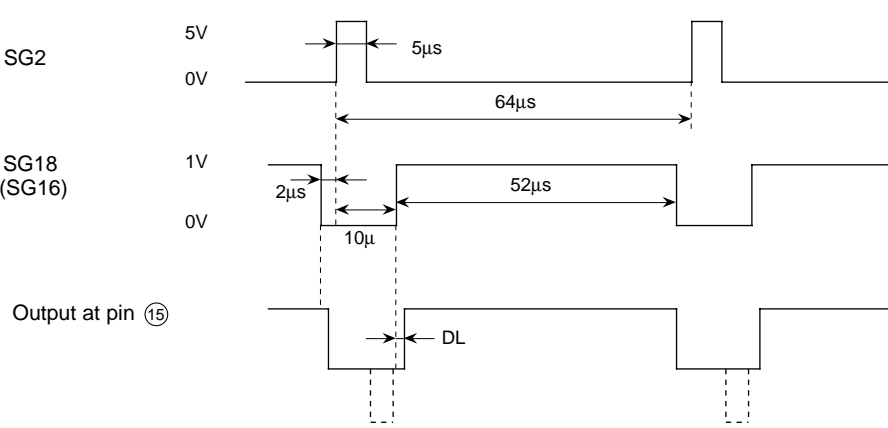
Mode	Conditions	Functions
FREE RUN MODE		VCXO FREE RUN
PAL MODE		Carrier phase for MOD R is inverted on line
SUPER IMPOSE MODE	 <p>Hi : 2 ~ 5V Lo : 0 ~ 1V</p>	<p>⑩ VIDEO OUT RGB ENCODE signal out VIDEO IN signal out</p>
<p>TEST MODE MR TEST MODE MB TEST MODE DR TEST MODE DB</p>	 <p>4.7 ~ 5V 2 ~ 5V OPEN 4.7 ~ 5V 0 ~ 1V OPEN 4.7 ~ 5V 2 ~ 5V 0 ~ 0.3V 4.7 ~ 5V 0 ~ 1V 0 ~ 0.3V</p>	<p>⑤ Chroma difference output MOD R-Y out MOD B-Y out DIFF R-Y out DIFF B-Y out</p>
TEST MODE P		<p>⑮ PULSE output PAL MODE : BFP, HHK mix NTSC MODE : BFP</p>

V4, V6, V9, V16, V17, V18	Voltage at each pin when SYNC is input to pin ② (C.SYNC IN). (In clamp operation)
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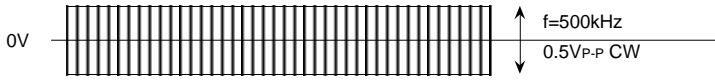
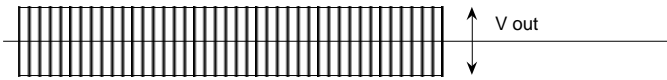
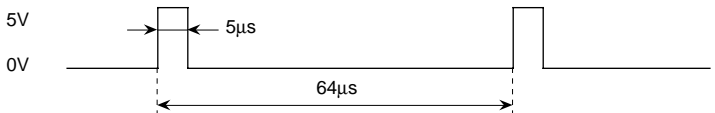

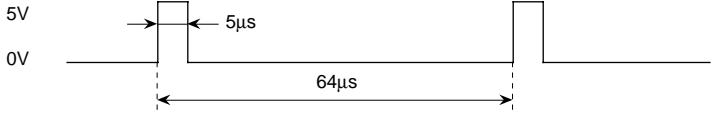

TEST METHOD AND LIMITS CALCULATION METHOD

Test No.	Test method and limits calculation method
1 2	Measure the current to flow in pin ⑪
3 4 5	
6	
7 8 9	<p style="text-align: center;"> $F = 20 \log \frac{V_{out} (5\text{MHz})}{V_{out} (500\text{kHz})} \text{ (dB)}$ </p>

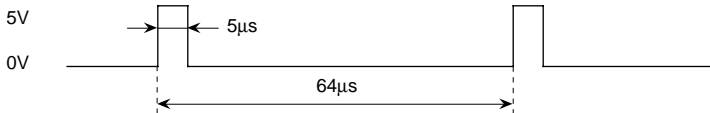
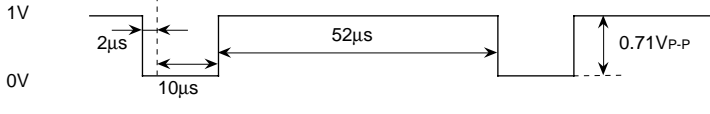
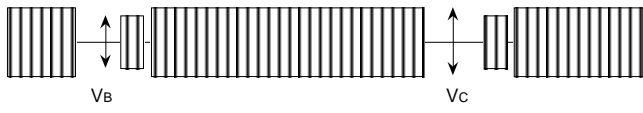
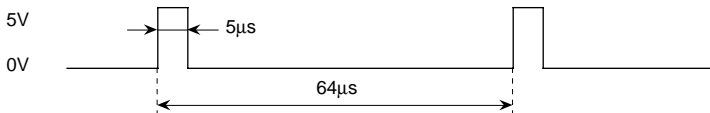
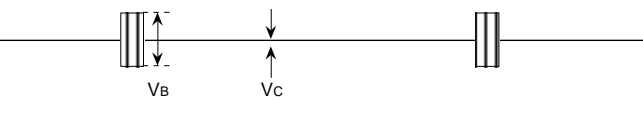
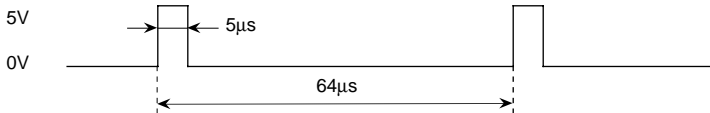
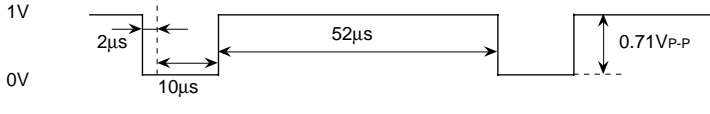
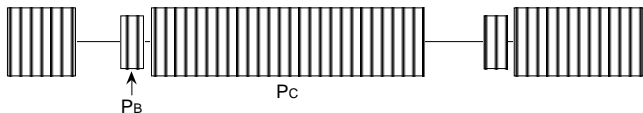
TEST METHOD AND LIMITS CALCULATION METHOD (cont.)

Test No.	Test method and limits calculation method
<p>10 11</p>	<p>SG2</p>  <p>Output at pin ⑮</p>
<p>12</p>	<p>SG14</p>  <p>.Frequency:500kHz</p> <p>Measure the element of 500kHz at pin ⑩ (V₁₂) and calculate GY as follows.</p> $G_Y = 20 \log \frac{V_{12}}{0.5V_{P-P}} \text{ (dB)}$
<p>13</p>	<p>SG14</p>  <p>.Frequency:5MHz</p> <p>Measure the element of 5MHz at pin ⑩ (V₁₃) and calculate fcY as follows.</p> $f_{cY} = 20 \log \frac{V_{13}}{V_{12}} \text{ (dB)}$
<p>14 (15)</p>	<p>SG2</p>  <p>SG18 (SG16)</p> <p>Output at pin ⑮</p>

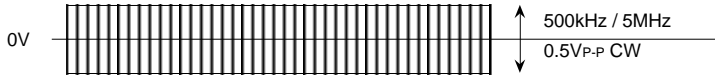
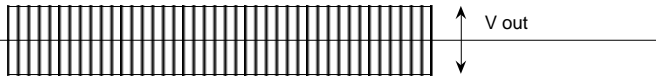
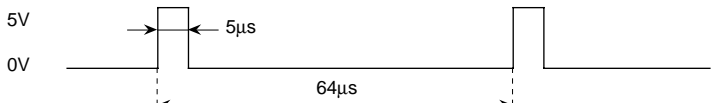

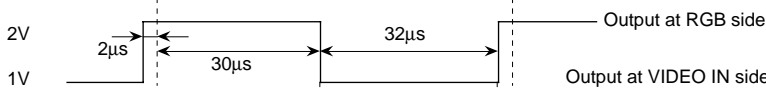
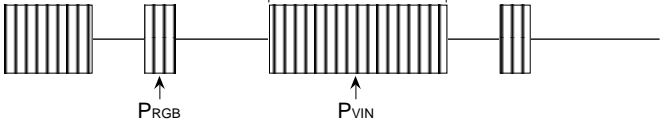
TEST METHOD AND LIMITS CALCULATION METHOD (cont.)

Test No.	Test method and limits calculation method
<p>16 (17) 18 (19)</p>	<p>SG18 (SG16)</p>  <p>Output at pin ⑮</p>  $GH = 20 \log \frac{V_{out} \text{ (⑰) } 5V}{V_{out} \text{ (⑰) } 2.5V} \text{ (dB)}$ $GL = 20 \log \frac{V_{out} \text{ (⑰) } 5V}{V_{out} \text{ (⑰) } 2.5V} \text{ (dB)}$
<p>20 21 22</p>	<p>SG2</p>  <p>Output at pin ⑩B</p>  $V_{B1} = V_{nH}$ $V_{B2} = V_{nH}$ $V_{B3} = V_{nH} - V_{(n+1)H}$
<p>23</p>	<p>SG2</p>  <p>Output at pin ⑩B</p>  $P_{PB} = P_{nH} \text{ burst phase} - P_{(n+1)H} \text{ burst phase} $

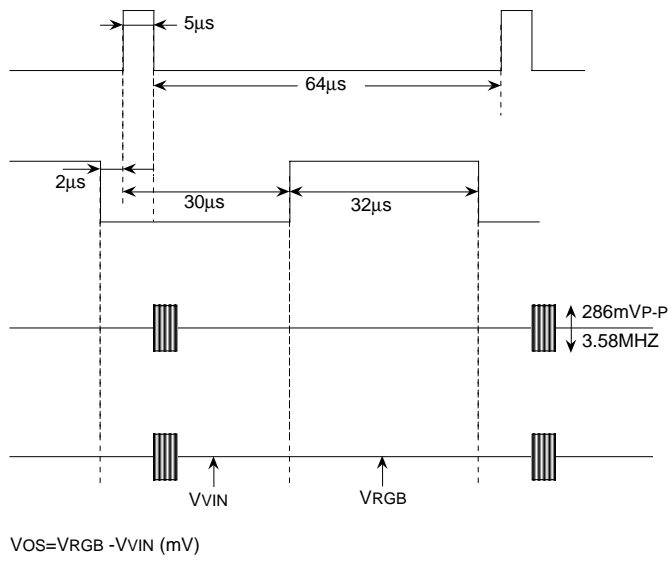
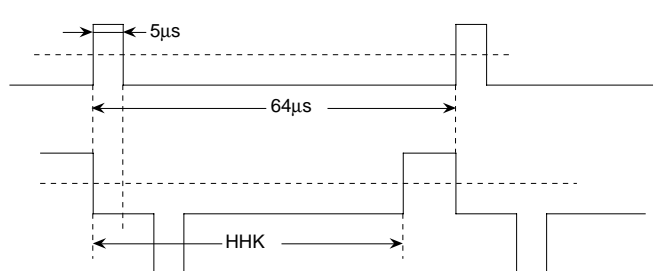
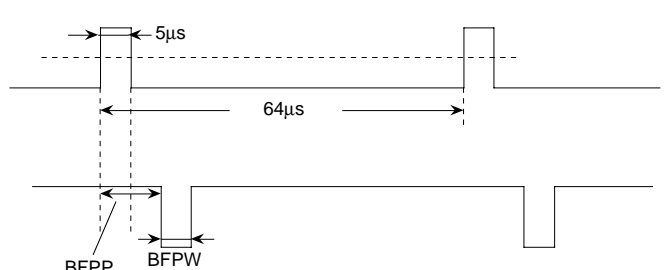
TEST METHOD AND LIMITS CALCULATION METHOD (cont.)

Test No.	Test method and limits calculation method
<p>24 (25) (26)</p>	<p>SG2</p>  <p>SG18 (SG17) (SG16)</p>  <p>Output at pin ⑩B</p>  $R(G, B) / \text{Burst level ratio} = \frac{V_c}{V_B}$
<p>27</p>	<p>SG2</p>  <p>Output at pin ⑩B</p>  $VC/B = 20 \log \frac{V_c}{V_B} \text{ (dB)}$
<p>28 (29) (30)</p>	<p>SG2</p>  <p>SG18 (SG17) (SG16)</p>  <p>Output at pin ⑩B</p>  $R(G, B) / \text{Burst phase difference} = P_c - P_b \text{ (deg)}$

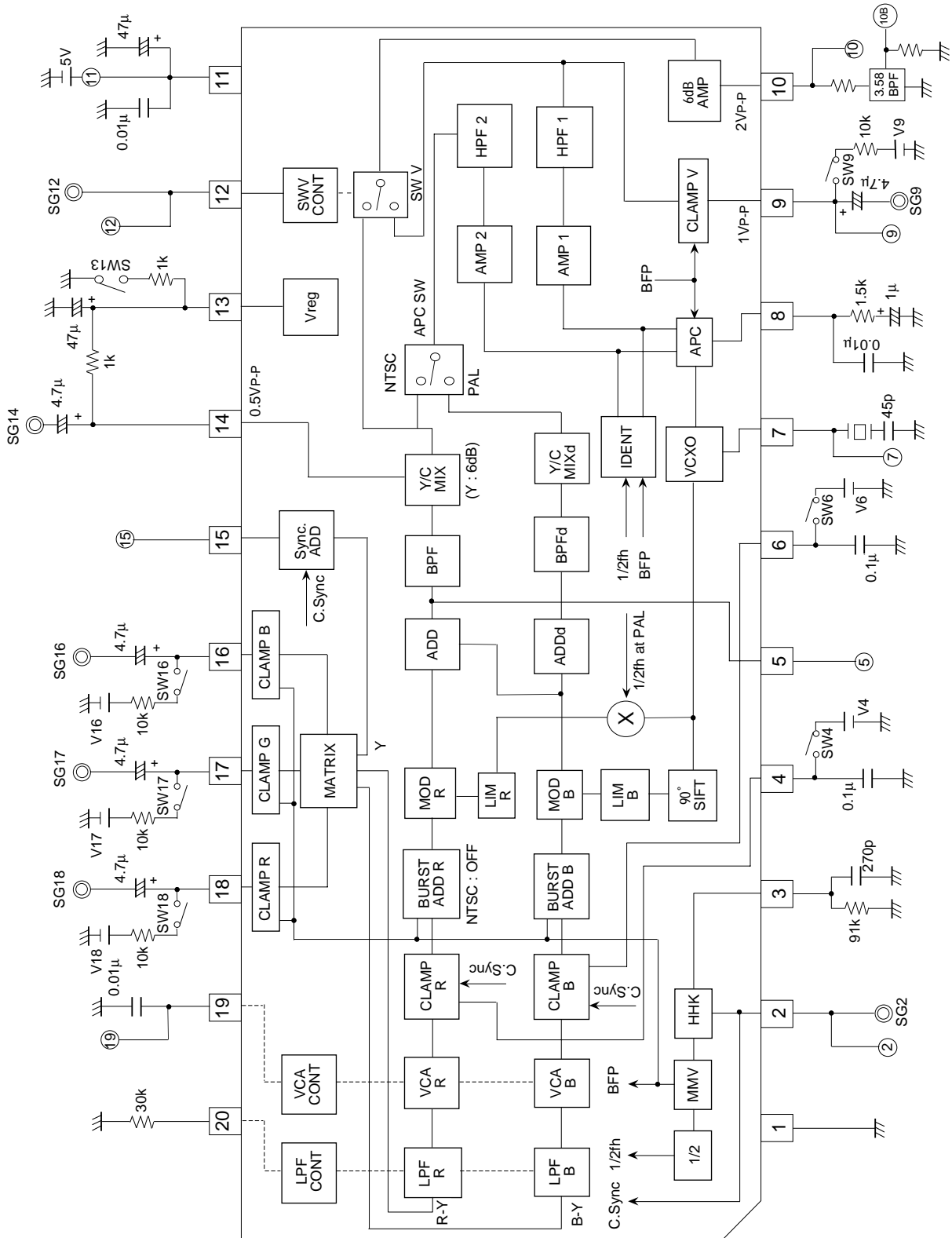
TEST METHOD AND LIMITS CALCULATION METHOD (cont.)

Test No.	Test method and limits calculation method
<p>31 32</p>	<p>SG9 </p> <p>Output at pin ⑩ </p> $G_{VIO} = 20 \log \frac{V_{out} (500kHz)}{0.5V_{P-P}} \text{ (dB)}$ $F_{VIO} = 20 \log \frac{V_{out} (5MHz)}{V_{out} (500kHz)} \text{ (dB)}$
<p>33</p>	<p>SG2 </p> <p>SG9 </p> <p>SG12 </p> <p>Output at pin ⑩ </p> $P_{SI} = P_{RGB} - P_{VIN} \text{ (deg)}$

TEST METHOD AND LIMITS CALCULATION METHOD (cont.)

Test No.	Test method and limits calculation method	
34	<p>SG2</p> <p>5V</p> <p>0V</p> <p>SG12</p> <p>2V</p> <p>1V</p> <p>SG9</p> <p>0V</p> <p>output at pin ⑩</p> <p>0V</p>	 <p>VOS=VRGB - VVIN (mV)</p>
35	<p>SG2</p> <p>5V</p> <p>2.5V</p> <p>0V</p> <p>output at pin ⑮</p> <p>2.8V</p>	 <p>HHK</p>
36 37	<p>SG2</p> <p>5V</p> <p>2.5V</p> <p>0V</p> <p>output at pin ⑮</p>	 <p>BFPP</p> <p>BFPW</p>

TEST CIRCUIT



Unit Resistance : Ω
Capacitance : F

PRECAUTIONS FOR APPLICATION

(1) Input signal

Pin No.	Name	Specifications
②	C.Sync IN	<p>5V 0V $V_{TH}=2.5V$</p>
⑨	VIDEO IN In case that no signal is input, this pin should be set to free run mode.	<p>100IRE 40IRE 40IRE V_{DL} Refer to (9) 1VP-P 286mVP-P</p>
⑫	Ys	<p>RGB ENCODE OUTPUT 2V 1V $V_{TH}=1.5V$ Ys DL Refer to (9) VIDEO OUTPUT VIDEO OUTPUT</p>
⑯ ⑰ ⑱	B IN G IN R IN	<p>0.71VP-P</p>

(2) Setting of free run frequency

In this IC, the VCXO circuit generates fsc. Therefore, set the oscillator frequency of VCXO to fsc as follows before using this IC.

- 1) Connect pin ⑨ (VIDEO IN) to GND and set it to free run mode.
- 2) V4 is the voltage at pin ④ (OFFSET R) when sync is input to pin ② (C.Sync IN). Apply voltage $V4 - 0.5V$ to pin ④ (OFFSET R).
- 3) Set pin ② (C.Sync IN) to H. (5V is applied.)
- 4) Set the output frequency at pin ⑤ (TRAP) by adjusting the trimmer capacitor at pin ⑦ (VCXO IN).

(3) Setting of chroma difference LPF

The frequency characteristics of the chroma difference LPF which is built in this IC can be set as shown in Fig. 1 by connecting a resistor externally to pin ⑳ (fc CONT.).

The group delay characteristics also change as shown in Fig. 2.

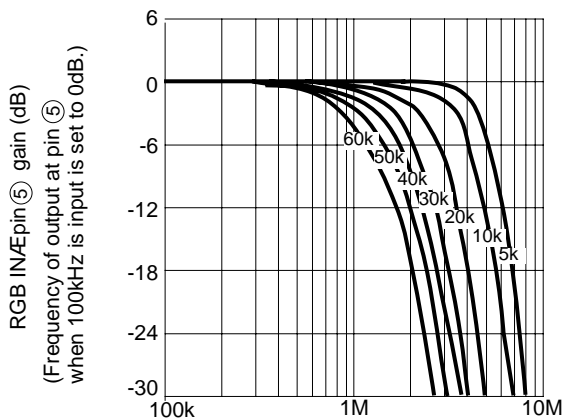


Fig. 1 Frequency characteristics of color difference LPF
 (As for the test conditions, refer to test No.14 and 15.)

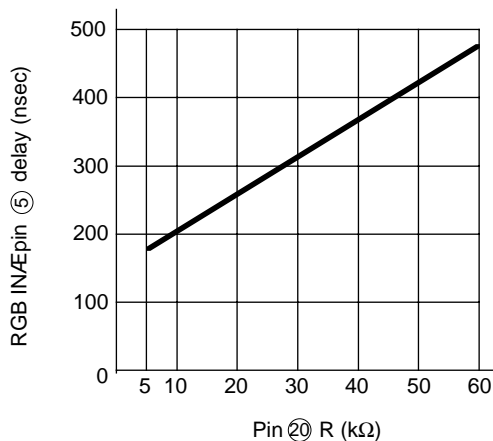


Fig. 2 Group delay characteristics of color difference LPF
 (As for the test conditions, refer to test No.14 and 15.)

(4) Setting of Y DL

The group delay characteristics of color signal of RGB encode output changes by connecting a resistor externally to pin ⑳ (fc CONT.). Therefore, set Y DL based on the delay volume (group delay volume derived from group delay characteristics + 40ns).

In case that a trap circuit is connected to pin ⑤, take the delay from +5 to +10ns into consideration.

(5) Color control characteristics

Gain in chroma section can be set as shown in Fig. 3 by applying voltage to pin ⑲ (COLOR CONT.). (The burst amplitude is fixed.)

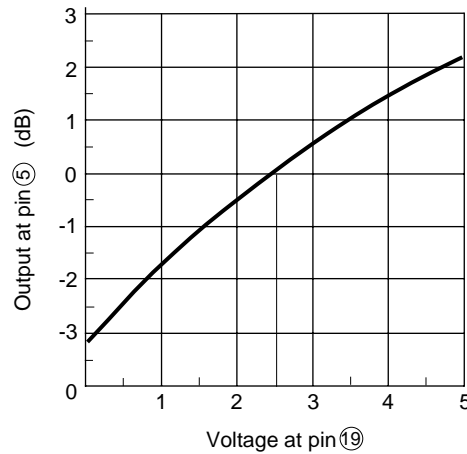


Fig. 3 Color control characteristics
 (As for the test conditions, refer to test No.16, 17, 18 and 19.)

(6) Relation between BFP and HHK

The pulse width of GFP and HHK can be set as shown in Fig. 4 by connecting DR externally to pin ③ (HHK).

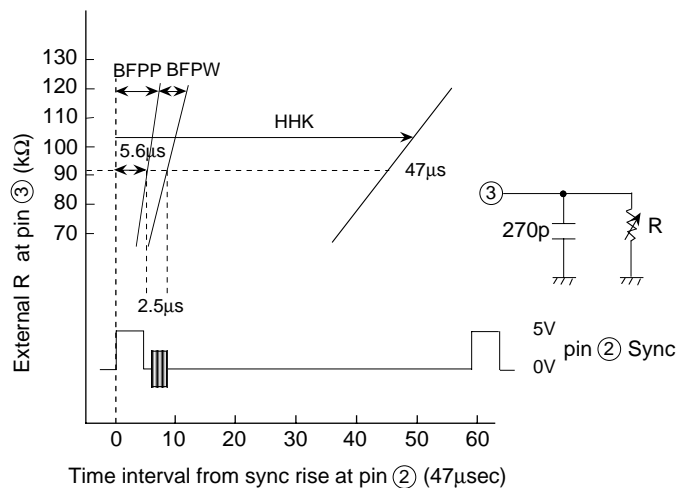
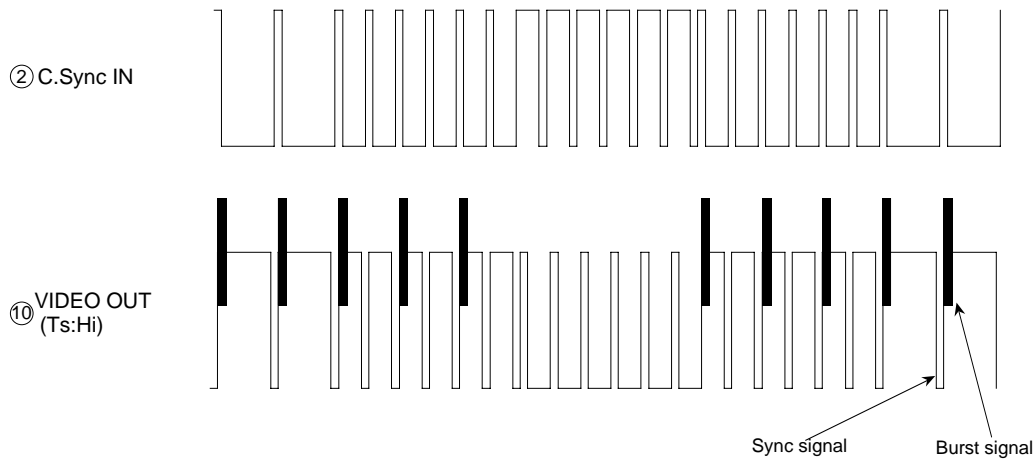


Fig. 4 RC product at pin ③ vs. internal pulse
 (As for the test conditions, refer to test No.35, 36 and 37.)

(7) Driving of input pins

Drive pins ⑨, ⑯, ⑰ and ⑱ at low impedance because they are clamped by IC input.

(8) I/O relation between sync signal and burst signal during the period V

I/O relation between sync signal and burst signal

(9) Setting of V DL and Ys DL in superimpose mode

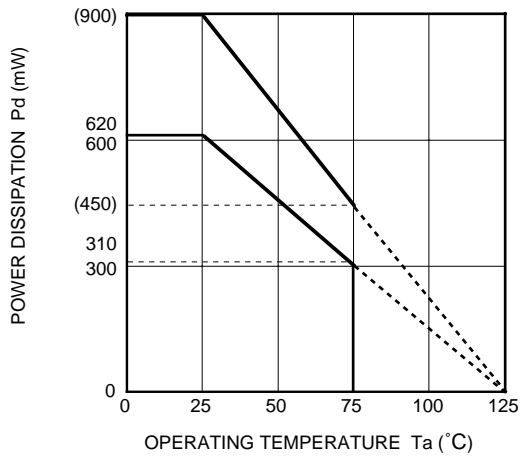
- 1) V DL is used to adjust the timing of RGB encode signal and VIDEO IN signal.
- 2) Ys DL is used to adjust the timing of RGB encode signal and Ys IN signal.
- 3) In case that signals are input to C.SYNC IN, RGB IN, VIDEO IN or Ys IN at the same timing, set V DL and Ys DL based on the delay volume as below.

$$V DL = Y DL (\text{Refer to (4)}) + 10 (\text{nsec})$$

$$Ys DL = Y DL - 10 (\text{nsec})$$

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



Values are measured when any external circuits are connected to this IC.
 Values in parentheses are those measured when the IC is mounted on a standard board.

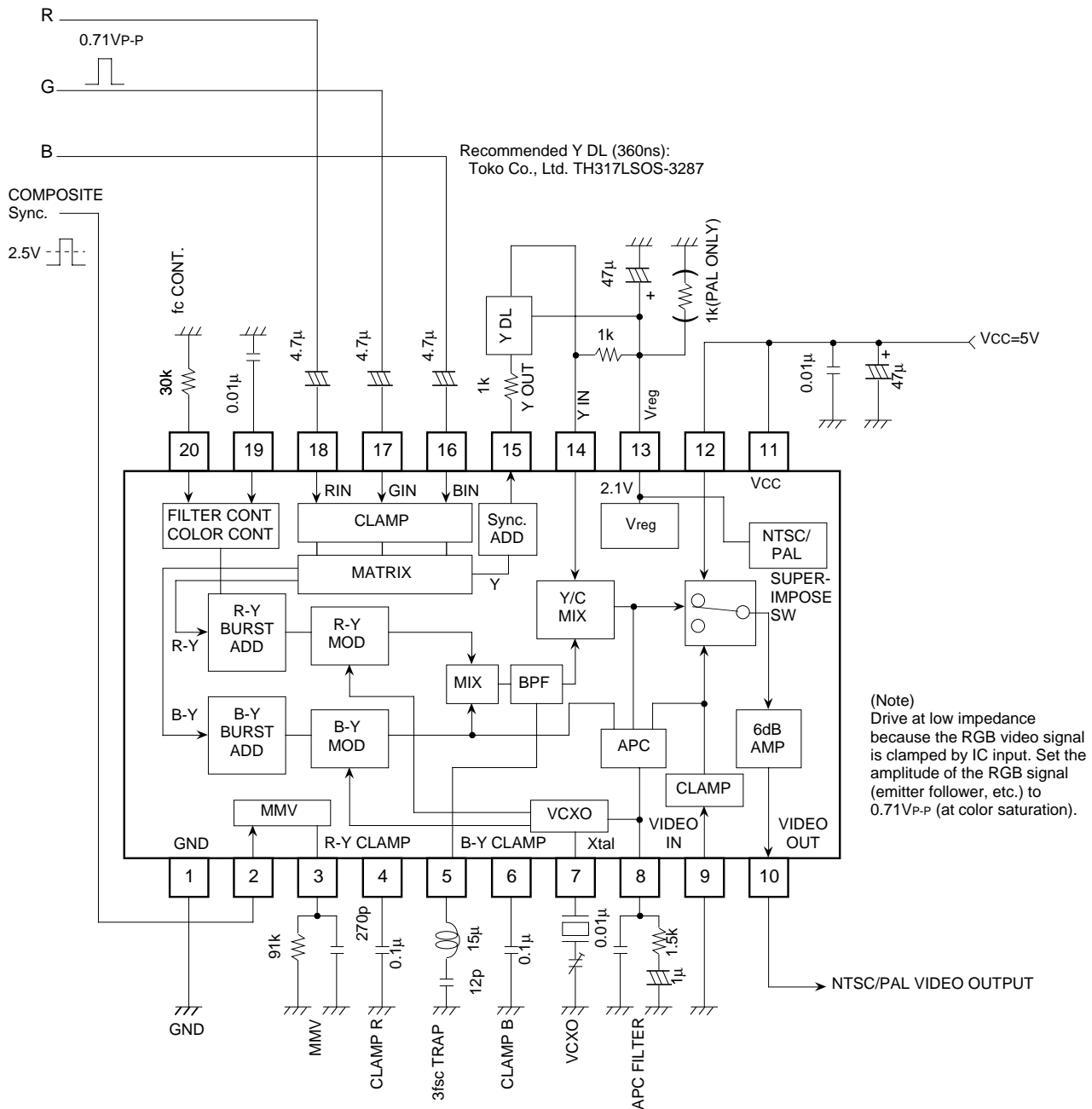
Standard board

Material : glass epoxy (Cu leaf pattern is put over one side of the board.)
 Size : 70mm, thickness=1.6mm
 Thickness of Cu leaf : 18μm

APPLICATION EXAMPLE (1)

Encoding RGB video signal to NTSC/PAL signal RGB video signal input

RGB VIDEO SIGNAL INPUT



Unit Resistance : Ω
 Capacitance : F

Example of Xtal: Nippon denpa industry Co., Ltd. AT-51
 (NTSC = 3.579545MHz)
 (PAL = 4.433619MHz)

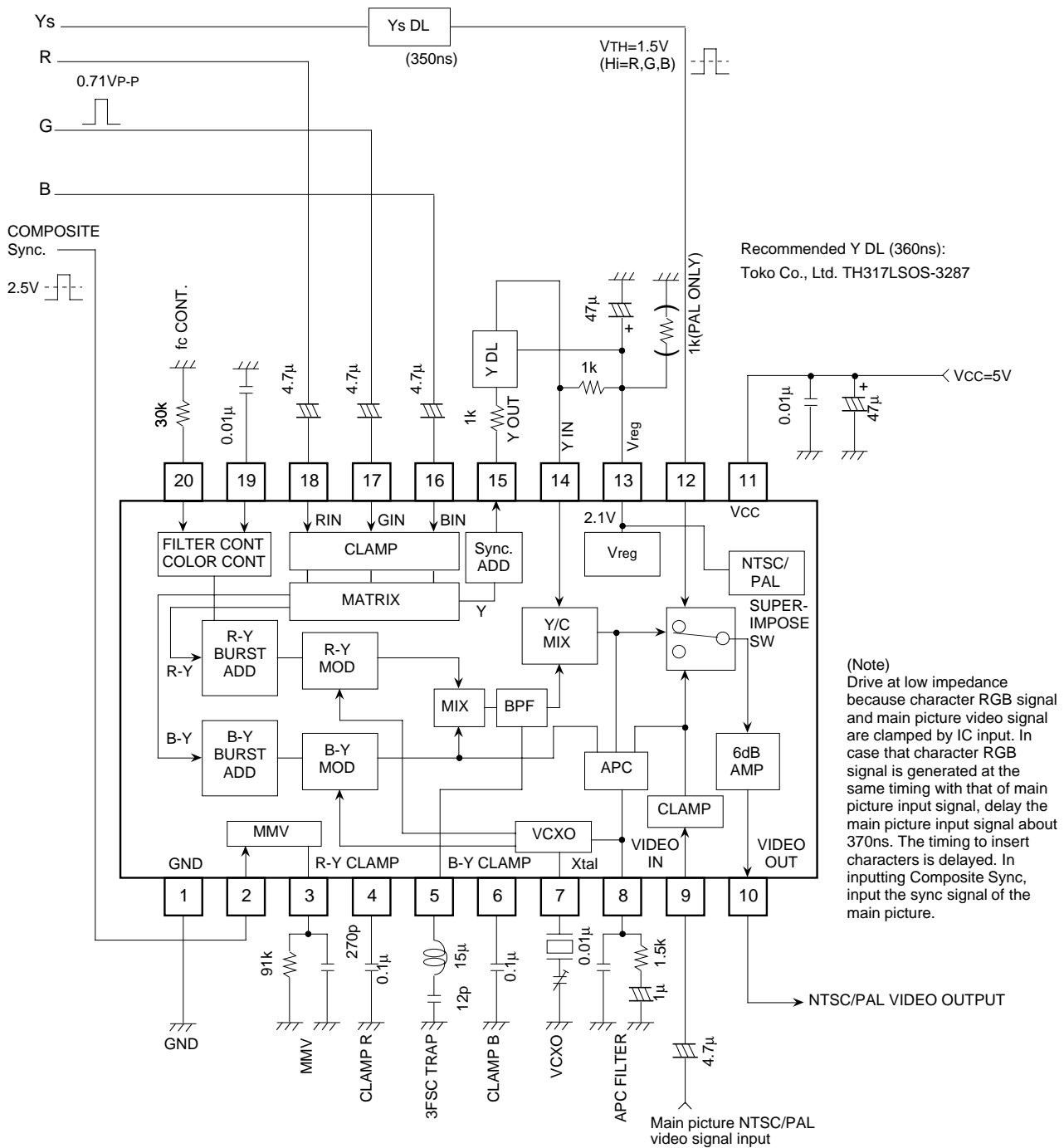
APPLICATION EXAMPLE (2)

Superimposing RGB Character Signal on NTSC/PAL Signal
 (*The case that RGB signal of personal computers, etc. is superimposed on NTSC/PAL signal as a child picture is mentioned in parentheses.)

In case that the signal which is about 350ns behind the character (*child picture) RGB signal is directly generated as Ys signal, Ys DL is not necessary. When the timing of RGB coincides with that of Ys, set the delay time of Ys DL to 350ns (typ.).

RGB CHARACTER SIGNAL INPUT

(*RGB child picture signal input after processing time axis)



Example of Xtal: Nippon denpa industry Co., Ltd. AT-51
 (NTSC = 3.579545MHz)
 (PAL = 4.433619MHz)

Unit Resistance : Ω
 Capacitance : F

DESCRIPTION OF PIN

Pin No.	Name	Peripheral circuit of pins	Pin voltage	Remarks
①	GND			
②	C.SYNC IN		AC : Sync input 	$V_{TH}=2.5V\pm 0.3V$
③	HHK		AC 	HHK pulse width can be adjusted by connecting RC externally. Recommended value HHK:3/4H R=91K C=270p
④	OFFSET R		DC : 3.1V	Recommended value of external circuit C=0.1µ
⑤	TRAP		AC : Chroma Burst : 300mVp-p ⑮ Test mode output when voltage at pin ⑮ is 5V ⑫ Hi : R-Y output ⑬ Lo : B-Y output	Recommended value of external circuit L C NTSC : 15µ 12P PAL : 10µ 12P ⑮ 5V : Test mode setting ⑮ Pulse output

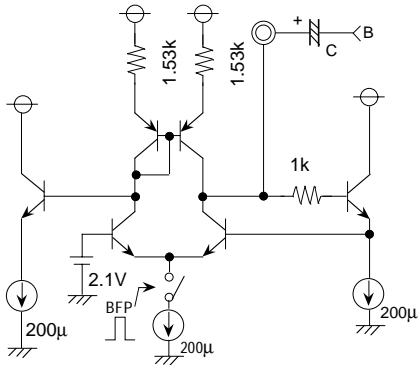
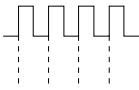
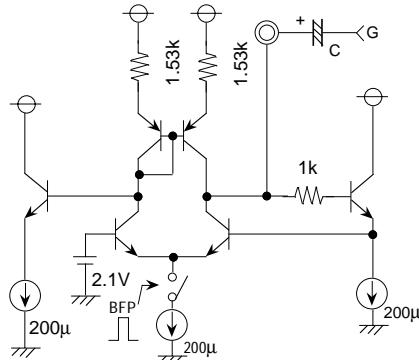
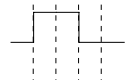
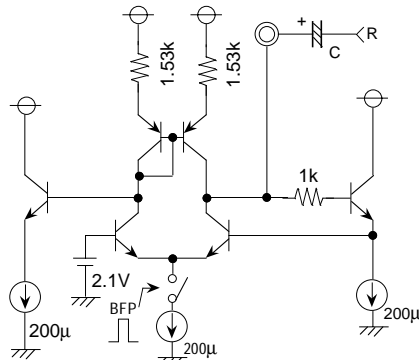
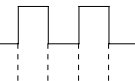
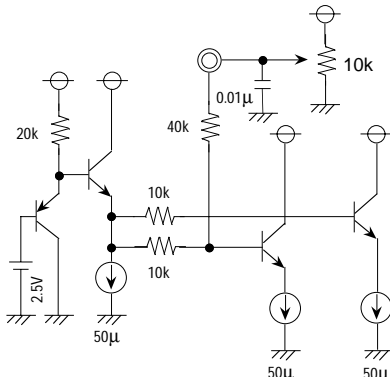
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin voltage	Remarks
⑥	OFFSET B		DC : 3.1V	Recommended value of external circuit C=0.1µ
⑦	VCXO IN		DC : 3.2V	Free run frequency is set by the trimmer capacitor ⑦ 0V : Carrier OFF
⑧	APC FILTER		DC : 3.3V In free run mode DC : 2.7V	β characteristics Frequency Recommended value of external circuit R=1.5k C1=0.001µ C2=1µ
⑨	VIDEO IN		AC : VIDEO 1VP-P Pedestal section 2.9V	Clamp input (burst timing) Recommended value of external circuit C=4.7µ ⑨ 0V : Free run mode setting

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin voltage	Remarks						
⑩	VIDEO OUT		AC : VIDEO 2VP-P Pedestal section 1.8V 							
⑪	Vcc		DC : 5V	Icc : 50mA						
⑫	Ys		Switching signal input for superimposing 	V _{TH} =1.5±0.3V Hi : RGB IN output Lo : VIDEO IN output Setting of output at pin ⑤ when voltage at pin ⑫ is ⑤ V <table border="1"><tr><td>⑫</td><td>⑤ Output at pin</td></tr><tr><td>Hi</td><td>R-Y</td></tr><tr><td>Lo</td><td>B-Y</td></tr></table>	⑫	⑤ Output at pin	Hi	R-Y	Lo	B-Y
⑫	⑤ Output at pin									
Hi	R-Y									
Lo	B-Y									
⑬	VRE G		DC : 2.1V	Recommended value of external circuit C=47µ 						
⑭	Y IN		AC : Y 0.5VP-P Pedestal section 2.1V 							
⑮	Y OUT		AC : Y 1VP-P Pedestal section 2.1V ⑮ Test mode output when voltage at pin ⑤ is 5V Pulse output	<table border="1"><tr><td>⑫</td><td>⑤ Output at pin</td></tr><tr><td>Hi</td><td>R-Y</td></tr><tr><td>Lo</td><td>B-Y</td></tr></table>	⑫	⑤ Output at pin	Hi	R-Y	Lo	B-Y
⑫	⑤ Output at pin									
Hi	R-Y									
Lo	B-Y									

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin voltage	Remarks
16	B IN		<p>AC : B0.71VP-P Sync section : 2.9V</p> 	<p>Clamp input (burst timing) C=4.7µ</p>
17	G IN		<p>AC : B0.71VP-P Sync section : 2.9V</p> 	<p>Clamp input (burst timing) C=4.7µ</p>
18	R IN		<p>AC : B0.71VP-P Sync section : 2.9V</p> 	<p>Clamp input (burst timing) C=4.7µ</p>
19	COLOR CONT.		<p>DC : 2.5V</p>	<p>Color control of RGB encode output 5V : Chroma section+2dB 2.5V : Standard 0V : Chroma section-3dB</p>

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Peripheral circuit of pins	Pin voltage	Remarks
⑳	fc. CONT.	<p>The diagram shows a multi-stage transistor circuit. It starts with a 20k resistor connected to a pin terminal. This is followed by a series of transistors. A 20k resistor is connected to the base of the first transistor. The circuit includes several other resistors: 10k, 16k, 100, 10k, and 34k. An external resistor R is connected to ground through a 100 resistor. The circuit is grounded at several points.</p>	DC : 3.3V	fc of LPF can be adjusted by connecting a resistor externally. R=30k