

# M52390FP

## NTSC/PAL Encoder

REJ03F0080-0100Z

Rev.1.0

Sep.22.2003

---

### Description

The M52390FP is a semiconductor integrated circuit that has a function for converting R, G and B signals into NTSC/PAL composite video signals, as well as a superimpose function, on a single chip.

### Features

- RGB encoder-related
  - Built-in LPF for color discrimination. An external resistor enables cutoff frequency control.
  - An internal VCA circuit enables gain control of the chroma unit.
  - A high-precision modulation circuit and clamping circuit realize low carrier leaks.
  - Burst and synch signals are generated in the IC.
- Superimpose-related
  - $Y_S$  IN (control input) enables switching between two input signals, VIDEO IN and RGB IN.
  - An internal high-speed analog switch makes it possible to insert fine text.
  - An internal APC circuit automatically adjusts the color phases of new screen (VIDEO IN) and RGB encoder signals.
- Overall
  - The VIDEO OUT signal is output at  $2 V_{P-P}$ , making it possible to configure a  $75 \Omega$  drive circuit with a single transistor.
  - Both NTSC and PAL are supported.

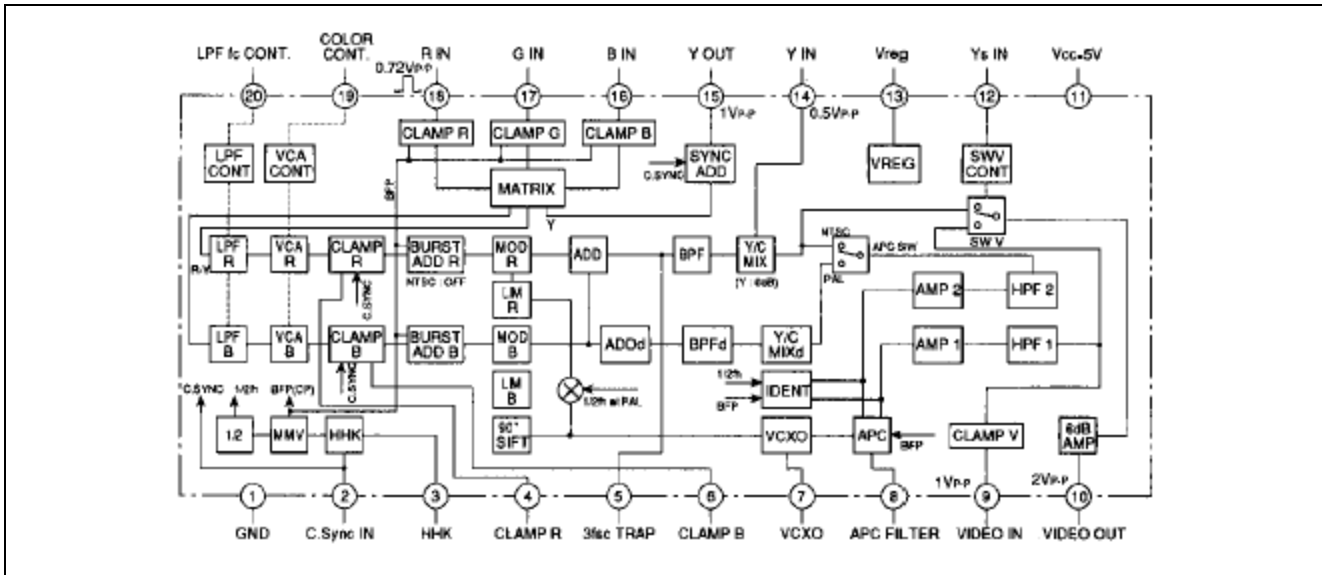
### Application

- TVs, VCRs, monitors and other audio/video devices

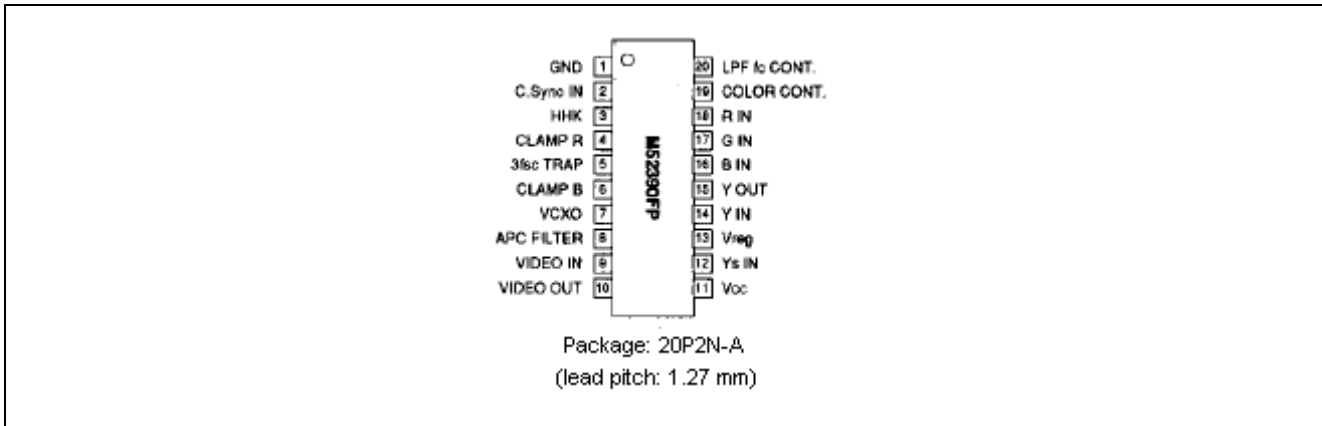
### Recommended Operating Conditions

- Power supply voltage range: 4.7 to 5.3 V
- Recommended power supply voltage: 5.0 V

Block Diagram



Pin Configuration



Description of Pin

Pin no.	Pin name	Pin peripheral circuit	Pin voltage	Notes
1	GND			
2	C.SYVC IN		<p>AC: Sync input</p>	$V_{TH} = 2.5 V \pm 0.3 V$
3	HHK		<p>AC</p>	<p>The HHK pulse width can be varied using the external resistor. Recommended value: HHK: 3/4H</p> <p>R = 91 k C = 270 p</p>
4	OFFSET R		<p>DC = 3.1 V</p>	<p>External recommended value. C = 0.1 µ.</p>
5	TRAP		<p>AC: Chroma</p> <p>Burst: 300 mV<sub>P-P</sub></p>	<p>External recommended value.</p> <p style="text-align: center;">L    C</p> <p>NTSC : 15 µ   12P</p> <p>PAL    : 10 µ   12P</p>
			<p>[15] Test mode output at 5 V</p> <p>[12] Hi: R-Y output</p> <p>[12] Lo: B-Y output</p>	<p>[5] 5 V: Test mode setting</p> <p>[15] Pulse output</p>

Description of Pin (cont)

Pin no.	Pin name	Pin peripheral circuit	Pin voltage	Notes
6	OFFSET B		DC: 3.1 V	External recommended value C = 0.1 µ
7	VCXO IN		DC: 3.2 V	The free run frequency is set using the trimmer capacitor. [7] 0 V: Carrier OFF
8	APC FILTER		DC: 3.3 V In Free Run mode: DC: 2.7 V	β characteristic Frequency  External recommended values R = 1.5 k C1 = 0.01 µ C2 = 1 µ
9	VIDEO IN		AC: VIDEO 1 V <sub>P-P</sub> Pedestal: 2.9 V 	Clamping input (burst timing) External recommended value C = 4.7 µ [9] 0 V: Free Run mode setting

Description of Pin (cont)

Pin no.	Pin name	Pin peripheral circuit	Pin voltage	Notes						
10	VIDEO OUT		AC: VIDEO 2 V <sub>P-P</sub> Pedestal: 1.8 V 							
11	V <sub>CC</sub>		DC: 5 V	I <sub>CC</sub> : 50 mA						
12	Y <sub>s</sub>		Switching signal input when using Superimpose  Hi: Insertion screen (RGB IN output)	V <sub>TH</sub> = 1.5 V ± 0.3 V Hi: RGB IN output Lo: VIDEO IN output  [15 Output setting when using 5 V [5] Output <table border="1"> <tr> <td>[12]</td> <td>[5]output</td> </tr> <tr> <td>Hi</td> <td>R-Y</td> </tr> <tr> <td>Lo</td> <td>B-Y</td> </tr> </table>	[12]	[5]output	Hi	R-Y	Lo	B-Y
[12]	[5]output									
Hi	R-Y									
Lo	B-Y									
13	VRE G		DC: 2.1 V	External recommended value C = 4.7 µ 						
14	Y IN		AC: Y 0.5 V <sub>P-P</sub> Pedestal: 2.1 V 							
15	Y OUT		AC: Y 1 V <sub>P-P</sub> Pedestal: 2.1 V 	(5) Test mode output at 5 V Pulse output  [12] 5 V: Test mode setting <table border="1"> <tr> <td>[12]</td> <td>[5]output</td> </tr> <tr> <td>Hi</td> <td>R-Y</td> </tr> <tr> <td>Lo</td> <td>B-Y</td> </tr> </table>	[12]	[5]output	Hi	R-Y	Lo	B-Y
[12]	[5]output									
Hi	R-Y									
Lo	B-Y									



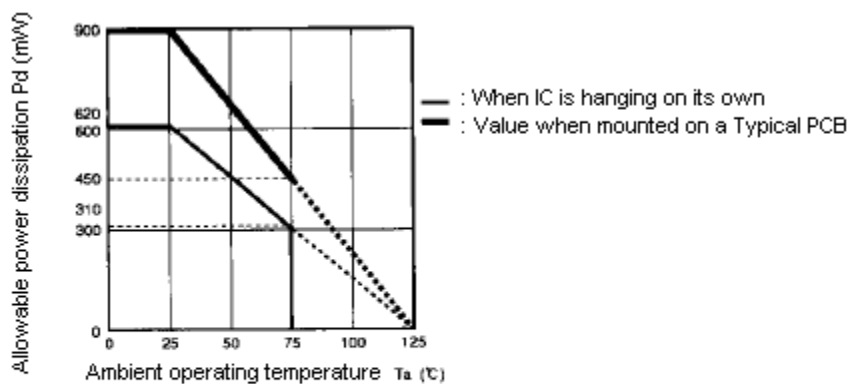
## Absolute Maximum Rating

(Unless otherwise noted,  $T_a = 25^\circ\text{C}$ )

Symbol	Item	Ratings	Units
Vcc	Power supply voltage	7	V
Pd	Internal current consumption	620 (900)	mW
Topr	Ambient operating temperature	-20 to 75	$^\circ\text{C}$
Tstg	Storage temperature	-40 to 125	$^\circ\text{C}$
k $\theta$	Thermal derating ( $T_a = 25^\circ\text{C}$ )	6.2 (9.0)	mW/ $^\circ\text{C}$

Note: Values in parentheses are the values when mounted on a typical PCB.

## Thermal Derating (Maximum Rating)



Typical PCB

Material --- Glass epoxy (Cu foil pattern on one side)

Size: 70 mm<sup>2</sup>, thickness = 1.6 mm

Cu foil thickness - 18  $\mu\text{m}$

## Electrical Characteristics

(unless otherwise noted, Ta=25°C, Vcc = 5 V, SG2 = sync)

No.	Symbol	Item	Measurement conditions	Mea- sure- ment point	Limits			Unit
					Min.	Typ.	Max.	
1	I <sub>CC1</sub>	Circuit current 1	NTSC MODE, [12] 5 V	[11]	35	50	65	mA
2	I <sub>CC2</sub>	Circuit current 2	NTSC MODE, [12] 5 V	[11]	37	52	67	mA
<b>RGB IN → Y OUT</b>								
3	ER	Matrix ratio R	SG18: 1 Vp-p	[15]	0.27	0.30	0.33	Vp-p
4	EG	Matrix ratio G	SG17: 1 Vp-p	[15]	0.53	0.59	0.65	Vp-p
5	EB	Matrix ratio B	SG16: 1 Vp-p	[15]	0.09	0.11	0.13	Vp-p
6	EY	At RGB 100% Y level	SG16, SG17, SG18: 0.71 Vp-p	[15]	0.63	0.71	0.79	Vp-p
7	FR	R IN → Y OUT frequency characteristic	SG18: 500 kHz/5 MHz, 0.5 Vp-p CW, SW16, 17, 18:ON [2] 0 V (SG2: OFF)	[15]	-1.5	0	1.5	dB
8	FG	G IN → Y OUT frequency characteristic	SG17: 500 kHz/5 MHz, 0.5 Vp-p CW, SW16, 17, 18:ON [2] 0 V (SG2: OFF)	[15]	-1.5	0	1.5	dB
9	FB	B IN → Y OUT frequency characteristic	SG16: 500 kHz/5 MHz, 0.5 Vp-p CW, SW16, 17, 18:ON [2] 0 V (SG2: OFF)	[15]	-1.5	0	1.5	dB
10	VS1	Sync level 1	NTSC MODE	[15]	257	286	315	Vp-p
11	VS2	Sync level 2	PAL MODE (SW13: ON)	[15]	270	300	330	Vp-p
<b>Y IN → VIDEO OUT</b>								
12	G <sub>Y</sub>	Y IN → VIDEO OUT gain	SG14: 500 kHz, 0.5 Vp-p CW, [12] 5 V	[10]	10.5	12	13.5	dB
13	F <sub>Y</sub>	Y IN → VIDEO OUT frequency characteristic	SG14: 500 kHz, 0.5 Vp-p CW, [12] 5 V	[10]	-1.5	0	1.5	dB
<b>RGB IN → TRAP</b>								
14	D <sub>L(R-Y)</sub>	Delay (R-Y)	SG18: 1 Vp-p [15] 5 V, [12] 5 V, [7] 0 V	[5]	210	310	410	ns
15	D <sub>L(B-Y)</sub>	Delay (B-Y)	SG16: 1 Vp-p [15] 5 V, [12] 0 V, [7] 0 V	[5]	210	310	410	ns
16	G <sub>H(R-Y)</sub>	Gain (R-Y) VCA: Hi	SG18: 500 kHz, 0.5 Vp-p CW, SW4, 6, 17, 18: ON [15] 5 V, [12] 5 V, [7] 0 V, [19] 5 V/2.5 V, [2] 0V (SG2: OFF)	[5]	1	2	3.5	dB
17	G <sub>H(B-Y)</sub>	Gain (B-Y) VCA: Hi	SG16: 500 kHz, 0.5 Vp-p CW, SW4, 6, 17, 18: ON [15] 5 V, [12] 0 V, [7] 0 V, [19] 5 V/2.5 V, [2] 0V (SG2: OFF)	[5]	1	2	3.5	dB
18	G <sub>L(R-Y)</sub>	Gain (R-Y) VCA: Lo	SG18: 500 kHz, 0.5 Vp-p CW, SW4, 6, 17, 18: ON [15] 5 V, [12] 5 V, [7] 0 V, [19] 0 V/2.5 V, [2] 0V (SG2: OFF)	[5]	-4.5	-3	-2	dB
19	G <sub>L(B-Y)</sub>	Gain (B-Y) VCA: Lo	SG18: 500 kHz, 0.5 Vp-p CW, SW4, 6, 17, 18: ON [15] 5 V, [12] 5 V, [7] 0 V, [19] 0 V/2.5 V, [2] 0V (SG2: OFF)	[5]	-4.5	-3	-2	dB

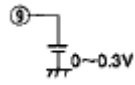
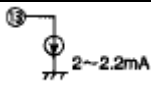
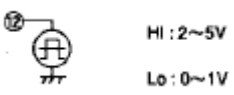
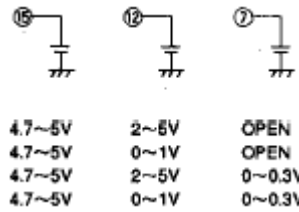



## Electrical Characteristics (cont)

No.	Symbol	Item	Measurement conditions	Measurement point	Limits			Unit
					Min.	Typ.	Max.	
<b>RGB IN → VIDEO OUT</b>								
20	V <sub>B1</sub>	NTSC burst level	NTSC MODE [12] 5 V	[10B]	243	286	329	mVp-p
21	V <sub>B2</sub>	PAL burst level	PAL MODE (SW13: ON) [12] 5 V	[10B]	255	300	345	mVp-p
22	V <sub>B3</sub>	PAL burst level differential	PAL MODE (SW13: ON) [12] 5 V	[10B]	-30	0	30	mVp-p
23	P <sub>PB</sub>	PAL burst phase differential	PAL MODE (SW13: ON) [12] 5 V	[10B]	82	90	98	deg
24	V <sub>R/B</sub>	R/burst level ratio	SG18: 0.71 Vp-p [12] 5 V	[10B]	2.68	3.15	3.62	
25	V <sub>G/B</sub>	G/burst level ratio	SG17: 0.71 Vp-p [12] 5 V	[10B]	2.51	2.95	3.39	
26	V <sub>B/B</sub>	B/burst level ratio	SG16: 0.71 Vp-p [12] 5 V	[10B]	1.91	2.25	2.59	
27	V <sub>C/B</sub>	NTSC MODE carrier leak	NTSC MODE [12] 5 V	[10B]	—	-40	-28	dB
28	P <sub>R/B</sub>	R/burst phase differential	SG18: 0.71 Vp-p [12] 5 V	[10B]	96	104	112	deg
29	P <sub>G/B</sub>	G/burst phase differential	SG17: 0.71 Vp-p [12] 5 V	[10B]	233	241	249	deg
30	P <sub>B/B</sub>	B/burst phase differential	SG16: 0.71 Vp-p [12] 5 V	[10B]	339	347	355	deg
<b>VIDEO IN → VIDEO OUT</b>								
31	GVIO	VIDEO IN → VIDEO OUT gain	SG9: 500 kHz, 0.5 Vp-p CW, SW9: ON [12] 0 V, [2] 0 V (SG2: OFF)	[10]	5	6	7	dB
32	FVIO	VIDEO IN → VIDEO OUT frequency characteristic	SG9: 5 MHz, 0.5 Vp-p CW, SW9: ON [12] 0 V, [2] 0 V (SG2: OFF)	[10]	-1.5	0	1.5	dB
<b>SUPER IMPOSE</b>								
33	PDI	RGB/VIDEO IN burst phase differential	SG9: 3.85 MHz, 286 mVp-p CW, SG12: 1 Vp-p	[10B]	-5	0	5	deg
34	VOS	DC offset	SG9: burst, 286 mVp-p CW, SG12: 1 Vp-p	[10]	-20	0	20	mV
<b>MMV</b>								
35	HHK	HHK width	PAL MODE (SW13: ON) [5] 5V	[2] [15]	40	47	54	μs
36	BFPP	BFP position (burst position)	[5] 5V	[2] [15]	4.5	5.6	6.7	μs
37	BFPW	BFP width (burst width)	[5] 5V	[15]	2.0	2.5	3.0	μs

**Electrical Characteristics Measurement Method**

Tables for the various modes (common to all tests)

Mode	Setting condition	Function
FREE RUN MODE		VCXO FREE RUN
PAL MODE		Carrier phase for MOD R reversed at each 1H
SUPER IMPOSE MODE		[10] VIDEO OUT RGB ENCODE signal out VIDEO IN signal out
TEST MODE MR TEST MODE MB TEST MODE DR TEST MODE DB		[5] Color difference output MOD R-Y out MOD B-Y out DIFF R-Y out DIFF B-Y out
TEST MODE P		[10] PULSE output PAL MODE: BFP, HHK mix NTSC MODE: BFP
V4, V6, V9, V16, V17, V18	Various pin voltages when SYNC is input to [2] (C. SYNC IN) (for clamping)	

Measurement method and method for computing limit values

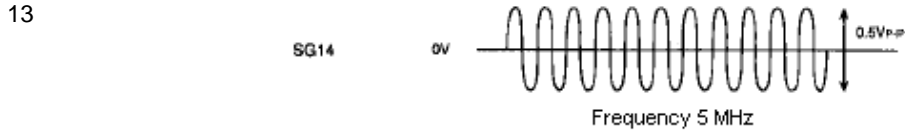
Meas. no.	Measurement method and method for computing limit values		
1	Current flowing into [11] is measured.		
2			
3	SG2	5V	
4		0V	
5	SG16 (SG17) (SG16)	1V	
		0V	
	Ⓜ output		
6	SG2	5V	
		0V	
	SG16 SG17 SG16	0.71V	
		0V	
	Ⓜ output		
7 (8, 9)	SG16 (SG17) (SG16)	0V	<p> <math>f = 500\text{kHz} / 5\text{MHz}</math>  <math>0.5\text{Vpp CW}</math> </p> <p> <math>F = 20 \log \frac{V_{\text{out}}(5\text{MHz})}{V_{\text{out}}(500\text{kHz})} \text{ (dB)}</math> </p>
	Ⓜ output		<p><math>V_{\text{out}}</math></p>
10	SG2	5V	
11		0V	
	Ⓜ output		<p><math>V_b</math></p>
12	SG14	0V	<p>Frequency 500 kHz</p> <p><math>0.5\text{Vpp}</math></p>

The 500 kHz component V12 with respect to [10] is measured, and is computed using the following equation.

$$G_V = 20 \log \frac{V_{12}}{0.5\text{Vpp}} \text{ (dB)}$$

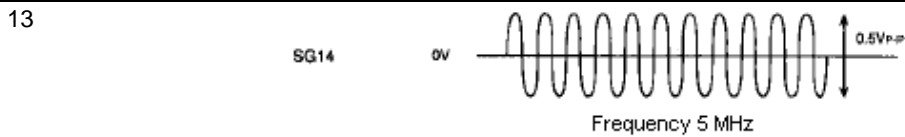
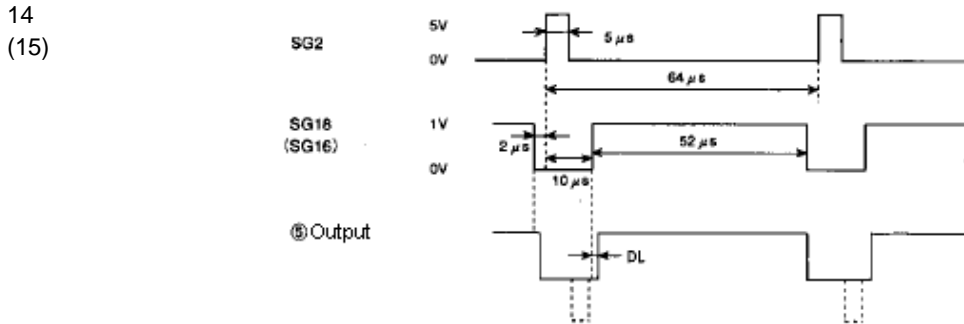
Measurement method and method for computing limit values (cont)

Meas. no. Measurement method and method for computing limit values



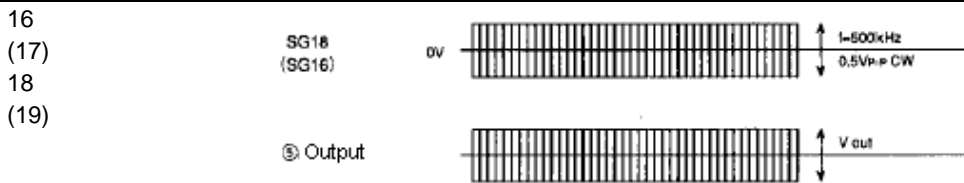
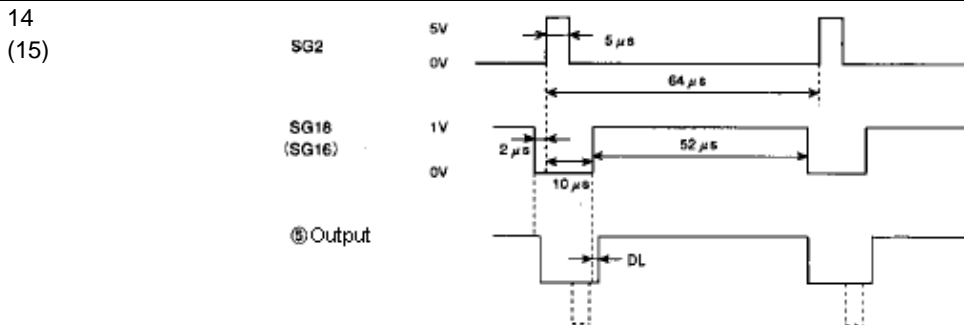
The 500 MHz component V13 with respect to (10) is measured, and is computed using the following equation.

$$fcY = 20 \log \frac{V_{13}}{V_{12}} \text{ (dB)}$$



The 500 MHz component V13 with respect to (10) is measured, and is computed using the following equation.

$$fcY = 20 \log \frac{V_{13}}{V_{12}} \text{ (dB)}$$





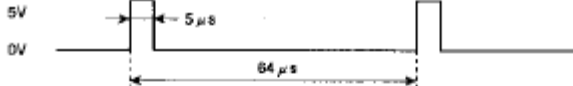

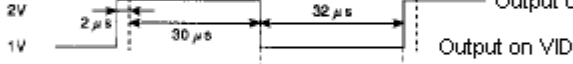
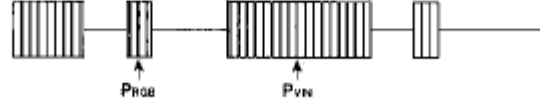
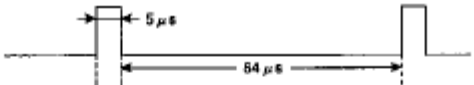



$$GH = 20 \log \frac{V_{out} \text{ (Ⓢ 5V)}}{V_{out} \text{ (Ⓢ 2.5V)}} \text{ (dB)}$$

$$GL = 20 \log \frac{V_{out} \text{ (Ⓢ 0V)}}{V_{out} \text{ (Ⓢ 2.5V)}} \text{ (dB)}$$

Measurement method and method for computing limit values (cont)

Meas. no.	Measurement method and method for computing limit values	
20 21 22	SG2	<p> <math>V_{S1} = V_{nH}</math>  <math>V_{S2} = V_{n+1H}</math>  <math>V_{SS} = V_{nH} - V_{(n+1)H}</math> </p>
23	SG2	<p> <math>P_{PS} =  P_{nH} \text{ burst phase} - P_{(n+1)H} \text{ burst phase} </math> </p>
24 (25, 26)	SG2  SG18 (SG17) (SG16)	<p> <math>R(G, B) / \text{Burst level ratio} = \frac{V_c}{V_b}</math> </p>
27	SG2	<p> <math>VC/B = 20 \log \frac{V_c}{V_b} \text{ (dB)}</math> </p>
28 (29, 30)	SG2  SG18 (SG17) (SG16)	

Measurement method and method for computing limit values (cont)

Meas. no.	Measurement method and method for computing limit values	
31 32	<p>SG9</p>  <p>Output</p>  $G_{500} = 20 \log \frac{V_{out}(500\text{kHz})}{0.5\text{V}_{p-p}} \text{ (dB)}$ $F_{500} = 20 \log \frac{V_{out}(5\text{MHz})}{V_{out}(500\text{kHz})} \text{ (dB)}$	
33	<p>SG2</p>  <p>SG9</p>  <p>SG12</p>  <p>Output</p>  <p>Output on RGB side Output on VIDEO IN side</p> $P_{SI} = P_{RGB} - P_{VIN} \text{ (deg)}$	
34	<p>SG2</p>  <p>SG12</p>  <p>SG9</p>  <p>Output</p>  $V_{OS} = V_{RGB} - V_{VIN} \text{ (mV)}$	

Measurement method and method for computing limit values (cont)

Meas. no.	Measurement method and method for computing limit values		
35	SG2	5V 2.5V 0V	
36	SG2	5V 2.5V 0V	





## Usage Precautions

## (1) Typical values for input signals

Pin no.	Pin name	Specifications
②	C.Sync IN	
⑨	VIDEO IN	<p>VIDEO IN If there is no input, this should always be set to the Free Run mode.</p>
⑩	Ys	
⑮ ⑰ ⑱	B IN G IN R IN	

## (2) Setting the Free Run frequency

This IC generates the fsc by means of the VCXO circuit.

Consequently, the VCXO oscillation frequency must always be set to fsc before the IC is used, by following the procedure outlined below.

1. Connect [9] (VIDEO IN) to GND, and set the Free Run mode.
2. Set the [2] (OFFSET R) voltage when SYNC was input to [4] (C. SYNC IN) to  $V_4$ , and apply a voltage of  $V_4 = 0.5$  V to [4] (OFFSET R).
3. Fix C.[2] (SYNC IN) in the High state. (5 V applied)
4. Adjust the output frequency of [5] (TRAP) to the trimmer capacitor of [7] (VCXO IN), and set it to fsc.

**(3) Setting the color difference LPF**

The frequency characteristic of the color difference LPF built into this IC can be set as shown in Fig. 1, using the [20] (fc CONT.) external resistor.

When doing this, the group delay characteristic also changes, as shown in Fig. 2.

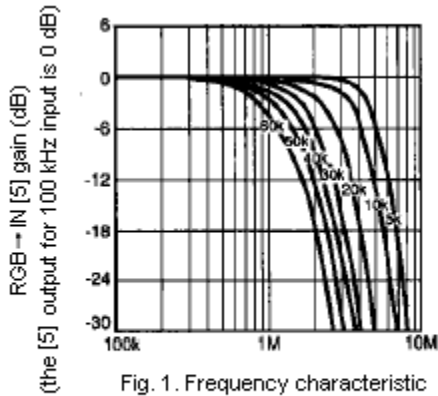


Fig. 1. Frequency characteristic of the color difference LPF (for measurement conditions, see TEST nos. 14 and 15)

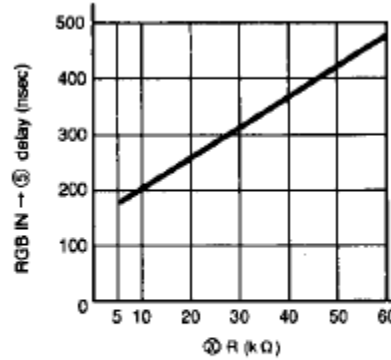


Fig. 2. Group delay characteristic for the color difference LPF (for measurement conditions, see TEST nos. 14 and 15)

**(4) Setting Y DL**

The group delay characteristic of the color signal of the RGB encoder output changes in response to the [20] (fc CONT) external resistor, so Y DL should be set in such a way that the group delay characteristic is the amount of group delay obtained from the group delay characteristic of Fig. 2, with 40 ns added.

Also, if the [6] (TRAP) circuit is being added, a further delay of +5 to +10 ns should be taken into consideration.

**(5) COLOR CONT characteristic**

The gain of the chroma unit can be set as shown in Fig. 3, using the [19] (COLOR CONT) applied voltage. (The burst amplitude is constant.)

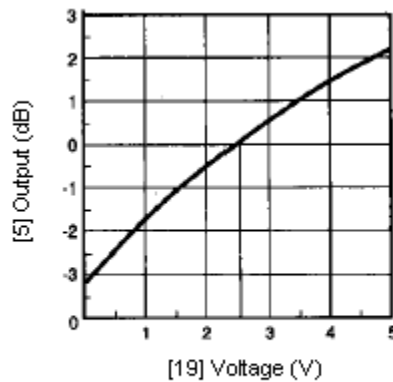


Fig. 3. COLOR CONT characteristic (for measurement conditions, see TEST nos. 16, 17, 18, and 19)

### (6) The relationship between BFP and HHK

The pulse width of BFP and HHK can be set as shown in Fig. 4, using the [3] (HHK) external CR.

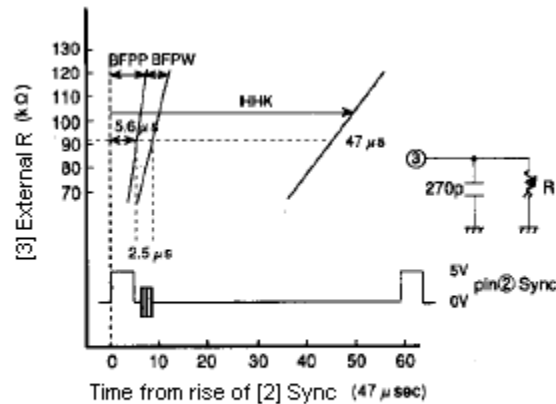
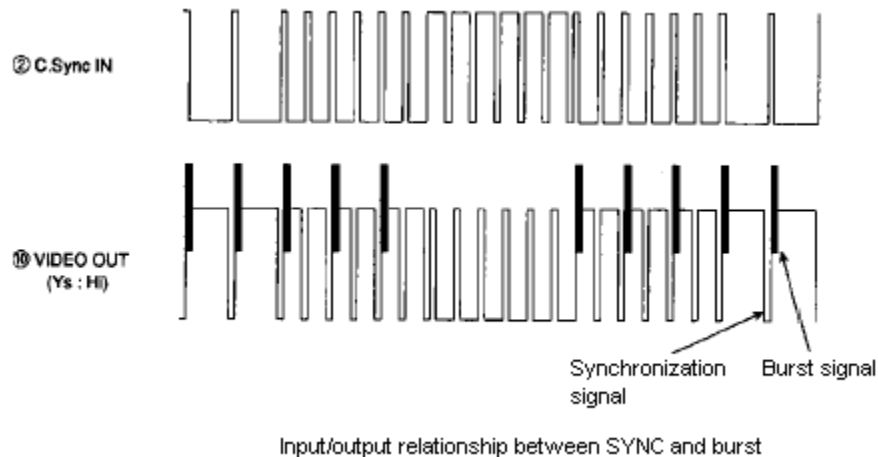


Fig. 4. [3] RC product versus pulse generated internally  
(for measurement conditions, see TEST nos. 35, 36, and 37)

### (7) Input pin drive

Input pins [9], [16], [17], and [18] use clamp input, so they should always be driven with a low impedance.

### (8) Input/output relationship between SYNC and burst during the V cycle



### (9) V DL and Y<sub>S</sub> DL settings when the SUPERIMPOSE mode is being used

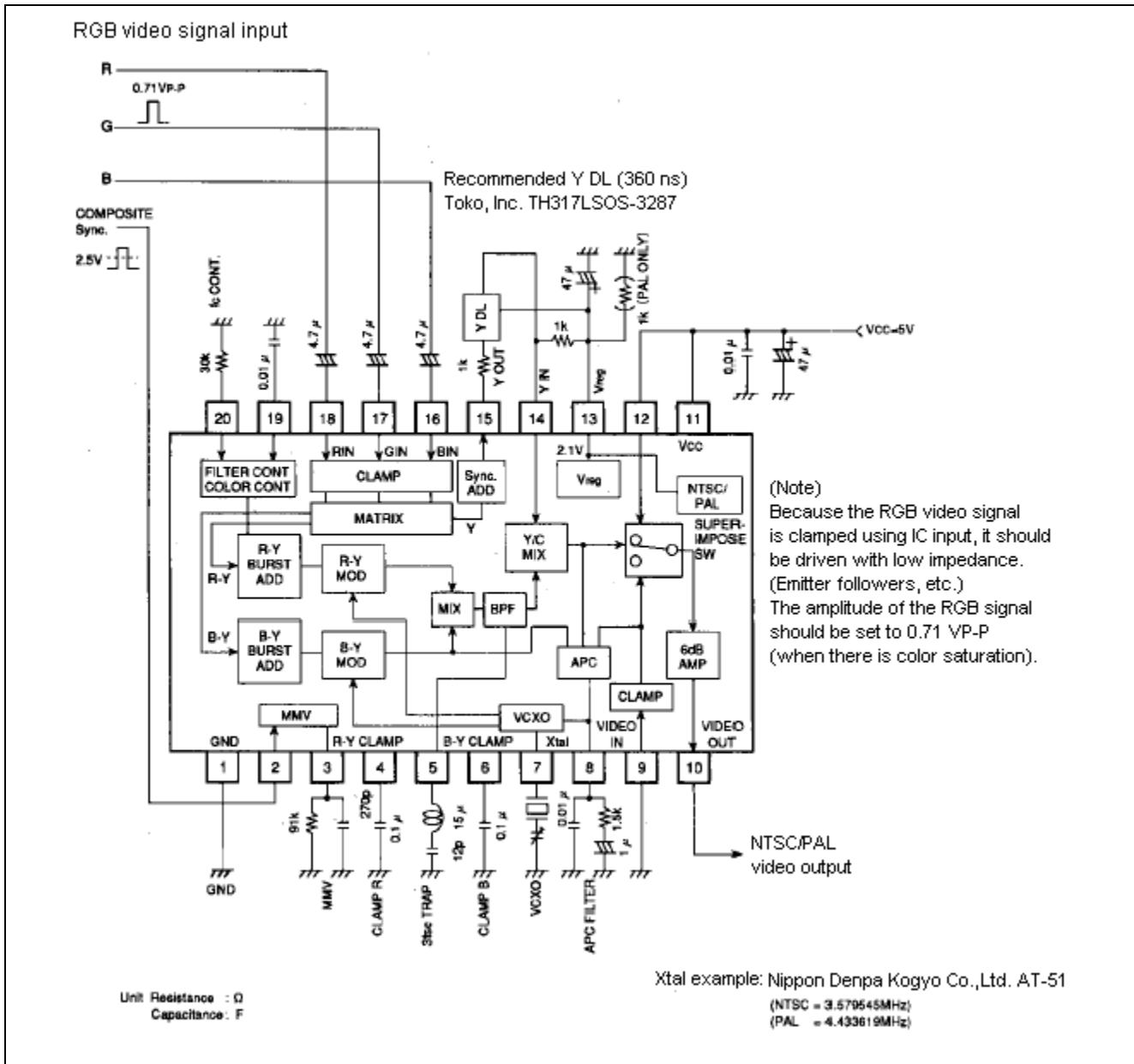
- 1) V DL is used to adjust the timing of the RGB encoder signal and the VIDEO IN signal.
- 2) Y<sub>S</sub> DL is used to adjust the timing of the RGB encoder signal and the Y<sub>S</sub> IN signal.
- 3) When the timing is the same for C. SYNC IN, RGB IN, VIDEO IN and Y<sub>S</sub> IN, V DL and Y<sub>S</sub> DL should be set using the amount of delay shown below as a guide.

$$V DL = Y DL (\text{item 4}) + 10 (\text{ns})$$

$$Y_S DL = Y DL - 10 (\text{ns})$$

### Application Example (1)

Example showing RGB video signals being encoded in NTSC/PAL signal

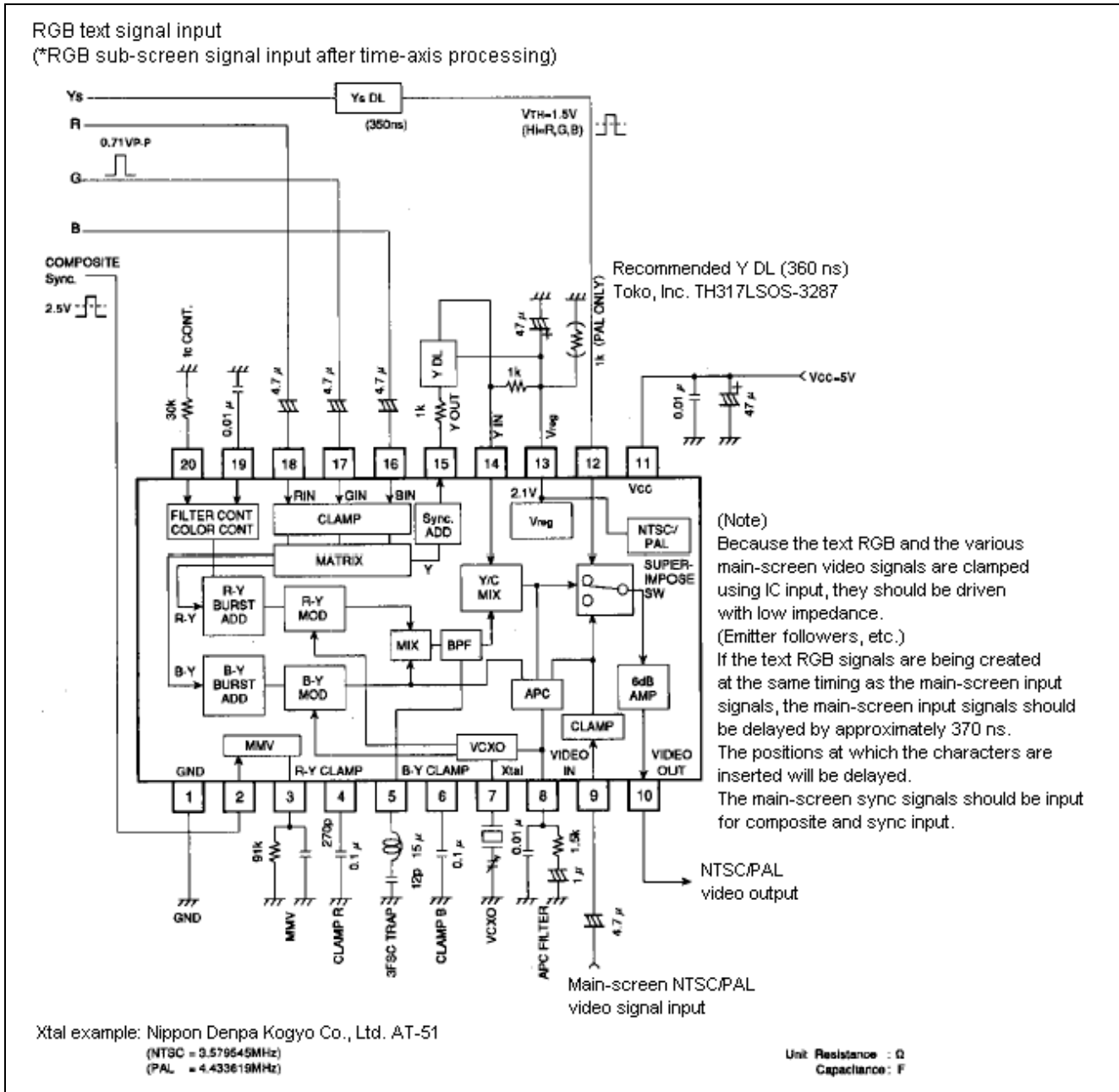


## Application Example (2)

Example showing RGB text signals superimposed on NTSC/PAL signals

(\*The values in brackets show what takes place when the RGB signals of a personal computer or other device are superimposed on NTSC/PAL signals as a sub-screen.)

If signals delayed by approximately 350 ns after the text (\*sub-screen) RGB signals are created directly, as Ys signals, Ys DL is not necessary. If RGB and Ys are at same timing, the delay time of Ys DL should be set to 350 ns (typical).



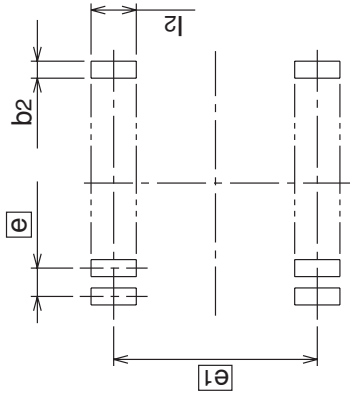
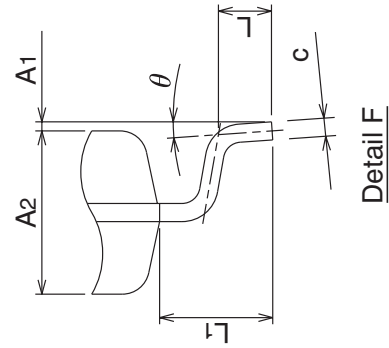
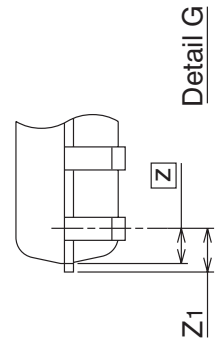
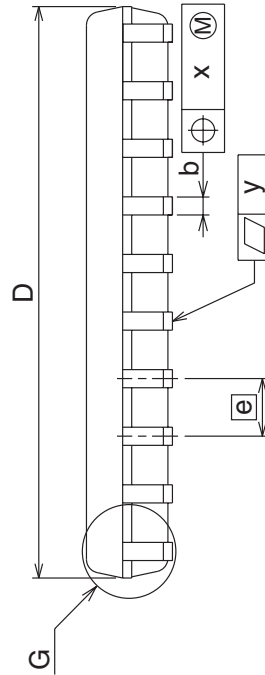
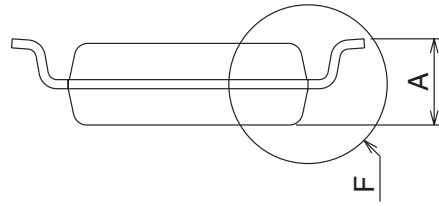
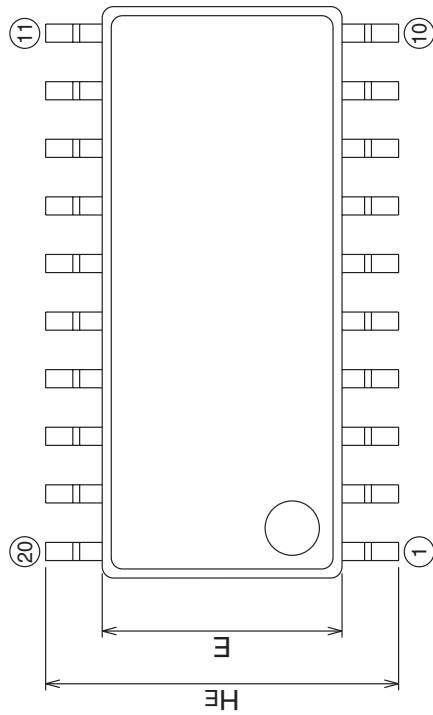
Package Dimensions

**20P2N-A**

(MMP)

**Plastic 20pin 300mil SOP**

EIAJ Package Code SOP20-P-300-1.27	JEDEC Code —	Weight(g) 0.26	Lead Material Cu Alloy
---------------------------------------	-----------------	-------------------	---------------------------



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A1	0	0.1	0.2
A2	—	1.8	—
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	12.5	12.6	12.7
E	5.2	5.3	5.4
e	—	1.27	—
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	—	1.25	—
Z	—	0.585	—
Z1	—	—	0.735
x	—	—	0.25
y	—	—	0.1
theta	0°	—	8°
b2	—	0.76	—
e1	—	7.62	—
l2	1.27	—	—

## RENESAS Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

---

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
  2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
  3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
  4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
  5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
  6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
  7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
  8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
- 



### RENESAS SALES OFFICES

<http://www.renesas.com>

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited.**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom  
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

**Renesas Technology Europe GmbH**  
Dornacher Str. 3, D-85622 Feldkirchen, Germany  
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

**Renesas Technology Hong Kong Ltd.**  
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2375-6836

**Renesas Technology Taiwan Co., Ltd.**  
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology (Shanghai) Co., Ltd.**  
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

**Renesas Technology Singapore Pte. Ltd.**  
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001