M52756SP

WIDE BAND ANALOG SWITCH

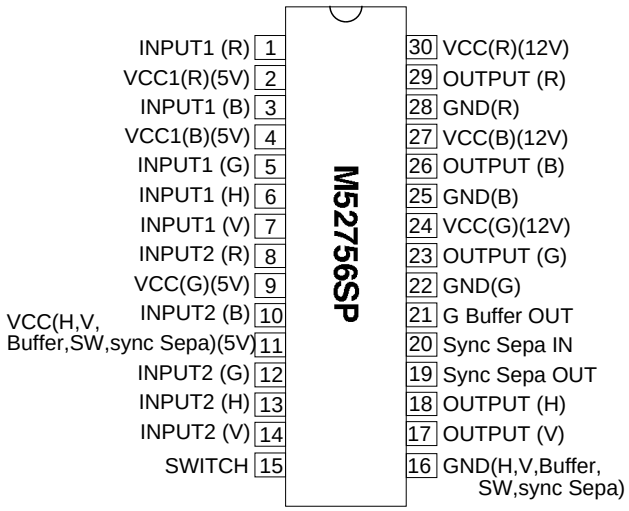
DESCRIPTION

The M52756SP is a semiconductor integrated circuit for the RGBHV interface. The device features switching signals input from two types of image sources and outputting the signals to the CRT display, etc. Synchronous signals, meeting a frequency band of 10kHz to 200kHz, are output at TTL. The frequency band of video signals is 250MHz, acquiring high-resolution images, and are optimum as an interface IC with high-resolution CRT display and various new media.

DESCRIPTION

- Frequency band: RGB 250MHz
  HV.....10kHz to 200kHz
- Input level: RGB.....0.7Vp-p(typ.)
  HV TTL input.....3.5Vo-p(both channel)
- RGBOUT can drive connected load of 75Ω.
- Only the G channel is provided with sync-on video output.
- The TTL format is adopted for HV output.
- It is possible to save the consumption current by stopping current supply to Pin 2, 4, 24, 27, 30.
- Sync Separation circuit

PIN CONFIGURATION (TOP VIEW)



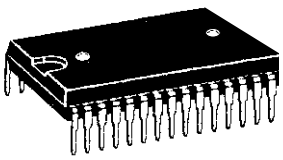
Outline 30P4B

APPLICATION

Display monitor

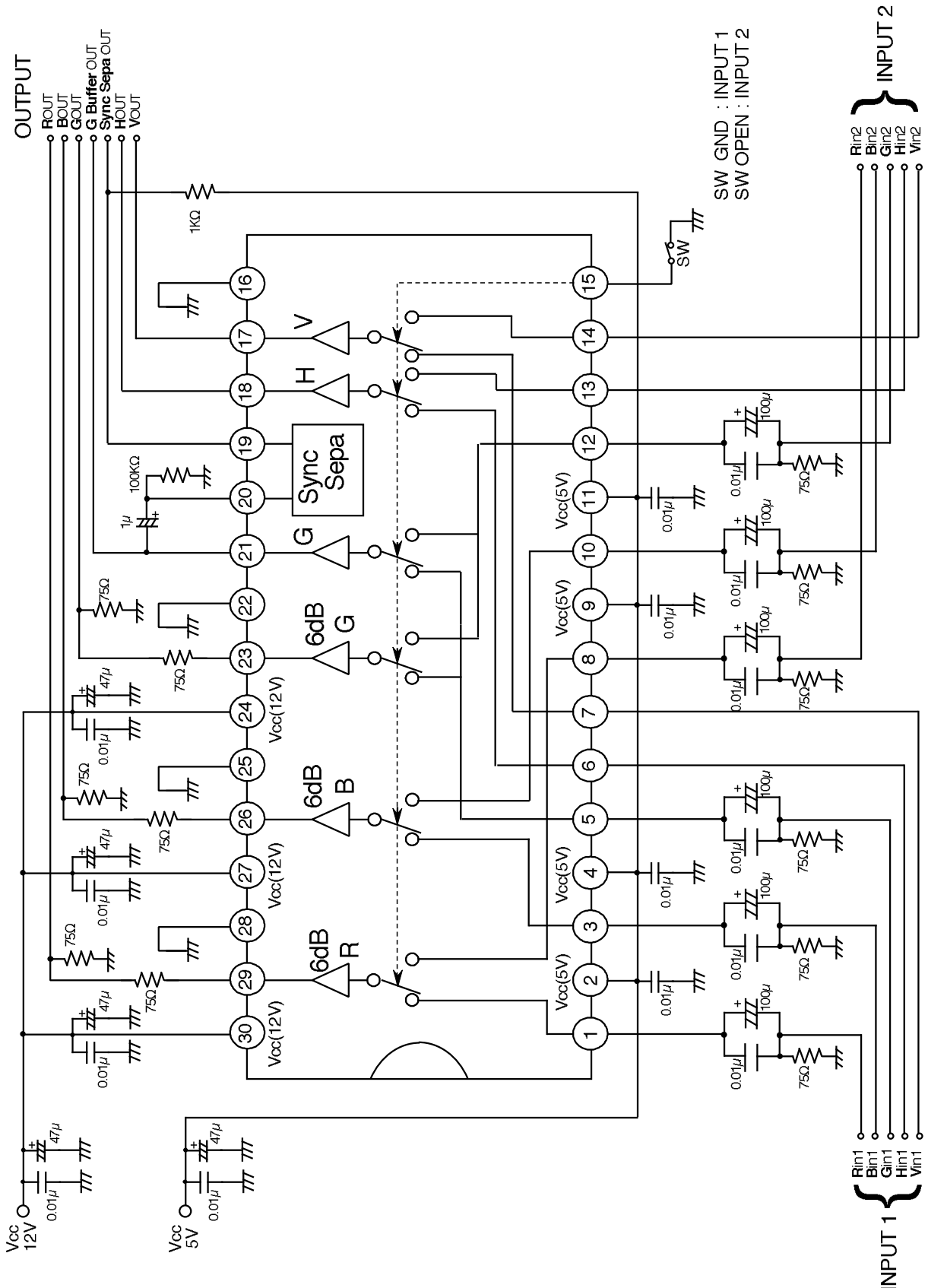
RECOMMENDED OPERATING CONDITION

Supply voltage range.....4.75 to 5.25V, 11.5 to 12.5V
Rated supply voltage.....5.0V, 12.0V



30 pin plastic SDIP

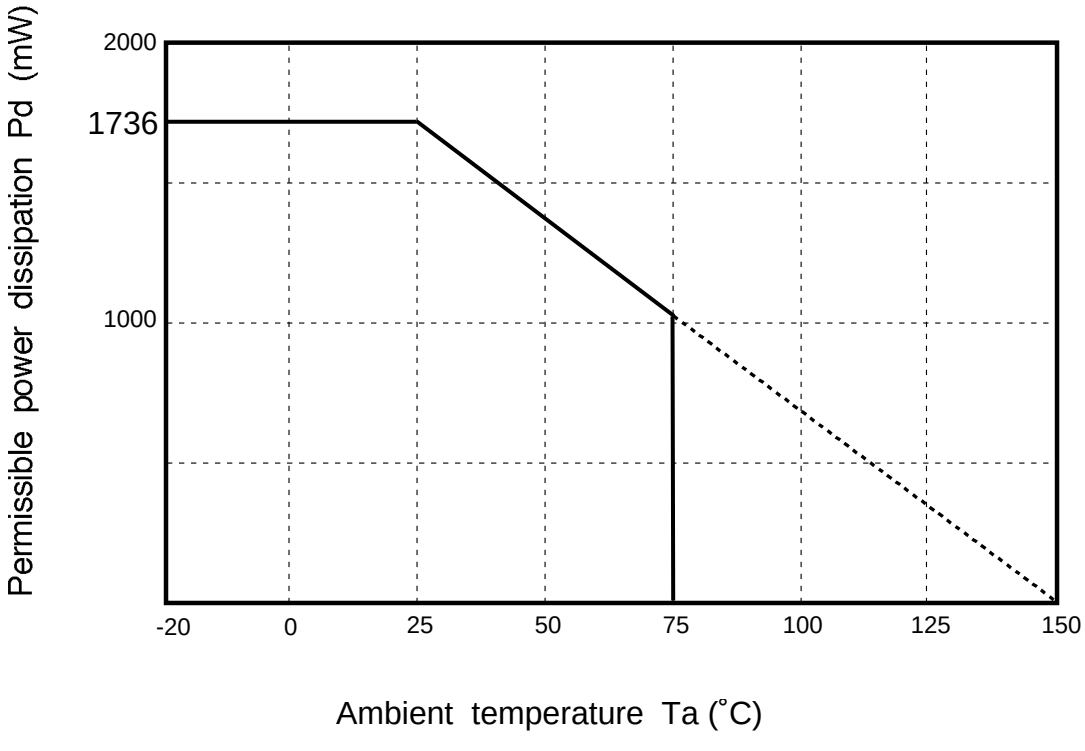
M52756SP BLOCK DIAGRAM and APPLICATION EXAMPLE



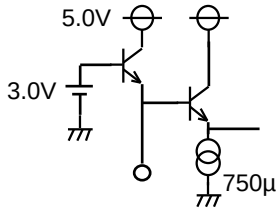
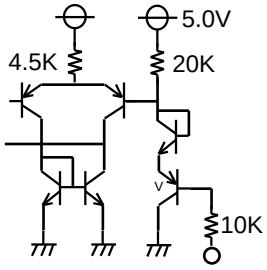
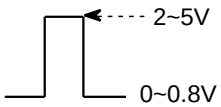
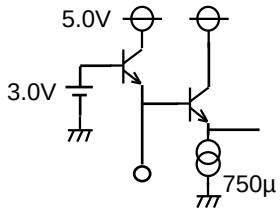
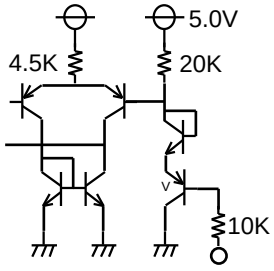
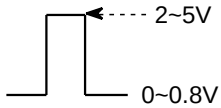
Absolute Maximum Rating (Ambient temperature: 25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	Vcc	6.0,13.0	V
Power dissipation	Pd	1736	mW
Ambient temperature	Topr	-20~+75	˚C
Storage temperature	Tstg	-40~+150	˚C
Recommended supply voltage	Vopr	5.0,12.0	V
Recommended sopply voltage range	Vopr'	4.75~5.25,11.5~12.5	V
Electrostatic discharge	Surge	±150	V

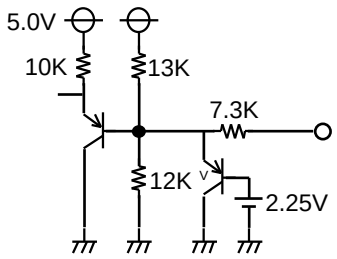
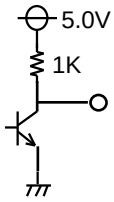
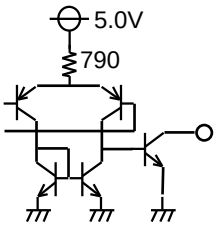
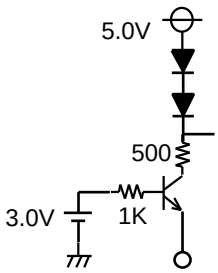
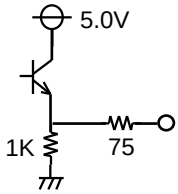
Thermal Derating Curve



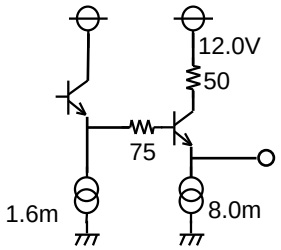
Pin Description

Pin No.	Description	DC Voltage[V]	Peripheral circuits at pins	Notes
1 3 5	Input 1 (R) Input 1 (B) Input 1 (G)	2.25		Input signal with low impedance.
2 4 9 11	Vcc(R) Vcc(B) Vcc(G) Vcc(H,V,Buffer, SW,SyncSep)	5.0	———	
6 7	Input 1 (H) Input 1 (V)	———		Input pulse between 2V and 5V. 
8 10 12	Input 2 (R) Input 2 (B) Input 2 (G)	2.25		Input signal with low impedance.
13 14	Input 2 (H) Input 2 (V)	———		Input pulse between 2V and 5V. 

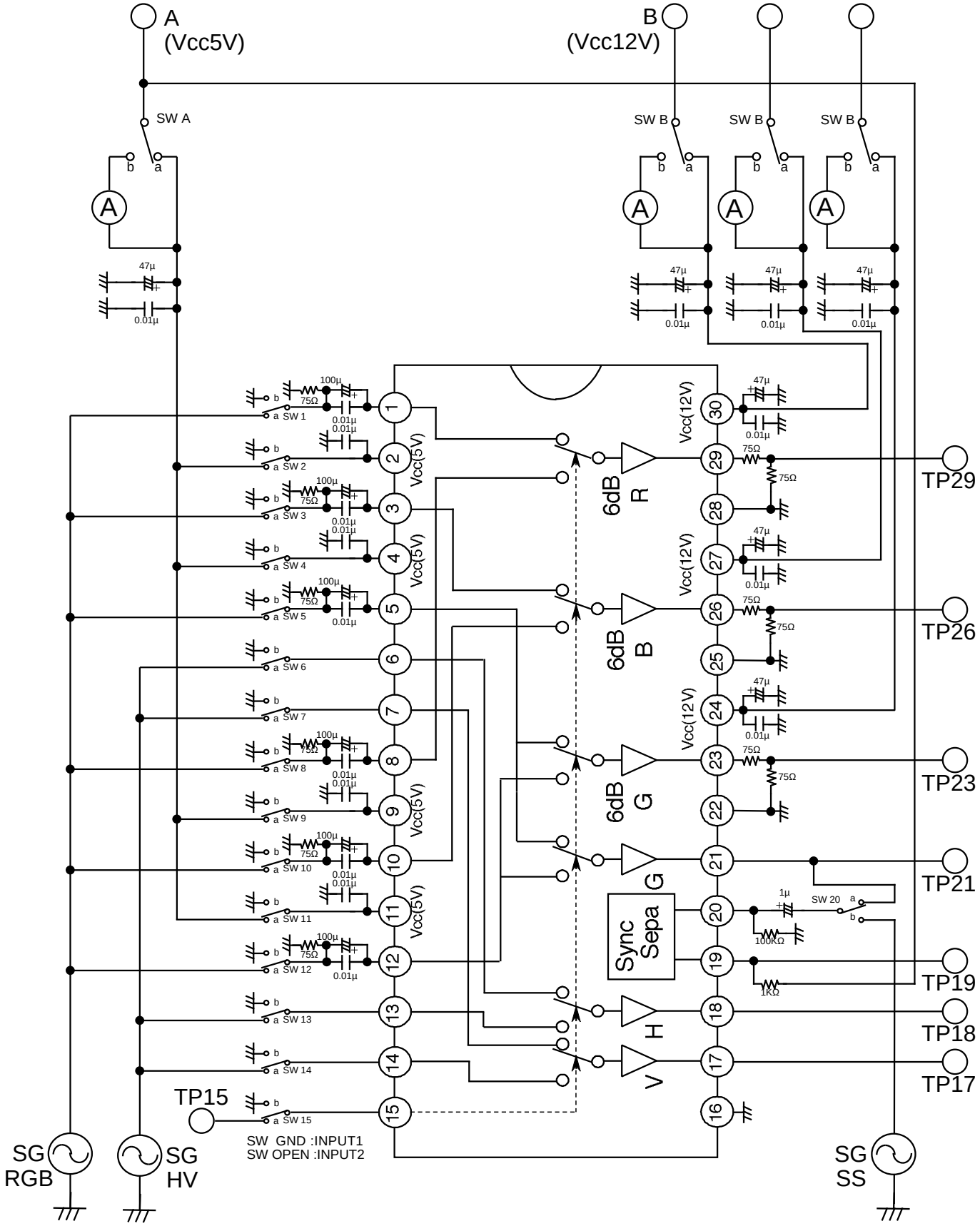
Pin Description

Pin No.	Description	DC Voltage[V]	Peripheral circuits at pins	Notes
15	Switch	2.4		Switch by OPEN and GND.
16 22 25 28	GND(H,V,Buffer, SW,SyncSep) GND(G) GND(B) GND(R)	GND	———	
17 18	Output(V) Output(H)	———		Output impedance is built in.
19	Sync Sepa OUT	———		Connect resistance more than 1KΩ is necessary during power supply and terminal that open collector output type. When not used, ground the pin to GND.
20	Sync Sepa IN	2.3		Input signal with low impedance. When not used, set to OPEN
21	OUTPUT (G Buffer)	0.75		Output impedance is built in.

Pin Description

Pin No.	Description	DC Voltage[V]	Peripheral circuits at pins	Notes
22 26 29	OUTPUT(G) OUTPUT(B) OUTPUT(R)	1.8		This output pin can drive connected load of 75Ω.
24 27 30	Vcc(G) Vcc(B) Vcc(R)	12.0	———	

Attached Fig.3 Measuring Circuit Diagram



Supplementary Table1 Electrical Characteristics (Vcc = 5V,12V; Ta = 25°C unless otherwise specified)

No.	Conditions / parameter	Symbol	Test Point(s)	Vcc (V)	Vcc (5V)				Input										S.Sep	SW	Standard			Unit	Remark
				Vcc	SW2 Vcc5V	SW4 Vcc5V	SW9 Vcc5V	SW11 Vcc5V	SW1 R1in	SW3 B1in	SW5 G1in	SW6 H1in	SW7 V1in	SW8 R2in	SW10 B2in	SW12 G2in	SW13 H2in	SW14 V2in	SW20 S.Sepin	SW15 Swich	MIN	TYP	MAX		
1	Circuit current 1 (no signal)	Icc1	A	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	a / b –	27	37	47	mA	note 1
	Circuit current 2 (no signal)	Icc2	B	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	a / b –	58	78	98	mA	note 1
	Circuit current 3 (power save)	Icc3	A	5	b –	b –	b –	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	a / b –	15	20	25	mA	note 1

RGB SW

No.	Conditions / parameter	Symbol	Test Point(s)	Vcc (V)	Vcc (5V)				Input										S.Sep	SW	Standard			Unit	Remark
				Vcc	SW2 Vcc5V	SW4 Vcc5V	SW9 Vcc5V	SW11 Vcc5V	SW1R 1in	SW3B1i n	SW5 G1in	SW6 H1in	SW7 V1in	SW8 R2in	SW10 B2in	SW12 G2in	SW13 H2in	SW14 V2in	SW20 S.Sepin	SW15 Swich	MIN	TYP	MAX		
2	Output DC voltage 1	$V_{DC}1$	T.P.29 T.P.26 T.P.23	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	b GND	0.7	1.0	1.3	V	note2
	Output DC voltage 2	$V_{DC}2$	T.P.29 T.P.26 T.P.23	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	a OPEN	0.7	1.0	1.3	V	note2
3	Output DC voltage 3	$V_{DC}3$	T.P.21	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	b GND	0.7	1.0	1.3	V	note3
	Output DC voltage 4	$V_{DC}4$	T.P.21	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	a –	a OPEN	0.7	1.0	1.3	V	note3
4	Maximum allowable input 1	$Vi_{max}1$	T.P.1 T.P.3 T.P.5	5,12	a 5V	a 5V	a 5V	a 5V	a b b SG1	b a b SG1	b b a SG1	b –	b –	b –	b –	b –	b –	b –	a –	b GND	1.6	2.0	—	Vp-p	note4
	Maximum allowable input 2	$Vi_{max}2$	T.P.8 T.P.10 T.P.12	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	a b b SG1	b a b SG1	b b a SG1	b –	b –	a –	a OPEN	1.6	2.0	—	Vp-p	note4

No.	Conditions / parameter	Symbol	Test Point(s)	Vcc (V)	Vcc (5V)					Input												S.Sep	SW	Standard			Unit	Remark
				Vcc	SW2 Vcc5V	SW4 Vcc5V	SW9 Vcc5V	SW11 Vcc5V	SW1 R1in	SW3 B1in	SW5 G1in	SW6 H1in	SW7 V1in	SW8 R2in	SW10 B2in	SW12 G2in	SW1 3H2in	SW14 V2in	SW20 S.Sepin	SW15 Swich	MIN	TYP	MAX		
5	Voltage gain1	$G_{V}1$	T.P.29 T.P.26 T.P.23	5,12	a 5V	a 5V	a 5V	a 5V	a b SG2	b a SG2	b a SG2	b –	b –	b –	b –	b –	b –	b –	a –	b GND	0.5	1.2	1.9	dB	note5
	Relative voltage qain1	$\Delta G_{V}1$			Relative to measured values above																-0.4	0	0.4	dB	note5
	Voltage gain2	$G_{V}2$	T.P.29 T.P.26 T.P.23	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	a b SG2	b a SG2	b a SG2	b –	b –	a –	a OPEN	0.5	1.2	1.9	dB	note5
	Relative voltage gain2	$\Delta G_{V}2$			Relative to measured values above																-0.4	0	0.4	dB	note5
	Relative voltage gain'	$\Delta G_{V}'$			Relative to measured values above																-0.4	0	0.4	dB	note5'
6	Voltage gain 3	$G_{V}3$	T.P.2 1	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	a SG2	b –	b –	b –	b –	b –	b –	b –	a –	b GND	-1.5	-0.8	0	dB	note6
	Voltage gain 4	$G_{V}4$	T.P.2 1	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	a SG2	b –	b –	a –	a OPEN	-1.5	-0.8	0	dB	note6
7	Freq. charactreistic 1 (100MHz)	Fc1	T.P.29 T.P.26 T.P.23	5,12	a 5V	a 5V	a 5V	a 5V	a b SG4	b a SG4	b a SG4	b –	b –	b –	b –	b –	b –	b –	a –	b GND	0	1.5	3.0	dB	note7
	Relative Freq. charactreistic 1 (100MHz)	$\Delta Fc1$			Relative to measured values above																-1.0	0	1.0	dB	note7
	Freq. charactreistic 2 (100MHz)	Fc2	T.P.29 T.P.26 T.P.23	5,1 2	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	a b SG4	b a SG4	b a SG4	b –	b –	a –	a OPEN	0	1.5	3.0	dB	note7
	Relative Freq. charactreistic 2 (100MHz)	$\Delta Fc2$			Relative to measured values above																-1.0	0	1.0	dB	note7
8	Freq. charactreistic3 (250MHz)	Fc3	T.P.29 T.P.26 T.P.23	5,1 2	a 5V	a 5V	a 5V	a 5V	a b SG5	b a SG5	b a SG5	b –	b –	b –	b –	b –	b –	b –	a –	b GND	-3.0	-1.5	1.0	dB	note8
	Freq. charactreistic4 (250MHz)	Fc4	T.P.29 T.P.26 T.P.23	5,1 2	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	a b SG5	b a SG5	b a SG5	b –	b –	a –	a OPEN	-3.0	-1.5	1.0	dB	note8

No.	Conditions / parameter	Symbol	Test Point(s)	Vcc (V)	Vcc (5V)				Input											S.Sep	SW	Standard			Unit	Remark
				Vcc	SW2 Vcc5V	SW4 Vcc5V	SW9 Vcc5V	SW11 Vcc5V	SW1 R1in	SW3 B1in	SW5 G1in	SW6 H1in	SW7 V1in	SW8 R2in	SW10 B2in	SW12 G2in	SW1 3H2in	SW14 V2in	SW20 S.Sepin	SW15S wich	MIN	TYP	MAX		
9	Crosstalk between two inputs 1 (10MHz)	C.T.I.1	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	a b b SG3	b a b SG3	b b a SG3	b —	b —	b —	b —	b —	b —	b —	a —	GND → OPEN	—	-60	-50	dB	note9
	Crosstalk between two inputs 2 (10MHz)	C.T.I.2	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	a b b SG3	b a b SG3	b b a SG3	b —	b —	a —	OPEN → GND	—	-60	-50	dB	note9
10	Crosstalk between two inputs 3 (100MHz)	C.T.I.3	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	a b b SG4	b a b SG4	b b a SG4	b —	b —	b —	b —	b —	b —	b —	a —	GND → OPEN	—	-40	-30	dB	note10
	Crosstalk between two inputs 4 (100MHz)	C.T.I.4	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	a b b SG4	b a b SG4	b b a SG4	b —	b —	a —	OPEN → GND	—	-40	-30	dB	note10
11	Crosstalk between channels 1 (10MHz)	C.T.C1	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	a b b SG3	b a b SG3	b b a SG3	b —	b —	b —	b —	b —	b —	b —	a —	b GND	—	-50	-40	dB	note11
	Crosstalk between channels 2 (10MHz)	C.T.C2	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	a b b SG3	b a b SG3	b b a SG3	b —	b —	a —	a OPEN	—	-50	-40	dB	note11
12	Crosstalk between channels 3 (100MHz)	C.T.C3	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	a b b SG4	b a b SG4	b b a SG4	b —	b —	b —	b —	b —	b —	b —	a —	b GND	—	-30	-25	dB	note12
	Crosstalk between channels 4 (100MHz)	C.T.C4	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	b a b SG4	a b b SG4	b b a SG4	b —	b —	a —	a OPEN	—	-30	-25	dB	note12
13	Pulse characteristic 1	Tr1	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	a SG6	a SG6	a SG6	b —	b —	b —	b —	b —	b —	b —	a —	b GND	—	1.0	2.0	nsec	note13
		Tf1	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	a SG6	a SG6	a SG6	b —	b —	b —	b —	b —	b —	b —	a —	b GND	—	1.0	2.0	nsec	note13
	Pulse characteristic 2	Tr2	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	a SG6	a SG6	a SG6	b —	b —	a —	a OPEN	—	1.0	2.0	nsec	note13
		Tf2	T.P.29 T.P.26 T.P.23	5, 12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	a SG6	a SG6	a SG6	b —	b —	a —	a OPEN	—	1.0	2.0	nsec	note13

HV SW

No	Conditions / parameter	Symbol	Test Point(s)	Vcc (V)	Vcc (5V)					Input											S.Sep	SW	Standard			Unit	Remark
				Vcc	SW2 Vcc5V	SW4 Vcc5V	SW9 Vcc5V	SW11 Vcc5V	SW1 R1in	SW3 B1in	SW5 G1in	SW6 H1in	SW7 V1in	SW8 R2in	SW10 B2in	SW12 G2in	SW13 H2in	SW14 V2in	SW20 S.Sepin	SW15 Swich	MIN	TYP	MAX		
14	High level output voltage 1	VoH1	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	ab 5.0V	ba 5.0V	b —	b —	b —	b —	b —	a —	b GND	4.5	5.0	—	V	note14
	High level output voltage 2	VoH2	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	b —	b —	b —	ab 5.0V	ba 5.0V	a —	a OPEN	4.5	5.0	—	V	note14
15	Low level output voltage 1	VoL1	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	ab 0V	ba 0V	b —	b —	b —	b —	b —	a —	b GND	—	0.2	0.5	V	note15
	Low level output voltage 2	VoL2	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	b —	b —	b —	ab 0V	ba 0V	a —	a OPEN	—	0.2	0.5	V	note15
16	Input selectional voltage 1	Vith1	T.P.6 T.P.7	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	ab Voltage	ba Voltage	b —	b —	b —	b —	b —	a —	b GND	1.2	1.6	2.0	V	note16
	Input selectional voltage 2	Vith2	T.P.13 T.P.14	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	b —	b —	b —	ab Voltage	ba Voltage	a —	a OPEN	1.2	1.6	2.0	V	note16
17	Rising delay time 1	Trd1	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	ab SG7	ba SG7	b —	b —	b —	b —	b —	a —	b GND	—	100	150	nsec	note17
	Rising delay time 2	Trd2	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	b —	b —	b —	ab SG7	ba SG7	a —	a OPEN	—	100	150	nsec	note17
18	Falling delay time 1	Tfd1	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	ab SG7	ba SG7	b —	b —	b —	b —	b —	a —	b GND	—	50	100	nsec	note18
	Falling delay time 2	Tfd2	T.P.17 T.P.18	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	b —	b —	b —	ab SG7	ba SG7	a —	a OPEN	—	50	100	nsec	note18
19	Switching selectional voltage 1	Vsth1	T.P.15	5,12	a 5V	a 5V	a 5V	a 5V	a SG1	a SG1	a SG1	a SG7	a SG7	b —	b —	a SG1	a SG1	a SG7	a —	a Voltage	0.5	1.7	2.0	V	note19
	Switching selectional voltage 2	Vsth2	T.P.15	5,12	a 5V	a 5V	a 5V	a 5V	b —	b —	b —	b —	b —	a SG1	a SG1	a SG1	a SG7	a SG7	a —	a Voltage	0.5	1.7	2.0	V	note19

SYNC SEP

No	Conditions / parameter	Symbol	Test Point(s)	Vcc (V)	Vcc (5V)				Input										S.Sep	SW	Standard			Unit	Remark
				Vcc	SW2 Vcc5V	SW4 Vcc5V	SW9 Vcc5V	SW11 Vcc5V	SW1 R1in	SW3 B1in	SW5 G1in	SW6 H1in	SW7 V1in	SW8 R2in	SW10 B2in	SW12 G2in	SW13 H2in	SW14 V2in	SW20 S.Sepin	SW15S wich	MIN	TYP	MAX		
20	SOG input maximum noize voltage	SS_{NV}	T.P.19	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b SG8	b –	—	—	0.03	Vpp	note20
21	SOG minimum input voltage	SS_{SV}	T.P.19	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b SG8	b –	0.2	—	—	Vpp	note21
22	Sync output hi level	V_{SH}	T.P.19	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b SG8	b –	4.5	4.9	—	V	note22
	Sync output lo level	V_{SL}	T.P.19	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b SG8	b –	—	0.3	0.5	V	note22
23	Sync output delay time 1	Tdsf	T.P.19	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b SG8	b –	—	50	100	nsec	note23
	Sync output delay time 2	Tdsr	T.P.19	5,12	a 5V	a 5V	a 5V	a 5V	b –	b –	b –	b –	b –	b –	b –	b –	b –	b –	b SG8	b –	—	120	200	nsec	note23

note) It omits the SW.No accorded with signal input pin because it is already written in Table 1.
SW A is in side a if there is not defined specially.

note1) The condition is shown as Table 1. Set SW15 to GND(or OPEN) and SW A to side b, measure the current by current meter A(or B). The current is as Icc1(Icc2,Icc3).

note2) Set SW15 to GND (or OPEN), measure the DC voltage of T.P.29(T.P.26,T.P.23) when there is no signal input.The DC voltage is as $V_{DC}1$(or $V_{DC}2$).

note3) Measure the DC voltage of T.P.21 same as note2, the DC voltage is as $V_{DC}3$(or $V_{DC}4$).

note4) Set SW15 to GND, SG1 as the input signal of Pin 1.Rising up the amplitude of SG1 slowly, read the amplitude of input signal when the output waveform is distorted. The amplitude is as Vimax1. And measure Vimax1 when SG1 as the input signal of Pin 3,Pin 5 in same way.
Next, set SW 15 to OPEN, measure Vimax2 when SG1 as the input signal of Pin8, 10, 12.

note5) 1. The condition is shown as Table 1.
2. Set SW15 to GND, SG2 as the input signal of Pin 1. At this time, read the amplitude output from T.P 29. The amplitude is as $V_{OR}1$.
3. Voltage gain Gv1 is

$$G_V1 = 20 \text{ LOG} \frac{V_{OR}1 \text{ [Vp-p]}}{0.7 \text{ [Vp-p]}} \text{ [dB]}$$

4. The method as same as 2 and 3, measure the voltage gain Gv1 when SG2 as the input signal of Pin 3, 5.
5. The difference of each channel relative voltage gain is as ΔGv1.
ΔGv1=Gv1R-Gv1B,Gv1B-Gv1G,Gv1G-Gv1R
6. Set SW15 to OPEN, measure Gv2, ΔGv2 in the same way.

note5') Voltage gain ΔGv' is
ΔGv'=Gv1R-Gv2R,Gv1G-Gv2G,Gv1B-Gv2B

note6) 1. The condition is shown as table 1. This test is by active probe.
2. Measure the amplitude output from T.P.21.
3. Measure the G_V3,G_V4 by the same way as note5.

note7) 1. The condition is shown as table 1. This test is by active probe.
2. Set SW15 to GND, SG2 as the input signal of Pin 1. Measure the amplitude output from T.P.29. The amplitude is as $V_{OR}1$.By the same way, measure the output when SG4 is as input signal of Pin 1, the output is as $V_{OR}2$.
3. The frequency characteristic Fc1 is

$$F_C1 = 20 \text{ LOG} \frac{V_{OR}2 \text{ [Vp-p]}}{V_{OR}1 \text{ [Vp-p]}} \text{ [dB]}$$

4. The method as same as 2 and 3, measure the frequency Fc1 when input signal to Pin 3, 5.
5. The difference between of each channel frequency characteristic is as ΔFc1.
6. Set SW15 to OPEN, measure Fc2,ΔFc2.

note8) By the same way as Note7 measure the Fc3, Fc4 when SG5 of input signal.

note9) 1. The condition is shown as Table1. This test is by active prove.
2. Set SW15 to GND, SG3 as the input signal of Pin 1. Measure the amplitude output from T.P.29. The amplitude is as $V_{OR}3$.
3. Set SW15 to OPEN, measure the amplitude output from T.P.29. The amplitude is as $V_{OR}3'$.
4. The crosstalk between two inputs C.T.I.1 is

$$\text{C.T.I.1} = 20 \text{ LOG} \frac{V_{OR}3' \text{ [Vp-p]}}{V_{OR}3 \text{ [Vp-p]}} \text{ [dB]}$$

5. By the same way, measure the crosstalk between two inputs when SG3 as the input signal of Pin3, Pin 5.

6. Next, set SW15 to OPEN, SG3 as the input signal of Pin 8, measure the amplitude output from T.P.29. The amplitude is as $V_{OR}4$.
7. Set SW15 to GND, measure the amplitude output from T.P.29. The amplitude is as $V_{OR}4'$.
8. The crosstalk between two inputs C.T.I.2 is

$$C.T.I.2 = 20\ LOG \frac{V_{OR}4'[Vp\text{-}p]}{V_{OR}4[Vp\text{-}p]}\ [dB]$$

9. By the same way, measure the crosstalk between channels when SG3 as the input signal of Pin 10,12.

note10) Set SG4 as the input signal, and then the same method as note9, measure C.T.I.3, C.T.I.4.

note11) 1. The condition is as Table 1. This test is by active prove.
2. Set SW15 to GND, SG3 as the input signal of Pin 1. Measure the amplitude output from T.P.29. The amplitude is as $V_{OR}5$.
3. Next, measure T.P.26, T.P.23 in the same state, and the amplitude is as V_{OG} 5, V_{OB} 5.
4. The crosstalk between channels C.T.C.1 is

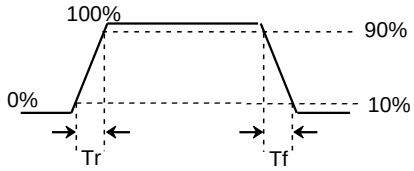
$$C.T.C1 = 20\ LOG \frac{V_{OG}5\ \text{or}\ V_{OB}5}{V_{OR}5}\ [dB]$$

5. Measure the crosstalk between channels when SG3 is as the input signal of Pin 3, Pin 5 .
6. Next, set SW15 to OPEN, SG3 as the input signal of Pin8, measure the amplitude output from T.P.29. The amplitude is as $V_{OR}6$.
7. Next, measure the amplitude output from T.P.26, T.P.23 in the same state. The amplitude is as $V_{OG}6$, $V_{OB}6$.
8. The crosstalk between channels C.T.C.2 is $C.T.C2 = 20\ LOG \frac{V_{OG}6\ \text{or}\ V_{OB}6}{V_{OR}6}\ [dB]$

9. By the same way, measure the crosstalk between channels when input signal to Pin10, 12.

note12) Set SG4 as the input signal, and the same method as note11, measure C.T.C.3, C.T.C.4.

note13) 1. The condition is as Table 1. Set SW15 to GND (or OPEN).
2. The rising of 10 % ~ 90 % for input pulse is Tri, the falling of 10 % ~ 90 % for input pulse is Tfi.
3. Next, the rising of 10 % ~ 90 % for output pulse is Tro, the falling of 10 % ~ 90 % for output pulse is Tfo.
4. The pulse characteristic Tr1, Tf1 (Tr2, Tf2) is



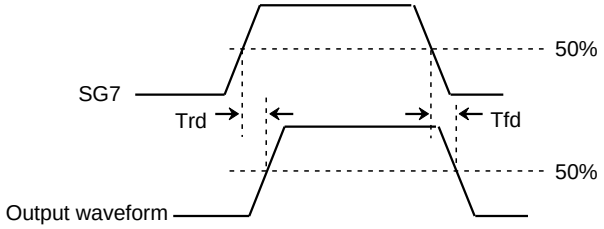
$$Tr1(Tr2) = \sqrt{(Tro)^2 - (Tri)^2}\ (nsec) \qquad Tf1(Tf2) = \sqrt{(Tfo)^2 - (Tfi)^2}\ (nsec)$$

note14) The condition is as Table 1. Set SW15 to GND (OPEN), input 5V at input terminal. Measure the output voltage, the voltage is as $V_{OH}1$ ($V_{OH}2$).

note15) The condition is as Table 1. Set SW15 to GND (OPEN), input 0V at input terminal. Measure the output voltage, the voltage is as $V_{OL}1$ ($V_{OL}2$).

note16) The condition is as table 1. Set SW15 to GND (OPEN), increasing gradually the voltage of input terminal from 0V, measure the voltage of input terminal when output terminal is 4.5V. The input voltage is as Vith1(Vith 2).

note17, note18) The condition is as table 1. Set SW15 to GND (OPEN), SG7 is as the input signal of input terminal, measure the waveform of output. Rising delay time is as Trd1 (Trd2). Falling delay time is as Tfd1(Tfd2). Reference to the Fig. as shown below.



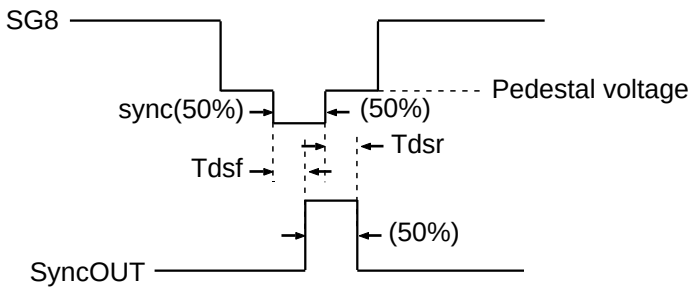
note19) 1. The condition is as table 1. SG1 is as the input signal of Pin1, Pin3, Pin5, and SG7 is as the input signal of Pin6, Pin7. There is no input at another pins.
2. Input 0V at Pin15, confirm that there are signals output from T.P.29, T.P.26, T.P.23, T.P.21, T.P.18,T.P.17.
3. Increasing gradually the voltage of terminal Pin15. Read the voltage when there is no signal output from the terminals listed as above. The voltage is as Vsth1.
4. SG1 as the input signal of Pin8, Pin10, Pin12, and SG7 as the input signal of Pin13, Pin14. There is no input at another pins.
5. Inputs 5V at Pin15, confirm that there is no signal output from T.P29, T.P.26, T.P.23, T.P.21, T.P.18,T.P.17.
6. Decreasing gradually the voltage of terminal Pin 15. Read the voltage when there are signals output from the terminals listed as above. The voltage is as Vsth2.

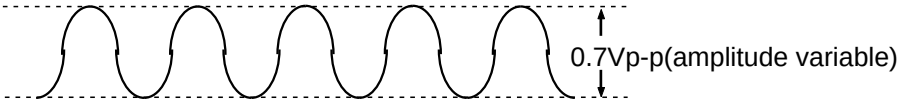
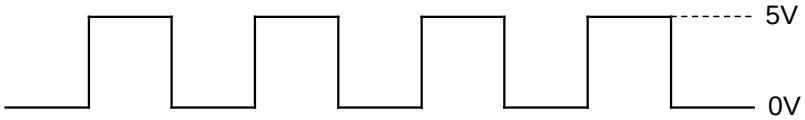
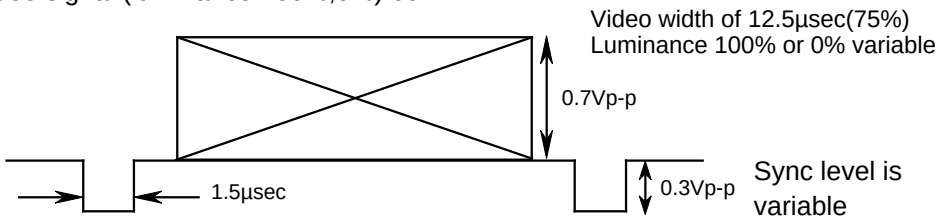
note20) The condition is as table 1. SG8 of luminance 0% is the input signal of Pin20. Increase sync level from 0Vp-p to 0.02Vp-p. Confirm outputting no pluse.

note21) The condition is as table 1. SG8 of luminance 100%(or 0%) is the input signal of Pin20. Decrease sync level from 0.3Vp-p to 0.2Vp-p. Confirm no malfunction produced by noise.

note22) The condition is as table 1. SG8 of luminance 100%(or 0%) is the input signal of Pin20. Measure the high(low) at SyncOUT. The measured value is treated as V_{SH}(V_{SL}).

note23) The condition is as table 1. SG8 of luminance 100%(or 0%) is the input signal of Pin20. SyncOUT becomes High with sync part of SG8. Measure the time needed for the front(rear) edge of SG8 sync to fall(rise) from 50% and for SyncOUT to rise(fall) from 50% with an active prove. The measured value is treated as Tdsf(Tdsr).



Symbol	Input Signal
SG1	Sine wave (f = 60 kHz, 0.7Vp-p, amplitude variable) 
SG2	Sine wave (f = 1 MHz, amplitude 0.7Vp-p)
SG3	Sine wave (f = 10 MHz, amplitude 0.7Vp-p)
SG4	Sine wave (f = 100 MHz, amplitude 0.7Vp-p)
SG5	Sine wave (f = 250 MHz, amplitude 0.7Vp-p)
SG6	Pulse with amplitude 0.7Vp-p (f = 60 kHz, duty 80%) 
SG7	Square wave (Amplitude 5.0 Vo-p TTL, f = 60 KHz, duty 50%) 
SG8	Video signal (luminance 100%,0%) 60KHz 

Note how to use this IC

1. R, G, B input signal is 0.7Vp-p of standard video signal.

2. H, V input is 2.0V(minimum) TTL type.

3. Input signal with sufficient low impedance to input terminal.

4. The terminal of H, V output pin are shown as Fig.4. It is possible to reduce rise time by insert the resistor between Vcc line and H, V output Pin, but set the value of resistor in order that the current is under 7.5 mA. Setting the value of R is more than 2kΩ as shown in Fig.4 .

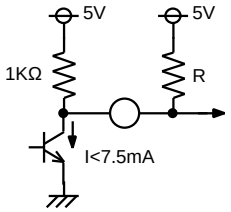


Fig.4

5. Switch (Pin 15) can be changed when this terminal is GND or OPEN
   When GND : Signal output from input 1
   When OPEN : Signal output from input 2
   When the switch is being used as Fig.5
   0 ~ 0.5V : Signal output from input 1
   2 ~ 5 V : Signal output from input 2
   It is not allowable to set voltage higher than Vcc.

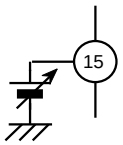
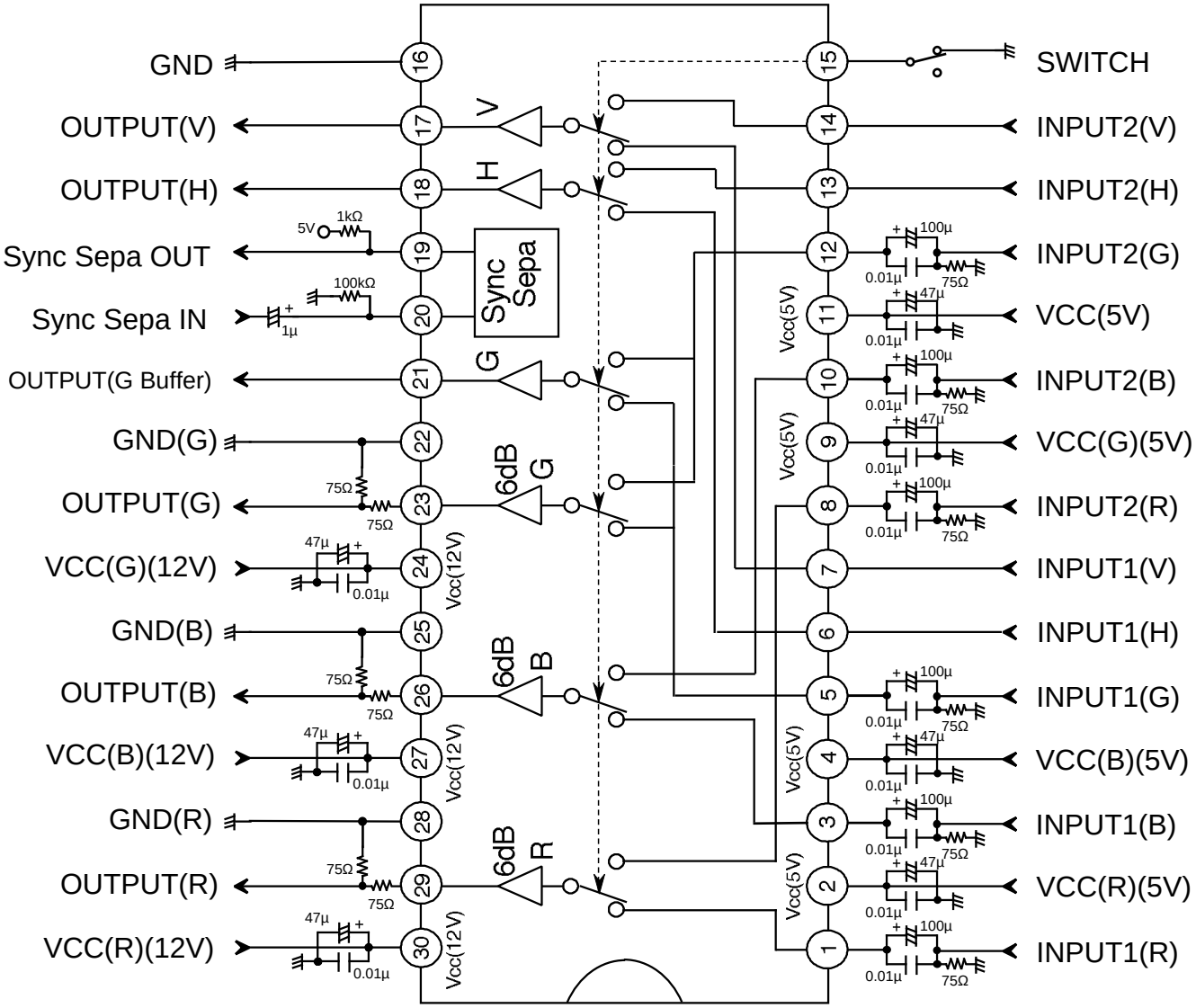


Fig.5

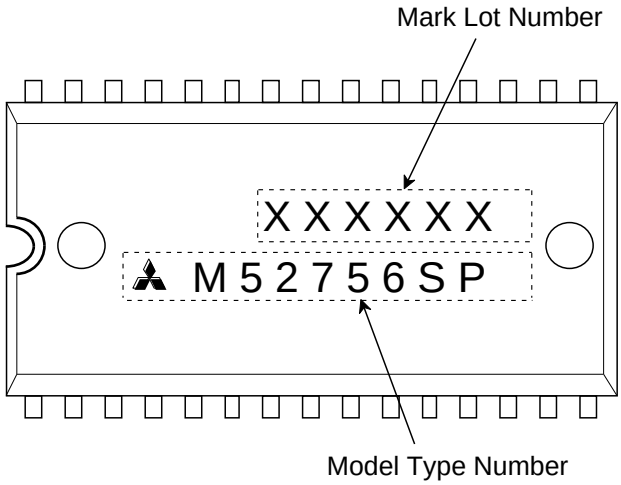
Notice of making printed circuit board.

Please notice following as shown below. It will maybe cause something oscillation because of the P.C.B. layout of the wide band analog switch.
- The distance between resistor and output pin is as short as possible.
- The capacitance of output terminal as small as possible.
- Set the capacitance between Vcc and GND near the pins if possible.
- Using stable power-source.
  The separated 12V-power-source (if possible the separated 5V-power-source will be better).
- Assign an area as large as possible for grounding.
- Pay attention to leak of signaling from the output.

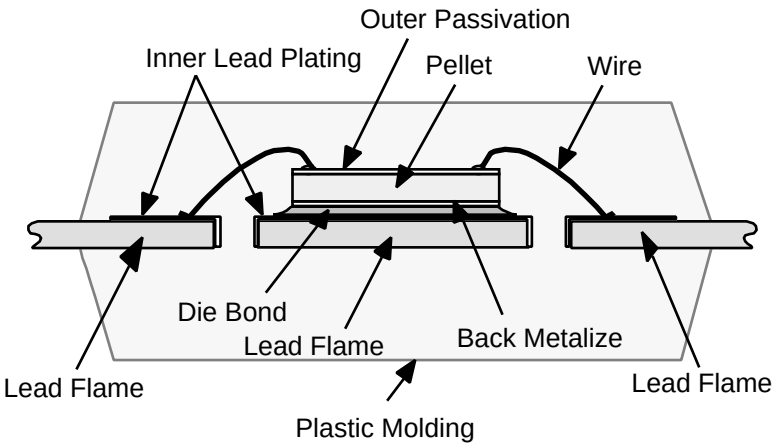
Attached Fig.6 Application Example



Marking



Structure



Material

Mold Material	: Epoxy
Wire Material	: Au
Outer Lead Treatment	: Solder Plating
Lead Flame Material	: Tin Nickel Copper
Inner Lead Treatment	: Silver Plating
Over Passivation	: SiN

Factory

Fukuoka,Japan