M58CR032C
M58CR032D

32 Mbit (2Mb x 16, Dual Bank, Burst)
1.8V Supply Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 1.65V to 2V for Program, Erase and Read
  - V_{DDQ} = 1.65V to 3.3V for I/O Buffers
  - V_{PP} = 12V for fast Program (optional)
- SYNCHRONOUS / ASYNCHRONOUS READ
  - Burst mode Read: 54MHz
  - Page mode Read (4 Words Page)
  - Random Access: 85, 100, 120 ns
- PROGRAMMING TIME
  - 10µs by Word typical
  - Double/Quadruple Word programming option
- MEMORY BLOCKS
  - Dual Bank Memory Array: 8/24 Mbit
  - Parameter Blocks (Top or Bottom location)
- DUAL OPERATIONS
  - Read in one Bank while Program or Erase in other
  - No delay between Read and Write operations
- BLOCK LOCKING
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for Block Lock-Down
- SECURITY
  - 64 bit user programmable OTP cells
  - 64 bit unique device identifier
  - One parameter block permanently lockable
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

Figure 1. Packages

TFBGA56 (ZB)
6.5 x 10 mm

- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M58CR032C: 88C8h
  - Bottom Device Code, M58CR032D: 88C9h

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SUMMARY DESCRIPTION

The M58CR032 is a 32 Mbit (2Mbit x16) non-volatile Flash memory that may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.65V to 2.0V V_{DD} supply for the circuitry and a 1.65V to 3.3V V_{DDQ} supply for the Input/Output pins. An optional 12V V_{PP} power supply is provided to speed up customer programming. The V_{PP} pin can also be used as a control pin to provide absolute protection against program or erase.

The device features an asymmetrical block architecture. M58CR032 has an array of 71 blocks and is divided into two banks, Banks A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible in Bank B or vice versa. Only one bank at a time is allowed to be in program or erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architecture is summarized in Table 2, and the memory maps are shown in Figure 4. The Parameter Blocks are located at the top of the memory address space for the M58CR032C and at the bottom for the M58CR032D.

Each block can be erased separately. Erase can be suspended, in order to perform either read or program in any other block, and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for page mode read. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 54MHz.

The M58CR032 features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power Up.

The device includes a 128 bit Protection Register and a Security Block to increase the protection of a system's design. The Protection Register is divided into two 64 bit segments. The first segment contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. The Security Block, parameter block 0, can be permanently protected by the user. Figure 5, shows the Security Block and Protection Register Memory Map.

The memory is offered in a TFBGA56, 0.75 mm ball pitch package and is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

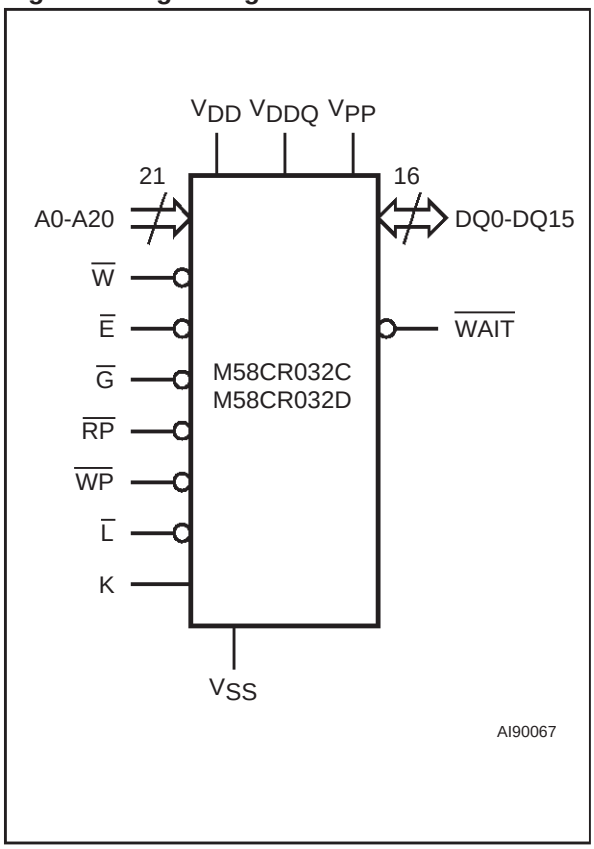


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ15	Data Input/Outputs or Address Inputs, Command Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power-down
$\overline{WP}$	Write Protect
K	Burst Clock
$\overline{L}$	Latch Enable
$\overline{WAIT}$	Wait Data in Burst Mode
V_{DD}	Supply Voltage
V_{DDQ}	Supply Voltage for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
V_{SSQ}	Ground Input/Output Supply
NC	Not Connected Internally

Figure 3. TFBGA Connections (Top view through package)

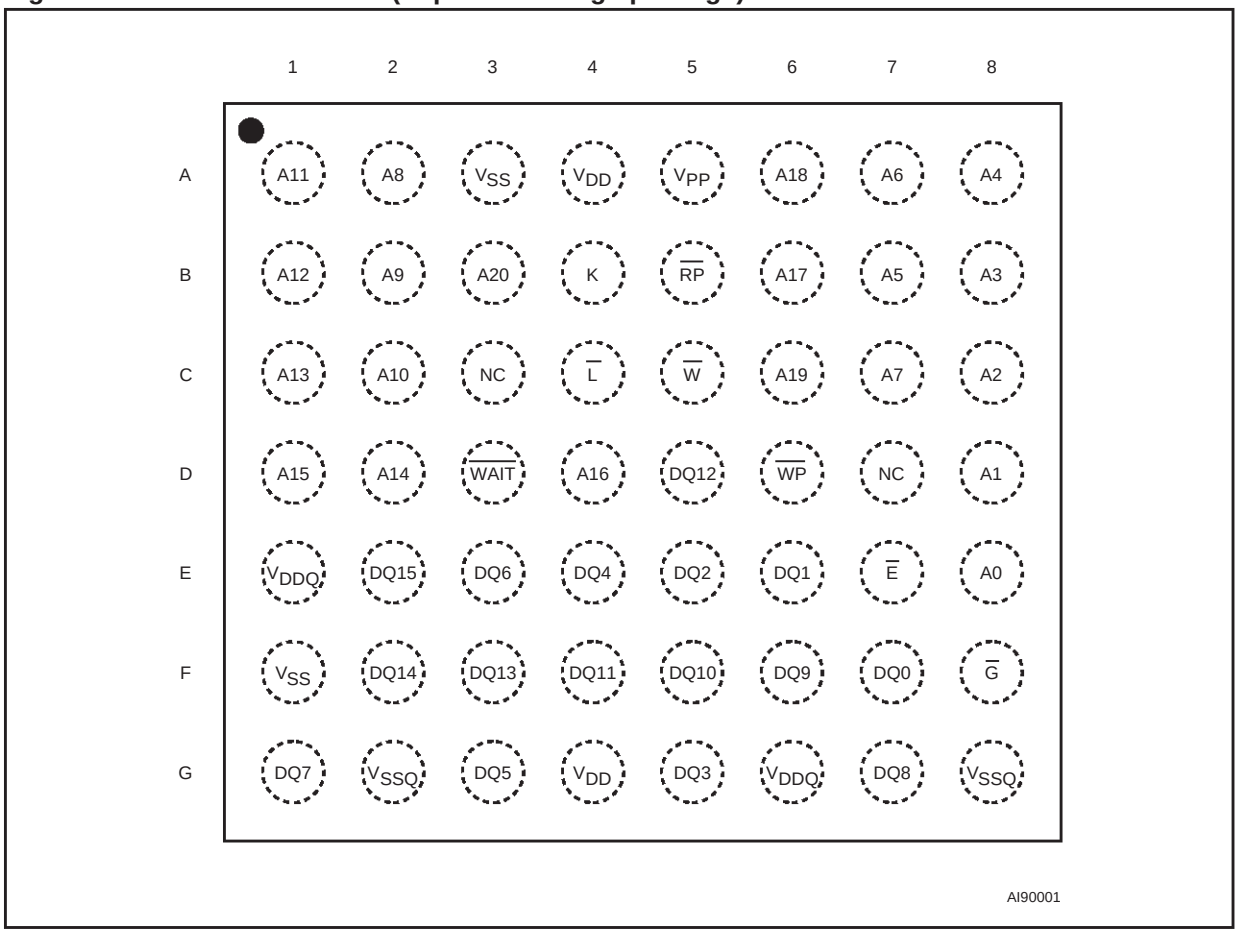


Table 2. Bank Architecture

	Bank Size	Parameter Blocks	Main Blocks
Bank A	8 Mbit	8 blocks of 4 KWord	15 blocks of 32 KWord
Bank B	24 Mbit	-	48 blocks of 32 KWord

Figure 4. Memory Map

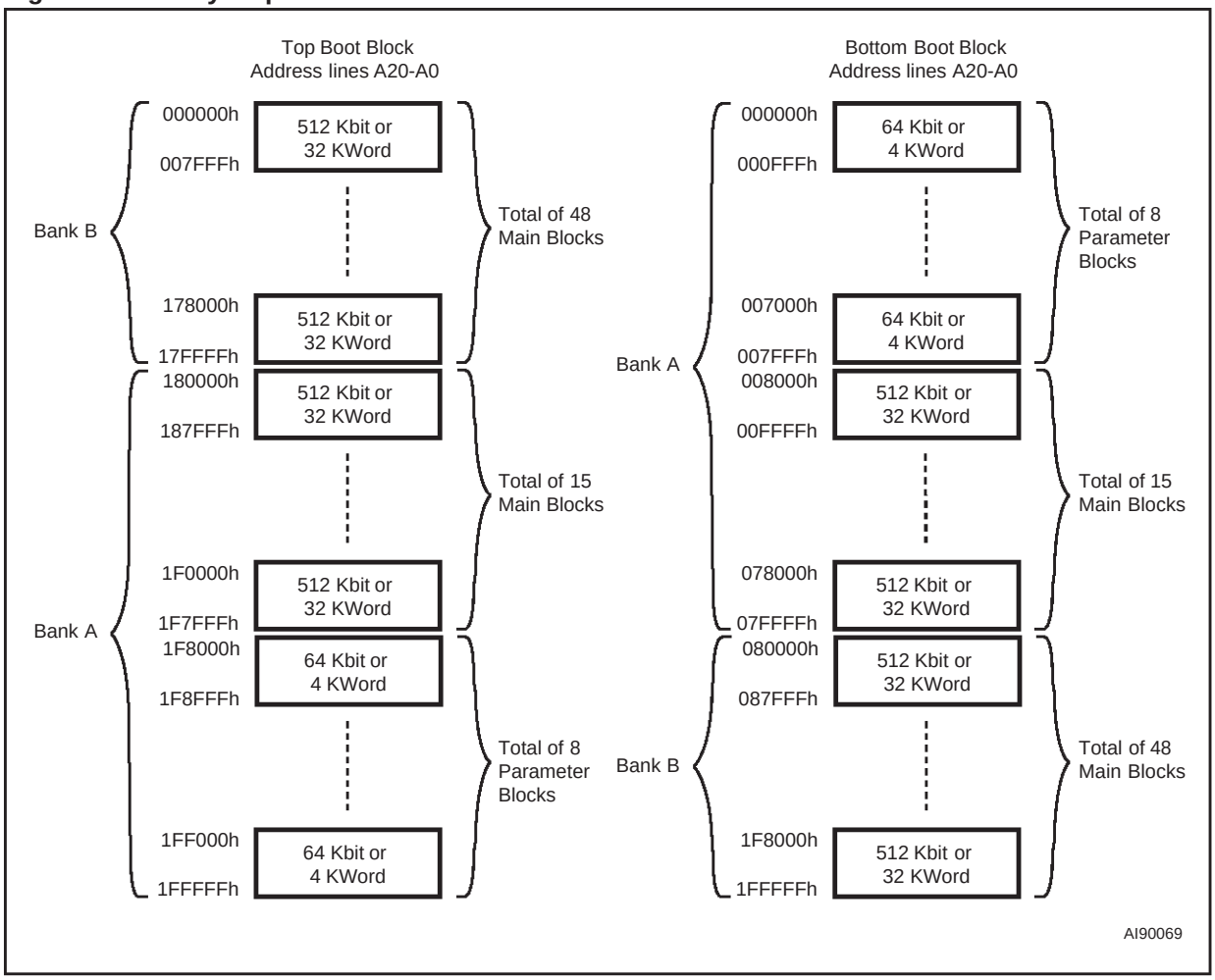
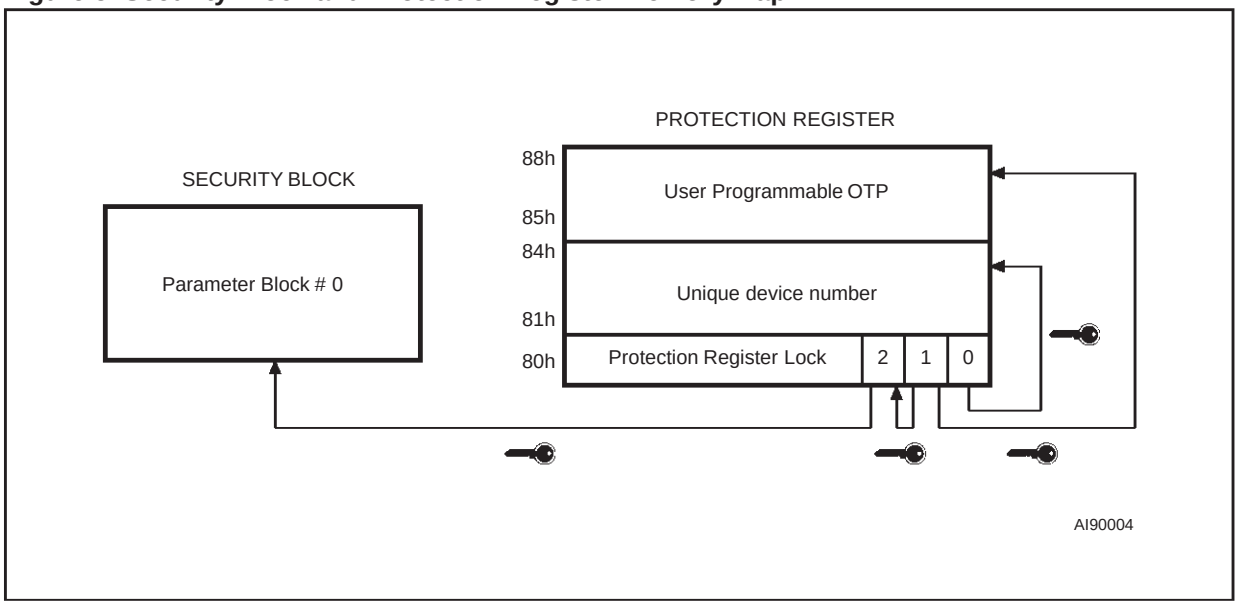


Figure 5. Security Block and Protection Register Memory Map



SIGNAL DESCRIPTIONS

See Figure 2 Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A20). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

The address inputs for the memory array are latched on the rising edge of Latch Enable L. The address latch is transparent when L is at V_{IL}. In synchronous operations the address is also latched on the first rising/falling edge of K (depending on clock configuration) when L is low. During a Write operation the address is latched on the rising edge of L or W, whichever occurs first.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

Both input data and commands are latched on the rising edge of Write Enable, W. When Chip Enable, E, and Output Enable, G, are at V_{IL} the data bus outputs data from the Memory Array, the Electronic Signature, Manufacturer or Device codes, the Block Protection Status, the Burst Configuration Register, the Protection Register or the Status Register. The data bus is high impedance when the chip is deselected, Output Enable, G, is at V_{IH}, or Reset/Power-Down, RP, is at V_{IL}.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable, E, is at V_{IH}, the memory is deselected and the power consumption is reduced to the standby level. Chip Enable can also be used to control writing to the Command Interface and to the memory array, while Write Enable, W, remains at V_{IL}.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When Output Enable, G, is at V_{IH} the outputs are high impedance.

Write Enable ($\overline{W}$). The Write Enable controls the Bus Write operation of the memory's Command Interface. Data are latched on the rising edge of Write Enable.

Write Protect ($\overline{WP}$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the block cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the block can be locked or unlocked. (refer to Table 10, Read Protection Register).

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down input provides hardware reset of the memory, and/or Power-Down functions, depending on the Burst Configuration Register status. A Reset or Power-Down of the memory is achieved by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPH}. When the reset pulse is given, the memory will recover from Power-Down (when enabled) in a minimum of t_{PHEL}, t_{PHLL} or t_{PHWL} (see Table 25 and Figure 16) after the rising edge of $\overline{RP}$. After a Reset or Power-Up the device is configured for asynchronous page read (M15=1) and the power save function is disabled (M10=0). All blocks are locked after a Reset or Power-Down. Either Chip Enable or Write Enable must be tied to V_{IH} during Power-Up to allow maximum security and the possibility to write a command on the first rising edge of Write Enable.

Latch Enable ($\overline{L}$). Latch Enable latches the address bits A0-A20 on its rising edge. The address latch is transparent when L is at V_{IL} and it is inhibited when L is at V_{IH}.

Clock (K). The clock input synchronizes the memory to the microcontroller during burst mode read operation; the address is latched on a K edge (rising or falling, according to the configuration settings) when L is at V_{IL}. K is don't care during asynchronous page mode read and in write operations.

Wait ($\overline{WAIT}$). Wait is an output signal used during burst mode read, indicating whether the data on the output bus are valid or a wait state must be inserted. This output is high impedance when Chip Enable or Output Enable are at V_{IH} or Reset/Power-Down is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance.

V_{DD} Supply Voltage (1.65V to 2V). V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase). It ranges from 1.65V to 2.0V.

V_{DDQ} Supply Voltage (1.65V to 3.3V). V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or it can use a separate supply. It can be powered either from 1.65V to 2.0V or from 1.65V to 3.3V.

V_{PP} Program Supply Voltage (12V).

V_{PP} is a power supply pin. The Supply Voltage V_{DD} and the Program Supply Voltage V_{PP} can be applied in any order. The pin can also be used as a control input.

The two functions are selected by the voltage range applied to the pin. If V_{PP} is kept in a low voltage range (0V to 2V) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase,

while $V_{PP} > V_{PP1}$ enables these functions (see Table 19, DC Characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect on Program or Erase, however for Double or Quadruple Word Program the results are uncertain.

If V_{PP} is in the range 11.4V to 12.6V it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed (see Table 16 and 17). In read mode the current sunk is less then 0.5mA, while during program and erase operations the current may increase up to 10mA.

V_{SS} and V_{SSQ} Grounds. V_{SS} and V_{SSQ} grounds are the reference for the core supply and the input/output voltage measurements respectively.

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1µF capacitor close to the pin. See Figure 10, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required V_{PP} program and erase currents.

BUS OPERATIONS

There are two types of bus operations that control the device: Asynchronous (Read, Page Read, Write, Output Disable, Standby, Automatic Standby and Reset/Power-Down) and Synchronous (Synchronous Read and Synchronous Burst Read).

The Dual Bank architecture of the M58CR032 allows read/write operations in Bank A, while read operations are being executed in Bank B or vice versa. Write operations are only allowed in one bank at a time (see Table 7).

See Table 3, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Asynchronous Read. Asynchronous Read operations read from the Memory Array, or specific registers (Electronic Signature, Status Register, CFI, Block Protection Status, Read Configuration Register status and Protection Register) in the Command Interface.

A valid Asynchronous Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The address is latched on the rising edge of the Latch, $\overline{L}$, input. The Data Inputs/Outputs will output the value, see Figure 11, Asynchronous Read AC Waveforms, and Table 21, Asynchronous Read AC Characteristics, for details of when the output becomes valid.

According to the device configuration the following Read operations: Electronic Signature, Status Register, CFI, Block Protection Status, Burst Configuration Register Status and Protection Register must be accessed as asynchronous read or as single synchronous read.

Asynchronous Page Read. Asynchronous Page Read operations can be used to read the content of the memory array, where data is internally read and stored in a page buffer. The page has a size of 4 words and is addressed by A0 and A1 address inputs.

Valid bus operations are the same as Asynchronous Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. See Figure 12, Asynchronous Page Read AC Waveforms and Table 21, Asynchronous Read AC Characteristics for details on when the outputs become valid.

Asynchronous Page Read is the default state of the device when exiting power-down or after power-up.

Asynchronous Write. Bus Write operations are used to write to the Command Interface of the memory or latch Input Data to be programmed. A valid Bus Write operation begins by setting the desired address on the Address Inputs and setting Chip Enable, $\overline{E}$, and Write Enable, $\overline{W}$, to V_{IL} and Output Enable to V_{IH}. Addresses are latched on the rising edge of $\overline{L}$, $\overline{W}$ or $\overline{E}$ whichever occur first. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 14 and 15, Write AC Waveforms, and Tables 23 and 24, Write AC Characteristics, for details of the timing requirements.

Write operations are asynchronous and the clock is ignored during write.

Output Disable. The data outputs are high impedance when the Output Enable, $\overline{G}$, and Write Enable, $\overline{W}$, are High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, and the Program/Erase Controller is idle, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high impedance state, independent of Output Enable, $\overline{G}$, or Write Enable, $\overline{W}$. For the Standby current level see Table 19, DC Characteristics.

Reset/Power-Down. The memory is in Power-Down when the Burst Configuration Register is set for Power-Down and $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the Power-Down level, and Outputs are in high impedance, independent of Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$. The memory is in reset mode when the Burst Configuration Register is set for Reset and $\overline{RP}$ is at V_{IL}. The power consumption is the same of the standby and the outputs are in high impedance. After a Reset/Power-Down the device defaults to Asynchronous Page Read, the Status Register is cleared and the Burst configuration register defaults to Asynchronous Page read.

Automatic Standby. If CMOS levels ($V_{DD} \pm 0.2V$) are used to drive the bus and the bus is inactive for 150ns or more in Read mode, the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{DD2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress. The automatic standby feature is not available when the device is configured for synchronous burst mode.

Synchronous Single Read. Synchronous single Reads can be used to read the Electronic Signature, Status Register, CFI, Block Protection Status, Burst Configuration Register Status or

Protection Register, see Figure 6, for an example of a single synchronous read operation.

Synchronous Burst Read. The device also supports a synchronous burst read. In this mode a burst sequence is started at the first clock edge (rising or falling according to configuration settings) after the falling edge of Latch Enable. After a configurable delay of 2 to 5 clock cycles a new data is output at each clock cycle. The burst sequence may be configured to be sequential or interleaved and for a length of 4 or 8 words or for continuous burst mode (see Table 5, Burst Type Definition). Wrap and no-wrap modes are also supported.

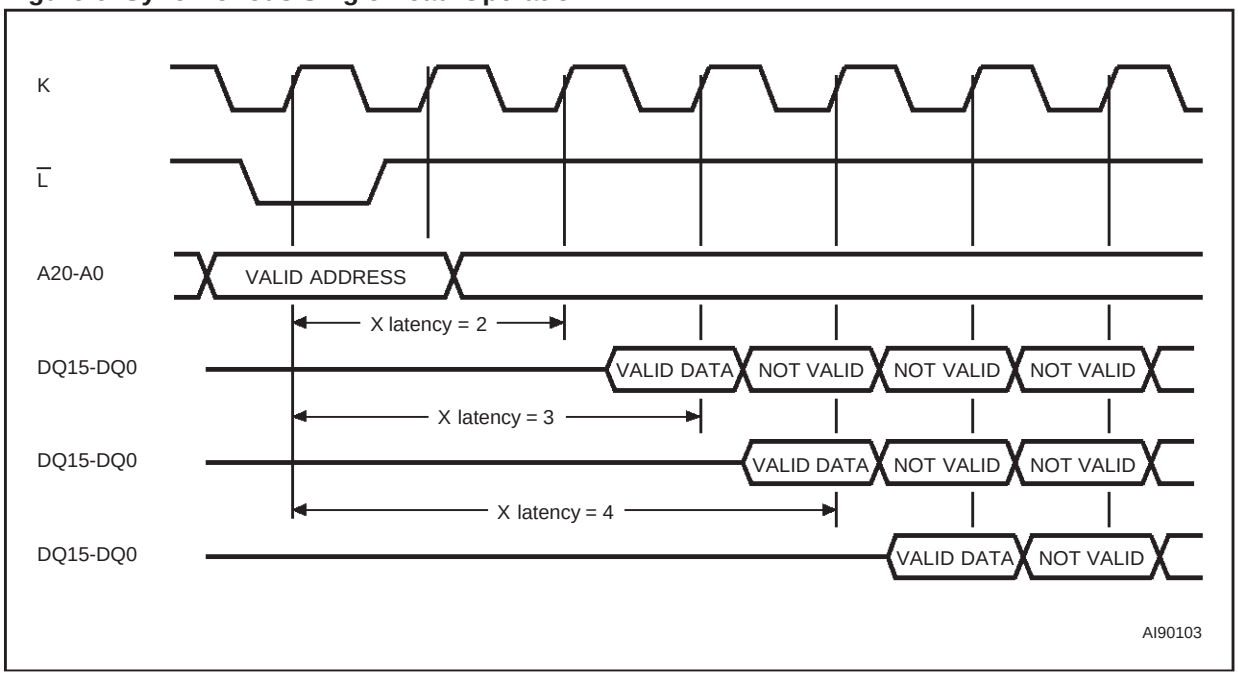
A $\overline{WAIT}$ signal may be asserted to indicate to the system that an output delay will occur. This delay will depend on the starting address of the burst sequence; the worst case delay will occur when the sequence is crossing a 64 word boundary and the starting address was at the end of a four word boundary. See the Burst Configuration Register command for more details on all the possible settings for the synchronous burst read (see Table 4). It is possible to perform burst read across bank boundaries (all banks in read array mode).

Table 3. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{L}$	K	$\overline{RP}$	$\overline{WP}$	DQ15-DQ0
Asynchronous Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	X	Data Output
Asynchronous Page Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	X	Data Output
Asynchronous Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	X	X	V_{IH}	X	Hi-Z
Reset / Power-Down	X	X	X	X	X	V_{IL}	X	Hi-Z
Synchronous Read	V_{IL}	V_{IL}	V_{IH}	T(2)	T(2)	V_{IH}	X	Data Output
Synchronous Burst Read	V_{IL}	V_{IL}	V_{IH}	T(2)	T(2)	V_{IH}	X	Data Output

Note: 1. X = Don't care.
2. T = transition, falling edge for $\overline{L}$, rising or falling edge for K depending on M6 in the Burst Configuration Register. The burst sequence is started on the first active clock edge after the falling edge of Latch Enable.

Figure 6. Synchronous Single Read Operation



Burst Configuration Register

The Burst Configuration Register is used to configure the type of bus access that the memory will perform.

The Burst Configuration Register is set through the Command Interface. After a Reset or Power-Up the device is configured for asynchronous page read (M15 = 1) and the power save function is disabled (M10 = 0). The Burst Configuration Register bits are described in Table 4. They specify the selection of the burst length, burst type, burst X latency and the Read operation. Refer to Figures 7 and 8 for examples of synchronous burst configurations.

Read Select Bit (M15). The Read Select bit, M15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to '1', Bus Read operations are asynchronous; when the Read Select but is set to '0', Bus Read operations are synchronous. Synchronous Burst Read is supported in both parameter and main blocks and can be performed across banks.

On reset or power-up the Read Select bit is set to'1' for asynchronous access.

X-Latency Bits (M13-M11). The X-Latency bits are used during Synchronous Bus Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in Table 4, Burst Configuration Register.

The correspondence between X-Latency settings and the maximum sustainable frequency must be calculated taking into account some system parameters.

Two conditions must be satisfied:

– $(n + 2)\ t_K \geq t_{ACC} + t_{AVK\_CPU} + t_{AVK\_CPU}$

– $t_K > t_{KQV} + t_{QVK\_CPU}$

where "n" is the chosen X-Latency configuration code, t_K is the clock period, t_{AVK_CPU} is the address setup time guaranteed by the system CPU, and t_{QVK_CPU} is the data setup time required by the system CPU.

Power-Down Bit (M10). The Power-Down bit is used to enable or disable the power-down function. When the Power-Down bit is set to '0' (default) the power-down function is disabled. When the Power-Down bit is set to '1' power-down is enabled and the device goes into the power-down state where the I_{DD} supply current is reduced to a typical figure of I_{DD2}.

if this function is disabled the Reset/Power-Down, $\overline{RP}$, pin causes only a reset of the device and the supply current is the standby value. The recovery time after a Reset/Power-Down, $\overline{RP}$, pulse is significantly longer when power-down is enabled (see Table 25).

Wait Bit (M8). In burst mode the Wait bit controls the timing of the Wait output pin, $\overline{WAIT}$. When the Wait bit is '0' the Wait output pin is asserted during the wait state. When the Wait bit is '1' (default) the Wait output pin is asserted one clock cycle before the wait state.

$\overline{WAIT}$ is asserted during a continuous burst and also during a 4 or 8 burst length if no-wrap configuration is selected. $\overline{WAIT}$ is not asserted during asynchronous reads, single synchronous reads or during latency in synchronous reads.

Burst Type Bit (M7). The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' (default) the memory outputs from sequential addresses. See Tables 5, Burst Type Definition, for the sequence of addresses output from a given starting address in each mode.

Valid Clock Edge Bit (M6). The Valid Clock Edge bit, M6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

Wrap Burst Bit (M3). The burst reads can be confined inside the 4 or 8 Double-Word boundary (wrap) or overcome the boundary (no wrap). The Wrap Burst bit is used to select between wrap and no wrap. When the Wrap Burst bit is set to '0' the burst read wraps; when it is set to '1' the burst read does not wrap.

Burst length Bits (M2-M0). The Burst Length bits set the number of Words to be output during a Synchronous Burst Read operation; 4 words, 8 words or continuous burst, where all the words are read sequentially.

In continuous burst mode the burst sequence can cross bank boundaries.

In continuous burst mode or in 4, 8 words no-wrap, depending on the starting address, the device activates the $\overline{WAIT}$ output to indicate that a delay is necessary before the data is output.

If the starting address is aligned to a 4 word boundary no wait states are needed and the $\overline{WAIT}$ output is not activated.

If the starting address is shifted by 1,2 or 3 positions from the four word boundary, $\overline{WAIT}$ will be asserted for 1, 2 or 3 clock cycles when the burst sequence crosses the first 64 word boundary, to indicate that the device needs an internal delay to read the successive words in the array. $\overline{WAIT}$ will

be asserted only once during a continuous burst access. See also Table 5, Burst Type Definition.

M14, M9, M5 and **M4** are reserved for future use.

Table 4. Burst Configuration Register

Bit	Description	Value	Description
M15	Read Select	0	Synchronous Burst Read
		1	Asynchronous Page Read (Default at power-on)
M14			Reserved
M13-M11	X-Latency (2)	010	2 clock latency
		011	3 clock latency
		100	4 clock latency
		101	5 clock latency
		111	Reserved
		Other configurations reserved	
M10	Power-Down (3)	0	Power-Down disabled
		1	Power-Down enabled
M9			Reserved
M8	Wait	0	$\overline{\text{WAIT}}$ is active during wait state
		1	$\overline{\text{WAIT}}$ is active one data cycle before wait state (default)
M7	Burst Type	0	Interleaved
		1	Sequential (default)
M6	Valid Clock Edge	0	Falling Burst Clock edge
		1	Rising Burst Clock edge
M5-M4			Reserved
M3	Wrapping	0	Wrap
		1	No wrap
M2-M0	Burst Length	001	4 words
		010	8 words
		111	Continuous (M7 must be set to ‘1’)

Table 5. Burst Type Definition

Mode	Start Address	4 Words		8 Words		Continuous Burst
		Sequential	Interleaved	Sequential	Interleaved	
Wrap	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6...
	1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7...
	2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8...
	3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9...
	...					
	7	7-4-5-6	7-6-5-4	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13...
	...					
	60					60-61-62-63-64-65-66...
	61					61-62-63-WAIT-64-65-66...
	62					62-63-WAIT-WAIT-64-65-66...
	63					63-WAIT-WAIT-WAIT-64-65-66...
		Sequential	**Interleaved**	**Sequential**	**Interleaved**	
No-wrap	0	0-1-2-3		0-1-2-3-4-5-6-7		0-1-2-3-4-5-6...
	1	1-2-3-4		1-2-3-4-5-6-7-8		1-2-3-4-5-6-7...
	2	2-3-4-5		2-3-4-5-6-7-8-9...		2-3-4-5-6-7-8...
	3	3-4-5-6		3-4-5-6-7-8-9-10		3-4-5-6-7-8-9...
	...					
	7	7-8-9-10		7-8-9-10-11-12-13-14		7-8-9-10-11-12-13...
	...					
	60	60-61-62-63		60-61-62-63-64-65-66-67		60-61-62-63-64-65-66...
	61	61-62-63-WAIT-64		61-62-63-WAIT-64-65-66-67-68		61-62-63-WAIT-64-65-66...
	62	62-63-WAIT-WAIT-64-65		62-63-WAIT-WAIT-64-65-66-67-68-69		62-63-WAIT-WAIT-64-65-66...
	63	63-WAIT-WAIT-WAIT-64-65-66		63-WAIT-WAIT-WAIT-64-65-66-67-68-69-70		63-WAIT-WAIT-WAIT-64-65-66...

Figure 7. X-Latency Configuration Sequence

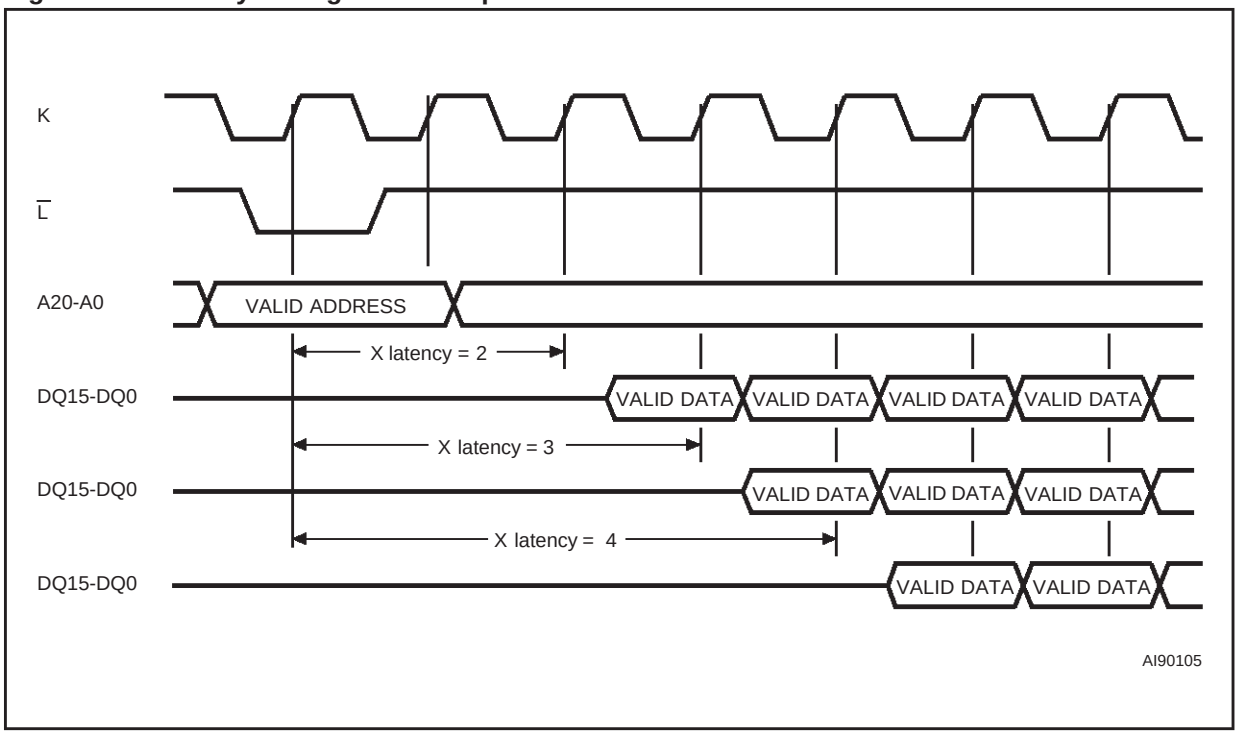
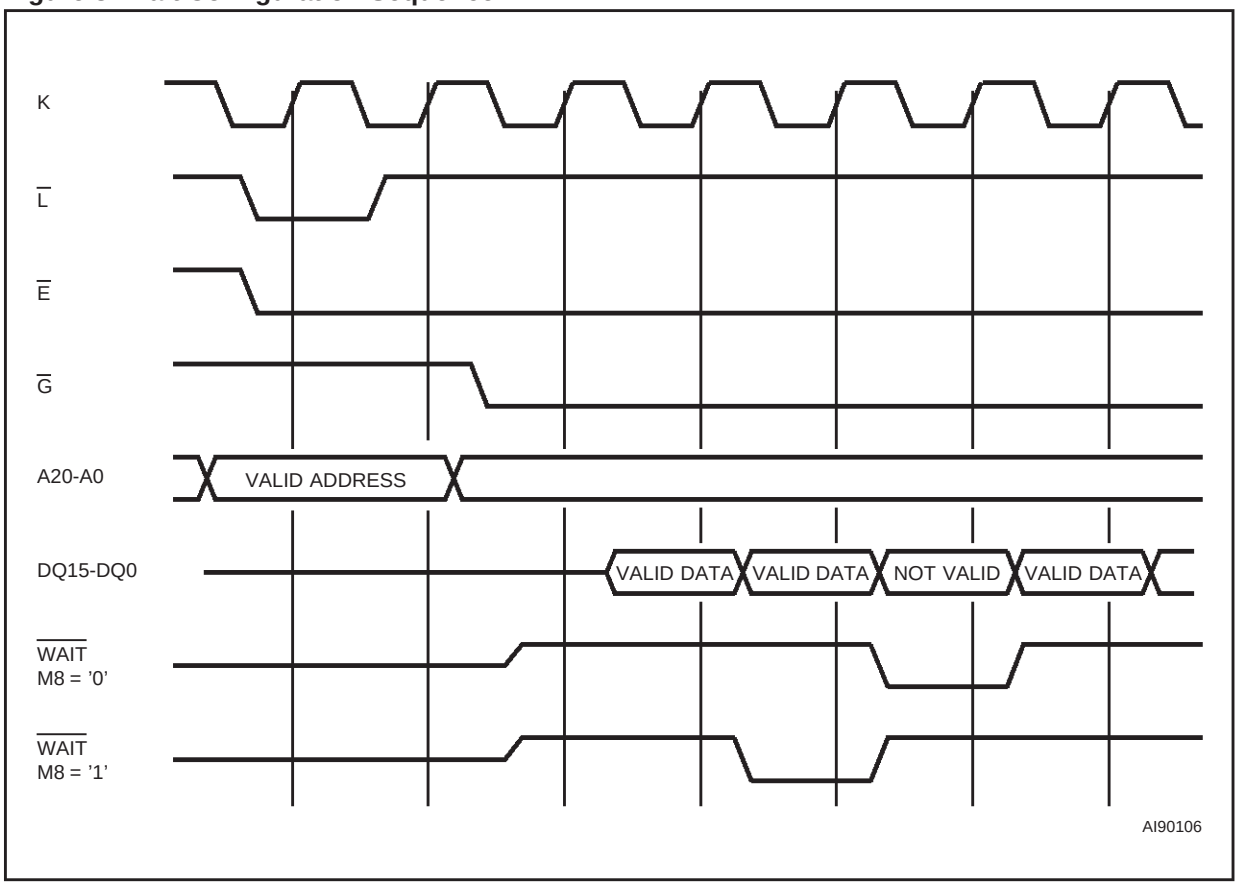


Figure 8. Wait Configuration Sequence



COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time during, to monitor the progress of the operation, or the Program/Erase states. See Appendix C, Tables 36 and 37, Command Interface States - Lock and Modify Tables, for a summary of the Command Interface.

The Command Interface is reset to Read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode. Refer to Table 6, Commands, in conjunction with the text descriptions below.

Read Command.

The Read command returns the addressed bank to Read mode. One Bus Write cycle is required to issue the Read command and return the addressed Bank to Read mode. Subsequent read operations will read the addressed location and output the data. A Read command can be issued in one bank while programming or erasing in the other bank. However if a Read command is issued to a bank currently executing a program or erase operation the command will be ignored.

When a device Reset occurs, the memory defaults to Read mode.

Read Status Register Command

A bank's Status Register indicates when a program or erase operation is complete and the success or failure of operation itself. Issue a Read Status Register command to read the Status Register content of the addressed bank. The status of the other bank is not affected by the command. The Read Status Register command can be issued at any time, even during program or erase operations.

The following Read operations output the content of the Status Register of the addressed bank. The Status Register is latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to V_{IH}. Either $\overline{E}$ or $\overline{G}$ must be toggled to update the latched data. See Table 15 for the description of the Status Register Bits. This mode supports asynchronous or single synchronous reads only.

Read Electronic Signature Command

The Read Electronic Signature command reads the Manufacturer and Device Codes and the Block Locking Status, or the Protection Register.

The Read Electronic Signature command consists of one write cycle to an address within the bottom bank. A subsequent read operation in the address of the bottom bank will output the Manufacturer Code, the Device Code, the protection Status of Blocks of the bottom bank, the Die Revision Code, the Protection Register, or the Read Configuration Register (see Table 11).

If the first write cycle of Read Electronic Signature command is issued to an address within the top bank, a subsequent read operation in an address of the top bank will output the protection Status of blocks of the top bank. The status of the other bank is not affected by the command (see Table 7). This mode supports asynchronous or single synchronous reads only.

See Tables 8, 9, 10 and 11 for the valid addresses.

Read CFI Query Command

The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) Memory Area, located in the bottom bank. One Bus Write cycle, addressed to the bottom bank, is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations in the bottom bank read from the Common Flash Interface Memory Area. The status of the top bank is not affected by the command (see Table 7). After issuing a Read CFI Query command, a Read command should be issued to return the bank to read mode.

See Appendix B, Common Flash Interface, Tables 29, 30, 31, 32, 33, 34 and 35 for details on the information contained in the Common Flash Interface memory area.

Clear Status Register Command

The Clear Status Register command can be used to reset (set to '0') bits 1, 3, 4 and 5 in the Status Register of the addressed bank'. One bus write cycle is required to issue the Clear Status Register command. After the Clear Status Register command the bank returns to read mode.

The bits in the Status Register do not automatically return to '0' when a new Program or Erase command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

Block Erase Command

The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error. It is not necessary to pre-program the block as the Pro-

gram/Erase Controller does it automatically before erasing.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.
- The second latches the block address in the internal state machine and starts the Program/ Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits b4 and b5 are set and the command aborts. Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

Once the command is issued the device outputs the Status Register data when any address within the bank is read. At the end of the operation the bank will remain in Read Status Register until a Read command is issued.

During Erase operations the bank containing the block being erased will only accept the Read Status Register command and the Program/Erase Suspend command, all other commands will be ignored. Typical Erase times are given in Table 12, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix B, Figure 22, Block Erase Flowchart and Pseudo Code, for a suggested flowchart for using the Block Erase command.

Bank Erase Command

The Bank Erase command can be used to erase a bank. It sets all the bits within the selected bank to '1'. All previous data in the bank is lost. The Bank Erase command will ignore any protected blocks within the bank. If the bank is protected then the Erase operation will abort, the data in the bank will not be changed and the Status Register will output the error.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Bank Erase command.
- The second latches the bank address in the internal state machine and starts the Program/ Erase Controller.

If the second bus cycle is not Write Bank Erase Confirm (D0h), Status Register bits b4 and b5 are set and the command aborts. Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the Erase operation is aborted, the bank must be erased again.

Once the command is issued the device outputs the Status Register data when any address within the bank is read. At the end of the operation the bank will remain in Read Status Register until a Read command is issued.

During Erase operations the bank being erased will only accept the Read Status Register command and the Program/Erase Suspend command, all other commands will be ignored. Typical Erase times are given in Table 12, Program, Erase Times and Program/Erase Endurance Cycles.

Program Command

The memory array can be programmed word-by-word. Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend. Two bus write cycles are required to issue the Program Command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

After programming has started, Read operations in the bank being programmed output the Status Register content.

During Program operations the bank being programmed will only accept the Read Status Register command and the Program/Erase Suspend command. Typical Program times are given in Table 12, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix B, Figure 18, Program Flowchart and Pseudo Code, for the flowchart for using the Program command.

Double Word Program Command

This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel. The two words must differ only for the address A0. Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend.

Programming should not be attempted when V_{PP} is not at V_{PPH}. The command can be executed if V_{PP} is below V_{PPH} but the result is not guaranteed.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations in the bank being programmed output the Status Register content after the programming has started.

During Double Word Program operations the bank being programmed will only accept the Read Status Register command and the Program/Erase Suspend command. Typical Program times are given in Table 12, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix B, Figure 19, Double Word Program Flowchart and Pseudo Code, for the flowchart for using the Double Word Program command.

Quadruple Word Program Command

This feature is offered to improve the programming throughput, writing a page of four adjacent words in parallel. The four words must differ only for the addresses A0 and A1. The first write cycle must be addressed to the bank to be programmed.

Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend.

Programming should not be attempted when V_{PP} is not at V_{PPH}. The command can be executed if V_{PP} is below V_{PPH} but the result is not guaranteed.

Five bus write cycles are necessary to issue the Quadruple Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written.
- The fourth bus cycle latches the Address and the Data of the third word to be written.
- The fifth bus cycle latches the Address and the Data of the fourth word to be written and starts the Program/Erase Controller.

Read operations to the bank being programmed output the Status Register content after the programming has started.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

During Quadruple Word Program operations the bank being programmed will only accept the Read Status Register command and the Program/Erase Suspend command. Typical Program times are given in Table 12, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix B, Figure 20, Quadruple Word Program Flowchart and Pseudo Code, for the flowchart for using the Quadruple Word Program command.

Program/Erase Suspend Command

The Program/Erase Suspend command is used to pause a Program or Erase operation. One bus write cycle is required to issue the Program/Erase command and pause the Program/Erase controller. The command must be addressed to the bank containing the program or erase operation.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read, Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Program, Block Lock, Block Lock-Down or Protection Program commands will also be accepted. The block being erased may be protected by issuing the Block Lock, Block Lock-Down or Protection Program commands. Only the blocks not being erased may be read or programmed correctly. When the Program/Erase Resume command is issued the operation will complete.

During a Program/Erase Suspend, the device can be placed in a pseudo-standby mode by taking Chip Enable to V_{IH}. Program/Erase is aborted if Reset turns to V_{IL}.

See Appendix B, Figure 21, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 23, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Suspend command.

Program/Erase Resume Command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend command has paused it. One Bus Write cycle is required to issue the command. The command must be addressed to the bank containing the program or erase operation. Once the command is issued subsequent Bus Read operations read the Status Register.

If a Program command is issued during a Block Erase Suspend, then the erase cannot be resumed until the programming operation has completed. It is possible to accumulate suspend operations. For example: suspend an erase operation, start a programming operation, suspend the programming operation then read the array. See Appendix B, Figure 21, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 23, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Resume command.

Protection Register Program Command

The Protection Register Program command is used to Program the 64 bit user One-Time-Programmable (OTP) segment of the Protection Register. The segment is programmed 16 bits at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The segment can be protected by programming bit 1 of the Protection Lock Register. Bit 1 of the Protection Lock Register protects bit 2 of the Protection Lock Register. Programming bit 2 of the Protection Lock Register will result in a permanent protection of the Security Block (see Figure 5, Security Block and Protection Register Memory Map). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register and/or the Security Block is not reversible.

The Protection Register Program cannot be suspended. See Appendix B, Figure 25, Protection Register Program Flowchart and Pseudo Code, for a flowchart for using the Protection Register Program command.

Block Lock Command

The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at power-up or reset.

Two Bus Write cycles are required to issue the Block Lock command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Table. 14 shows the Lock Status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until a hardware reset or power-down/power-up. They are cleared by a Blocks Unlock command. Refer to the section, Block Locking, for a detailed explanation. See Appendix B, Figure 24, Locking Operations Flowchart and Pseudo Code, for a flowchart for using the Lock command.

Block Unlock Command

The Blocks Unlock command is used to unlock a block, allowing the block to be programmed or erased. Two Bus Write cycles are required to issue the Blocks Unlock command.

- The first bus cycle sets up the Block Unlock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Table. 13 shows the protection status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation and Appendix B, Figure 24, Locking Operations Flowchart and Pseudo Code, for a flowchart for using the Unlock command.

Block Lock-Down Command

A locked block cannot be Programmed or Erased, or have its protection status changed when $\overline{WP}$ is low, V_{IL}. When $\overline{WP}$ is high, V_{IH}, the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Two Bus Write cycles are required to issue the Block Lock-Down command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Locked-Down blocks revert to the locked (and not locked-down) state when the device is reset on power-down. Table. 14 shows the Lock Status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation and Appendix B, Figure 24, Locking Operations Flowchart and Pseudo Code, for a flowchart for using the Lock-Down command.

Set Burst Configuration Register Command.

The Set Burst Configuration Register command is used to write a new value to the Burst Configuration Control Register which defines the burst length, type, X latency, Synchronous/Asynchronous Read mode and the valid Clock edge configuration.

Two Bus Write cycles are required to issue the Set Burst Configuration Register command. The first cycle writes the setup command and the address corresponding to the Set Burst Configuration Register content. The second cycle writes the Burst Configuration Register data and the confirm command. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Burst Configuration Register is always presented on A0-A15. M0 is on A0, M1 on A1, etc.; the other address bits are ignored.

Table 6. Commands

Commands	Cycles	Bus Write Operations														
		1st Cycle			2nd Cycle			3rd Cycle			4th Cycle			5th Cycle		
		Op.	Add	Data	Op.	Add	Data	Op.	Add	Data	Op.	Add	Data	Op.	Add	Data
Read Memory Array	1+	Write	BKA	FFh	Read	RA	RD									
Read Status Register	1+	Write	BKA	70h	Read	BKA	SRD									
Read Electronic Signature	1+	Write	ESA	90h	Read	ESA(2)	IDh									
Read CFI Query	1+	Write	QA	98h	Read	QA	QD									
Block Erase	2	Write	BA	20h	Write	BA	D0h									
Bank Erase	2	Write	BKA	80h	Write	BKA	D0h									
Program	2	Write	PA	40h or 10h	Write	PA	PD									
Double Word Program(3)	3	Write	PA1	30h	Write	PA1	PD1	Write	PA2	PD2						
Quadruple Word Program(4)	5	Write	PA1	55h	Write	PA1	PD1	Write	PA2	PD2	Write	PA3	PD3	Write	PA4	PD4
Clear Status Register	1	Write	BKA	50h												
Program/Erase Suspend	1	Write	BKA	B0h												
Program/Erase Resume	1	Write	BKA	D0h												
Block Lock	2	Write	BA	60h	Write	BA	01h									
Block Unlock	2	Write	BA	60h	Write	BA	D0h									
Block Lock-Down	2	Write	BA	60h	Write	BA	2Fh									
Protection Register Program	2	Write	PRA	C0h	Write	PRA	PRD									
Set Burst Configuration Register	2	Write	BCRA	60h	Write	BCRA	03h									

Note: 1. X = Don't Care, RA=Read Address, RD=Read Data, SRD=Status Register Data, ESA= Electronic Signature Address, ID=Identifier (Manufacture and Device Code), QA=Query Address, QD=Query Data, BA=Block Address, PA=Program Address, PD=Program Data, PRA=Protection Register Address, PRD=Protection Register Data, BCRA=Burst Configuration Register Address, BCRD=Burst Configuration Register Data.
2. The signature addresses are listed in Tables 8, 9 and 10.
3. Program Addresses 1 and 2 must be consecutive Addresses differing only for A0.
4. Program Addresses 1,2,3 and 4 must be consecutive Addresses differing only for A0 and A1.

Table 7. Dual Bank Operations

Status of one bank	Commands allowed in the other bank							
	Read Array	Read Status	Read CFI	Program	Erase/ Erase Resume	Program Suspend	Erase Suspend	Lock Unlock
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Reading	–	–	–	–	–	–	–	–
Programming	Yes	Yes	Yes	–	–	–	–	Yes
Erasing	Yes	Yes	Yes	–	–	–	–	Yes
Program Suspended	Yes	Yes	Yes	–	–	–	–	Yes
Erase Suspended	Yes	Yes	Yes	Yes	–	Yes	–	Yes

Note: 1. For detailed description of command see Table 6, 36 and 37.
2. There is a Status Register for each bank; Status Register indicates bank state, not P/E.C. status.
3. Command must be written to an address within the block targeted by that command.

Table 8. Read Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A1	A0	Other Addresses	DQ15-DQ0
Manufacturer Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	ESA (2)	0020h
Device Code	M58CR032C	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	ESA (2)	88C8h
	M58CR032D	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	ESA (2)	88C9h

Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. ESA means Electronic Signature Address (see Read Electronic Signature)

Table 9. Read Block Protection

Block Status	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	Other Address	DQ15-DQ0
Locked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	BA (3)	0001
Unlocked Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	BA (3)	0000
Locked and Locked-Down Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	BA (3)	0003
Unlocked and Locked-Down	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	BA (3)	0002

Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. A locked block can only be unlocked with $\overline{WP}$ at V_{IH}.
3. BA means Block Address. First cycle command address should indicate the bank of the block address.

Table 10. Read Protection Register

Word	$\overline{E}$	$\overline{G}$	$\overline{W}$	A20-16	A15-8	A7-0	DQ15-8	DQ7-3	DQ2	DQ1	DQ0
Lock	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	80h	00h	00000B	Security prot.data	OTP prot.data	0
Unique ID 0	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	81h	ID data	ID data	ID data	ID data	ID data
Unique ID 1	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	82h	ID data	ID data	ID data	ID data	ID data
Unique ID 2	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	83h	ID data	ID data	ID data	ID data	ID data
Unique ID 3	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	84h	ID data	ID data	ID data	ID data	ID data
OTP 0	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	85h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 1	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	86h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 2	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	87h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 3	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	88h	OTP data	OTP data	OTP data	OTP data	OTP data

Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. X = Don't care.

Table 11. Identifier Codes

Code		Address (h)	Data (h)
Manufacturer Code		Bank Address + 00	0020
Device Code	Top (M58CR032C)	Bank Address + 01	88C8
	Bottom (M58CR032D)		88C9
Block Protection	Lock	Bank Address + 02	0001
	Unlocked		0000
	Locked and Locked-Down		0003
	Unlocked and Locked-Down		0002
Die Revision Code		Bank Address + 03	DRC
Burst Configuration Register		Bank Address + 05	BCR
Lock Protection Register		Bank Address + 80	LPR
Protection Register		Bank Address + 81 Bank Address + 88	PR

Note: DRC=Die Revision Code, BCR=Burst Configuration Register, LPR= Lock Protection Register, PR=Protection Register (Unique Device Number and User Programmable OTP).

Table 12. Program, Erase Times and Program, Erase Endurance Cycles

	Parameter	Condition	Min	Typ	Typical after 100k W/E Cycles	Max	Unit
$V_{PP} = V_{DD}$	Parameter Block (4 KWord) Erase(2)			0.3	1	2.5	s
	Main Block (32 KWord) Erase	Preprogrammed		0.8	3	4	s
		Not Preprogrammed		1.1		4	s
	Bank A (8Mbit) Erase	Preprogrammed		5.5			s
		Not Preprogrammed		9			s
	Bank B (24Mbit) Erase	Preprogrammed		16.5			s
		Not Preprogrammed		27			s
	Parameter Block (4 KWord) Program(3)			40			ms
	Main Block (32 KWord) Program(3)			300			ms
	Word Program (3)			10	10	100	µs
	Program Suspend Latency			5		10	µs
	Erase Suspend Latency			5		20	µs
	Program/Erase Cycles (per Block)	Main Blocks	100,000				cycles
		Parameter Blocks	100,000				cycles
$V_{PP} = V_{PPH}$	Parameter Block (4 KWord) Erase			0.3		2.5	s
	Main Block (32 KWord) Erase			0.9		4	s
	Bank A (8Mbit) Erase			6.5			s
	Bank B (24Mbit) Erase			19.5			s
	4Mbit Program	Quadruple Word		510			ms
	Word/ Double Word/ Quadruple Word Program(3)			8		100	µs
	Parameter Block (4 KWord) Program(3)	Quadruple Word		8			ms
		Word		32			ms
	Main Block (32 KWord) Program(3)	Quadruple Word		64			ms
		Word		256			ms
	Program/Erase Cycles (per Block)	Main Blocks				1000	cycles
		Parameter Blocks				2500	cycles

Note: 1. T_A = –40 to 85°C; V_{DD} = 1.65V to 2V; V_{DDQ} = 1.65V to 3.3V.
2. The difference between Preprogrammed and not preprogrammed is not significant (‹30ms).
3. Excludes the time needed to execute the command sequence.

BLOCK LOCKING

The M58CR032 features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency. This locking scheme has three levels of protection.

- Lock/Unlock - this first level allows software-only control of block locking.
- Lock-Down - this second level requires hardware interaction before locking can be changed.
- $V_{PP} \leq V_{PPLK}$ - the third level offers a complete hardware protection against program and erase on all blocks.

For all devices the protection status of each block can be set to Locked, Unlocked, and Lock-Down. Table 14, defines all of the possible protection states ($\overline{WP}$, DQ1, DQ0), and Appendix B, Figure 24, shows a flowchart for the locking operations.

Reading a Block's Lock Status

The lock status of every block can be read in the Read Electronic Signature mode of the device. To enter this mode write 90h to the device. Subsequent reads at the address specified in Table 9, will output the protection status of that block. The lock status is represented by DQ0 and DQ1. DQ0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when entering Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a hardware reset or power-down.

The following sections explain the operation of the locking system.

Locked State

The default status of all blocks on power-up or after a hardware reset is Locked (states (0,0,1) or (1,0,1)). Locked blocks are fully protected from any program or erase. Any program or erase operations attempted on a locked block will return an error in the Status Register. The Status of a Locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be Locked by issuing the Lock command.

Unlocked State

Unlocked blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unlocked blocks return to the Locked state after a hardware reset or when the device is powered-down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A locked block can be unlocked by issuing the Unlock command.

Lock-Down State

Blocks that are Locked-Down (state (0,1,x))are protected from program and erase operations (as for Locked blocks) but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-Down by issuing the Lock-Down command. Locked-Down blocks revert to the Locked state when the device is reset or powered-down.

The Lock-Down function is dependent on the $\overline{WP}$ input pin. When $\overline{WP}$=0 (V_{IL}), the blocks in the Lock-Down state (0,1,x) are protected from program, erase and protection status changes. When $\overline{WP}$=1 (V_{IH}) the Lock-Down function is disabled (1,1,1) and Locked-Down blocks can be individually unlocked to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be re-locked (1,1,1) and unlocked (1,1,0) as desired while $\overline{WP}$ remains high. When $\overline{WP}$ is low , blocks that were previously Locked-Down return to the Lock-Down state (0,1,x) regardless of any changes made while $\overline{WP}$ was high. Device reset or power-down resets all blocks , including those in Lock-Down, to the Locked state.

Locking Operations During Erase Suspend

Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is locked or locked-down during an erase suspend of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete. Locking operations cannot be performed during a program suspend. Refer to Appendix C, Command Interface State Table, for detailed information on which commands are valid during erase suspend.

Table 13. Block Lock Status

Item	Address	Data
Block Lock Configuration	xx002	LOCK
Block is Unlocked		DQ0=0
Block is Locked		DQ0=1
Block is Locked-Down		DQ1=1

Table 14. Lock Status

Current Protection Status(1) (WP, DQ1, DQ0)		Next Protection Status(1) (WP, DQ1, DQ0)			
Current State	**Program/Erase Allowed**	**After Block Lock Command**	**After Block Unlock Command**	**After Block Lock-Down Command**	**After $\overline{WP}$ transition**
1,0,0	yes	1,0,1	1,0,0	1,1,1	0,0,0
1,0,1(2)	no	1,0,1	1,0,0	1,1,1	0,0,1
1,1,0	yes	1,1,1	1,1,0	1,1,1	0,1,1
1,1,1	no	1,1,1	1,1,0	1,1,1	0,1,1
0,0,0	yes	0,0,1	0,0,0	0,1,1	1,0,0
0,0,1(2)	no	0,0,1	0,0,0	0,1,1	1,0,1
0,1,1	no	0,1,1	0,1,1	0,1,1	1,1,1 or 1,1,0 (3)

Note: 1. The lock status is defined by the write protect pin and by DQ1 ('1' for a locked-down block) and DQ0 ('1' for a locked block) as read in the Read Electronic Signature command with A1 = V_{IH} and A0 = V_{IL}.
2. All blocks are locked at power-up, so the default configuration is 001 or 101 according to $\overline{WP}$ status.
3. A $\overline{WP}$ transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

STATUS REGISTER

The M58CR032 has two Status Registers, one for each bank. The Status Registers provide information on the current or previous Program or Erase operations executed in each bank. The various bits convey information and errors on the operation. Issue a Read Status Register command to read the Status Register content of the addressed bank, refer to Read Status Register Command section for more details. To output the contents, the Status Register is latched on the falling edge of the Chip Enable or Output Enable signals, and can be read until Chip Enable or Output Enable returns to V_{IH}. Either Chip Enable or Output Enable must be toggled to update the latched data.

Bus Read operations from any address within the bank, always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 15, Status Register Bits. Refer to Table 15 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive in the addressed bank. When the Program/Erase Controller Status bit is Low (set to '0'), the Program/Erase Controller is active; when the bit is High (set to '1'), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High .

During Program, Erase, operations the Program/Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Lock Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended or is going to be suspended in the addressed block. When the Erase Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 7 is set within 30µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. When the Erase Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program failure. When the Program Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3). The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low (set to '0'), the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is High (set to '1'), the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected and Program and Erase operations cannot be performed.

Once set High, the V_{PP} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended in the addressed block. When the Program Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has

been issued and the memory is waiting for a Program/Erase Resume command. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 2 is set within 5µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a locked block.

When the Block Protection Status bit is High (set to '1'), a Program or Erase operation has been attempted on a locked block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value must be masked.

Note: Refer to Appendix B, Flowcharts and Pseudo Codes, for using the Status Register.

Table 15. Status Register Bits

Bit	Name	Logic Level	Definition
7	P/E.C. Status	'1'	Ready
		'0'	Busy
6	Erase Suspend Status	'1'	Suspended
		'0'	In progress or Completed
5	Erase Status	'1'	Erase Error
		'0'	Erase Success
4	Program Status	'1'	Program Error
		'0'	Program Success
3	V_{PP} Status	'1'	V_{PP} Invalid, Abort
		'0'	V_{PP} OK
2	Program Suspend Status	'1'	Suspended
		'0'	In Progress or Completed
1	Block Protection Status	'1'	Program/Erase on protected Block, Abort
		'0'	No operation to protected blocks
0	Reserved		

Note: Logic level '1' is High, '0' is Low.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 155	°C
V_{IO} (1)	Input or Output Voltage	–0.5 to V_{DDQ}+0.5	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.5 to 2.7	V
V_{PP}	Program Voltage	–0.5 to 13	V

Note: 1. Minimum Voltage may undershoot to –2V during transition and for less than 20ns during transitions.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 17, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 17. Operating and AC Measurement Conditions

Parameter	M58CR032C, M58CR032D						Units
	85		100		120		
	Min	Max	Min	Max	Min	Max	
V_{DD} Supply Voltage	1.65	2.0	1.65	2.0	1.65	2.0	V
V_{DDQ} Supply Voltage	1.65	3.3	1.65	3.3	1.65	3.3	V
Ambient Operating Temperature	– 40	85	– 40	85	– 40	85	°C
Load Capacitance (C_L)	30		30		30		pF
Input Rise and Fall Times		4		4		4	ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDQ}/2$		$V_{DDQ}/2$		V

Figure 9. AC Measurement I/O Waveform

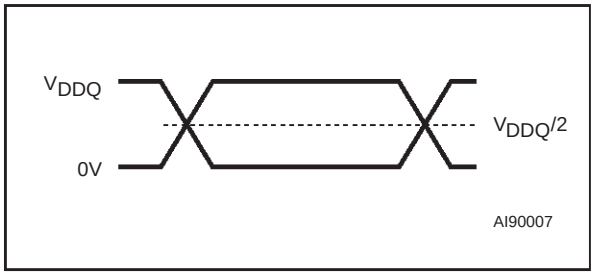


Figure 10. AC Measurement Load Circuit

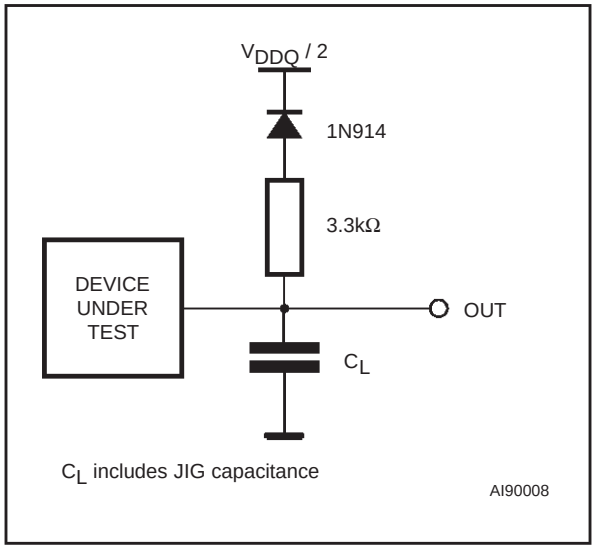


Table 18. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 19. DC Characteristics - Currents

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=6MHz)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		3	6	mA
	Supply Current Synchronous Read (f=40MHz)	4 Word		6	13	mA
		8 Word		8	14	mA
		Continuous		6	10	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		2	10	µA
I_{DD3}	Supply Current (Standby)	$\overline{E} = V_{DD} \pm 0.2V$		10	50	µA
I_{DD4} (1)	Supply Current (Program)	$V_{PP} = V_{PPH}$		8	15	mA
		$V_{PP} = V_{DD}$		10	20	mA
	Supply Current (Erase)	$V_{PP} = V_{PPH}$		8	15	mA
		$V_{PP} = V_{DD}$		10	20	mA
I_{DD5} (1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		13	26	mA
		Program/Erase in one Bank, Synchronous Read in another Bank		16	30	mA
I_{DD6}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E} = V_{DD} \pm 0.2V$		10	50	µA
I_{PP1}(1)	V_{PP} Supply Current (Program)	$V_{PP} = V_{PPH}$		2	5	mA
		$V_{PP} = V_{DD}$		0.2	5	µA
	V_{PP} Supply Current (Erase)	$V_{PP} = V_{PPH}$		2	5	mA
		$V_{PP} = V_{DD}$		0.2	5	µA
I_{PP2}	V_{PP} Supply Current (Read)	$V_{PP} = V_{PPH}$		100	400	µA
		$V_{PP} \le V_{DD}$		0.2	5	µA
I_{PP3}(1)	V_{PP} Supply Current (Standby)	$V_{PP} \le V_{DD}$		0.2	5	µA

Note: 1. Sampled only, not 100% tested.
2. V_{DD} Dual Operation current is the sum of read and program or erase currents.

Table 20. DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PP} Program Voltage-Logic	Program, Erase	1	1.8	1.95	V
V_{PPH}	V_{PP} Program Voltage Factory	Program, Erase	11.4	12	12.6	V
V_{PPLK}	Program or Erase Lockout				0.9	V
V_{LKO}	V_{DD} Lock Voltage		1			V
V_{RPH}	$\overline{RP}$ pin Extended High Voltage				3.3	V

Figure 11. Asynchronous Read AC Waveforms

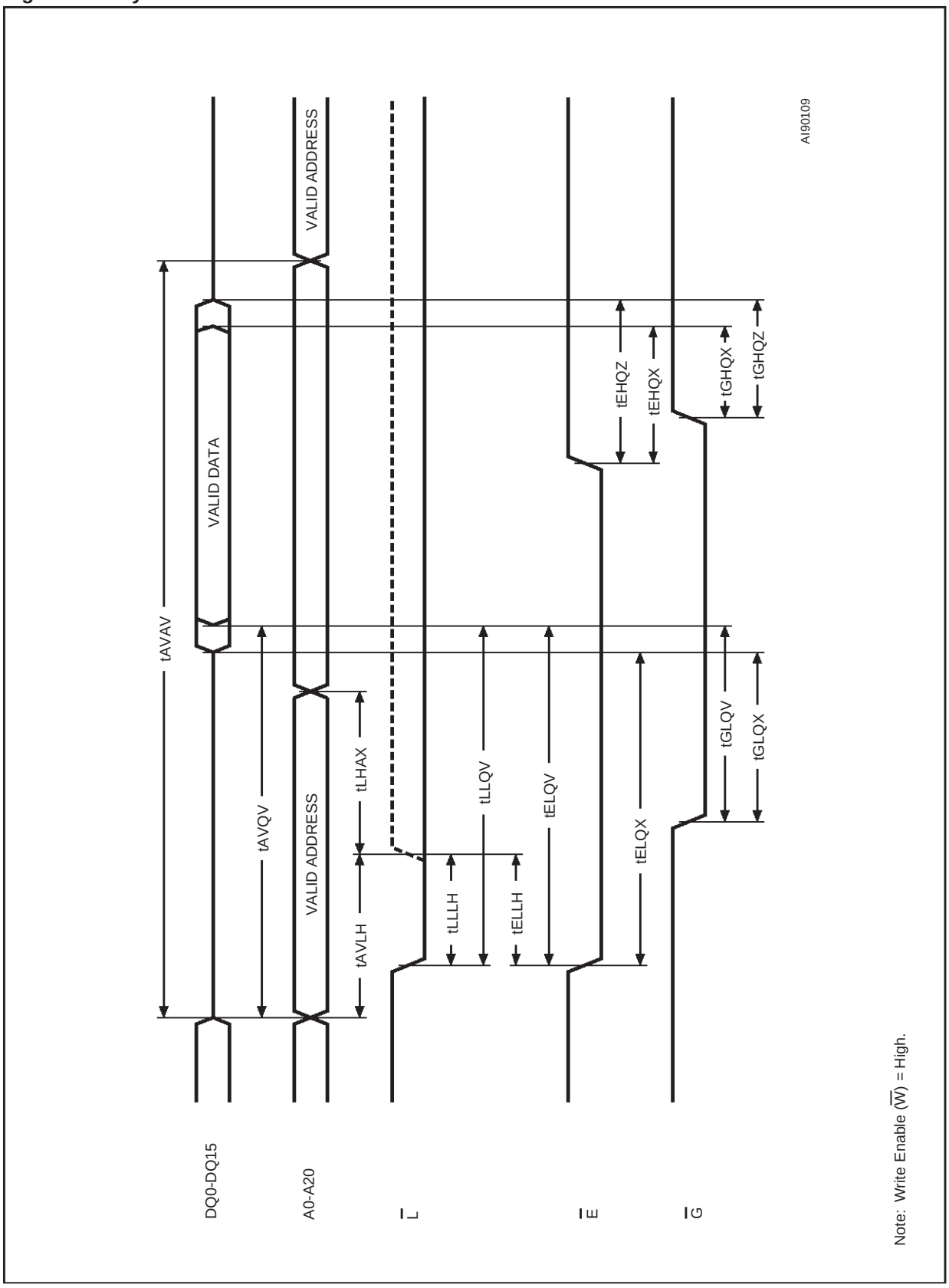


Figure 12. Asynchronous Page Read AC Waveforms

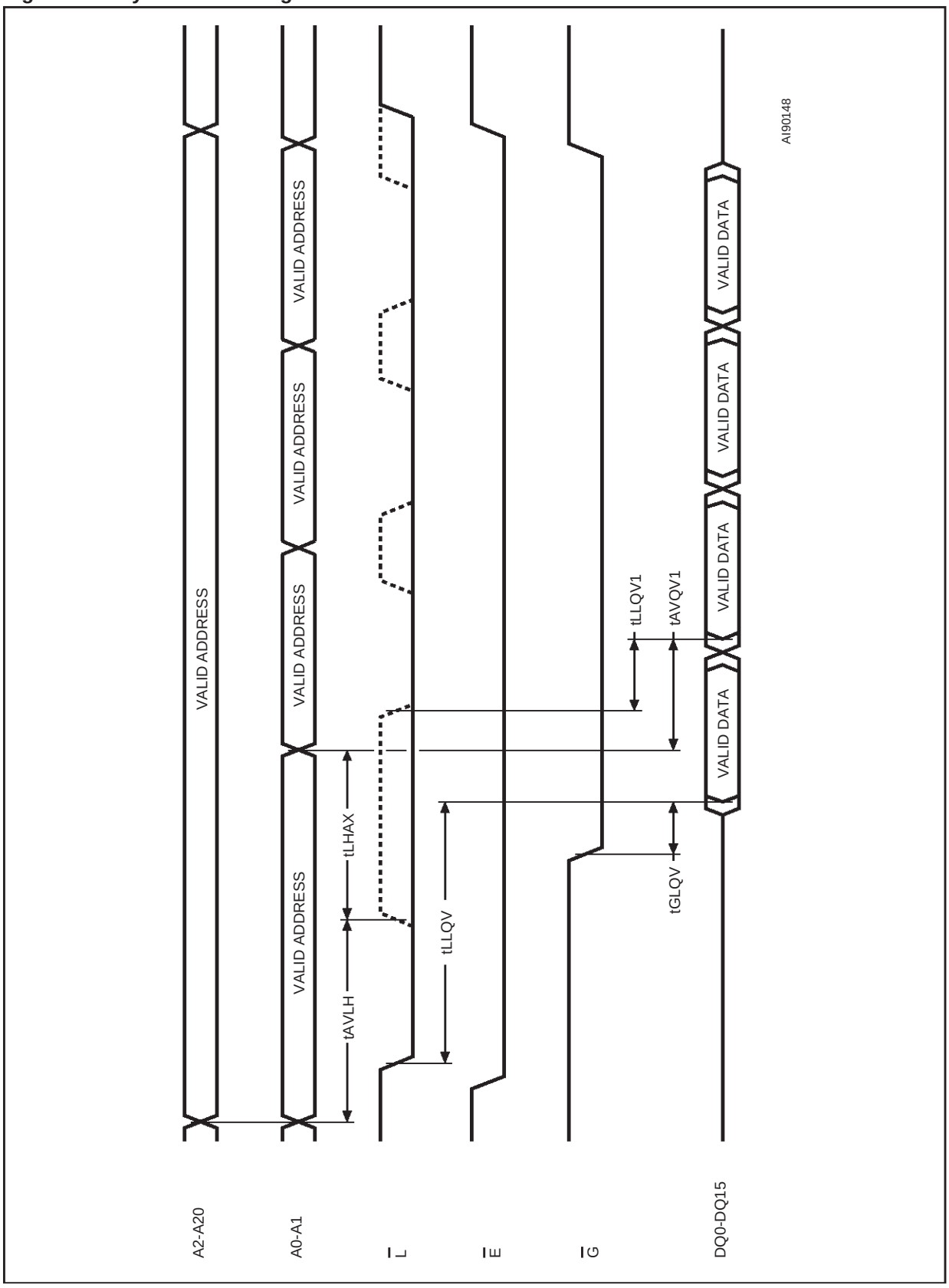
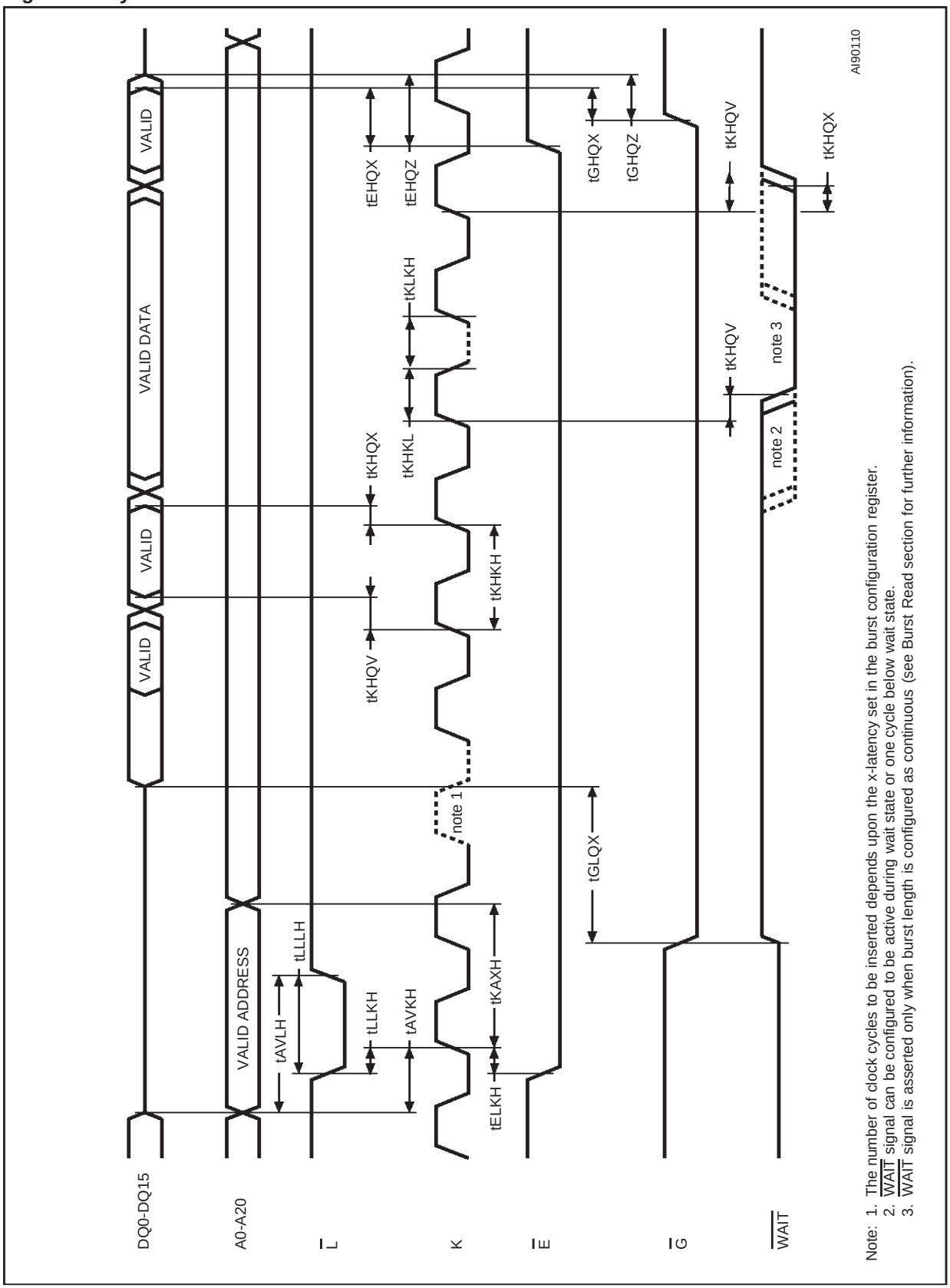


Table 21. Asynchronous Read AC Characteristics

Symbol	Alt	Parameter	Test Condition	M58CR032						Unit
				85		100		120		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	85		100		120		ns
t_{AVLH}	t_{AVAVDH}	Address valid to Latch Enable High	$\overline{G} = V_{IH}$	10		10		10		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		85		100		120	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		35		45		45	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$		20		20		20	ns
t_{ELLH}	t_{ELAVDH}	Chip Enable Low to Latch Enable High	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	10		10		10		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		85		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		0		ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$		20		20		20	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		25		25		35	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		0		0		ns
t_{LHAX}	t_{AVDHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	10		10		10		ns
t_{LLLH}	$t_{AVDLAVDH}$	Latch Enable Pulse Width	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	10		10		10		ns
t_{LLQV}	t_{AVDLQV}	Latch Enable Low to Output Valid (Random)	$\overline{E} = V_{IL}$		85		100		120	ns
t_{LLQV1}		Latch Enable Low to Output Valid (Page)	$\overline{E} = V_{IL}$		35		45		45	ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 13. Synchronous Burst Read



Note: 1. The number of clock cycles to be inserted depends upon the x-latency set in the burst configuration register.
2. WAIT signal can be configured to be active during wait state or one cycle below wait state.
3. WAIT signal is asserted only when burst length is configured as continuous (see Burst Read section for further information).

Table 22. Synchronous Burst Read AC Characteristics

Symbol	Alt	Parameter	Test Condition	M58CR032						Unit
				85		100		120		
				Min	Max	Min	Max	Min	Max	
t_{AVKH}	t_{AVCLKH}	Address Valid to Clock High		7		7		7		ns
t_{ELKH}	$t_{CELCLKH}$	Chip Enable Low to Clock High		7		7		7		ns
t_{KHKH}	t_{CLK}	Clock Period		18		18		25		ns
t_{KHAX}	t_{CLKHAX}	Clock High to Address Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	10		10		10		ns
t_{KHKL}	$t_{CLKHCLKL}$	Clock High to Clock Low		5		5		5		ns
t_{KLKH}	$t_{CLKLCLKH}$	Clock Low to Clock High		5		5		5		ns
t_{KHQV}	t_{CLKHQV}	Clock to Data Valid Clock to WAIT Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		14		14		18	ns
t_{KHQX}	t_{CLKHQX}	Clock to Output Transition Clock to WAIT Transition	$\overline{E} = V_{IL}$	4		4		4		ns
t_{LLKH}	$t_{AVDLCLKH}$	Latch Enable Low to Clock High		7		7		7		ns

Note: For other timings please refer to Table 21, Asynchronous Read AC Characteristics

Figure 14. Write AC Waveforms, Write Enable Controlled

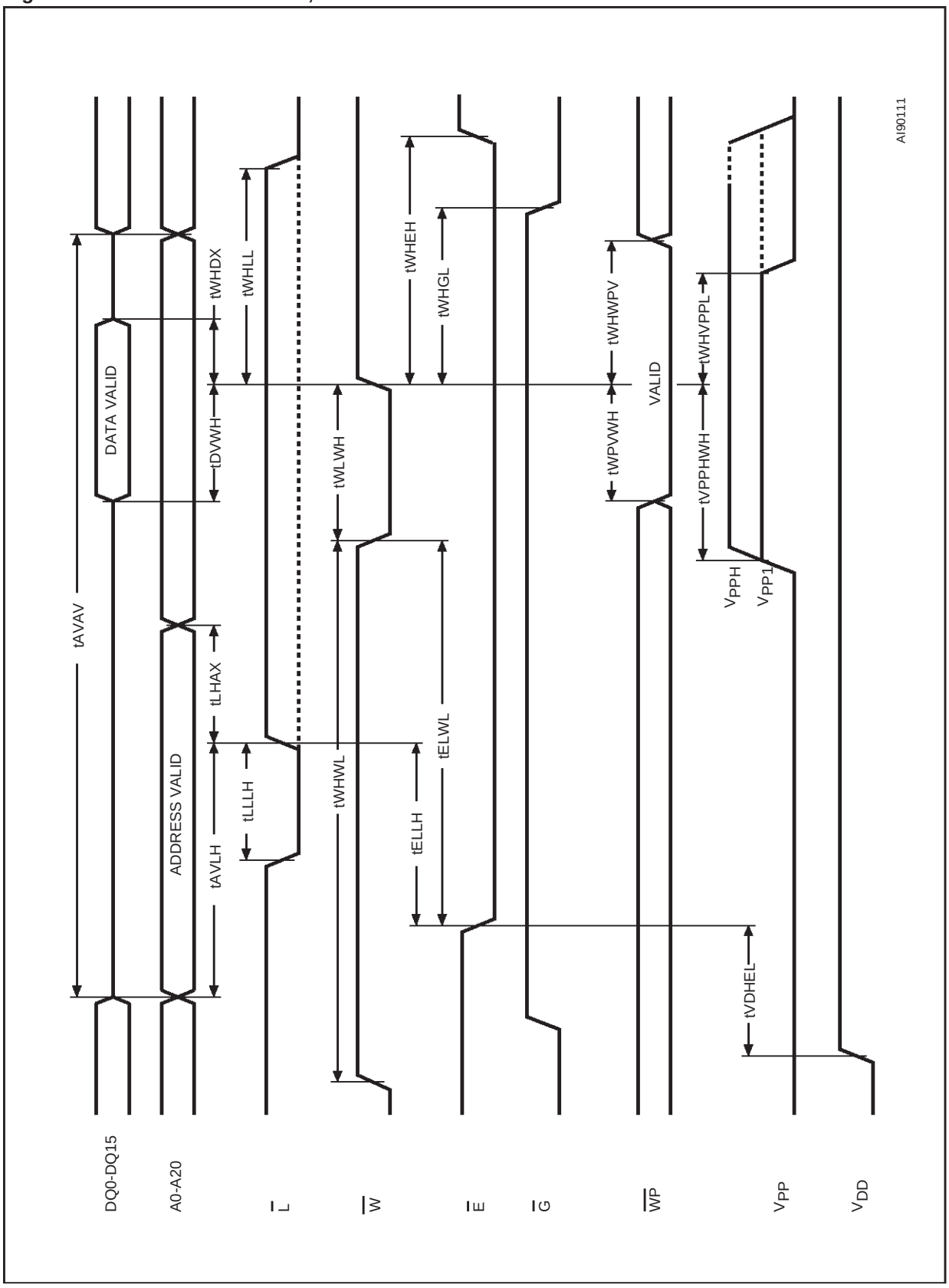


Table 23. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter	M58CR032						Unit
			85		100		120		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	85		100		120		ns
t_{AVLH}		Address Valid to Latch Enable High	10		10		10		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		40		ns
t_{ELLH}		Chip Enable Low to Latch Enable High	10		10		10		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{LHAX}		Latch Enable High to Address Transition	10		10		10		ns
t_{LLLH}		Latch Enable Pulse Width	10		10		10		ns
t_{VDHEL}	t_{VCS}	V_{DD} High to Chip Enable Low	50		50		50		µs
t_{VPPHWH}		V_{PP} High to Write Enable High	200		200		200		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		0		ns
t_{WHLL}		Write Enable High to Latch Enable Low	0		0		0		ns
t_{WHVPPL}		Write Enable High to V_{PP} Low	200		200		200		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		30		ns
t_{WHWPV}		Write Enable High to Write Protect Valid	200		200		200		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		50		ns
t_{WPVWH}		Write Protect Valid to Write Enable High	200		200		200		ns

Figure 15. Write AC Waveforms, Chip Enable Controlled

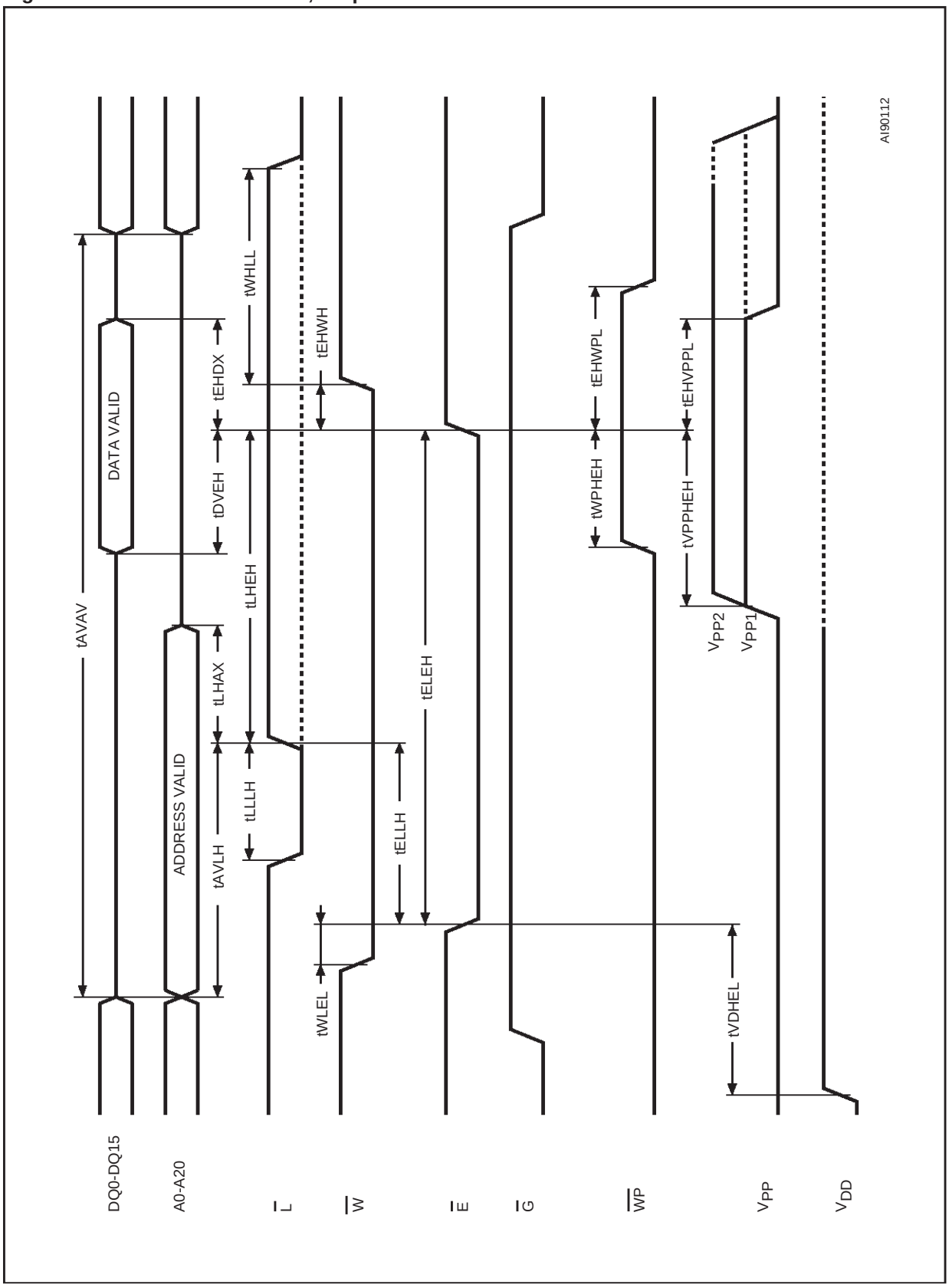


Table 24. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter	M58CR032						Unit
			85		100		120		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	85		100		120		ns
t_{AVLH}		Address Valid to Latch Enable High	10		10		10		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40		40		40		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		30		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	60		60		60		ns
t_{ELLH}		Chip Enable Low to Latch Enable High	10		10		10		ns
t_{LHAX}		Latch Enable High to Address Transition	10		10		10		ns
t_{LHEH}		Latch Enable High to Chip Enable High	10		10		10		ns
t_{LLLH}		Latch Enable Pulse Width	10		10		10		ns
t_{VDHEL}	t_{VCS}	V_{DD} High to Chip Enable Low	50		50		50		µs
t_{VPPHEH}		V_{PP} High to Chip Enable High	200		200		200		ns
t_{EHVPPL}		Chip Enable High to V_{PP} Low	200		200		200		ns
t_{EHWPL}		Chip Enable High to Write Protect Low	200		200		200		ns
t_{WLEL}	t_{WS}	Chip Enable Low to Chip Enable Low	0		0		0		ns
t_{WPHEH}		Write Protect High to Chip Enable High	200		200		200		ns

Figure 16. Reset and Power-up AC Waveforms

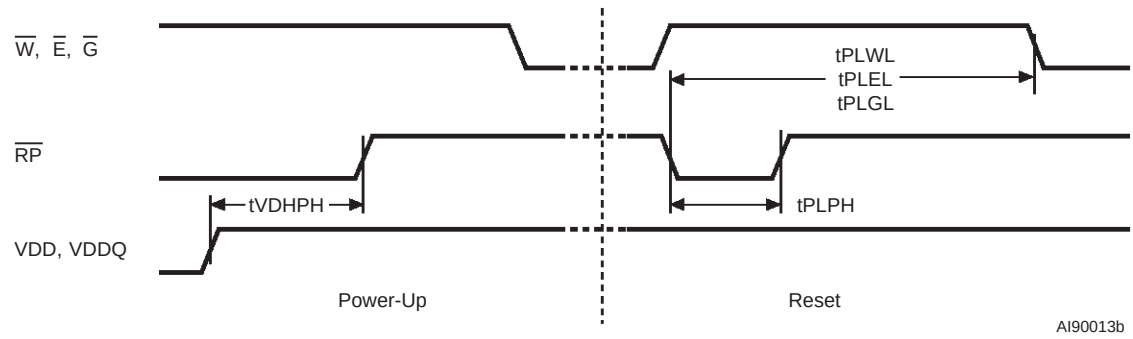


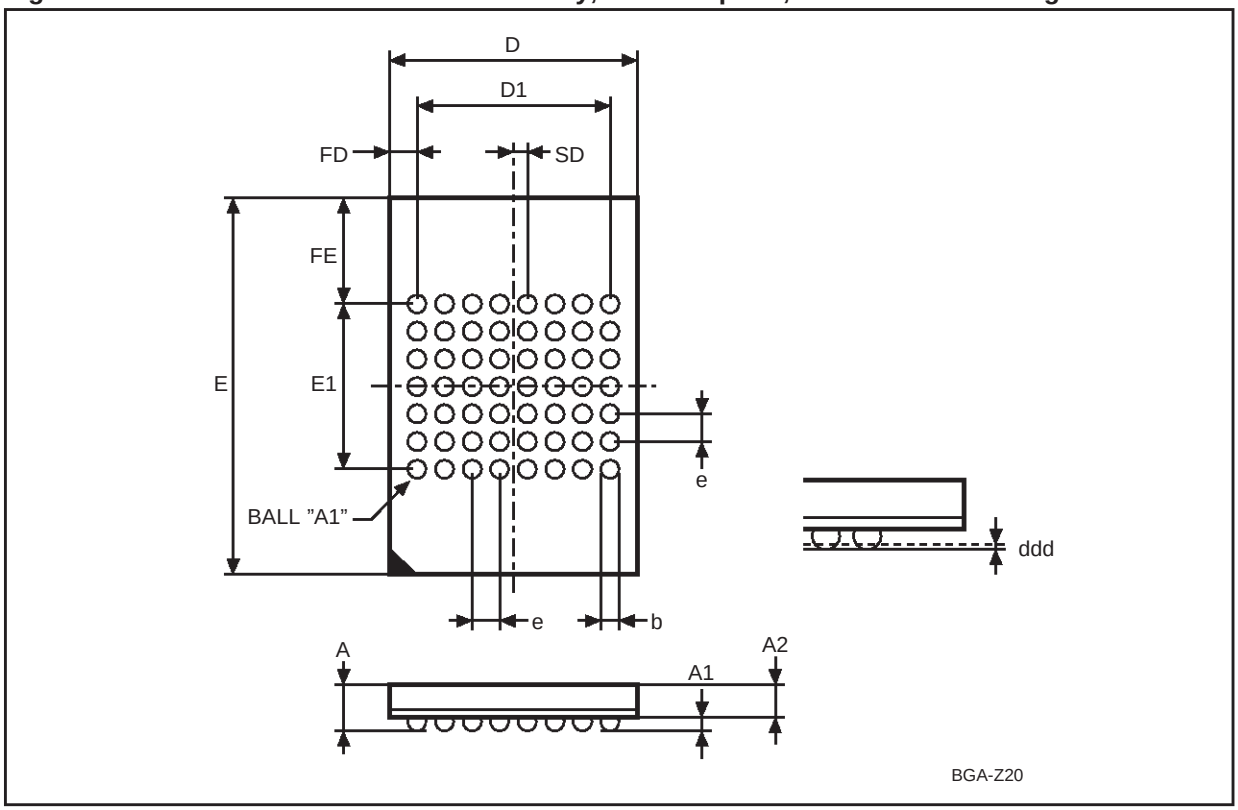
Table 25. Reset and Power-up AC Characteristics

Symbol	Parameter	Test Condition	Min	Unit
t_{PLPH} (1,2)	$\overline{RP}$ Pulse Width		50	ns
t_{PLWL} t_{PLEL} t_{PLGL}	Reset Low to Device Enabled	During Program and Erase	10/20	µs
		Other Conditions	80	ns
t_{VDHPH} (3)	Supply Valid to Reset High		50	µs

Note: 1. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
2. Sampled only, not 100% tested.
3. It is important to assert $\overline{RP}$ in order to allow proper CPU initialization during Power-up or System reset.

PACKAGE MECHANICAL

Figure 17. TFBGA56 6.5x10mm - 8x7 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 26. TFBGA56 6.5x10mm - 8x7 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.010	1.200		0.0398	0.0472
A1		0.250	0.400		0.0098	0.0157
A2	0.790			0.0311		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	6.500	6.400	6.600	0.2559	0.2520	0.2598
D1	5.250	–	–	0.2067	–	–
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	4.500	–	–	0.1772	–	–
e	0.750	–	–	0.0295	–	–
FD	0.625	–	–	0.0246	–	–
FE	2.750	–	–	0.1083	–	–
SD	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 27. Ordering Information Scheme

Example: M58CR032C 85 ZB 6 T

Device Type
M58

Architecture
C = Dual Bank, Burst Mode

Operating Voltage
R = V_{DD} = 1.65V to 2.0V, V_{DDQ} = 1.65V to 3.3V

Device Function
032C = 32 Mbit (x16), Dual Bank: 1/4-3/4 partitioning, Top Boot
032D = 32 Mbit (x16), Dual Bank: 1/4-3/4 partitioning, Bottom Boot

Speed
85 = 85 ns
100 = 100 ns
120 = 120 ns

Package
ZB = TFBGA56: 0.75 mm pitch

Temperature Range
6 = –40 to 85°C

Option
T = Tape & Reel packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc....) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 28. Document Revision History

Date	Version	Revision Details
April 2001	-01	First Issue
23-OCT-2001	-02	85ns speed class added, document classified as Preliminary Data
21-Mar-2002	-03	Document completely revised. Changes in CFI content, Program and Erase Times Table and DC Characteristics Table

APPENDIX A. COMMON FLASH INTERFACE

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 29, 30, 31, 32, 33, 34 and 35 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 35, Security Code area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read command to return to Read mode.

Table 29. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)
80h	Security Code Area	Lock Protection Register Unique device Number and User Programmable OTP

Note: The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in Tables 30, 31, 32, 33, 34 and 35. Query data are always presented on the lowest order data outputs.

Table 30. CFI Query Identification String

Offset	Sub-section Name	Description	Value
00h	0020h	Manufacturer Code	ST
01h	88C8h 88C9h	Device Code (M58CR032C/D)	Top Bottom
02h	reserved	Reserved	
03h	reserved	Reserved	
04h-0Fh	reserved	Reserved	
10h	0051h	Query Unique ASCII String "QRY"	"Q"
11h	0052h		"R"
12h	0059h		"Y"
13h	0003h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	
14h	0000h		
15h	offset = P = 0039h	Address for Primary Algorithm extended Query table (see Table 32)	p = 39h
16h	0000h		
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
18h	0000h		
19h	value = A = 0000h	Address for Alternate Algorithm extended Query table	NA
1Ah	0000h		

Note: Query data are always presented on the lowest - order data outputs (ADQ0-ADQ7) only. ADQ8-ADQ15 are '0'.

Table 31. CFI Query System Interface Information

Offset	Data	Description	Value
1Bh	0017h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts	1.7V
1Ch	0020h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts	2V
1Dh	0017h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts	1.7V
1Eh	00C0h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts	12V
1Fh	0004h	Typical time-out per single byte/word program = 2^n µs	16µs
20h	0003h	Typical time-out for quadruple word program = 2^n µs	8µs
21h	000Ah	Typical time-out per individual block erase = 2^n ms	1s
22h	0000h	Typical time-out for full chip erase = 2^n ms	NA
23h	0003h	Maximum time-out for word program = 2^n times typical	128µs
24h	0004h	Maximum time-out for quadruple word = 2^n times typical	128µs
25h	0002h	Maximum time-out per individual block erase = 2^n times typical	4s
26h	0000h	Maximum time-out for chip erase = 2^n times typical	NA

Table 32. Device Geometry Definition

Offset Word Mode	Data	Description	Value
27h	0016h	Device Size = 2^n in number of bytes	4 MByte
28h 29h	0001h 0000h	Flash Device Interface Code description	x16 Async.
2Ah 2Bh	0003h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	8 Byte
2Ch	0002h	Number of Erase Block Regions within the device bit 7 to 0 = x = number of Erase Block Regions It specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size.	2

Offset Word Mode		Data	Description	Value
M58CR032C	2Dh 2Eh	003Eh 0000h	Region 1 Information Number of identical-size erase block = 007Eh+1	63
	2Fh 30h	0000h 0001h	Region 1 Information Block size in Region 1 = 0100h * 256 byte	64 KByte
	31h 32h	0007h 0000h	Region 2 Information Number of identical-size erase block = 000Eh+1	8
	33h 34h	0020h 0000h	Region 2 Information Block size in Region 2 = 0020h * 256 byte	8 KByte
	35h 38h	0000h	Reserved for future raise block region information	NA
M58CR032D	2Dh 2Eh	0007h 0000h	Region 1 Information Number of identical-size erase block = 0007h+1	8
	2Fh 30h	0020h 0000h	Region 1 Information Block size in Region 1 = 0020h * 256 byte	8 KByte
	31h 32h	003Eh 0000h	Region 2 Information Number of identical-size erase block = 007Eh+1	63
	33h 34h	0000h 0001h	Region 2 Information Block size in Region 2 = 0100h * 256 byte	64 KByte
	35h 38h	0000h	Reserved for future raise block region information	NA

Table 33. Primary Algorithm-Specific Extended Query Table

Offset	Data	Description	Value
(P)h = 39h	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”	”P”
	0052h		”R”
	0049h		”I”
(P+3)h = 3Ch	0031h	Major version number, ASCII	”1”
(P+4)h = 3Dh	0030h	Minor version number, ASCII	”0”
(P+5)h = 3Eh	00E6h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte.	
	0003h		
(P+7)h	0000h	bit 0 Chip Erase supported (1 = Yes, 0 = No)	No
		bit 1 Erase Suspend supported (1 = Yes, 0 = No)	Yes
(P+8)h	0000h	bit 2 Program Suspend supported (1 = Yes, 0 = No)	Yes
		bit 3 Legacy Lock/Unlock supported (1 = Yes, 0 = No)	No
		bit 4 Queued Erase supported (1 = Yes, 0 = No)	No
		bit 5 Instant individual block locking supported (1 = Yes, 0 = No)	Yes
		bit 6 Protection bits supported (1 = Yes, 0 = No)	Yes
		bit 7 Page mode read supported (1 = Yes, 0 = No)	Yes
		bit 8 Synchronous read supported (1 = Yes, 0 = No)	Yes
		bit 9 Simultaneous operation supported (1 = Yes, 0 = No)	Yes
		bit 10 to 31 Reserved; undefined bits are ‘0’. If bit 31 is ’1’ then another 31 bit field of optional features follows at the end of the bit-30 field.	

Offset	Data	Description	Value
(P+9)h = 42h	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No) bit 7 to 1 Reserved; undefined bits are '0'	Yes
(P+A)h = 43h (P+B)h	0003h 0000h	Block Protect Status Defines which bits in the Block Status Register section of the Query are implemented. bit 0 Block protect Status Register Lock/Unlock bit active (1 = Yes, 0 = No) bit 1 Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No) bit 15 to 2 Reserved for future use; undefined bits are '0'	 Yes Yes
(P+C)h = 45h	0018h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	1.8V
(P+D)h = 46h	00C0h	V_{PP} Supply Optimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12V
(P+E)h = 47h (P+F)h (P+10)h (P+11)h (P+12)h	0000h	Reserved	

Table 34. Burst Read Information

Offset	Data	Description	Value
(P+13)h = 4Ch	0003h	Page-mode read capability bits 0-7 'n' such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width.	8 Byte
(P+14)h = 4Dh	0003h	Number of synchronous mode read configuration fields that follow.	3
(P+15)h = 4Eh	0001h	Synchronous mode read capability configuration 1 bit 3-7 Reserved bit 0-2 'n' such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bit 0-2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	4
(P+16)h = 4Fh	0002h	Synchronous mode read capability configuration 2	8
(P+17)h = 50h	0007h	Synchronous mode read capability configuration 3	Cont.
(P+18)h = 51h	0036h	Max operating clock frequency (MHz)	54 MHz

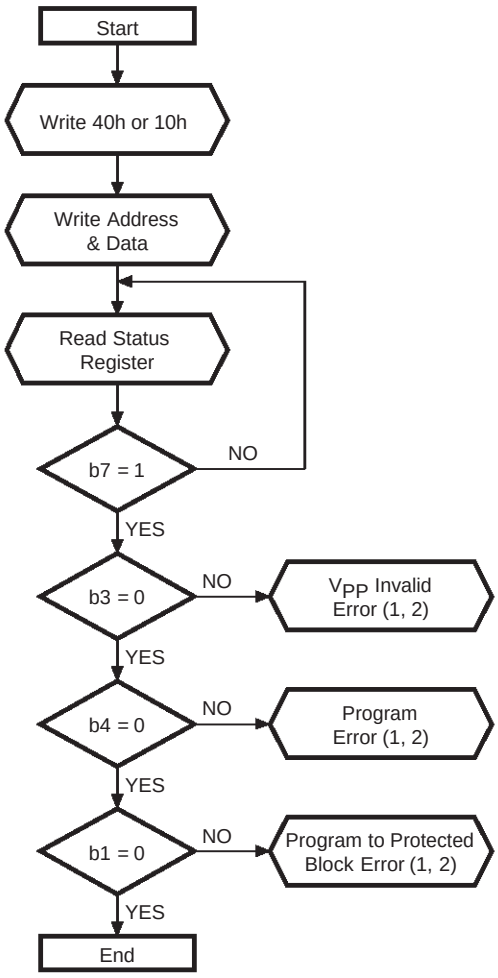
Offset	Data	Description			Value
(P+19)h = 52h	0001h	Supported handshaking signal ($\overline{\text{WAIT}}$ pin)			
		bit 0	during synchronous read	(1 = Yes, 0 = No)	Yes
		bit 1	during asynchronous read	(1 = Yes, 0 = No)	No

Table 35. Security Code Area

Offset	Data	Description
80h	LPR	Lock Protection Register bit 0: ST programmed, value 0 bit 1: OTP protection and bit 2 protection bit bit 2: Security Block Protection bit bits 3 - 15 reserved
81h 82h 83h 84h	ID data	64 bits: unique device number
85h 86h 87h 88h	OTP data	64 bits: User Programmable OTP

APPENDIX B. FLOWCHARTS AND PSEUDO CODES

Figure 18. Program Flowchart and Pseudo Code

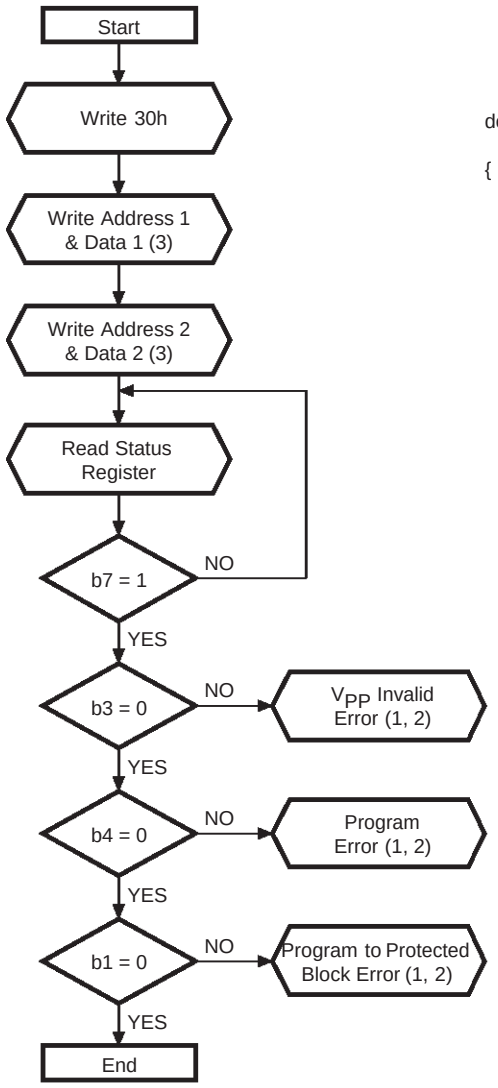



```
program_command (addressToProgram, dataToProgram) {:
        writeToFlash (any_address, 0x40) ;
        /*or writeToFlash (any_address, 0x10) ; */

         writeToFlash (addressToProgram, dataToProgram) ;
         /*Memory enters read status state after
         the Program Command*/

      do {
          status_register=readFlash (any_address) ;
          /* E or G must be toggled*/

          } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI090014b

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 19. Double Word Program Flowchart and Pseudo code

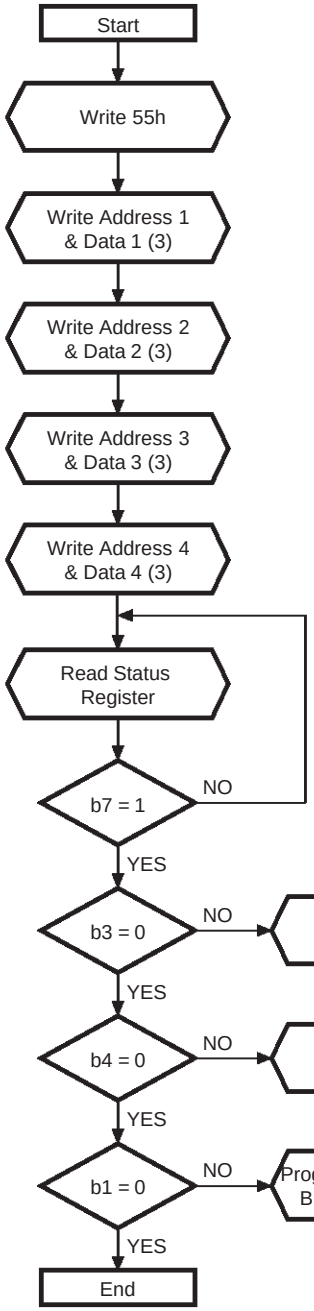



```
double_word_program_command (addressToProgram1, dataToProgram1,
                                        addressToProgram2, dataToProgram2)
{
        writeToFlash (any_address, 0x30) ;
        writeToFlash (addressToProgram1, dataToProgram1) ;
                                        /*see note (3) */
        writeToFlash (addressToProgram2, dataToProgram2) ;
                                        /*see note (3) */
         /*Memory enters read status state after
        the Program command*/

      do {
         status_register=readFlash (any_address) ;
         /* E or G must be toggled*/

       } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI090015b

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 and Address 2 must be consecutive addresses differing only for bit A0.

Figure 20. Quadruple Word Program Flowchart and Pseudo Code

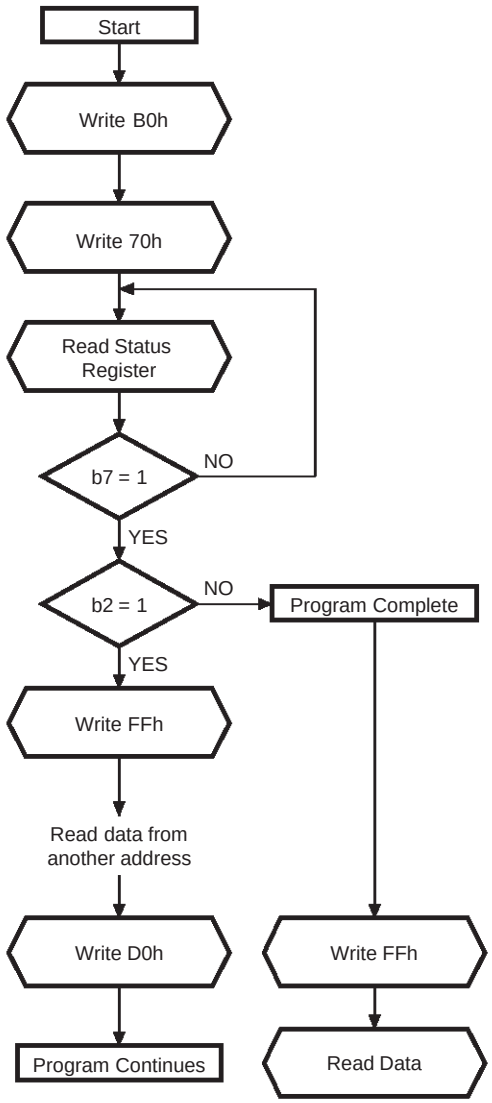



```
quadruple_word_program_command (addressToProgram1, dataToProgram1,
                                addressToProgram2, dataToProgram2,
                                addressToProgram3, dataToProgram3,
                                addressToProgram4, dataToProgram4)
{
        writeToFlash (any_address, 0x55) ;

        writeToFlash (addressToProgram1, dataToProgram1) ;
                                /*see note (3) */

        writeToFlash (addressToProgram2, dataToProgram2) ;
                                /*see note (3) */

        writeToFlash (addressToProgram3, dataToProgram3) ;
                                /*see note (3) */

        writeToFlash (addressToProgram4, dataToProgram4) ;
                                /*see note (3) */

         /*Memory enters read status state after
        the Program command*/

      do {
        status_register=readFlash (any_address) ;
        /* Ē or Ḡ must be toggled*/

        } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI05283

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 to Address 4 must be consecutive addresses differing only for bits A0 and A1.

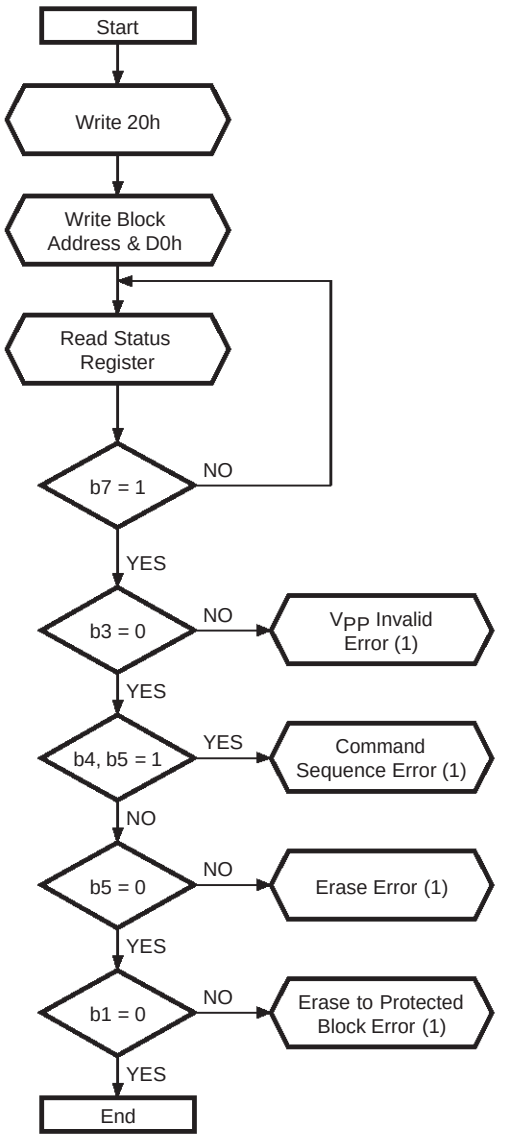
Figure 21. Program Suspend & Resume Flowchart and Pseudo Code




```
program_suspend_command  ( ) {
      writeToFlash (any_address, 0xB0) ;

      writeToFlash (any_address, 0x70) ;
      /* read status register to check if
      program has already completed */


  do {
      status_register=readFlash (any_address) ;
      /* E or G must be toggled*/




      } while (status_register.b7== 0) ;


if  (status_register.b2==0)  /*program completed */
      {  writeToFlash (any_address, 0xFF)  ;
        read_data ( ) ; /*read data from another block*/
        /*The device returns to Read Array
        (as if program/erase suspend was not issued).*/


       }
else
      {  writeToFlash (any_address, 0xFF)  ;
        read_data ( ); /*read data from another address*/
        writeToFlash (any_address, 0xD0) ;
        /*write 0xD0 to resume program*/
       }
}
```

AI90016b

Figure 22. Block Erase Flowchart and Pseudo Code

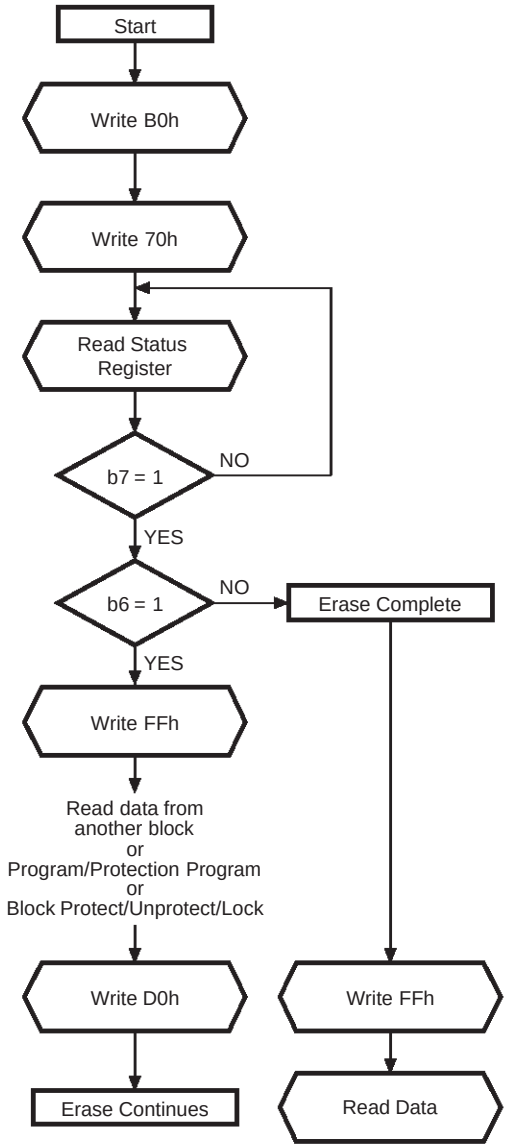



```
erase_command   ( blockToErase ) {
        writeToFlash (any_address, 0x20) ;

        writeToFlash (blockToErase, 0xD0) ;
        /* only A12-A20 are significannt */
        /* Memory enters read status state after
        the Erase Command */


    do {
        status_register=readFlash (any_address) ;
         /* E or G must be toggled*/




        } while (status_register.b7== 0) ;


if  (status_register.b3==1) /*VPP invalid error */
        error_handler ( ) ;


if  ( (status_register.b4==1) && (status_register.b5==1) )
/* command sequence error */
        error_handler ( ) ;


if  ( (status_register.b5==1) )
/* erase error */
        error_handler ( ) ;


if  (status_register.b1==1) /*program to protect block error */
        error_handler ( ) ;


}
```

AI90017b

Note: If an error is found, the Status Register must be cleared before further Program/Erase operations.

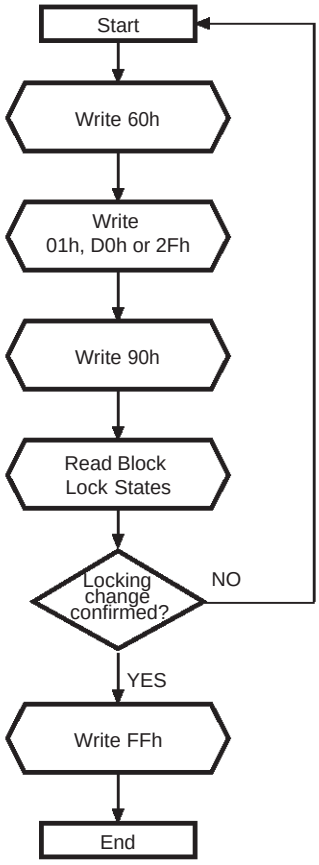
Figure 23. Erase Suspend & Resume Flowchart and Pseudo Code




```
erase_suspend_command   ( ) {
        writeToFlash (any_address, 0xB0) ;

        writeToFlash (any_address, 0x70) ;
        /* read status register to check if
        erase has already completed */


     do {
         status_register=readFlash (any_address) ;
         /* E or G must be toggled*/


        } while (status_register.b7== 0) ;


if  (status_register.b6==0)  /*erase completed */
        {  writeToFlash (any_address, 0xFF)  ;


           read_data ( ) ;
           /*read data from another block*/
           /*The device returns to Read Array
           (as if program/erase suspend was not issued).*/


         }
else
        {  writeToFlash (any_address, 0xFF)  ;
           read_program_data ( );
           /*read or program data from another address*/
           writeToFlash (any_address, 0xD0) ;
           /*write 0xD0 to resume erase*/
         }
}
```

AI90018b

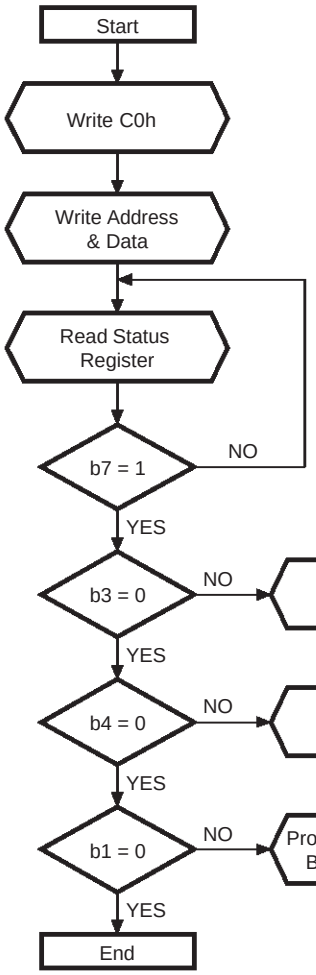
Figure 24. Locking Operations Flowchart and Pseudo Code




```
locking_operation_command   (address, lock_operation)  {
        writeToFlash (any_address, 0x60) ; /*configuration setup*/

        if  (lock_operation==LOCK)  /*to protect the block*/
                writeToFlash (address, 0x01)  ;
        else if  (lock_operation==UNLOCK)  /*to unprotect the block*/
                writeToFlash (address, 0xD0)  ;
        else if  (lock_operation==LOCK-DOWN)  /*to lock the block*/
                writeToFlash (address, 0x2F)  ;

                writeToFlash (any_address, 0x90)  ;

        if  (readFlash (address) ! = locking_state_expected)
                        error_handler () ;
                /*Check the locking state (see Read Block Signature table )*/

        writeToFlash (any_address, 0xFF) ; /*Reset to Read Array mode*/

}
```

AI05281

Figure 25. Protection Register Program Flowchart and Pseudo Code




```
protection_register_program_command (addressToProgram, dataToProgram) {:
                    writeToFlash (any_address, 0xC0) ;

                    writeToFlash (addressToProgram, dataToProgram) ;
                    /*Memory enters read status state after
                    the Program Command*/

                do {
                    status_register=readFlash (any_address) ;
                    /* E or G must be toggled*/

                } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI05282

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

APPENDIX C. COMMAND INTERFACE STATE TABLES

Table 36. Command Interface States - Lock table

Current State of Other Bank	Current State of the Current Bank		Command Input to the Current Bank (and Next State of the Current Bank)										
	Mode	State	Others	Read Array (FFH)	Erase Confirm P/E Resume Unlock Confirm (D0h)	Read Status Register (70h)	Clear Status Register (50h)	Read Electronic Signature (90h)	Read CFI Query (98h)	Block Lock Unlock Lock-Down setup Set BCR setup (60h)	Block lock Confirm (01h)	Block Lock-Down Confirm (2Fh)	Set BCR Confirm (03h)
Any State	Read	Array CFI Electronic Signature Status	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block Lock, Unlock, Lock-Down, Set BCR Setup	Read Array	Read Array	Read Array
Any State	Lock Unlock Lock-Down BCR	Setup	Block Lock Unlock Lock-Down Error, Set BCR Error	Block lock Unlock Lock-Down Error, Set BCR Error	Block Lock Unlock Lock-Down Block	Block Lock Unlock Lock-Down Error, Set BCR Error	Block Lock Unlock Lock-Down Error, Set BCR Error	Block Lock Unlock Lock-Down Error, Set BCR Error	Block Lock Unlock Lock-Down Error, Set BCR Error	Block Lock Unlock Lock-Down Error, Set BCR Error	Block Lock Unlock Lock-Down Block	Block Lock Unlock Lock-Down Block	Set BCR
		Error Lock Unlock Lock-Down Block Set BCR	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block LocK Unlock Lock-Down Setup, Set BCR Setup	Read Array	Read Array	Read Array
Any State	Protection Register	Done	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block LocK Unlock Lock-Down Setup, Set BCR Setup	Read Array	Read Array	Read Array
Any State	Program-Double/ Quadruple Program	Done	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block LocK Unlock Lock-Down Setup, Set BCR Setup	Read Array	Read Array	Read Array
Setup Idle Erase Suspend	Program Suspend	Read Array, CFI, Elect. Sign., Status	SEE MODIFY TABLE	PS Read Array	Program (Busy)	PS Read Status Register	PS Read Array	PS Read Elect. Sign.	PS Read CFI	PS Read Array	PS Read Array	PS Read Array	PS Read Array
Idle	Block/ Bank Erase	Setup	Erase Error	Erase Error	Erase (Busy)	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error
Any State		Error Done	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block LocK Unlock Lock-Down Setup, Set BCR Setup	Read Array	Read Array	Read Array
Setup Busy Idle Program Suspend	Erase Suspend	Read Array, CFI, Elect. Sign., Status	SEE MODIFY TABLE	ES Read Array	Erase (Busy) ES Read Array Erase (Busy) ES Read Array	ES Read Status Register	ES Read Array	ES Read Elect. Sign.	ES Read CFI	Block LocK Unlock Lock-Down Setup, Set BCR Setup	ES Read Array	ES Read Array	ES Read Array

Note: PS = Program Suspend, ES = Erase Suspend.

Table 37. Command Interface States - Modify Table

Current State of the Other Bank	Current State of the Current Bank		Command Input to the Current Bank (and Next State of the Current Bank)						
	Mode	State	Others	Program Setup (10h/40h)	Block Erase Setup (20h)	Program-Erase Suspend (B0h)	Protection Register Program Setup (C0h)	Double/ Quadruple Program Setup (30h/55h)	Bank Erase Setup (80h)
Setup	Read	Array, CFI, Electronic Signature, Status Register	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Busy									
Idle				Program setup	Block Erase Setup		Protection Register Setup	Double/ Quadruple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Setup	Lock Unlock Lock-Down BCR	Error, Lock Unlock Lock-Down Block, Set BCR	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Busy									
Idle				Program setup	Block Erase Setup		Protection Register Setup	Double/ Quadruple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Idle	Protection Register	Setup	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)
Setup		Busy							
Busy		Done	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Idle				Program Setup	Block Erase Setup		Protection Register Setup	Double/ Quadruple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Any State	Program Double/ Quadruple Word Program	Setup	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)
Idle		Busy				PS Read Status Register			
Setup		Done	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Busy									
Idle				Program Setup	Block Erase Setup		Protection Register Setup	Double/ Quadruple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Setup	Program Suspend	Read Array, CFI, Elect. Sign., Status Register	SEE LOCK TABLE	PS Read Array	PS Read Array	PS Read Array	PS Read Array	PS Read Array	PS Read Array
Idle									
Erase Suspend									
Idle	Block/ Bank Erase	Setup	SEE LOCK TABLE	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error
		Busy	Erase (Busy)	Erase (Busy)	Erase (Busy)	ES Read Status Register	Erase (Busy)	Erase (Busy)	Erase (Busy)
Setup	Erase Suspend	Read Array, CFI, Elect. Sign., Status Register	SEE LOCK TABLE	ES Read Array	ES Read Array	ES Read Array	ES Read Array	ES Read Array	ES Read Array
Busy									
Idle				Program Setup				Double/ Quadruple Program Setup	
Program Suspend				ES Read Array				ES Read Array	

Note: PS = Program Suspend, ES = Erase Suspend.