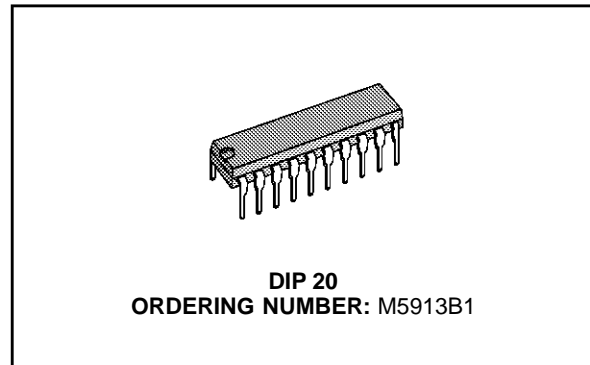


**COMBINED SINGLE CHIP PCM CODEC AND FILTER**

- SYNCHRONOUS CLOCKS ONLY
- AT&T D3/D4 AND CCITT COMPATIBLE
- TWO TIMING MODES:  
FIXED DATA RATE MODE 1.536MHz, 1.544MHz, 2.048MHz  
VARIABLE DATA MODE: 64KHz - 4.096MHz
- PIN SELECTABLE  $\mu$ -LAW OR A-LAW OPERATION
- NO EXTERNAL COMPONENTS FOR SAMPLE-AND-HOLD AND AUTO ZERO FUNCTIONS
- LOW POWER DISSIPATION:  
0.5mW POWER DOWN  
70mW OPERATING
- EXCELLENT POWER SUPPLY REJECTION



Office Switching Systems

- Concentration - M5913 Subscriber Carrier and Concentrators.

The wide dynamic range (78dB) and the minimal conversion time make it ideal products for other applications such as:

- Voice Store and Forward
- Secure Communications Systems
- Digital Echo Cancellers
- Satellite Earth Stations.

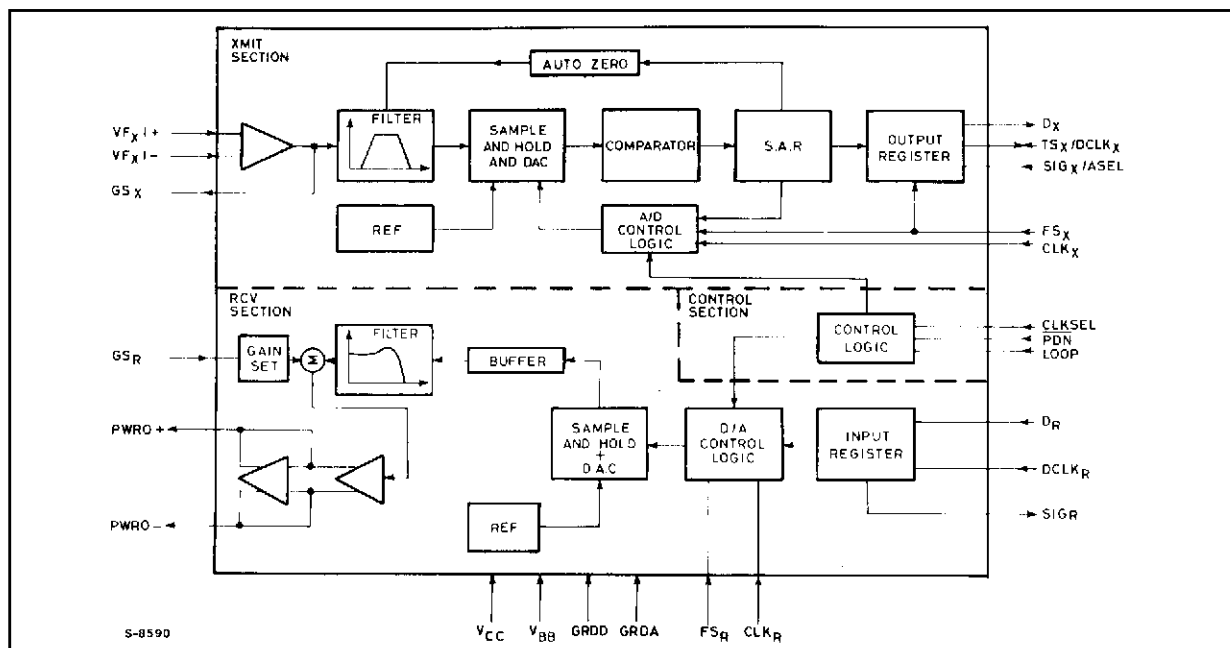
**DESCRIPTION**

The M5913 is fully integrated PCM (pulse code modulation) codecs and transmit/receive filter using CMOS silicon gate technology.

The primary applications for the M5913 are telephone systems :

- Switching - M5913-Digital PBX's and Central

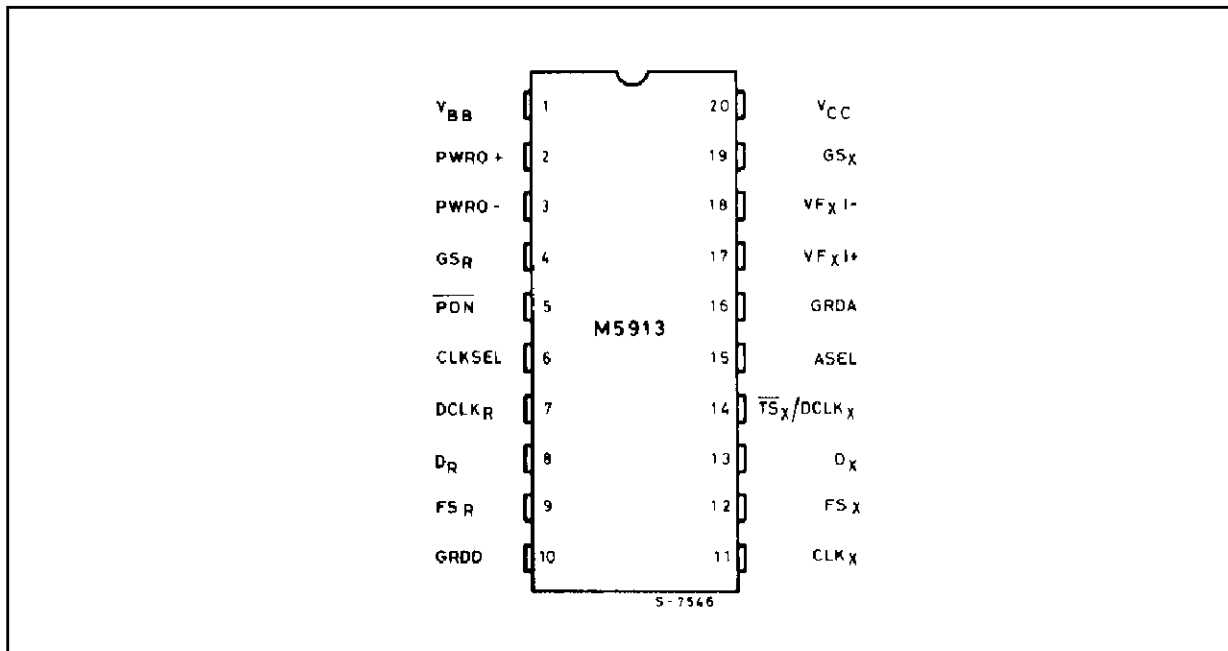
**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	With Respect GRDD, GRDA = 0V	- 0.6 to 7	V
V <sub>BB</sub>	With Respect GRDD, GRDA = 0V	- 0.6 to - 7	V
GRDD, GRDA	In Such Case : 0 ≤ V <sub>CC</sub> ≤ + 7V, - 7V ≤ V <sub>BB</sub> ≤ 0V	± 0.3	V
V <sub>I/O</sub>	Analog Inputs, Analog Outputs and Digital Inputs	V <sub>BB</sub> - 0.3 ≤ V <sub>IN</sub> /V <sub>OUT</sub> ≤ V <sub>CC</sub> + 0.3	V
V <sub>O DIG</sub>	Digital Outputs	GRDD - 0.3 ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> + 0.3	V
P <sub>tot</sub>	Total Power Dissipation	1	W
T <sub>stg</sub>	Storage Temperature Range	-65 to 150	°C

**PIN CONNECTION (Top view)**



**PIN NAMES**

Symbol	Parameter	Symbol	Parameter
V <sub>BB</sub>	Power (-5V)	G <sub>S</sub> X	Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VF <sub>X</sub> I-, VF <sub>X</sub> I+	Analog Inputs
G <sub>S</sub> R	Gain Setting Input for receive Channel	GRDA	Analog Ground
PDN	Power Pown Select	NC	No Connected
CLKSEL	Master Clock Select	SIG <sub>X</sub>	Transmit Digital Signaling Input
LOOP	Analog Loop Back	ASEL	μ or A-law Select
SIG <sub>R</sub>	Signaling Bit Output	TS <sub>X</sub>	Digital Output - Timeslot Strobe
DCLK <sub>R</sub>	Receive Data Rate Clock	DCLK <sub>X</sub>	Transmit Data Rate Clock
D <sub>R</sub>	Receive Channel Input	D <sub>X</sub>	Transmit (Digital) Output
F <sub>S</sub> R	Receive Frame Synchronization Clock	F <sub>S</sub> X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK <sub>X</sub>	Transmit Master Clock
V <sub>CC</sub>	Power (+5V)	CLK <sub>R</sub>	Receive Master Clock

## PIN DESCRIPTION

Symbol	Function
$V_{BB}$	Most Negative Supply. Input voltage is -5 volts $\pm 5\%$ .
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO -	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
$GS_R$	Input to the gain Setting Network on the Output Power Amplifier, Transmission level can be adjusted over a 12dB range depending on the voltage at $GS_R$ .
PDN	Power Down Select. When PDN is TTL high, the device is active. When low, the device is powered down.
CLKSEL	input which must be pinstrapped to reflect the master clock frequency at $CLK_X$ , $CLK_R$ . $CLKSEL = V_{BB}$ 2.048MHz $CLKSEL = GRDD$ 1.544MHz $CLKSEL = V_{CC}$ 1.536MHz
LOOP	Analog Loopback. When this pin is TTL high, the receive output (PWRO+) is internally connected to $VF_{X +}$ , $GS_R$ is internally connected to PWRO-, and $VF_{X -}$ is internally connected to $GS_X$ . A 0dBm0 digital signal input at $D_R$ is returned as a +3dBm0 digital signal output at $D_X$ .
$SIG_R$	Signalling Bit Output, Receive Channel. In fixed data rate mode, $SIG_R$ outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When $DCLK_R$ is connected to $V_{BB}$ , the fixed data rate mode is selected. When $DCLK_R$ is not connected to $V_{BB}$ , the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock which operates at TTL levels from 64kB to 4.096MB data rates
$D_R$	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock: $CLK_R$ in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
$FS_R$	8kHz frame synchronization clock input/timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever $FS_R$ is TTL low for 30 milliseconds
GRDD	Digital Ground for all Internal Logic Circuits. Not internally tied to GRDA.
$CLK_R$	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
$CLK_X$	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
$FS_X$	8kHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to $FS_R$ . The transmit channel enters the standby state whenever $FS_X$ is TTL low for 30 milliseconds.
$D_X$	Transmit PCM Output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : $CLK$ in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS}_X/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 4.096MB data rates.
$SIG_X/ASEL$	A dual purpose selects $\mu$ -law and pin. When connected to $V_{BB}$ , A law operation is selected. When it is not connected to $V_{BB}$ pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the $D_X$ lead.
NC	Not Connected.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
$VF_{X +}$	Non inverting analog input to uncommitted transmit operational amplifier.
$VF_{X -}$	Inverting analog input to uncommitted transmit operational amplifier.
$GS_X$	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
$V_{CC}$	Most positive supply ; input voltage is + 5 volts $\pm 5\%$

## FUNCTIONAL DESCRIPTION

The M5913 provides the analog-to-digital and the digital-to-analog conversion and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highway of a time division multiplexed (TDM) system. It is intended to be used at the analog termination of a PCM line.

The following major functions are provided :

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

## GENERAL OPERATION

### System Reliability Features

The combo-chip can be powered up by pulsing  $FS_X$  and/or  $FS_R$  while a TTL high voltage is applied to  $\overline{PDN}$ , provided that all clocks and supplies are connected. The M5913 has internal resets on power up (or when  $V_{BB}$  or  $V_{CC}$  are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs  $D_X$  and  $\overline{TS}_X$  are held in a high impedance state for approximately four frames (500 $\mu$ s) after power up or application of  $V_{BB}$  or  $V_{CC}$ . After this delay,  $D_X$  and  $\overline{TS}_X$  will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 40 milliseconds to reach their equilibrium value due to the autozero circuit setting time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output  $SIG_R$  is also held low for a maximum of four frames after power up or application of  $V_{BB}$  or  $V_{CC}$ ,  $SIG_R$  will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability,  $\overline{TS}_X$  and  $\overline{D}_X$  will be placed in a high impedance state approximately 20 $\mu$ s after an interruption of  $CLK_X$ . Simi-

larly  $SIG_R$  will be held low approximately 20 $\mu$ s after an interruption of  $CLK_R$ . These interruptions could possibly occur with some kind of fault condition.

### Power Down And Standby Modes

To minimize power consumption, two power down modes are provided in which most M5913 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the  $\overline{PDN}$  pin. In this mode, power consumption is reduced to an average of 0.5mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the  $\overline{PDN}$  pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire down by selectively removing  $FS_X$  and/or  $FS_R$ . With both channels in the standby state, power consumption is reduced to an average of 1mW. If transmit only operation is desired,  $FS_X$  should be applied to the device while  $FS_R$  is held low. Similarly, if receive only operation is desired,  $FS_R$  should be applied while  $FS_X$  is held low.

### Fixed Data Rate Mode

Fixed data rate timing, is selected by connecting  $DCLK_R$  to  $V_{BB}$ . It employs master clock  $CLK_X$ , and  $CLK_R$ , frame synchronization clocks  $FS_X$  and  $FS_R$ , and output  $\overline{TS}_X$ .

$CLK_X$ , and  $CLK_R$ , serve both as the master clock to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway.  $FS_X$  and  $FS_R$  are 8kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables

**Table 1:** Power Down Methods

Device Status	Power Down Methods	Digital Outputs Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and $D_X$ are placed in a high impedance state and $SIG_R$ is placed in a TTL low state within 10 $\mu$ s.
Stand-by Mode	$FS_X$ and $FS_R$ are TTL low	$\overline{TS}_X$ and $D_X$ are placed in a high impedance state and $SIG_R$ is placed in a TTL low state 30ms after $FS_X$ and $FS_R$ are removed.
Only transmit is on stand-by	$FS_X$ is TTL low	$\overline{TS}_X$ and $D_X$ are placed in a high impedance state within 30ms.
Only receive is on stand-by	$FS_R$ is TTL low	$SIG_R$ is placed in a TTL low state within 30ms.

the signaling function.  $TS_X$  is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at  $D_X$  on the first eight positive transitions of  $CLK_X$  following the rising edge of  $FS_X$ . Similarly, on the receive side, data is received on the first eight falling edges of  $CLK_R$ . The frequency of  $CLK_X$  and  $CLK_R$  is selected by the  $CLKSEL$  pin to be either 1.536, 1.544 or 2.048MHz. No other frequency of operation is allowed in the fixed data rate mode.

### Variable Data Rate Mode

Variable data rate timing is selected by connecting  $DCLK_R$  to the bit clock for the receive PCM highway rather than to  $V_{BB}$ . It employs master clocks  $CLK_X$  and  $CLK_R$ , bit clocks  $DCLK_R$  and  $DCLK_X$  and frame synchronization clocks  $FS_R$  and  $FS_X$ .

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64kHz to 4096MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048MHz.

In this mode,  $DCLK_R$  and  $DCLK_X$  become the data clocks for the receive and transmit PCM highways. While  $FS_X$  is high, PCM data from  $D_X$  is transmitted onto the highway on the next eight consecutive positive transitions of  $DCLK_X$ . Similarly, while  $FS_R$  is high, each PCM bit from the highway is received by  $D_R$  on the next eight consecutive negative transitions of  $DCLK_R$ .

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 $\mu$ s frame as long as  $DCLK_X$  is pulsed and  $FS_X$  is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

### Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive sections are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically  $\pm 0.04$ dB in absolute gain for each half

channel, providing the user a significant margin for error in other board components.

### Conversion Laws

The M5913 is designed to operate in both  $\mu$ -law and A-law systems. The user can select either conversion law according to the voltage present on the  $SIG_X/ASEL$  pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for  $\mu$ -law and A-law conversion. If A-law operation is desired,  $SIG_X$  should be tied to  $V_{BB}$ . Thus, signaling is not allowed during A-law operation. If  $\mu$  = 255-law operation is selected, then  $SIG_X$  is a TTL level input which modifies the LSB on the PCM output in signaling frames

## TRANSMIT OPERATION

### Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17V, a maximum DC offset of 25mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1MHz. Gain of up to 20dB can be set without degrading the performance of the filter. The load impedance to ground ( $GRDA$ ) at the amplifier output ( $GS_X$ ) must be greater than 10k $\Omega$  in parallel less than 50pF. The input signal on lead  $VF_{X1+}$  can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see figure 3).

A low pass anti-aliasing section is included on-chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

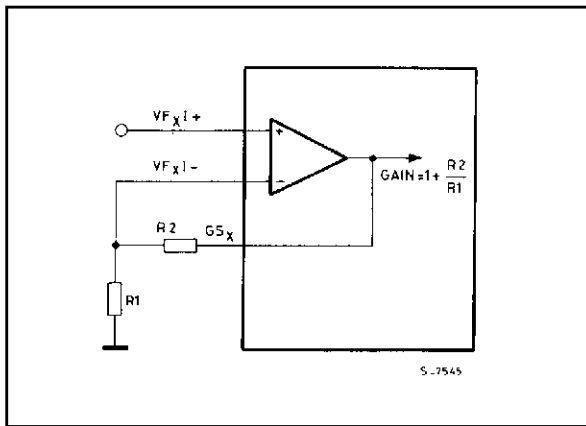
The passband section provides flatness and stop-band attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712.

The M5913 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown the relative table.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60Hz power lines, 17Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise.

Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200Hz. This feature allows the use of low-cost transformer hybrids without external components.

**Figure 3:** Transmit Filter Gain Adjustment.



**Encoding**

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor.

The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

**RECEIVE OPERATION**

**Decoding**

The PCM word at the D<sub>R</sub> lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on

an internal sample and hold capacitor. This sample is then transferred to the receive filter.

**Receive Filter**

The receive section of the filter provides pass-band flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin X)/X response of such decoders. The receive filter characteristics and specifications are shown in the relative table.

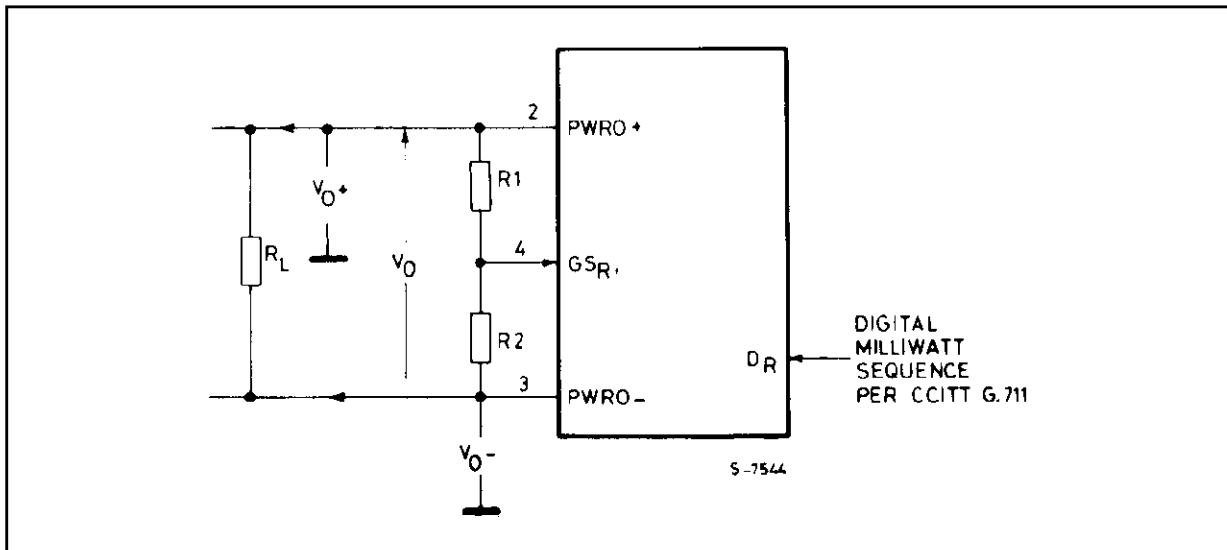
**Receive Output Power Amplifiers**

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12dBm or 600 ohms differentially to a level of 15dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS<sub>R</sub> input. GS<sub>R</sub> is internally connected to an analog gain setting network. When GS<sub>R</sub> is strapped to PWRO<sub>-</sub>, the receive level is minimized; when it is tied to PWRO<sub>+</sub>, the level is maximized. The output transmission level interpolates between 0 and -12dB as GS<sub>R</sub> is interpolated (with potentiometer) between PWRO<sub>-</sub> and PWRO<sub>+</sub>. The use of the output gain set is illustrated in figure 4.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D<sub>R</sub> is the eight-code sequence specified in CCITT recommendation G.711.

**Figure 4:** Gain Setting Configuration.



**OUTPUT GAIN SET: DESIGN CONSIDERATIONS** (refer to figure 4)

PWRO+ and PWRO- are low impedance complementary outputs. The voltages at the nodes are:

$V_O$  at PWRO+

$V_O$  at PWRO-

$V_O = V_{O+} - V_{O-}$  (total differential response)

R1 and R2 are a gain setting resistor network with the center tap connected to the  $GS_R$  input. A value greater than 10K $\Omega$  and less than 100K $\Omega$  for R1 + R2 is recommended because:

- The parallel combination of R1 + R2 and RL sets the total loading.
- The total capacitance at the  $GS_R$  input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

If  $V_A$  represents the output voltage without any gain setting network connected, you can have:

$$V_O = AV_A$$

$$\text{where } A = \frac{1 + (R_1 / R_2)}{4 + (R_1 / R_2)}$$

For design purposes, a useful form is R1/R2 as a function of A.

$$R_1 / R_2 = \frac{4A - 1}{1 - A}$$

(allowable values for A are those which make R1/R2 positive)

Examples are:

If A = 1 (maximum output), then  
 $R_1/R_2 = \infty$  or  $V(GS_R) = V_{O+}$ ;  
 i.e.,  $GS_R$  is tied to PWRO+

If A = 1/2, then  
 $R_1/R_2 = 2$

If A = 1/4 (minimum output) then  
 $R_1/R_2 = 0$  or  $V(GS_R) = V_{O+}$ ;  
 i.e.,  $GS_R$  is tied to PWRO+

**DC CHARACTERISTICS** ( $T_{amb} = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{BB} = -5\text{V} \pm 5\%$ ,  $GRDA = 0\text{V}$ , unless otherwise specified) Typical values are for  $T_{amb} = 25^\circ\text{C}$  and nominal power supply values.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE						
$I_{IL}$	Low Level Input Current	$GRDD \leq V_{IN} \leq V_{IL}$ (note 1)			10	$\mu\text{A}$
$I_{IH}$	High Level Input Current	$V_{IH} \leq V_{IN} \leq V_{CC}$			10	$\mu\text{A}$
$V_{IL}$	Input Low Voltage, Except CLKSEL				0.8	V
$V_{IH}$	Input High Voltage, Except CLKSEL		2.0			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 3.2\text{mA}$ at $D_x$ , $\overline{TS}_x$ and $SIG_R$			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = 9.6\text{mA}$ at $D_x$ $I_{OH} = 1.2\text{mA}$ at $SIG_R$	2.4			V
$V_{ILO}$	Input Low Voltage, CLKSEL (note 2)		$V_{BB}$		$V_{BB} + 0.5$	V
$V_{IIO}$	Input Intermediate Voltage, CLKSEL		GRDD -0.5		0.5	V
$V_{IHO}$	Input High Voltage, CLKSEL		$V_{CC} - 0.5$		VCC	V
$C_{OX}$	Digital Output Capacitance (note 3)			5		pF
$C_{IN}$	Digital Input Capacitance			5	10	pF

**Notes:**

- $V_{IN}$  is the voltage on any digital pin.
- $SIG_x$  and  $DCLK_R$  are TTL level inputs between GRDD and  $V_{CC}$ ; they are also pinstraps for mode selection when tied to  $V_{BB}$ . Under these conditions  $V_{ILO}$  is the input low voltage requirement.
- Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pF.

**DC CHARACTERISTICS** (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
POWER DISSIPATION All measurements made at $f_{DCLK} = 2.048\text{MHz}$ , outputs unloaded						
$I_{CC1}$	$V_{CC}$ Operating Current			6	10	mA
$I_{BB1}$	$V_{BB}$ Operating Current			6	9	mA
$I_{CC0}$	$V_{CC}$ Power Down Current	$P_{DN} \leq V_{IL}$ ; after $10\mu\text{s}$		40	300	$\mu\text{A}$
$I_{BB0}$	$V_{BB}$ Power Down Current	$P_{DN} \leq V_{IL}$ ; after $10\mu\text{s}$		40	300	$\mu\text{A}$
$I_{CCS}$	$V_{CC}$ Standby Current	$FS_X, FS_R \leq V_{IL}$ ; after 30ms		300	600	$\mu\text{A}$
$I_{BBS}$	$V_{BB}$ Standby Current	$FS_X, FS_R \leq V_{IL}$ ; after 30ms		40	300	$\mu\text{A}$
$P_{D1}$	Operating Power Dissipation			60	100	mW
$P_{D0}$	Power Down Dissipation	$P_{DN} \leq V_{IL}$ ; after $10\mu\text{s}$		0.4	3	mW
$P_{ST}$	Standby Power Dissipation	$FS_X, FS_R \leq V_{IL}$ ; after 30ms		1.7	5	mW

## ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

$I_{BX1}$	Input Leakage Current, $V_{FX1+}, V_{FX1-}$	$-2.17\text{V} \leq V_{IN} \leq 2.17\text{V}$			100	nA
$R_{IX1}$	Input Resistance, $V_{FX1+}, V_{FX1-}$		10			$\text{M}\Omega$
$V_{OSX1}$	Input Offset Voltage, $V_{FX1+}, V_{FX1-}$				25	mV
CMRR	Common Mode Rejection, $V_{FX1+}, V_{FX1-}$	$-2.17\text{V} \leq V_{IN} \leq 2.17\text{V}$	55			dB
$A_{VOL}$	DC Open Loop Voltage Gain, $GS_X$	$R_L = 10\text{K}$	5000	20.000		
$f_c$	Open Loop Unity Gain Bandwidth, $GS_X$			1		MHz
$V_{OX1}$	Output Voltage Swing $GS_X$	$R_L \geq 10\text{k}\Omega$	- 2.17		2.17	V
$C_{LX1}$	Load Capacitance, $GS_X$				50	pF
$R_{LX1}$	Minimum Load Resistance, $GS_X$		10			k $\Omega$

## ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

$R_{ORA}$	Output Resistance, $PWRO+, PWRO-$			1		$\Omega$
$V_{OSRA}$	Single-ended Output DC Offset, $PWRO+, PWRO-$	Relative to GRDA	-150	75	150	mV
$C_{LRA}$	Load Capacitance, $PWRO+, PWRO-$				100	pF

**AC CHARACTERISTICS - TRANSMISSION PARAMETERS**

Unless otherwise noted, the analog input is a 0dBm0, 1020Hz sine wave<sup>1</sup>. Input amplifier is set for unity gain, noninverting. The digital inputs is a PCM bit stream generated by passing a 0dBm0, 1020Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration<sup>2</sup>. All output levels are (sin X)/X corrected.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GAIN AND DYNAMIC RANGE						
EmW	Encoder Milliwatt Response (transmit gain tolerance)	$T_{amb} = 25^\circ\text{C}$ , $V_{BB} = -5\text{V}$ , $V_{CC} = +5\text{V}$	-0.15	$\pm 0.04$	+0.15	dBm0
EmW <sub>TS</sub>	EmW Variation with Temperature and Supplies	$\pm 5\%$ Supplies, 0 to $70^\circ\text{C}$ Relative to Nominal Conditions	-0.12		+0.12	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	$T_{amb} = 25^\circ\text{C}$ ; $V_{BB} = -5\text{V}$ , $V_{CC} = +5\text{V}$	-0.15	$\pm 0.04$	+0.15	dBm0
DmW <sub>TS</sub>	DmW Variation with Temperature and Supplies	$\pm 5\%$ , 0 to $70^\circ\text{C}$	-0.08		+0.08	dB
0TLP <sub>1X</sub>	Zero Transmission Level Point Transmit Channel (0dBm0) $\mu$ -law	Referenced to $600\Omega$ Referenced to $900\Omega$		+ 2.76 + 1.00		dBm dBm
0TLP <sub>2X</sub>	Zero Transmission Level Point Transmit Channel (0dBm0) A-law	Referenced to $600\Omega$ Referenced to $900\Omega$		+ 2.79 + 1.03		dBm dBm
0TLP <sub>1R</sub>	Zero Receive Level Point Receive Channel (0dBm0) $\mu$ -law	Referenced to $600\Omega$ Referenced to $900\Omega$		+ 5.76 + 4.00		dBm dBm
0TLP <sub>2R</sub>	Zero Transmission Level Point Transmit Channel (0dBm0) A-law	Referenced to $600\Omega$ Referenced to $900\Omega$		+ 5.79 + 4.03		dBm dBm



**AC CHARACTERISTICS** (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GAIN TRACKING Reference Level = - 10dBm0						
GT1 <sub>X</sub>	Transmit Gain Tracking Error Sinusoidal Input; $\mu$ -law	+ 3 to - 40dBm0 - 40 to - 50dBm0 - 50 to - 55dBm0			$\pm 0.2$ $\pm 0.4$ $\pm 1.0$	dB dB dB
GT2 <sub>X</sub>	Transmit Gain Tracking Error Sinusoidal Input; A-law	+ 3 to - 40dBm0 - 40 to - 50dBm0 - 50 to - 55dBm0			$\pm 0.2$ $\pm 0.4$ $\pm 1.0$	dB dB dB
GT1 <sub>R</sub>	Receive Gain Tracking Error Sinusoidal Input; $\mu$ -law	+ 3 to - 40dBm0 - 40 to - 50dBm0 - 50 to - 55dBm0			$\pm 0.2$ $\pm 0.4$ $\pm 1.0$	dB dB dB
GT2 <sub>R</sub>	Receive Gain Tracking Error Sinusoidal Input; A-law	+ 3 to - 40dBm0 - 40 to - 50dBm0 - 50 to - 55dBm0			$\pm 0.2$ $\pm 0.4$ $\pm 1.0$	dB dB dB

**NOISE**

N <sub>XC1</sub>	Transmit Noise, C-message Weighted	V <sub>FxI+</sub> = GRDA, V <sub>FxI-</sub> = GS <sub>X</sub>		0	13	dBrnc0
N <sub>XC2</sub>	Transmit Noise, C-message Weighted with Eighth Bit Signaling	V <sub>FxI+</sub> = GRDA, V <sub>FxI-</sub> = GS <sub>X</sub> 6 th Frame Signaling		13	18	dBrnc0
N <sub>XP</sub>	Transmit Noise, Psophometrically Weighted	V <sub>FxI+</sub> = GRDA, V <sub>FxI-</sub> = GS <sub>X</sub>		(note 3)	- 80	dBrnc0
N <sub>RC1</sub>	Receive Noise, C-message Weighted: Quiet Code	D <sub>R</sub> = 11111111 Measure at PWRO+		1	9	dBrnc0
N <sub>RC2</sub>	Receive Noise, C-message Weighted: Sign Bit Toggle	Input to D <sub>R</sub> is 0 code with Sign Bit Toggle at 1KHz Rate		1	10	dBm0p
N <sub>RP</sub>	Receive Noise, Psophometrically Weighted	D <sub>R</sub> = Lowest Positive Decode Level		-90	- 81	dB0p
N <sub>SF</sub>	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			- 50	dBm0
PSRR <sub>1</sub>	V <sub>CC</sub> Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D <sub>X</sub>		- 40		dB
PSRR <sub>2</sub>	V <sub>BB</sub> Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D <sub>X</sub>		- 40		dB
PSRR <sub>3</sub>	V <sub>CC</sub> Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		- 40		dB
PSRR <sub>4</sub>	V <sub>BB</sub> Power Supply, Rejection Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		- 40		dB
CT <sub>TR</sub>	Crosstalk, Transmit to Receive, Single Ended Outputs	V <sub>FxI+</sub> = 0dBm0, 1.02kHz, D <sub>R</sub> = Lowest Positive Decode Level, Measure at PWRO+			- 80	dB
CT <sub>RT</sub>	Crosstalk, Receive to Transmit, Single Ended Outputs	D <sub>B</sub> = 0dBm0, 1.02kHz, V <sub>FxI+</sub> = GRDA, Measure at D <sub>X</sub>			- 80	dB

**Notes:**

1. 0dBm0 is defined as the zero reference point of the channel under test (OTLP). This corresponds to an analog signal input of 1.064 V<sub>rms</sub> or an output of 1.503 V<sub>rms</sub> ( $\mu$ Law) dual 1.068 V<sub>rms</sub> or a output 1.516 V<sub>rms</sub> (A-Law)
2. Unity gain input amplifier : GS<sub>X</sub> is connected to V<sub>FxI</sub>, Signal input V<sub>FxI+</sub>; Maximum gain output amplifier: GS<sub>R</sub> is connected to PWRO, output to PWRO+.
3. Noise free: DX PCM Code stable at 01010101.

## A.C. CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DISTORTION						
SD1 <sub>X</sub>	Transmit Signal to Distortion, $\mu$ -law Sinusoidal Input; CCITT G.712-method 2	$0 \leq VF_{X +} \leq -30\text{dBm0}$ – 40dBm0 – 45dBm0	36 30 25			dB dB dB
SD2 <sub>X</sub>	Transmit Signal to Distortion, A-law Sinusoidal Input, CCITT G.712-method 2	$0 \leq VF_{X +} \leq -30\text{dBm0}$ – 40dBm0 – 45dBm0	36 30 25			dB dB dB
SD1 <sub>R</sub>	Transmit Signal to Distortion, $\mu$ -law Sinusoidal Input, CCITT G.712-method 2	$0 \leq VF_{X +} \leq -30\text{dBm0}$ – 40dBm0 – 45dBm0	36 30 25			dB dB dB
SD2 <sub>R</sub>	Receive Signal to Distortion, A-law Sinusoidal Input; CCITT G.712-method 2	$0 \leq VF_{X +} \leq -30\text{dBm0}$ – 40dBm0 – 45dBm0	36 30 25			dB dB dB
DP <sub>X1</sub>	Transmit Single Frequency Distortion Products	AT & T Advisory # 64 (3.8) 0dBm0 Input Signal			– 46	dB
DP <sub>R1</sub>	Receive Single Frequency Distortion Products	AT & T Advisory # 64 (3.8) 0dBm0 Input Signal			– 46	dB
IMD <sub>1</sub>	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			– 35	dB
IMD <sub>2</sub>	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			– 49	dB
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			– 30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			– 40	dBm0
D <sub>AX</sub>	Transmit Absolute Delay	Fixed Data Rate CLK <sub>X</sub> = 2.048MHz, 0dBm0, 1.02kHz Signal at VF <sub>X +</sub> Measure at D <sub>X</sub>		300		$\mu\text{s}$
D <sub>DX</sub>	Transmit Differential Envelope Delay Relative to D <sub>AX</sub>	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		170 95 45 80		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$
D <sub>AR</sub>	Receive Absolute Delay	Fixed data rate, CLK <sub>R</sub> = 2.048MHz; Digital input is DMW codes. Measure at PWRO+			190	$\mu\text{s}$
D <sub>DR</sub>	Receive Differential Envelope Delay Relative to D <sub>AR</sub>	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		10 10 85 110		$\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$

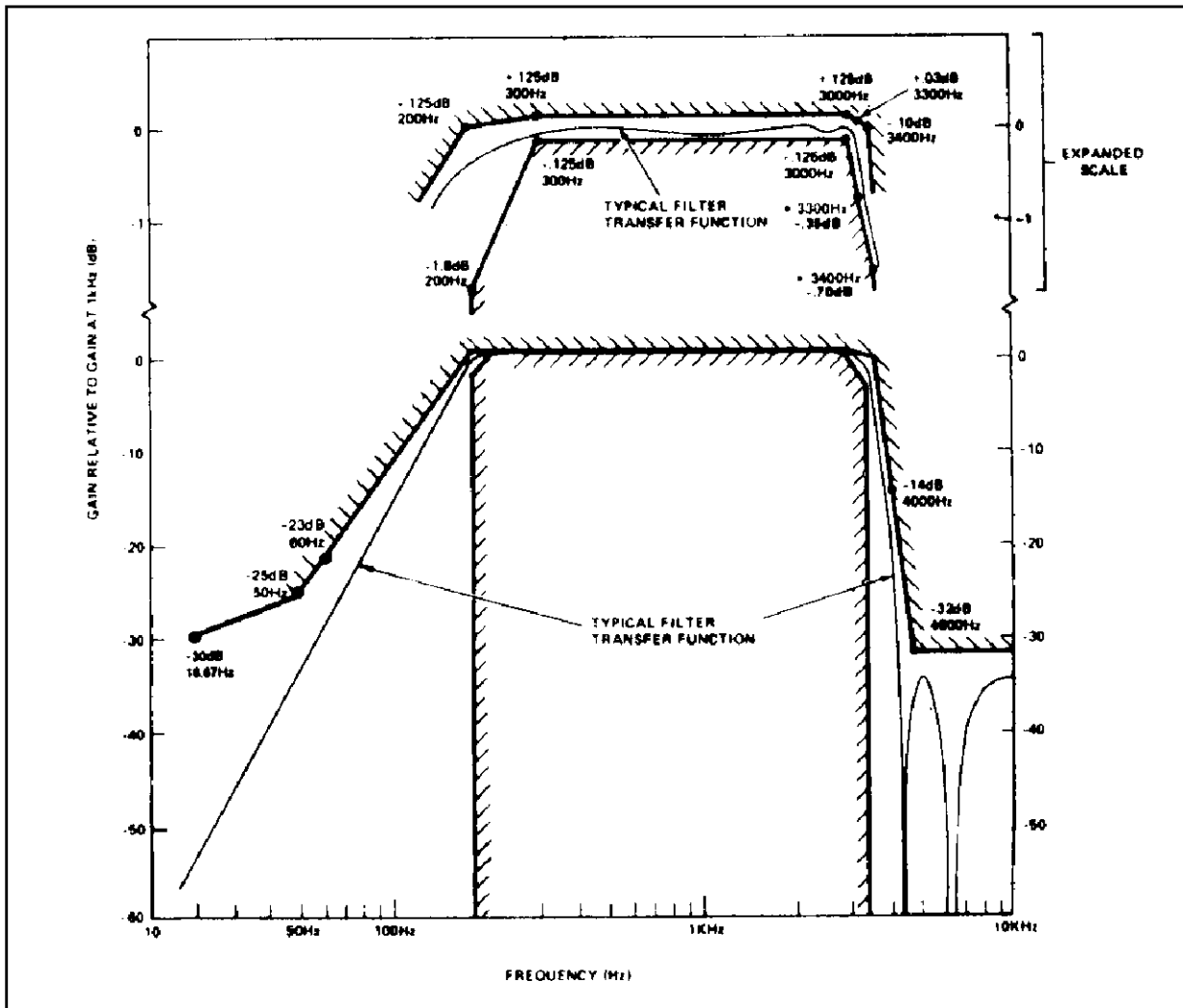
A.C. CHARACTERISTICS (continued)

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS

(Input amplifier is set for unity gain, noninverting; maximum gain output.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G <sub>RX</sub>	Gain Relative to Gain at 1.02 kHz	0 dBm <sub>0</sub> Signal Input at VF <sub>X1+</sub>				
	16.67Hz				- 30	dB
	50Hz				- 25	dB
	60Hz				- 23	dB
	200Hz		- 1.8		- 0.125	dB
	300 to 3000Hz		- 0.125		+ 0.125	dB
	3300Hz		- 0.35		+ 0.03	dB
	3400Hz		- 0.7		- 0.10	dB
	4000Hz				- 14	dB
	4600Hz and Above				- 32	dB

Figure 5: Transmit Filter

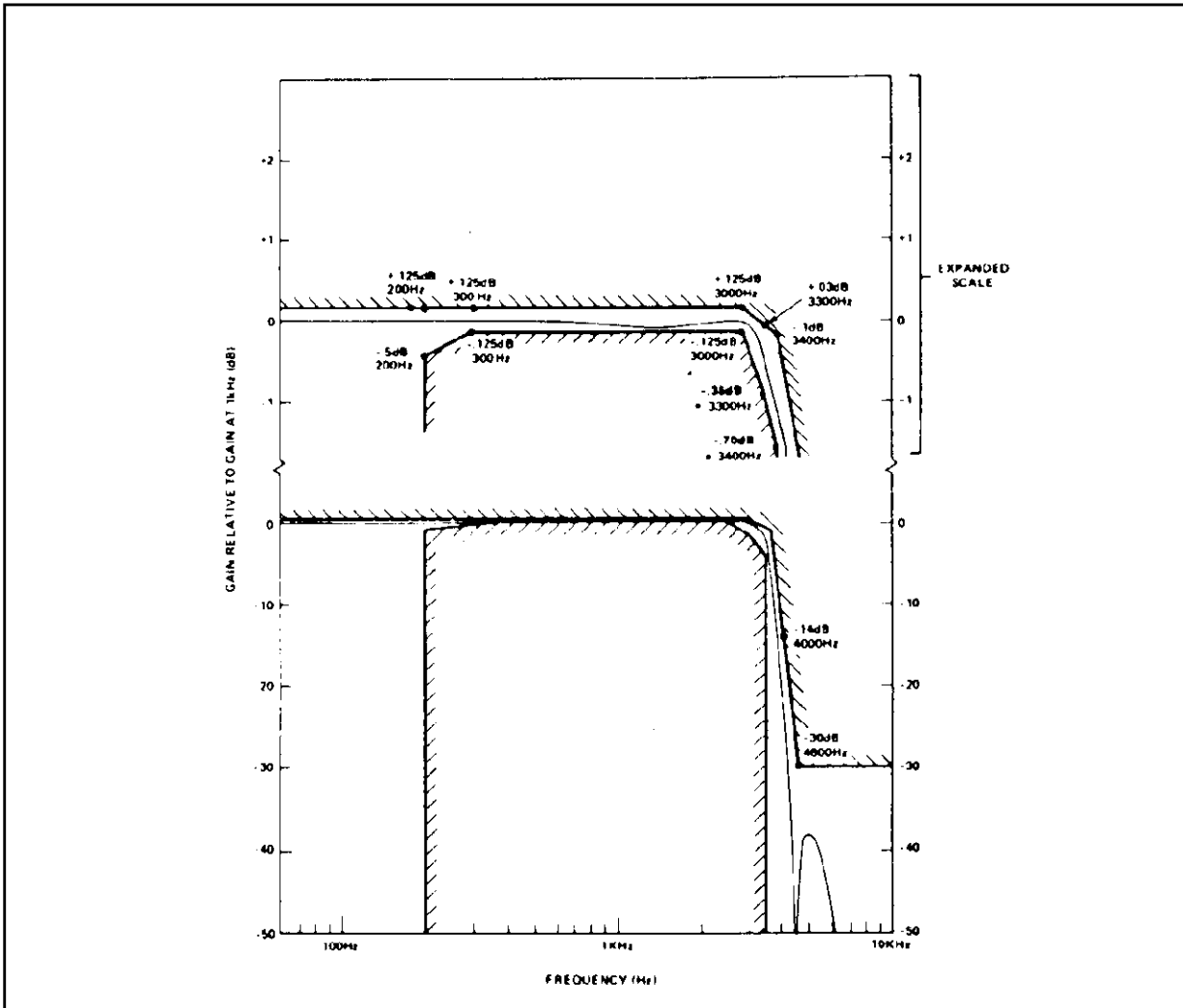


A.C. CHARACTERISTICS (continued)

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G <sub>RR</sub>	Gain Relative to Gain at 1.02kHz	0dBm0 Signal Input at D <sub>R</sub>				
	below 200Hz				+ 0.125	dB
	200Hz		- 0.5		+ 0.125	dB
	300 to 3000Hz		- 0.125		+ 0.125	dB
	3300Hz		- 0.35		+ 0.03	dB
	3400Hz		- 0.7		- 0.1	dB
	4000Hz				- 14	dB
	4600Hz and Above				- 30	dB

Figure 6: Receive Filter



## AC CHARACTERISTICS - TIMING PARAMETERS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>CLOCK SECTION</b>						
t <sub>CY</sub>	Clock Period, CLK <sub>X</sub> , CLK <sub>R</sub>	f <sub>CLKX</sub> = f <sub>CLKR</sub> = 2.048MHz	488			ns
t <sub>CLK</sub>	Clock Pulse Width	CLK <sub>X</sub> , CLK <sub>R</sub>	195			ns
t <sub>DCLK</sub>	Data Clock Pulse Width <sup>1</sup>	64kHz ≤ f <sub>DCLK</sub> ≤ 2.048MHz	195			ns
t <sub>CDC</sub>	Clock Duty Cycle	CLK <sub>X</sub> , CLK <sub>R</sub>	40	50	60	%
t <sub>r</sub> , t <sub>f</sub>	Clock Rise and Fall Time		5		30	ns
<b>TRANSMIT SECTION, FIXED DATA RATE MODE<sup>2</sup></b>						
t <sub>DX</sub>	Data Enabled on TS Entry	0 < C <sub>LOAD</sub> < 100pF	0		145	ns
t <sub>DDX</sub>	Data Delay from CLK <sub>X</sub>	0 < C <sub>LOAD</sub> < 100pF	0		145	ns
t <sub>HZ</sub>	Data Float on TS Exit	C <sub>LOAD</sub> = 0	60		190	ns
t <sub>SON</sub>	Timeslot X to Enable	0 < C <sub>LOAD</sub> < 100pF	0		145	ns
t <sub>SOFF</sub>	Timeslot X to Disable	C <sub>LOAD</sub> = 0	50		190	ns
t <sub>FSD</sub>	Frame Sync Delay		0		120	ns
t <sub>SS</sub>	Signal Setup Time		0			ns
t <sub>SH</sub>	Signal Setup Time		0			ns
<b>RECEIVE SECTION, FIXED DATA RATE MODE</b>						
t <sub>DSR</sub>	Receive Data Setup		10			ns
t <sub>DHR</sub>	Receive Data Hold		60			ns
t <sub>FSD</sub>	Frame Sync Delay		0		120	ns
t <sub>SIGR</sub>	SIG <sub>R</sub> Update		0		2	μs
<b>TRANSMIT SECTION, FIXED DATA RATE MODE<sup>2</sup></b>						
t <sub>TSDX</sub>	Timeslot Delay from DCLK <sub>X</sub>		-80		80	ns
t <sub>FSD</sub>	Frame Sync Delay		0		120	ns
t <sub>DDX</sub>	Data Delay from DCLK <sub>X</sub>	0 < C <sub>LOAD</sub> < 100pF	0		100	ns
t <sub>DON</sub>	Timeslot to D <sub>X</sub> Active	0 < C <sub>LOAD</sub> < 100pF	0		50	ns
t <sub>DOFF</sub>	Timeslot to D <sub>X</sub> Inactive	0 < C <sub>LOAD</sub> < 100pF	0		80	ns
f <sub>DX</sub>	Data Clock Frequency		64		2048 <sup>1</sup>	KHz
t <sub>DFSX</sub>	Data Delay from FS <sub>X</sub>	t <sub>TSDX</sub> = 80ns	0		140	ns
<b>RECEIVE SECTION, FIXED DATA RATE MODE</b>						
t <sub>TSDR</sub>	Timeslot Delay from DCLK <sub>R</sub>		-80		80	ns
t <sub>FSD</sub>	Frame Sync Delay		0		120	ns
t <sub>DSR</sub>	Receive Data Setup Time		10			ns
t <sub>DHR</sub>	Receive Data Hold Time		60			ns
t <sub>DR</sub>	Data Clock Frequency		64		2048 <sup>1</sup>	KHz
t <sub>SER</sub>	Timeslot End Receive Time		0			ns
<b>64KB OPERATION, VARIABLE DATA RATE MODE</b>						
t <sub>FSLX</sub>	Transmit Frame Sync Minimum Downtime	FS <sub>X</sub> is TTL high for remainder of frame	488			ns
t <sub>FSLR</sub>	Receive Frame Sync Minimum Downtime	FS <sub>R</sub> is TTL high for remainder of frame	1952			ns
t <sub>DCLK</sub>	Data Clock Pulse Width		10			μs

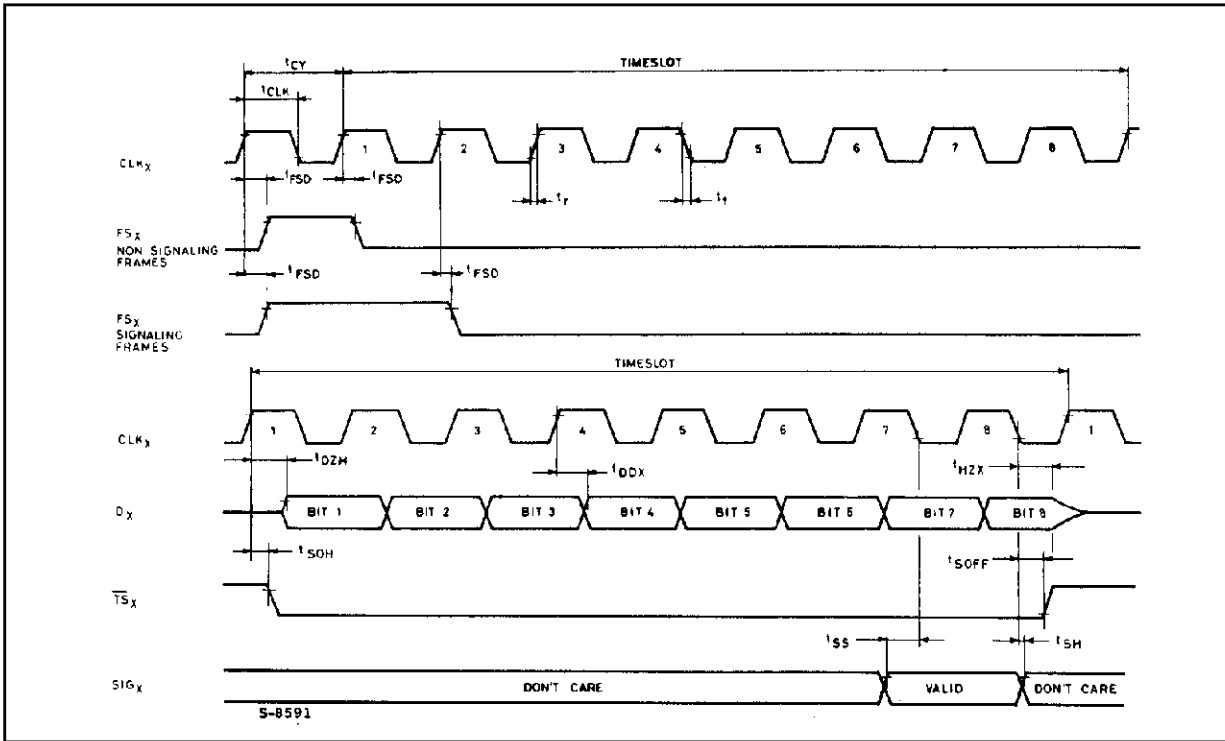
**Notes:**

1. Devices are available which operate at data rates up to 4.096MHz; the minimum data clock pulse width for these devices is 110ns
2. Timing parameters t<sub>BZX</sub>, t<sub>HZX</sub>, and t<sub>SOFF</sub> are referenced to a high impedance state.

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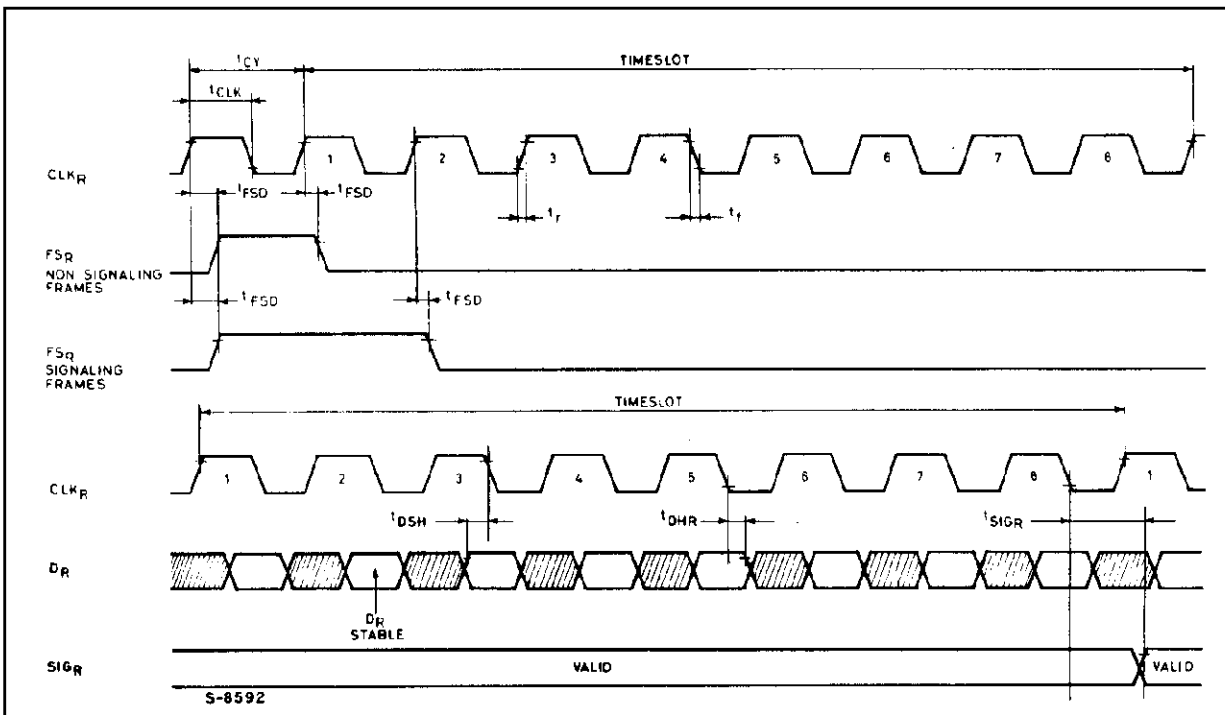
## WAVEFORMS:

### Fixed Data Rate Timing - Transmit Timing



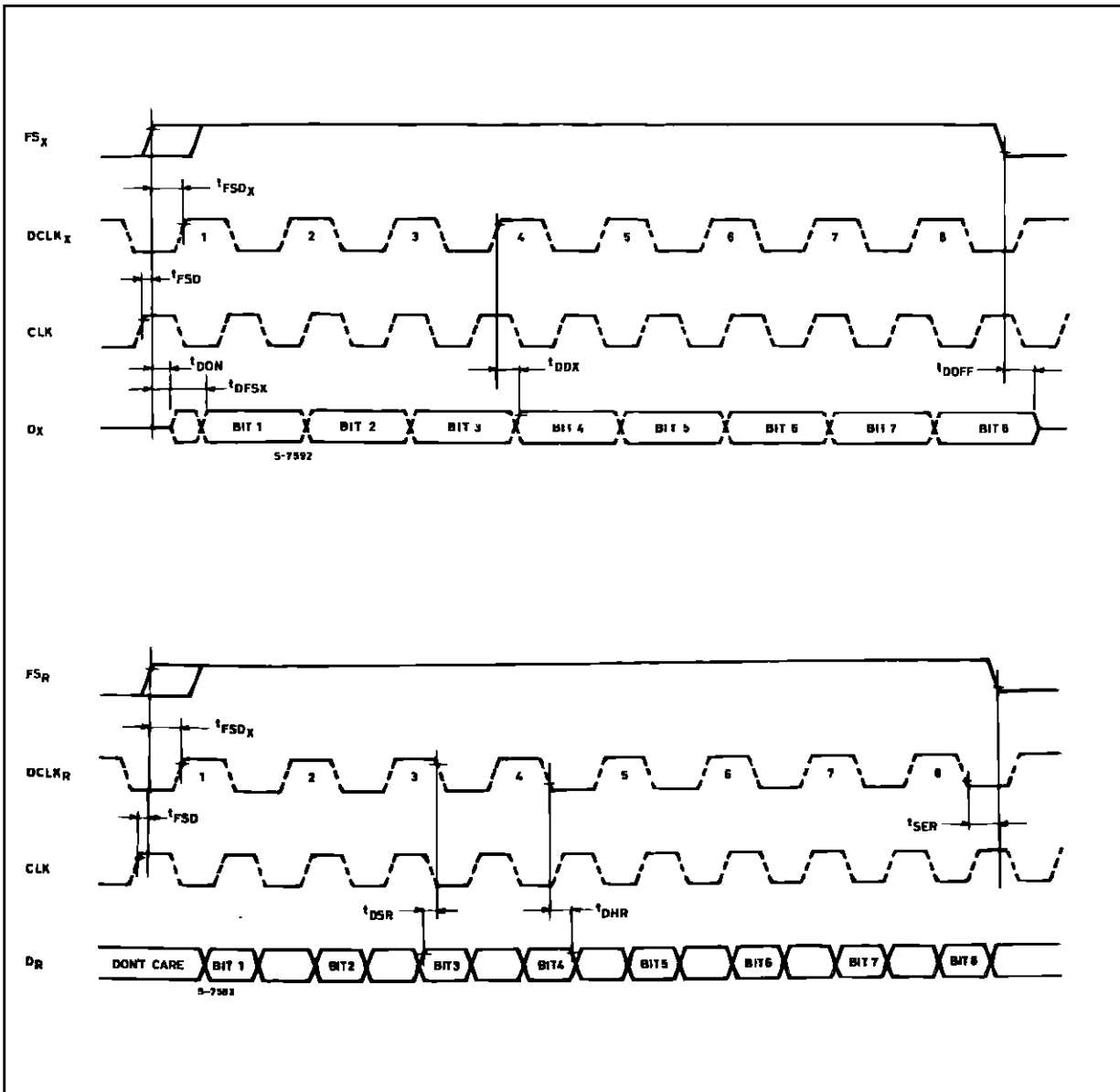
NOTE: All timing parameters referenced to V<sub>IH</sub> and V<sub>IL</sub> except t<sub>DZX</sub>, t<sub>SOFF</sub> and t<sub>HZX</sub> which reference a high impedance state.

### Receive Timing

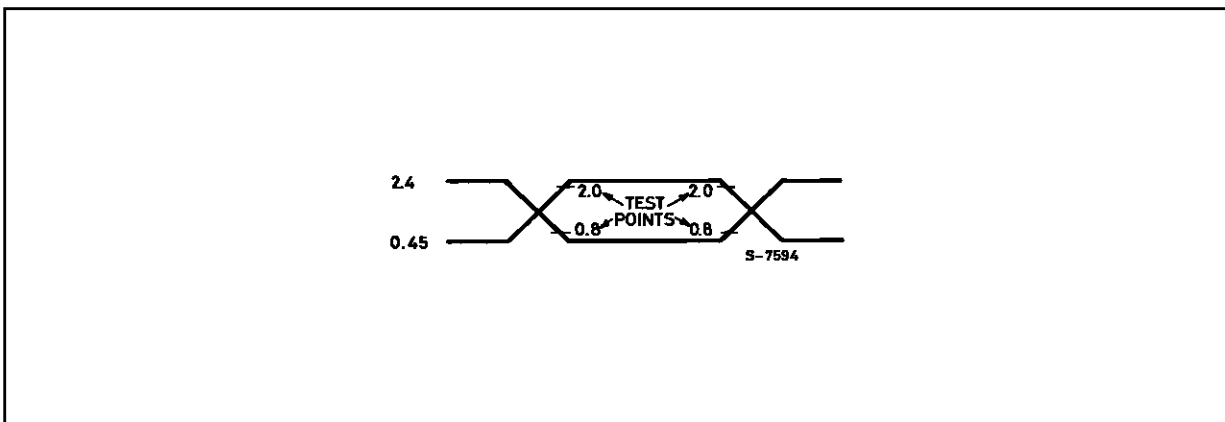


NOTE: All timing parameters referenced to V<sub>IH</sub> and V<sub>IL</sub>.

VARIABLE DATA RATE TIMING



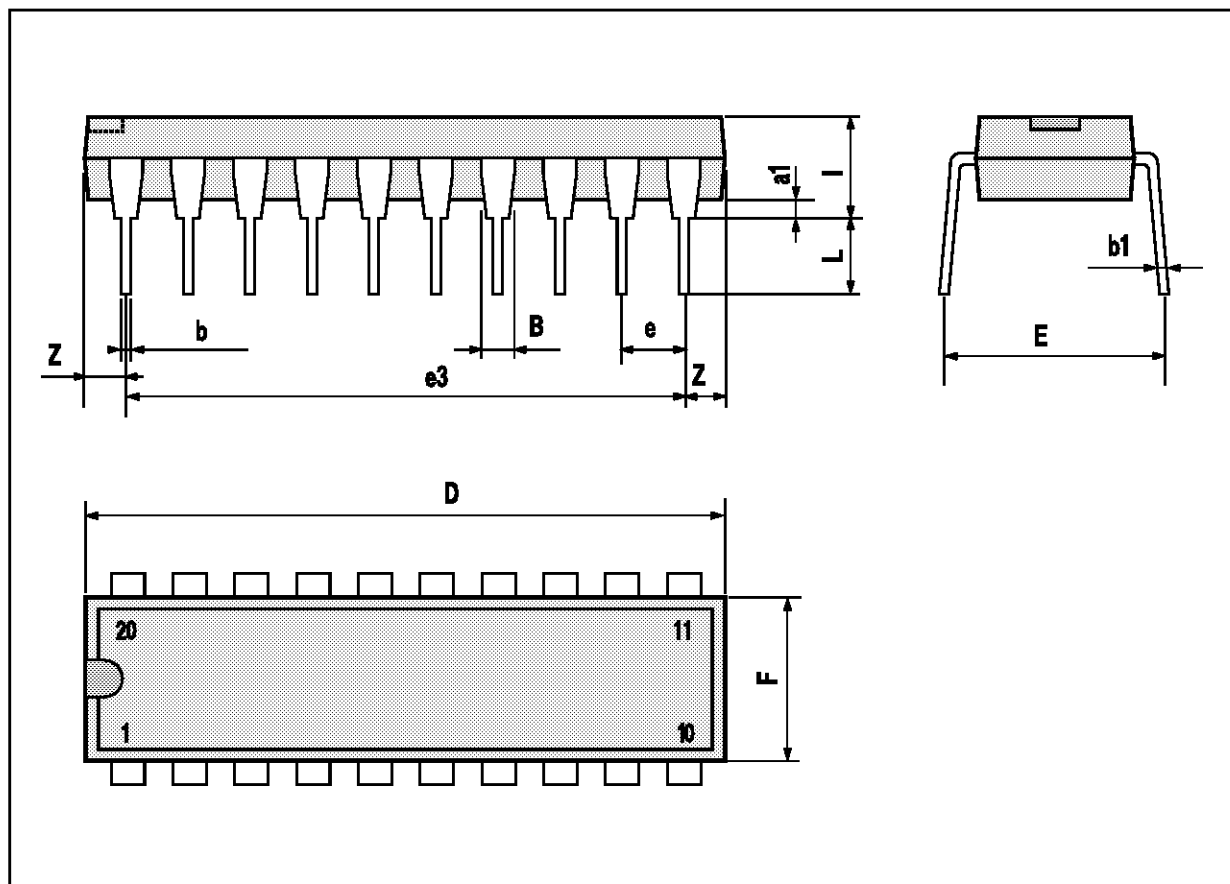
AC Timing Input, Output Waveform



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## DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
l			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053





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