

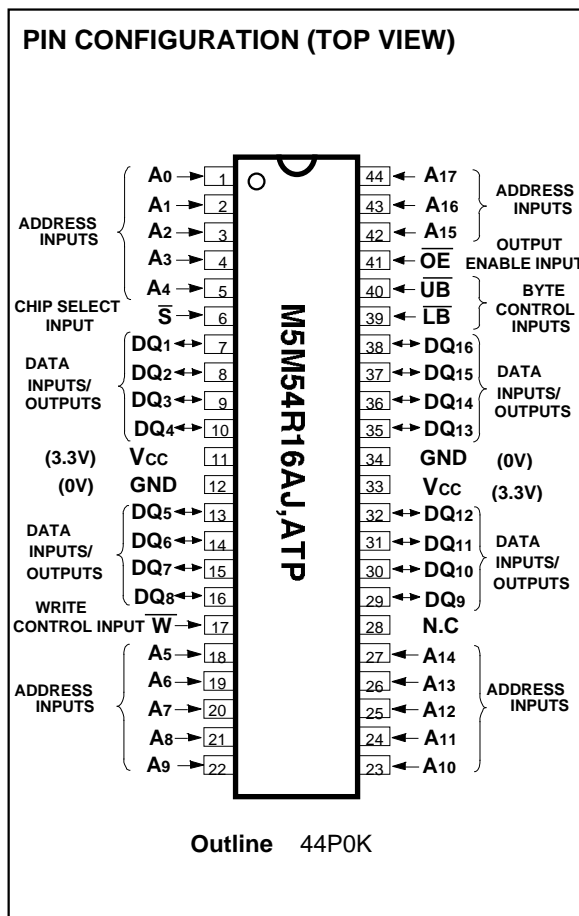
## DESCRIPTION

The M5M54R16A is a family of 262144-word by 16-bit static RAMs, fabricated with the high performance CMOS process and designed for high speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible.

They include a power down feature as well. In write and read cycles, the lower and upper bytes are able to be controlled either together or separately by  $\overline{LB}$  and  $\overline{UB}$ .

## FEATURES

- Fast access time
  - M5M54R16AJ,ATP-10 ... 10ns(max)
  - M5M54R16AJ,ATP-12 ... 12ns(max)
  - M5M54R16AJ,ATP-15 ... 15ns(max)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by  $\overline{S}$
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs
- Separate control of lower and upper bytes by  $\overline{LB}$  and  $\overline{UB}$



## APPLICATION

High-speed memory system

## FUNCTION

The operation mode of the M5M54R16A is determined by a combination of the device control inputs  $\overline{S}$ ,  $\overline{W}$ ,  $\overline{OE}$ ,  $\overline{LB}$ , and  $\overline{UB}$ . Each mode is summarized in the function table.

A write cycle is executed whenever the low level  $\overline{W}$  overlaps with low level  $\overline{LB}$  and/or low level  $\overline{UB}$  and low level  $\overline{S}$ . The address must be set-up before write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of  $\overline{W}$ ,  $\overline{LB}$ ,  $\overline{UB}$  or  $\overline{S}$ , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input  $\overline{OE}$  directly controls the output stage. Setting the  $\overline{OE}$  at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting  $\overline{W}$  at a high level and  $\overline{OE}$  at a low level while  $\overline{LB}$  and/or  $\overline{UB}$  and  $\overline{S}$  are in an active

## PACKAGE

- M5M54R16AJ ..... 44pin 400mil SOJ
- M5M54R16ATP ..... 44pin 400mil TSOP(II)

state. ( $\overline{LB}$  and/or  $\overline{UB}$ =L,  $\overline{S}$ =L)

When setting  $\overline{LB}$  at a high level and other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enable, and lower-Byte are in a non-selectable mode. And when setting  $\overline{UB}$  at a high level and other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enable, and upper-Byte are in a non-selectable mode.

When setting  $\overline{LB}$  and  $\overline{UB}$  at a high level or  $\overline{S}$  at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\overline{LB}$ ,  $\overline{UB}$  and  $\overline{S}$ .

Signal- $\overline{S}$  controls the power-down feature. When  $\overline{S}$  goes high, power dissipation is reduced extremely. The access time from  $\overline{S}$  is equivalent to the address access time.

# MITSUBISHI LSIs

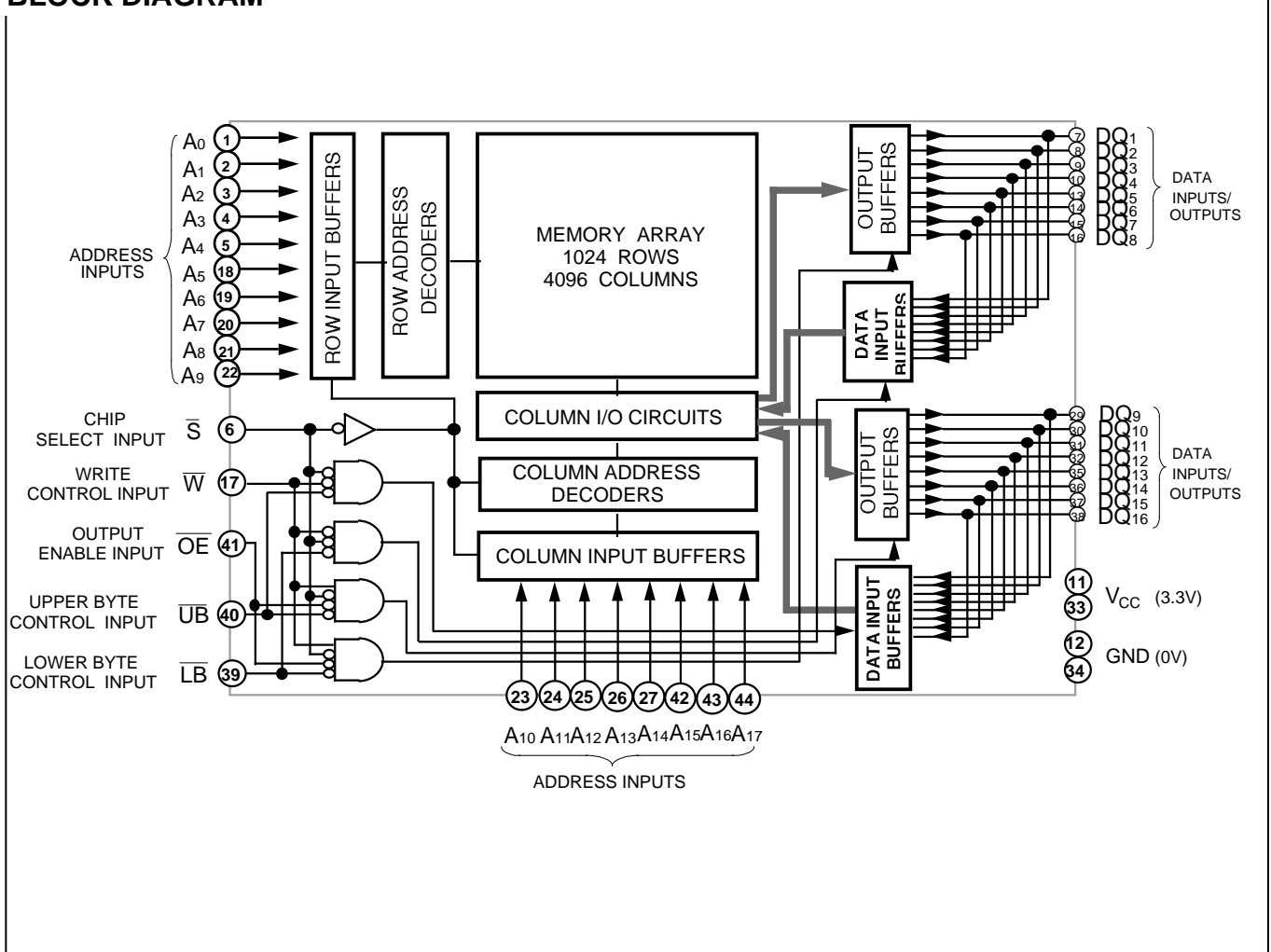
## M5M54R16AJ, ATP-10, -12, -15

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

### FUNCTION TABLE

S	$\overline{W}$	OE	$\overline{LB}$	UB	Mode	DQ1~8	DQ9~16	I <sub>cc</sub>
L	H	L	L	L	Read cycle All Bytes	D <sub>OUT</sub>	D <sub>OUT</sub>	Active
L	H	L	H	L	Read cycle Upper Bytes	High-impedance	D <sub>OUT</sub>	Active
L	H	L	L	H	Read cycle Lower Bytes	D <sub>OUT</sub>	High-impedance	Active
L	L	X	L	L	Write cycle All Bytes	D <sub>IN</sub>	D <sub>IN</sub>	Active
L	L	X	H	L	Write cycle Upper Bytes	High-impedance	D <sub>IN</sub>	Active
L	L	X	L	H	Write cycle Lower Bytes	D <sub>IN</sub>	High-impedance	Active
L	H	H	X	X	Output disable	High-impedance	High-impedance	Active
L	X	X	H	H				
H	X	X	X	X	Non selection	High-impedance	High-impedance	Stand by

### BLOCK DIAGRAM



# MITSUBISHI LSIs

## M5M54R16AJ,ATP-10,-12,-15

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		- 2.0* ~ 4.6	V
V <sub>I</sub>	Input voltage	With respect to GND	- 2.0* ~ V <sub>CC</sub> +0.5	V
V <sub>O</sub>	Output voltage		- 2.0* ~ V <sub>CC</sub>	V
P <sub>d</sub>	Power dissipation		T <sub>a</sub> =25°C	1000
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg(bias)</sub>	Storage temperature(bias)		- 10 ~ 85	°C
T <sub>stg</sub>	Storage temperature		- 65 ~ 150	°C

\*Pulse width  $\leq 3$ ns, In case of DC: - 0.5V

### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0~70°C, V<sub>CC</sub>=3.3V <sup>+10%</sup> <sub>-5%</sub>, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.0		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage				0.8	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = - 4mA	2.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 8mA			0.4	V
I <sub>I</sub>	Input current	V <sub>I</sub> = 0 ~ V <sub>CC</sub>			2	μA
I <sub>OZ</sub>	Output current in off-state	V <sub>I</sub> ( $\bar{s}$ ) = V <sub>IH</sub> V <sub>O</sub> = 0 ~ V <sub>CC</sub>			2	μA
I <sub>CC1</sub>	Active supply current (TTL level)	V <sub>I</sub> ( $\bar{s}$ ) = V <sub>IL</sub> other inputs V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	AC(10ns cycle)		260	mA
			AC(12ns cycle)		250	
			AC(15ns cycle)		230	
			DC		120	
I <sub>CC2</sub>	Stand-by supply current (TTL level)	V <sub>I</sub> ( $\bar{s}$ ) = V <sub>IH</sub>	AC(10ns cycle)		90	mA
			AC(12ns cycle)		70	
			AC(15ns cycle)		60	
			DC		40	
I <sub>CC3</sub>	Stand-by current (MOS level)	V <sub>I</sub> ( $\bar{s}$ ) = V <sub>CC</sub> - 0.2V other inputs V <sub>I</sub> 0.2V or V <sub>I</sub> V <sub>CC</sub> - 0.2V			10	mA

Note 1: Direction for current flowing into an IC is positive (no mark).

### CAPACITANCE (T<sub>a</sub>=0~70°C, V<sub>CC</sub>=3.3V <sup>+10%</sup> <sub>-5%</sub>, unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>i</sub> =25mVrms, f=1MHz			7	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>o</sub> =25mVrms, f=1MHz			8	pF

Note 2: C<sub>I</sub>, C<sub>O</sub> are periodically sampled and are not 100% tested.

### AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>= 0~70 °C, V<sub>CC</sub>=3.3V <sup>+10%</sup> <sub>-5%</sub>, unless otherwise noted)

#### (1) MEASUREMENT CONDITION

Input pulse levels ..... V<sub>IH</sub>=3.0V, V<sub>IL</sub>=0.0V  
 Input rise and fall time ..... 3ns  
 Input timing reference levels ..... V<sub>IH</sub>=1.5V, V<sub>IL</sub>=1.5V  
 Output timing reference levels ..... V<sub>OH</sub>=1.5V, V<sub>OL</sub>=1.5V  
 Output loads ..... Fig1 ,Fig2

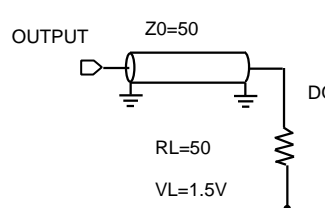


Fig.1 Output load

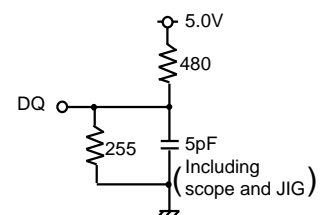


Fig.2 Output load for t<sub>en</sub>, t<sub>dis</sub>

MITSUBISHI LSIs  
**M5M54R16AJ,ATP-10,-12,-15**

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

**READ CYCLE**

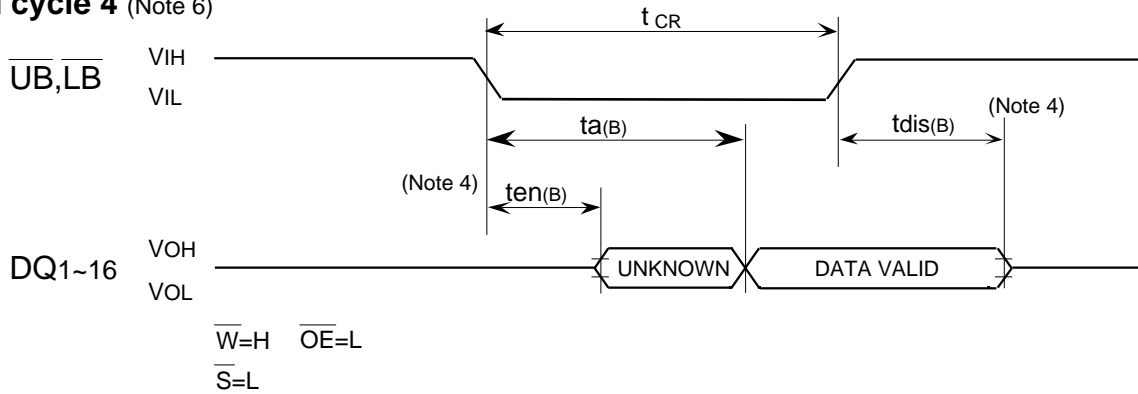
Symbol	Parameter	Limits						Unit
		M5M54R16AJ,ATP-10		M5M54R16AJ,ATP-12		M5M54R16AJ,ATP-15		
		Min	Max	Min	Max	Min	Max	
t <sub>CR</sub>	Read cycle time	10		12		15		ns
t <sub>a(A)</sub>	Address access time		10		12		15	ns
t <sub>a(S)</sub>	Chip select access time		10		12		15	ns
t <sub>a(OE)</sub>	Output enable access time		5		6		7	ns
t <sub>a(B)</sub>	LB,UB access time		5		6		7	ns
t <sub>dis(S)</sub>	Output disable time after $\overline{S}$ high	0	5	0	6	0	7	ns
t <sub>dis(OE)</sub>	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
t <sub>dis(B)</sub>	Output disable time after $\overline{LB},\overline{UB}$ high	0	5	0	6	0	7	ns
t <sub>en(S)</sub>	Output enable time after $\overline{S}$ low	2		3		3		ns
t <sub>en(OE)</sub>	Output enable time after $\overline{OE}$ low	0		1		1		ns
t <sub>en(B)</sub>	Output enable time after $\overline{LB},\overline{UB}$ low	0		1		1		ns
t <sub>v(A)</sub>	Data valid time after address change	2		3		3		ns
t <sub>PU</sub>	Power-up time after chip selection	0		0		0		ns
t <sub>PD</sub>	Power-down time after chip selection		10		12		15	ns

**Write cycle**

Symbol	Parameter	Limits						Unit
		M5M54R16AJ,ATP-10		M5M54R16AJ,ATP-12		M5M54R16AJ,ATP-15		
		Min	Max	Min	Max	Min	Max	
t <sub>cw</sub>	Write cycle time	10		12		15		ns
t <sub>w(W)</sub>	Write pulse width ( $\overline{OE}$ low)	10		12		15		ns
t <sub>w(W)</sub>	Write pulse width( $\overline{OE}$ high)	8		10		10		ns
t <sub>su(B)</sub>	$\overline{LB},\overline{UB}$ setup time	8		10		10		ns
t <sub>su(A)1</sub>	Address setup time( $\overline{W}$ )	0		0		0		ns
t <sub>su(A)2</sub>	Address setup time( $\overline{S}$ )	0		0		0		ns
t <sub>su(S)</sub>	Chip select setup time	8		10		10		ns
t <sub>su(D)</sub>	Data setup time	5		6		7		ns
t <sub>h(D)</sub>	Data hold time	0		0		0		ns
t <sub>rec(W)</sub>	Write recovery time	1		1		1		ns
t <sub>dis(W)</sub>	Output disable time after $\overline{W}$ low	0	5	0	6	0	7	ns
t <sub>dis(OE)</sub>	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
t <sub>en(W)</sub>	Output enable time after $\overline{W}$ high	0		0		0		ns
t <sub>en(OE)</sub>	Output enable time after $\overline{OE}$ low	0		0		0		ns
t <sub>en(B)</sub>	Output enable time after $\overline{LB},\overline{UB}$ low	0		0		0		ns
t <sub>su(A-<math>\overline{WH}</math>)</sub>	Address to $\overline{W}$ High	8		10		10		ns
t <sub>su(A-<math>\overline{SH}</math>)</sub>	Address to $\overline{S}$ High	8		10		10		ns
t <sub>su(A-<math>\overline{BH}</math>)</sub>	Address to $\overline{LB},\overline{UB}$ High	8		10		10		ns

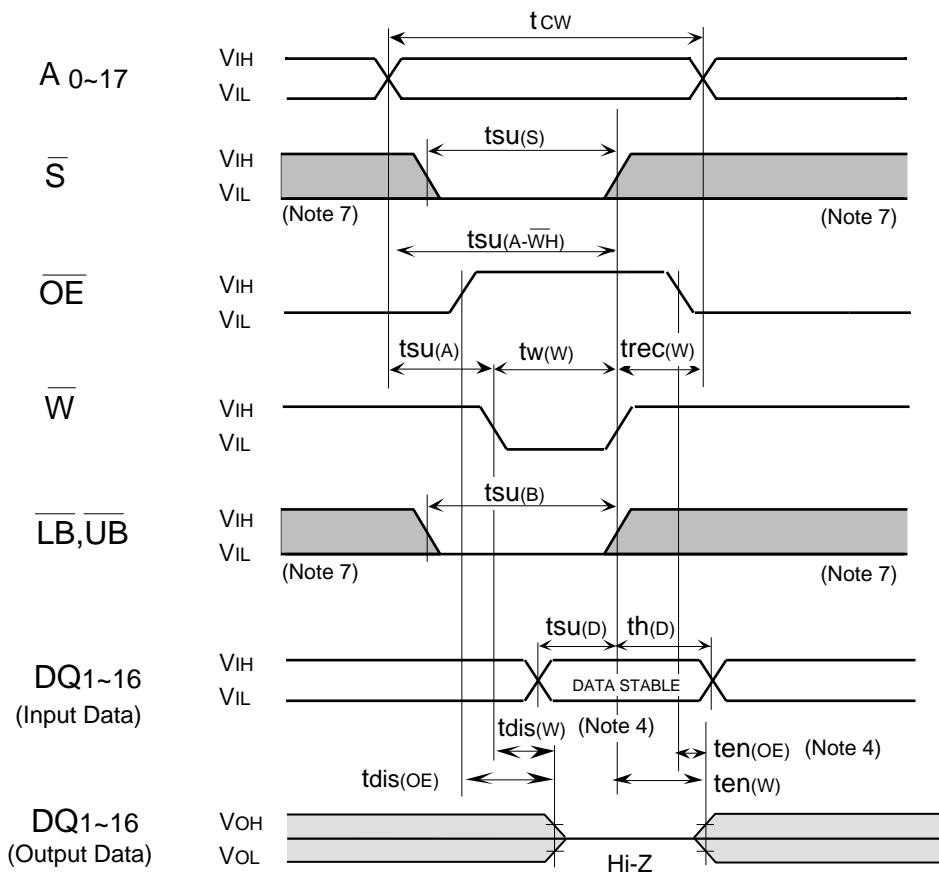


**Read cycle 4** (Note 6)



Note 6. Addresses,  $\overline{S}$  and  $\overline{OE}$  valid prior to  $\overline{LB}, \overline{UB}$  transition low by  $(t_{a(A)}-t_{a(B)})$ ,  $(t_{a(S)}-t_{a(B)})$ ,  $(t_{a(OE)}-t_{a(B)})$ .

**Write cycle ( $\overline{W}$  control mode)**

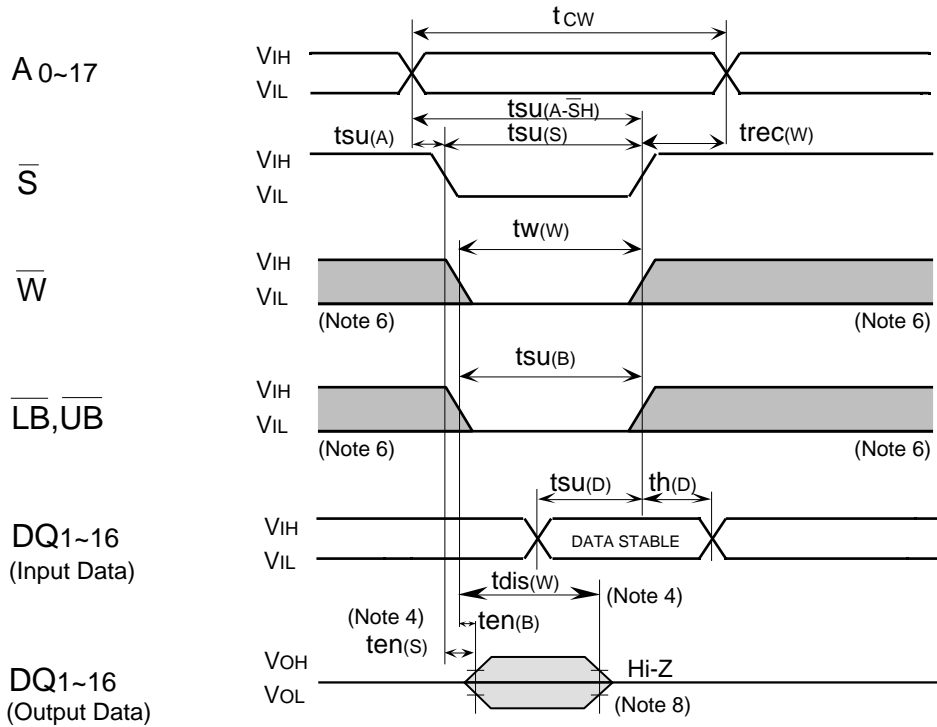


Note 7: Hatching indicates the state is don't care.

8: When the falling edge of  $\overline{W}$  is simultaneous or prior to the falling edge of  $\overline{S}$ , the output is maintained in the high impedance.

9:  $t_{en}, t_{dis}$  are periodically sampled and are not 100% tested.

**Write cycle ( $\overline{S}$  control)**



**Write cycle ( $\overline{LB}, \overline{UB}$  control)**

