

DESCRIPTION

The M5M5V208AKV is low voltage 2-Mbit static RAMs organized as 262,144-words by 8-bit, fabricated by high-performance 0.25µm CMOS technology.

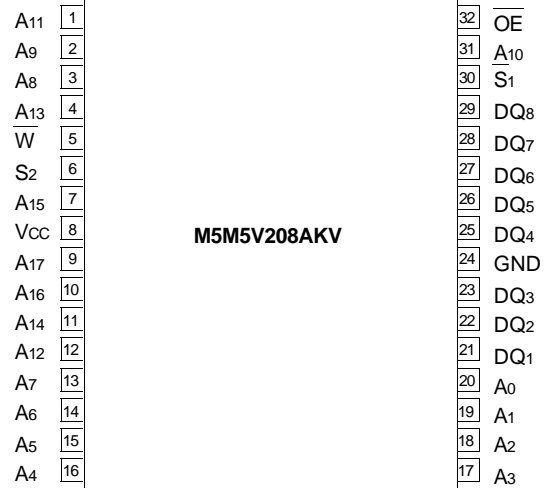
The M5M5V208AKV is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The M5M5V208AKV is packaged in 32-pin 8mm x 13.4mm sTSSOP packages which is a high reliability and high density surface mount device.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M5V208AKV-55HI	55ns	35mA (10MHz)	30µA (V _{CC} =3.6V)
M5M5V208AKV-70HI	70ns	7mA (1MHz)	0.3µA (V _{CC} =3.0V TYPICAL)

PIN CONFIGURATION (TOP VIEW)



Outline 32P3K-B(KV)

- Single 2.7 ~3.6V power supply
- No clock, No refresh
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by S1,S2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- OE prevents data contention in the I/O bus
- Common data I/O
- Package
M5M5V208AKV 32pin 8 X 13.4 mm² sTSSOP

FUNCTION

The operation mode of the M5M5V208AKV series are determined by a combination of the device control inputs $\overline{S_1}$, S_2 , \overline{W} and \overline{OE} .

Each mode is summarized in the function table.

A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}=L, S_2=H$).

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

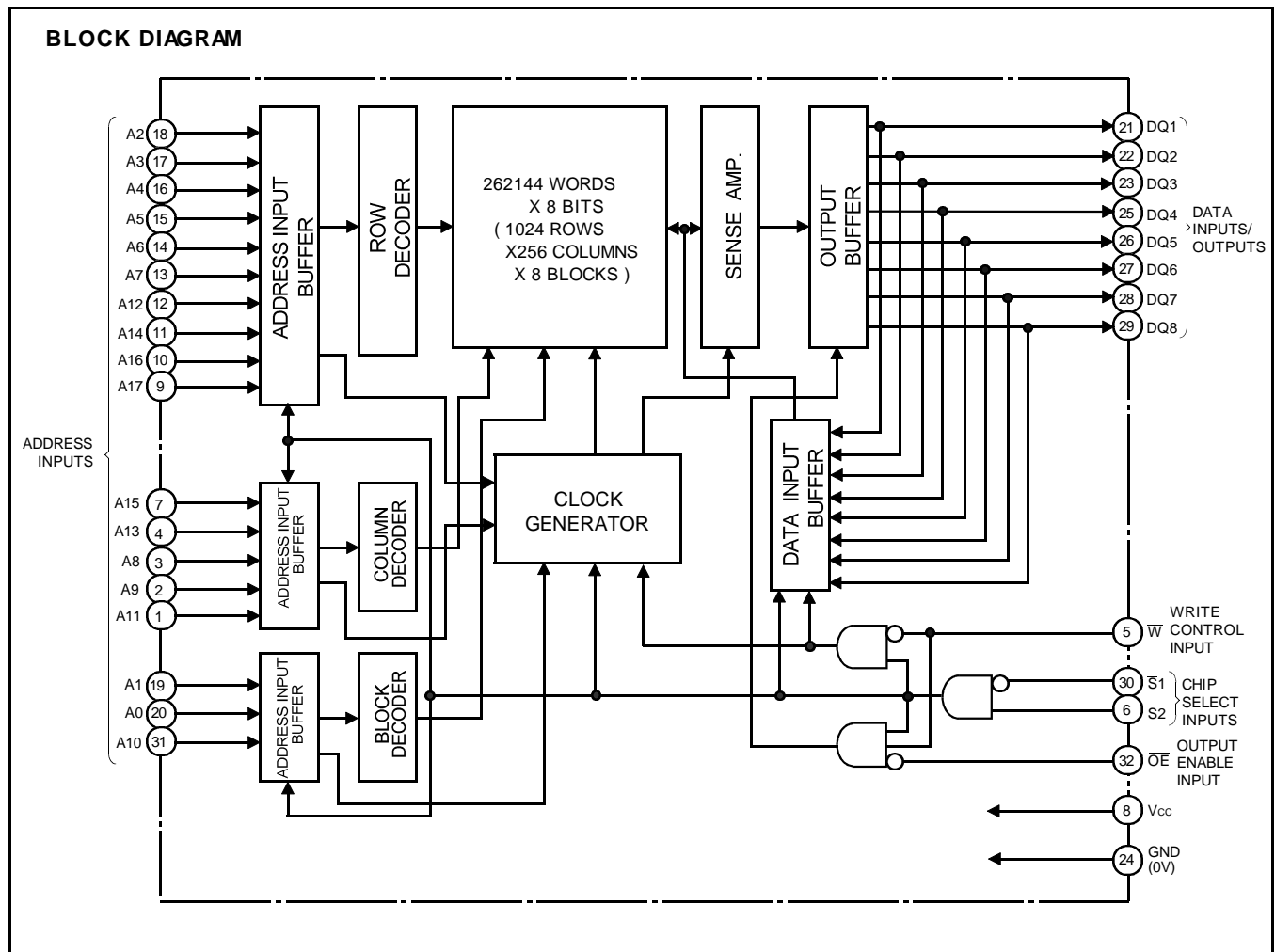
FUNCTION TABLE

$\overline{S_1}$	S_2	\overline{W}	\overline{OE}	Mode	DQ	I_{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H	—	High-impedance	Active

Note 1: "H" and "L" in this table mean V_{IH} and V_{IL} , respectively.

2: "X" in this table should be "H" or "L".

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	- 0.5*~4.6	V
V _I	Input voltage		- 0.5*~V _{CC} + 0.3	V
V _O	Output voltage		0~V _{CC}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		- 40~85	°C
T _{stg}	Storage temperature		- 65~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (T_a= -40~85°C, V_{CC}=2.7~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.6	V
V _{OH1}	High-level output voltage 1	I _{OH} = - 0.5mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} = - 0.05mA	V _{CC} - 0.5			V
V _{OL}	Low-level output voltage	I _{OL} = 2mA			0.4	V
I _I	Input current	V _I =0~V _{CC}			±1	μA
I _O	Output current in off-state	S ₁ =V _{IH} or S ₂ =V _{IL} or OE=V _{IH} V _{I/O} =0~V _{CC}			±1	μA
I _{CC1}	Active supply current (CMOS-level input)	S ₁ ≤ 0.2V, S ₂ ≥ V _{CC} -0.2V other inputs ≤ 0.2V or ≥ V _{CC} -0.2V, Output-open	10MHz	28	30	mA
			1MHz	5	7	
I _{CC2}	Active supply current (TTL-level input)	S ₁ =V _{IL} , S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} , Output-open	10MHz	33	35	mA
			1MHz	5	7	
I _{CC3}	Stand-by current	1) S ₂ ≤ 0.2V, other inputs=0 ~ V _{CC} 2) S ₁ ≥ V _{CC} - 0.2V, S ₂ ≥ V _{CC} - 0.2V other inputs=0 ~ V _{CC}	~25°C	0.3	2	μA
			~40°C		5	
			~70°C		10	
			~85°C		30	
I _{CC4}	Stand-by current	1) S ₁ =V _{IH} , other inputs=V _{IL} or V _{IH} 2) S ₂ =V _{IL} , other inputs=V _{IL} or V _{IH}			0.33	mA

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (T_a= -40~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	pF

Note 3: Direction for current flowing into an IC is positive (no mark).

4: Typical value is V_{CC} = 3V, T_a = 25°C

AC ELECTRICAL CHARACTERISTICS (Ta=- 40~85°C, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

VCC 2.7~3.6V
 Input pulse level VIH=2.2V, VIL=0.4V
 Input rise and fall time... 5ns
 Reference level V_{OH}=V_{OL}=1.5V
 Output loads Fig.1, C_L=30pF
 C_L=5pF (for t_{en}, t_{dis})
 Transition is measured ± 500mV from steady state voltage. (for t_{en}, t_{dis})

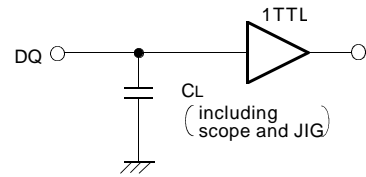


Fig.1 Output load

(2) READ CYCLE

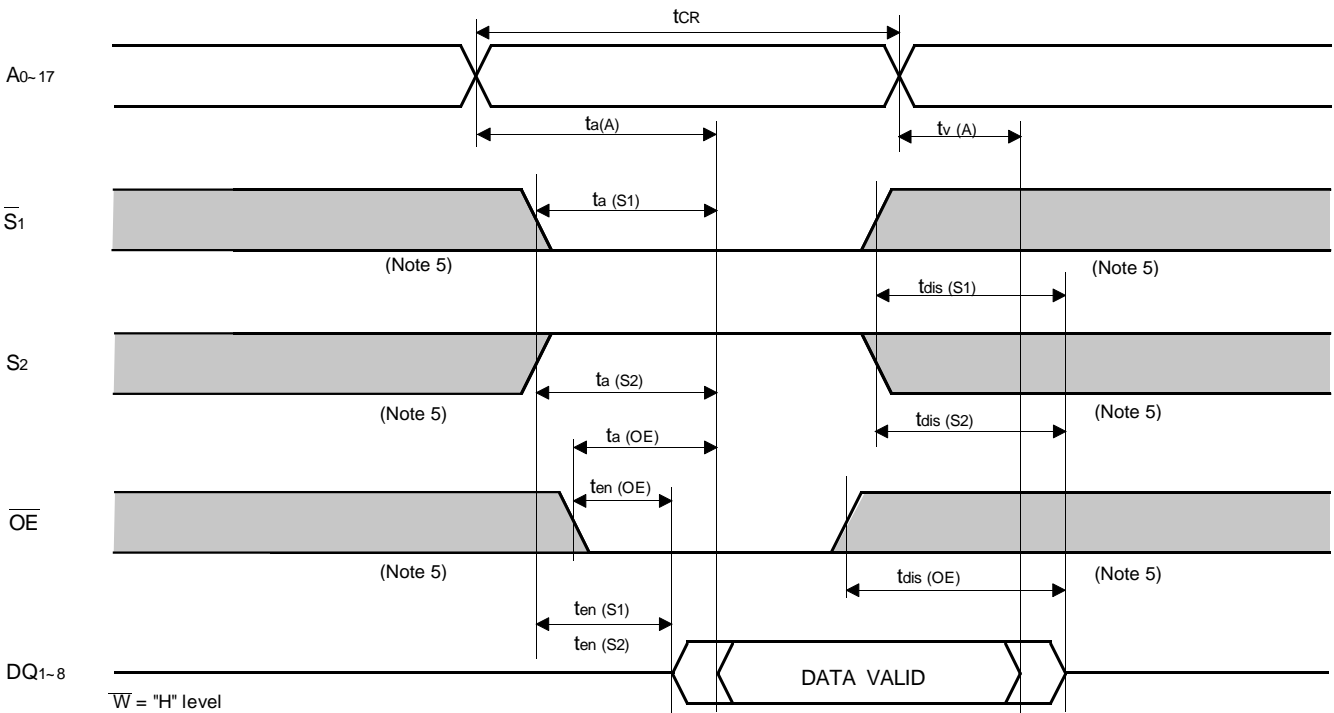
Symbol	Parameter	Limits				Unit
		-55HI		-70HI		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	55		70		ns
t _{a(A)}	Address access time		55		70	ns
t _{a(S1)}	Chip select 1 access time		55		70	ns
t _{a(S2)}	Chip select 2 access time		55		70	ns
t _{a(OE)}	Output enable access time		30		35	ns
t _{dis(S1)}	Output disable time after $\overline{S1}$ high		20		25	ns
t _{dis(S2)}	Output disable time after $S2$ low		20		25	ns
t _{dis(OE)}	Output disable time after \overline{OE} high		20		25	ns
t _{en(S1)}	Output enable time after $\overline{S1}$ low	10		10		ns
t _{en(S2)}	Output enable time after $S2$ high	10		10		ns
t _{en(OE)}	Output enable time after \overline{OE} low	5		5		ns
t _{V(A)}	Data valid time after address	10		10		ns

(3) WRITE CYCLE

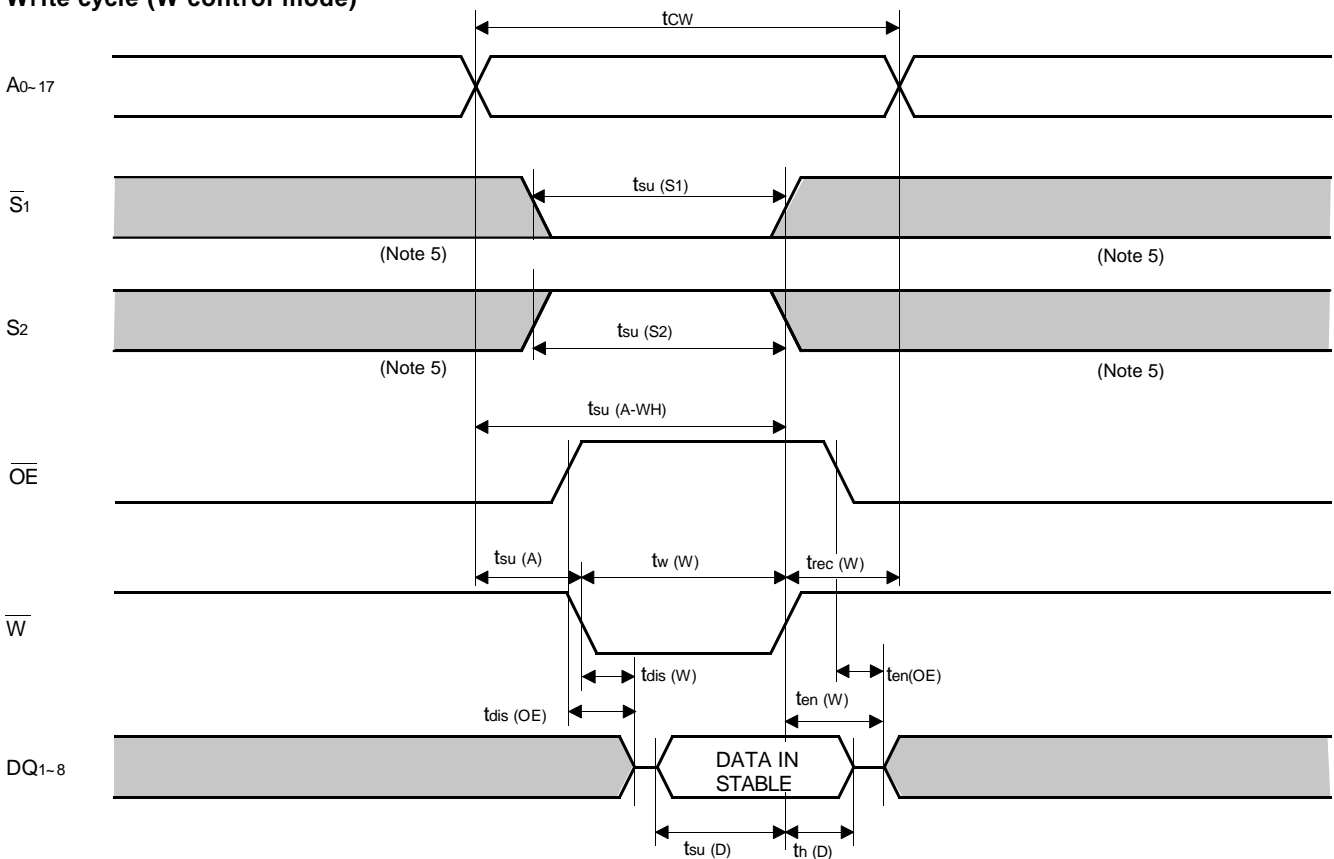
Symbol	Parameter	Limits				Unit
		-55HI		-70HI		
		Min	Max	Min	Max	
t _{cw}	Write cycle time	55		70		ns
t _{w(W)}	Write pulse width	45		55		ns
t _{su(A)}	Address setup time	0		0		ns
t _{su(A-WH)}	Address setup time with respect to \overline{W}	50		65		ns
t _{su(S1)}	Chip select 1 setup time	50		65		ns
t _{su(S2)}	Chip select 2 setup time	50		65		ns
t _{su(D)}	Data setup time	25		30		ns
t _{h(D)}	Data hold time	0		0		ns
t _{rec(W)}	Write recovery time	0		0		ns
t _{dis(W)}	Output disable time from \overline{W} low		20		25	ns
t _{dis(OE)}	Output disable time from \overline{OE} high		20		25	ns
t _{en(W)}	Output enable time from \overline{W} high	5		5		ns
t _{en(OE)}	Output enable time from \overline{OE} low	5		5		ns

(4) TIMING DIAGRAMS

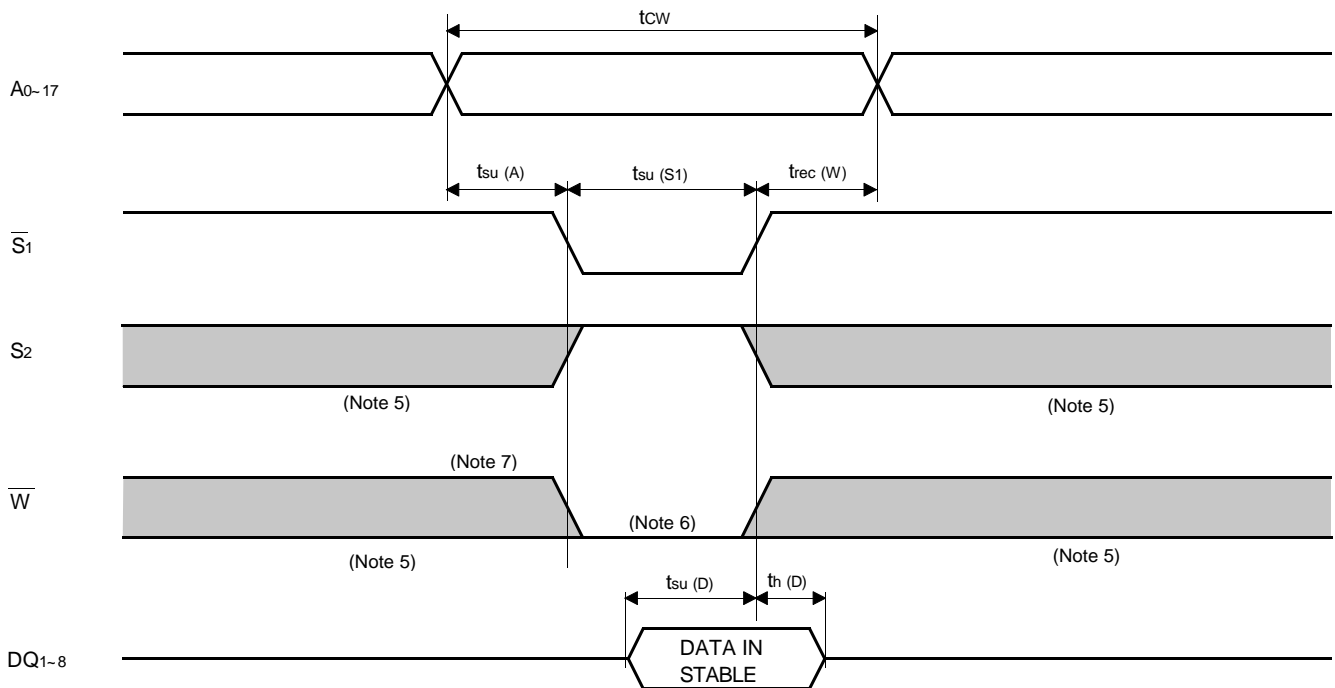
Read cycle



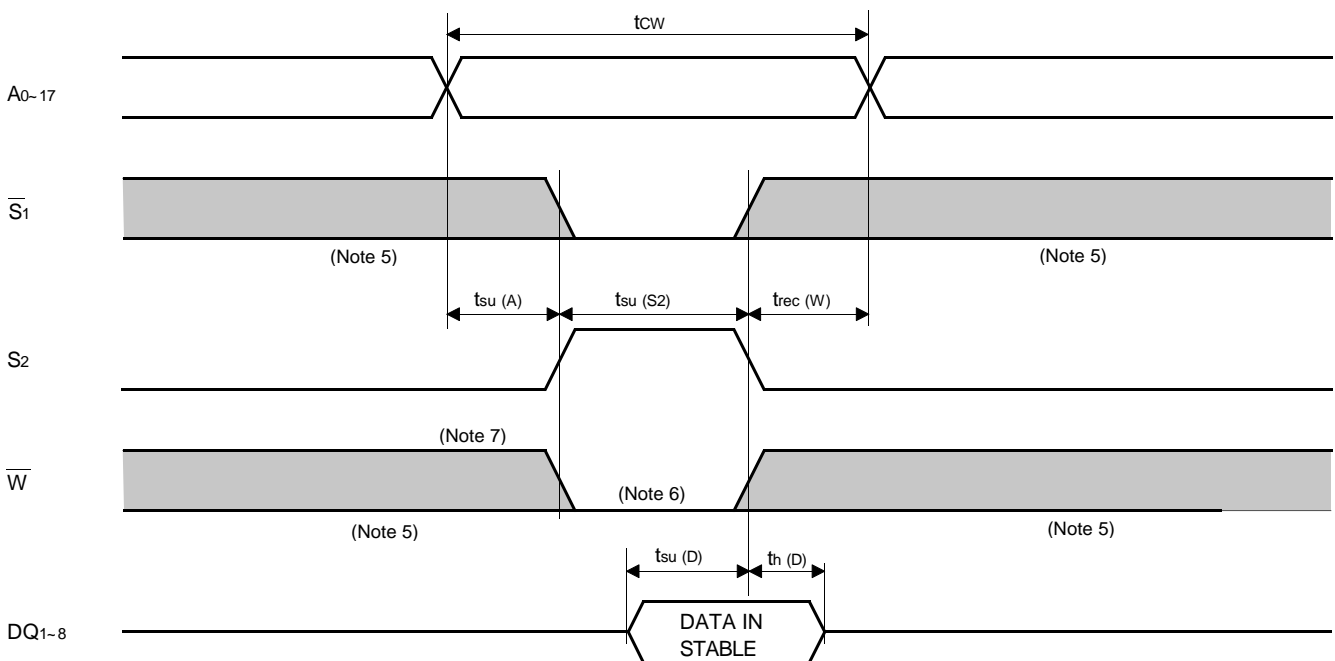
Write cycle (\overline{W} control mode)



Write cycle ($\overline{S1}$ control mode)



Write cycle (S2 control mode)



- Note 5: Hatching indicates the state is "don't care".
 6: Writing is executed while S2 high overlaps $\overline{S1}$ and \overline{W} low.
 7: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of S2, the outputs are maintained in the high impedance state.
 8: Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (T_a= -40~85°C, unless otherwise noted)

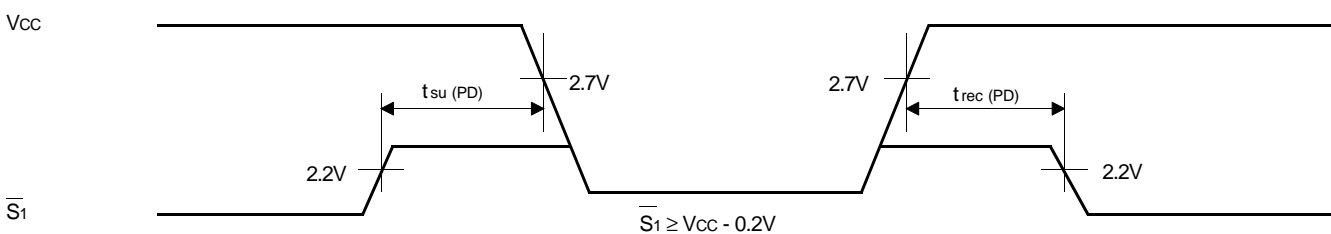
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage		2.0			V
V _I (S1)	Chip select input $\overline{S1}$		2.0			V
V _I (S2)	Chip select input S2				0.2	V
I _{CC} (PD)	Power down supply current	V _{CC} = 3.0V 1) S ₂ ≤ 0.2V, other inputs = 0~V _{CC} 2) $\overline{S1} \geq V_{CC}-0.2V$, S ₂ ≥ V _{CC} -0.2V, other inputs = 0~V _{CC}	~25°C	0.3	1	μA
			~40°C		3	
			~70°C		8	
			~85°C		24	

(2) TIMING REQUIREMENTS (T_a=-40~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

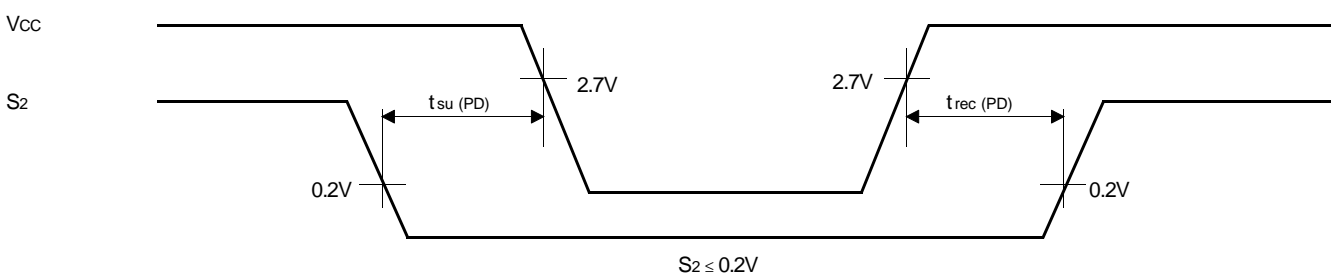
(3) POWER DOWN CHARACTERISTICS

$\overline{S1}$ control mode



Note 9: On the power down mode by controlling $\overline{S1}$, the input level of S2 must be S₂ ≥ V_{CC} - 0.2V or S₂ ≤ 0.2V. The other pins (Address, I/O, \overline{WE} , \overline{OE}) can be in high impedance state.

S2 control mode



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