

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M5M5V408BFP,TP,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V408B is a family of low voltage 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5V408B is suitable for memory applications where a simple interfacing, battery operating and battery

- Package:
 - M5M5V408BFP: 32 pin 525 mil SOP
 - M5M5V408BTP: 32 pin 400mil TSOP(II)
 - M5M5V408BKV: 32 pin 8mm x13.4mm STSOP

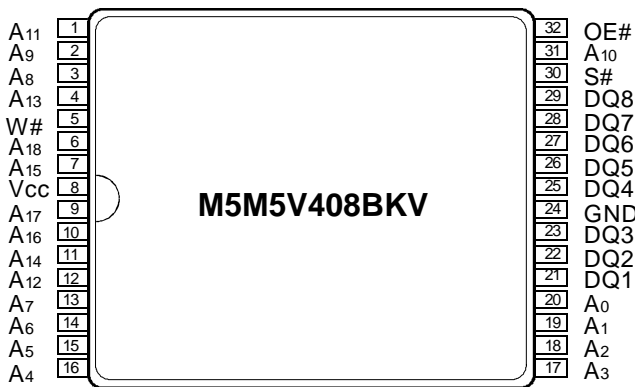
FEATURES

- Single 2.7 ~ 3.6V power supply
- Small stand-by current: 0.3µA (3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Process technology: 0.25µm CMOS

Version, Operating temperature	Part name (## stands for "FP", "TP" or "KV")	Power supply	Access time (max.)	Stand-by current I _{cc} (PD), V _{cc} =3.0V						Active current I _{cc} 1 (3.0V, typ.*)
				Typical *		Limits (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
Standard 0 ~ 70°C	M5M5V408B## -70H	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	-	30mA (10MHz)
	M5M5V408B## -85H		85ns							
I-version -40 ~ +85°C	M5M5V408B## -70HI	2.7 ~ 3.6V	70ns	0.3µA	1µA	1µA	3µA	15µA	30µA	5mA (1MHz)
	M5M5V408B## -85HI		85ns							

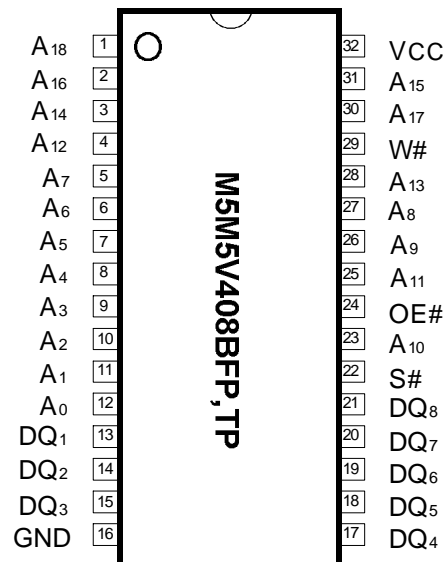
*Typical values are sampled, and are not 100% tested.

PIN CONFIGURATION (TOP VIEW)



Outline 32P3K-B (STSOP)

Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
S# (\bar{S})	Chip select input
W# (\bar{W})	Write control input
OE# (\bar{OE})	Output enable input
Vcc	Power supply
GND	Ground supply



Outline 32P2M-A (SOP)
32P3Y-H (TSOP II)

M5M5V408BFP,TP,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The M5M5408BFP,TP,KV is organized as 524,288-words by 8-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

A write operation is executed during the S# low and W# low overlap time. The address(A0~A18) must be set up before the write cycle

A read operation is executed by setting W# at a high level and OE# at a low level while S# are in an active

When setting S# at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips. Setting the OE# at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

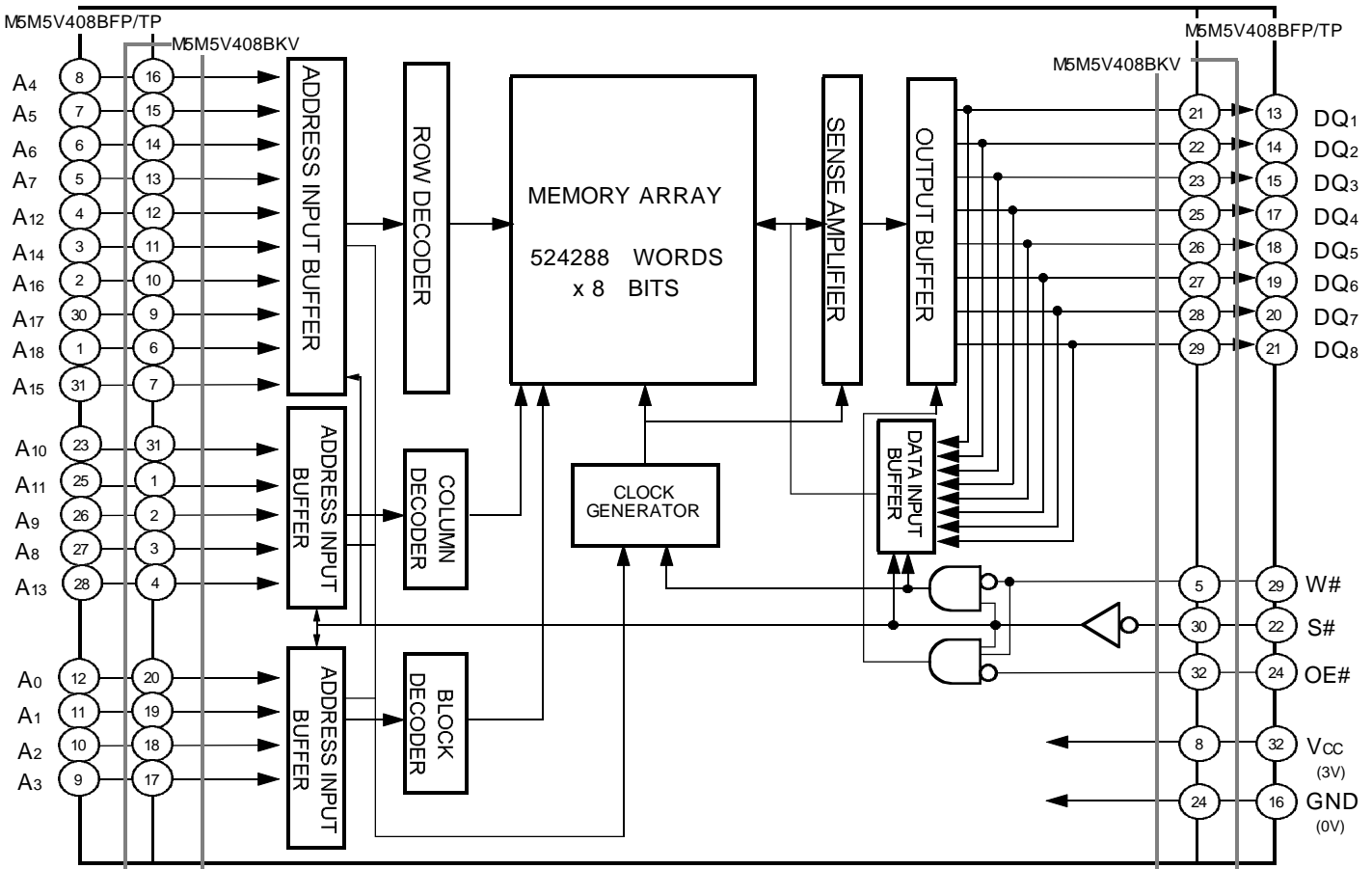
The power supply current is reduced as low as 0.3μA(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-

FUNCTION TABLE

S#	W#	OE#	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	Data input (D)	Active
L	H	L	Read	Data output (Q)	Active
L	H	H	Read	High-impedance	Active

note: "H" and "L" in this table mean VIH and VIL, respectively. "X" in this table should be "H" or "L".

BLOCK DIAGRAM



M5M5V408BFP,TP,KV**4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM****ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Units
V _{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V _I	Input voltage	With respect to GND	-0.5* ~ V _{CC} + 0.5	
V _O	Output voltage	With respect to GND	0 ~ V _{CC}	
P _d	Power dissipation	T _a =25°C	700	mW
T _a	Operating temperature	Standard (Commercial temp.)	0 ~ 70	°C
		I-version (Industrial temp.)	- 40 ~ +85	
T _{stg}	Storage temperature		- 65 ~ +150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units		
			Min	Typ	Max			
V _{IH}	High-level input voltage		2.2		V _{CC} +0.3V	V		
V _{IL}	Low-level input voltage		-0.3*		0.6			
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA	2.4					
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA	V _{CC} -0.5V					
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4			
I _I	Input leakage current	V _I =0 ~ V _{CC}			±1	μA		
I _O	Output leakage current	S#=V _{IH} or OE#=V _{IH} , V _{I/O} =0 ~ V _{CC}			±1	μA		
I _{CC1}	Active supply current (AC, CMOS-level)	S# ≤ 0.2V Output-open Other inputs ≤ 0.2V or ≥ V _{CC} -0.2V	f = 10MHz	-	30	45	mA	
			f = 1MHz	-	5	7		
I _{CC2}	Active supply current (AC, TTL-level)	S#=V _{IL} Output-open Other inputs=V _{IH} or V _{IL}	f = 10MHz	-	30	45		
			f = 1MHz	-	5	7		
I _{CC3}	Stand by supply current (CMOS-level input)	V _{CC} =3.6V, max. S# ≥ V _{CC} -0.2V Other inputs=0~V _{CC}	I-version	85°C	-	-	40	μA
			I-version, standard	70°C	-	-	20	
				40°C	-	1	5	
			I-version	0 ~ +25°C	-	0.3	2	
-40 ~ +25°C	-	0.3		2				
I _{CC4}	Stand by supply current (TTL-level input)	S#=V _{IH} , Other inputs= 0 ~ V _{CC}	-	-	0.5	mA		

* -3.0V in case of AC (Pulse width ≤ 30ns)

Note 1: Direction for current flowing into IC is indicated as positive (no mark).

Note 2: Typical values are sampled at V_{CC}=3.0V, and are not 100% tested.**CAPACITANCE**(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mV _{rms} , f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mV _{rms} , f=1MHz			10	

M5M5V408BFP,TP,KV**4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM****AC ELECTRICAL CHARACTERISTICS** ($V_{CC}=2.7 \sim 3.6V$, unless otherwise noted)**(1) TEST CONDITIONS**

Supply voltage	2.7V~3.6V
Input pulse	$V_{IH}=2.4V, V_{IL}=0.4V$
Input rise time and fall time	5ns
Reference level	$V_{OH}=V_{OL}=1.5V$ Transition is measured $\pm 500mV$ from steady state voltage.(for t_{en}, t_{dis})
Output loads	Fig.1, $CL=30pF$ $CL=5pF$ (for t_{en}, t_{dis})

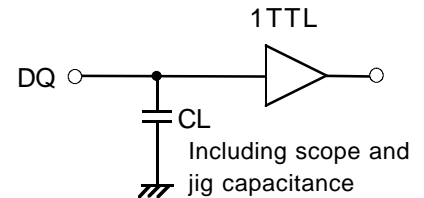


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Units
		-70H, -70HI		-85H, -85HI		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	70				ns
$t_{a(A)}$	Address access time		70		85	ns
$t_{a(S)}$	Chip select access time		70		85	ns
$t_{a(OE)}$	Output enable access time		35		45	ns
$t_{dis(S)}$	Output disable time after S# high	25			25	ns
$t_{dis(OE)}$	Output disable time after OE# high	25			25	ns
$t_{en(S)}$	Output enable time after S# low	10		10		ns
$t_{en(OE)}$	Output enable time after OE# low	5		5		ns
$t_V(A)$	Data valid time after address	10		10		ns

(3) WRITE CYCLE

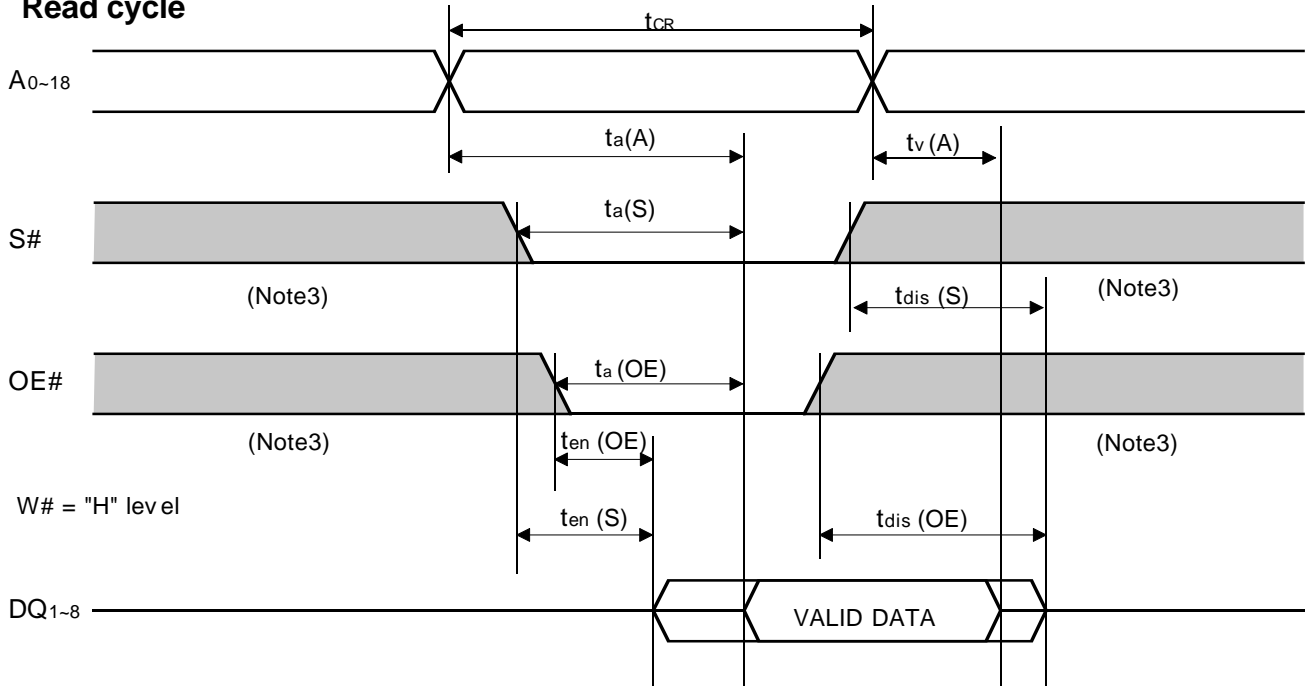
Symbol	Parameter	Limits				Units
		-70H, -70HI		-85H, -85HI		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		ns
$t_w(W)$	Write pulse width	55		55		ns
$t_{su(A)}$	Address set up time	0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to W# high	65		65		ns
$t_{su(S)}$	Chip select set up time	65		65		ns
$t_{su(D)}$	Data set up time	35		35		ns
$t_h(D)$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time after W# low		25		25	ns
$t_{dis(OE)}$	Output disable time after OE# high		25		25	ns
$t_{en(W)}$	Output enable time after W# high	5		5		ns
$t_{en(OE)}$	Output enable time after OE# low	5		5		ns

M5M5V408BFP,TP,KV

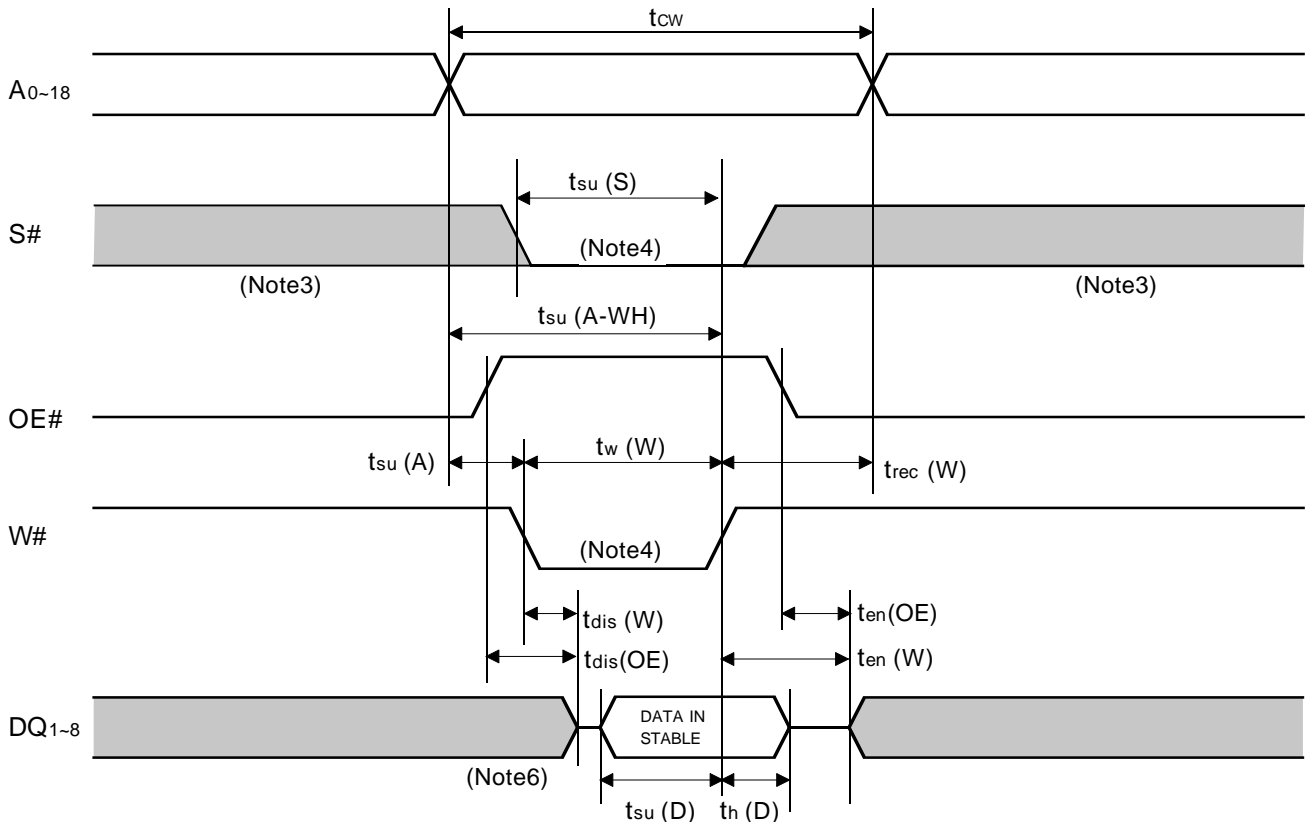
4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

(4) TIMING DIAGRAMS

Read cycle



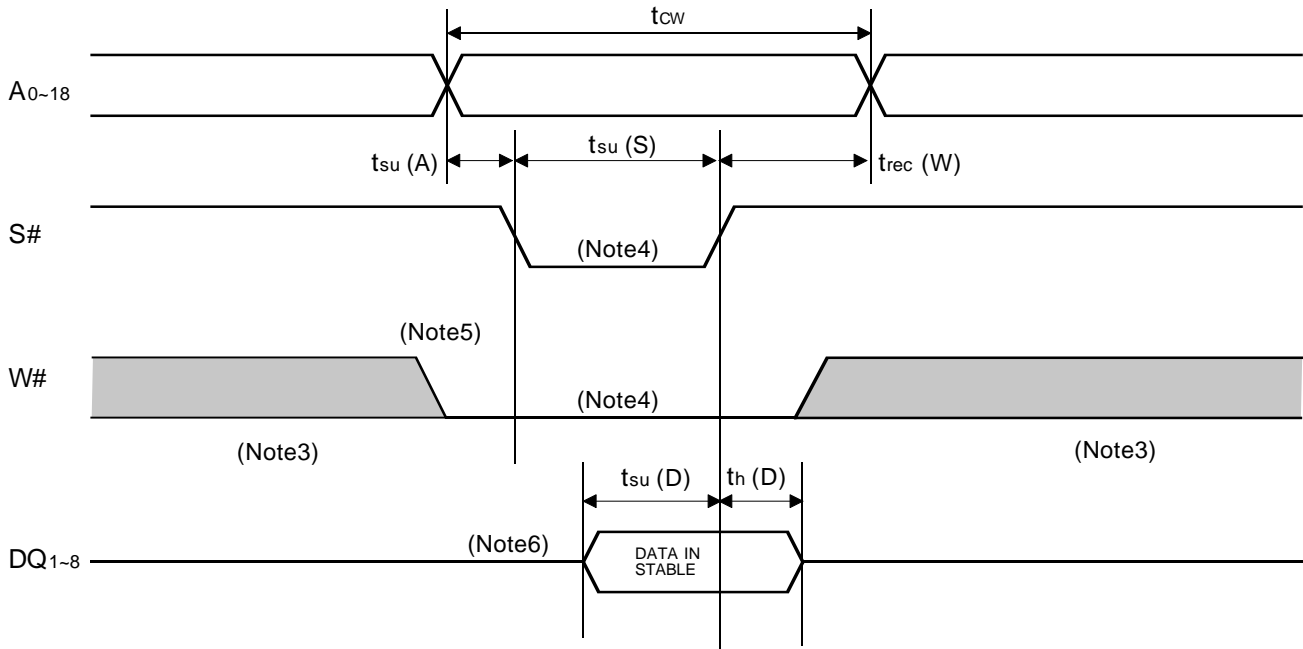
Write cycle (W# control mode)



M5M5V408BFP,TP,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle (S# control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during the overlap of a low S# and a low W#.

Note 5: If W# goes low simultaneously with or prior to S#, the output remains in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

M5M5V408BFP,TP,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Units		
			Min	Typ.	Max			
V _{CC} (PD)	Power down supply voltage		2.0			V		
V _I (S)	Chip select input S#		2.0			V		
I _{CC} (PD)	Power down supply current	V _{CC} =3.0V, S# ≥ V _{CC} -0.2V, Other inputs = 0 ~ V _{CC}	I-version	85°C	-	-	30	μA
			Standard,	70°C	-	-	15	
			I-version	40°C	-	1*	3	
			Standard	0~ 25°C	-	0.4*	1	
			I-version	-40~ 25°C	-	0.4*	1	

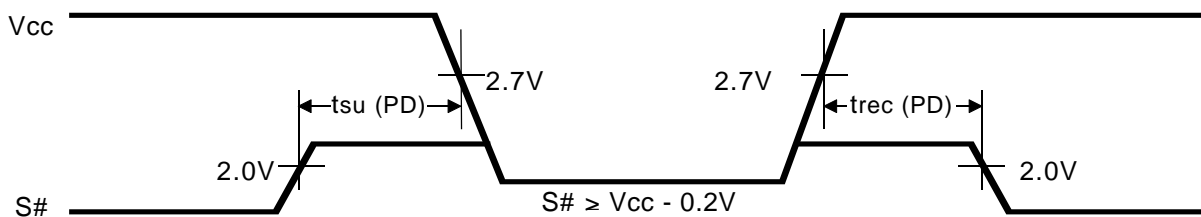
*Typical values are sampled, and are not 100% tested.

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{SU} (PD)	Power down set up time		0			ns
t _{REC} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

S# control mode



M5M5V408BFP,TP,KV

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Date</u>	<u>Remarks</u>
K0.1e	The first edition	Mar. 5, 1998	Preliminary
K0.2e	Added M5M5V408BFP/TP/RT	Jul.30, 1998	Preliminary
K1.0e	The first product version	Sep.7, 1998	---
K2.0e	1) Speed items revised: 70ns added and 100ns deleted 2) lcc3 and lcc(PD) limits revised	Mar.10,1999	---
3.0e	1) Product lineup revised 2) Symbol notations revised: \overline{S} -> S#, \overline{W} -> W#, \overline{OE} -> OE#	Feb.12, 2002	---

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss arising from these inaccuracies or errors.

Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (<http://www.mitsubishichips.com>).

When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.