

# M5M5V416CWG -70HI

## 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

Those are summarized in the part name table below.

### DESCRIPTION

The M5M5V416C is a family of low voltage 4-Mbit static RAMs organized as 262144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18μm CMOS technology.

The M5M5V416C is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5V416CWG is packaged in a CSP (chip scale package), with the outline of 7.0mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

### FEATURES

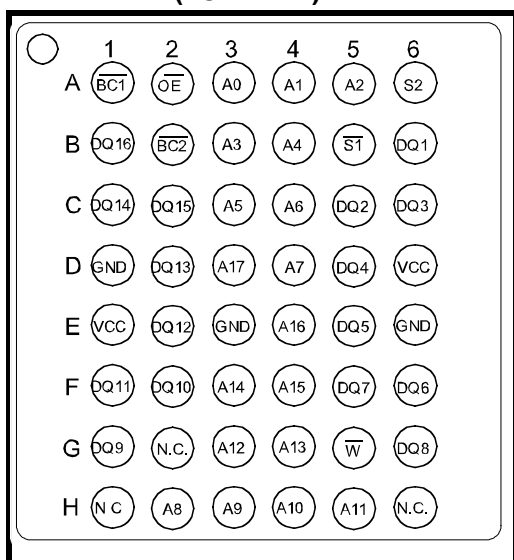
- Single 2.7~3.0V power supply
- Small stand-by current: 0.1μA (2.85V, typ.)
- No clocks, No refresh
- Data retention supply voltage =2.0V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by  $\overline{S1}$ ,  $S2$ ,  $\overline{BC1}$  and  $\overline{BC2}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Process technology: 0.18μm CMOS
- Package: 48ball 7.0mm x 8.5mm CSP

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current (Vcc=3.0V)						Active current Icc1 (3.0V, typ.)
				* Typical		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
I-version -40 ~ +85°C	M5M5V416CWG -70HI	2.7 ~ 3.0V	70ns	0.2	0.4	1	2	10	20	40mA (10MHz) 5mA (1MHz)

\* Typical parameter indicates the value for the center of distribution, and not 100% tested.

### PIN CONFIGURATION

(TOP VIEW)



Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
$\overline{S1}$	Chip select input 1
S2	Chip select input 2
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
$\overline{BC1}$	Lower Byte (DQ1 ~ 8)
$\overline{BC2}$	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

Outline: 48FJA  
NC: No Connection

# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## FUNCTION

The M5M5V416CWG is organized as 262144-words by 16-bit. These devices operate on a single +2.7~3.0V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs  $\overline{BC1}$ ,  $\overline{BC2}$ ,  $S1$ ,  $S2$ ,  $\overline{W}$  and  $\overline{OE}$ . Each mode is summarized in the function table.

A write operation is executed whenever the low level  $\overline{W}$  overlaps with the low level  $\overline{BC1}$  and/or  $\overline{BC2}$  and the low level  $\overline{S1}$  and the high level  $S2$ . The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting  $\overline{W}$  at a high level and  $\overline{OE}$  at a low level while  $\overline{BC1}$  and/or  $\overline{BC2}$  and  $\overline{S1}$  and  $S2$  are in an active state( $S1=L, S2=H$ ).

When setting  $\overline{BC1}$  at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting  $\overline{BC2}$  at a high level and other pins are in an active stage, lower-

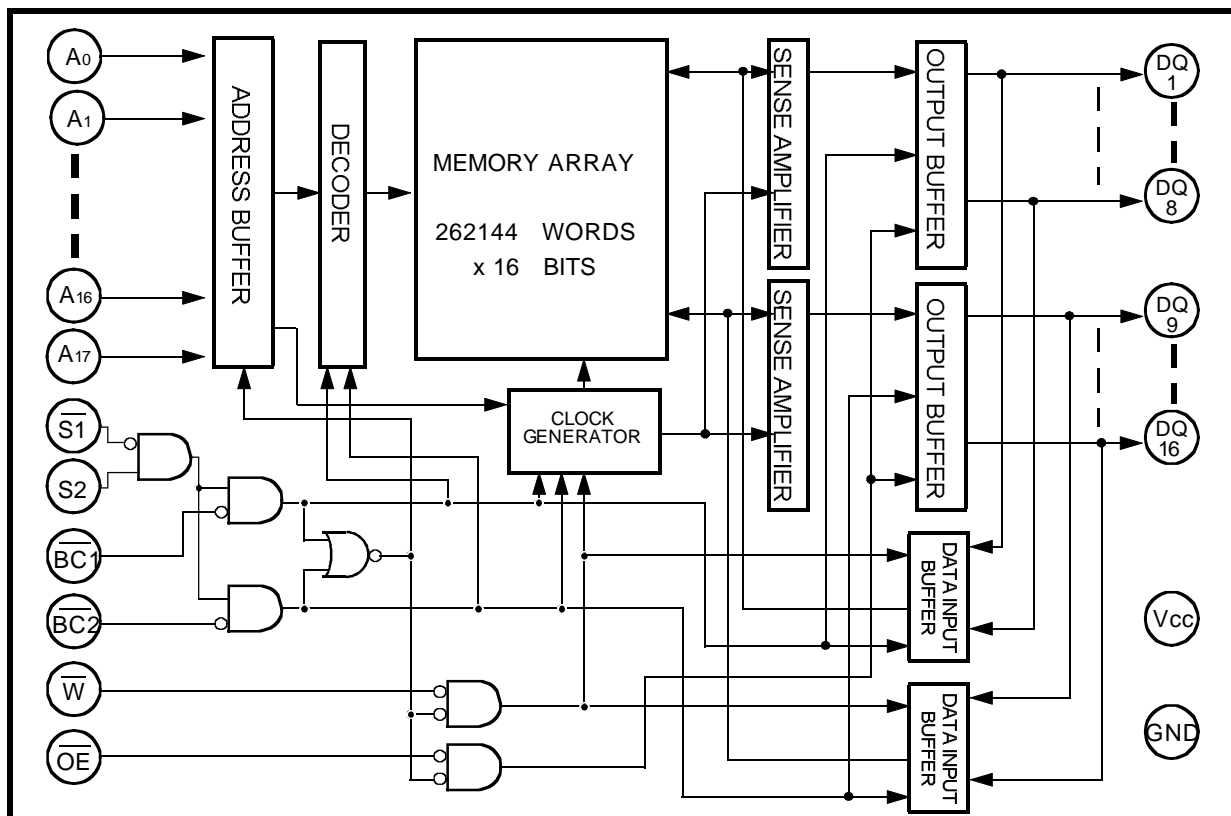
When setting  $\overline{BC1}$  and  $\overline{BC2}$  at a high level or  $\overline{S1}$  at a high level or  $S2$  at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\overline{BC1}$ ,  $\overline{BC2}$  and  $\overline{S1}$ ,  $S2$ .

The power supply current is reduced as low as 0.1 $\mu$ A(25°C, typical), and the memory data can be held at +1V power supply, enabling battery back-up operation during power

## FUNCTION TABLE

$\overline{S1}$	$S2$	$\overline{BC1}$	$\overline{BC2}$	$\overline{W}$	$\overline{OE}$	Mode	DQ1~8	DQ9~16	Icc
X	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	————	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	————	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	————	High-Z	High-Z	Active

## BLOCK DIAGRAM



# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V <sub>CC</sub>	Supply voltage	With respect to GND	-0.5* ~ +3.6	V
V <sub>I</sub>	Input voltage	With respect to GND	-0.2* ~ V <sub>CC</sub> + 0.2	
V <sub>O</sub>	Output voltage	With respect to GND	0 ~ V <sub>CC</sub>	
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	700	mW
T <sub>a</sub>	Operating temperature	I-version	- 40 ~ +85	°C
T <sub>stg</sub>	Storage temperature		- 65 ~ +150	°C

\* -3.0V in case of AC (Pulse width ≤ 30ns)

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub>=2.7 ~ 3.0V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units	
			Min	Typ	Max		
V <sub>IH</sub>	High-level input voltage		2.2		V <sub>CC</sub> +0.2V	V	
V <sub>IL</sub>	Low-level input voltage		-0.2*		0.4		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -0.5mA	2.4				
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2mA			0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> =0 ~ V <sub>CC</sub>			±1	μA	
I <sub>O</sub>	Output leakage current	$\overline{BC1}$ and $\overline{BC2}$ =V <sub>IH</sub> or $\overline{S1}$ =V <sub>IH</sub> or S <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}$ =V <sub>IH</sub> , V <sub>I/O</sub> =0 ~ V <sub>CC</sub>			±1	μA	
I <sub>CC1</sub>	Active supply current (AC, MOS level)	$\overline{BC1}$ and $\overline{BC2}$ ≤ 0.2V, $\overline{S1}$ ≤ 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> -0.2V other inputs ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V Output - open (duty 100%)	f = 10MHz	-	40	50	mA
			f = 1MHz	-	5	10	
I <sub>CC2</sub>	Active supply current (AC, TTL level)	$\overline{BC1}$ and $\overline{BC2}$ =V <sub>IL</sub> , $\overline{S1}$ =V <sub>IL</sub> , S <sub>2</sub> =V <sub>IH</sub> other pins =V <sub>IH</sub> or V <sub>IL</sub> Output - open (duty 100%)	f = 10MHz	-	40	50	mA
			f = 1MHz	-	5	10	
I <sub>CC3</sub>	Stand by supply current (MOS level)	(1) $\overline{S1}$ ≥ V <sub>CC</sub> - 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V, other inputs = 0 ~ V <sub>CC</sub> (2) S <sub>2</sub> ≤ 0.2V, other inputs = 0 ~ V <sub>CC</sub> (3) $\overline{BC1}$ and $\overline{BC2}$ ≥ V <sub>CC</sub> - 0.2V $\overline{S1}$ ≤ 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V other inputs = 0 ~ V <sub>CC</sub>	~ +25°C	-	0.1	1	μA
			~ +40°C	-	0.2	2	
			~ +85°C	-	-	20	
I <sub>CC4</sub>	Stand by supply current (TTL level)	$\overline{BC1}$ and $\overline{BC2}$ =V <sub>IH</sub> or $\overline{S1}$ =V <sub>IH</sub> or S <sub>2</sub> =V <sub>IL</sub> Other inputs= 0 ~ V <sub>CC</sub>	-	-	0.5	mA	

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

\* -1.0V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical parameter indicates the value for the center of distribution at 2.85V, and is not 100% tested.

## CAPACITANCE

(V<sub>CC</sub>=2.7 ~ 3.0V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz			10	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms, f=1MHz			10	

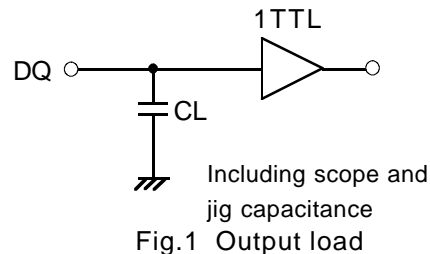
# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=2.7 ~ 3.0V, unless otherwise noted)

### (1) TEST CONDITIONS

Supply voltage	2.7~3.0V
Input pulse	V <sub>IH</sub> =2.4V, V <sub>IL</sub> =0.2V
Input rise time and fall time	5ns
Reference level	V <sub>OH</sub> =V <sub>OL</sub> =1.5V <small>Transition is measured ±200mV from steady state voltage.(for ten,tdis)</small>
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)



### (2) READ CYCLE

Symbol	Parameter	Limits		Units
		70HI		
		Min	Max	
t <sub>CR</sub>	Read cycle time	70		ns
t <sub>a(A)</sub>	Address access time		70	ns
t <sub>a(S1)</sub>	Chip select 1 access time		70	ns
t <sub>a(S2)</sub>	Chip select 2 access time		70	ns
t <sub>a(BC1)</sub>	Byte control 1 access time		70	ns
t <sub>a(BC2)</sub>	Byte control 2 access time		70	ns
t <sub>a(OE)</sub>	Output enable access time		35	ns
t <sub>dis(S1)</sub>	Output disable time after $\overline{S1}$ high		25	ns
t <sub>dis(S2)</sub>	Output disable time after $\overline{S2}$ low		25	ns
t <sub>dis(BC1)</sub>	Output disable time after $\overline{BC1}$ high		25	ns
t <sub>dis(BC2)</sub>	Output disable time after $\overline{BC2}$ high		25	ns
t <sub>dis(OE)</sub>	Output disable time after $\overline{OE}$ high		25	ns
t <sub>en(S1)</sub>	Output enable time after $\overline{S1}$ low	10		ns
t <sub>en(S2)</sub>	Output enable time after $\overline{S2}$ high	10		ns
t <sub>dis(BC1)</sub>	Output enable time after $\overline{BC1}$ low	10		ns
t <sub>dis(BC2)</sub>	Output enable time after $\overline{BC2}$ low	10		ns
t <sub>en(OE)</sub>	Output enable time after $\overline{OE}$ low	5		ns
t <sub>v(A)</sub>	Data valid time after address	10		ns

### (3) WRITE CYCLE

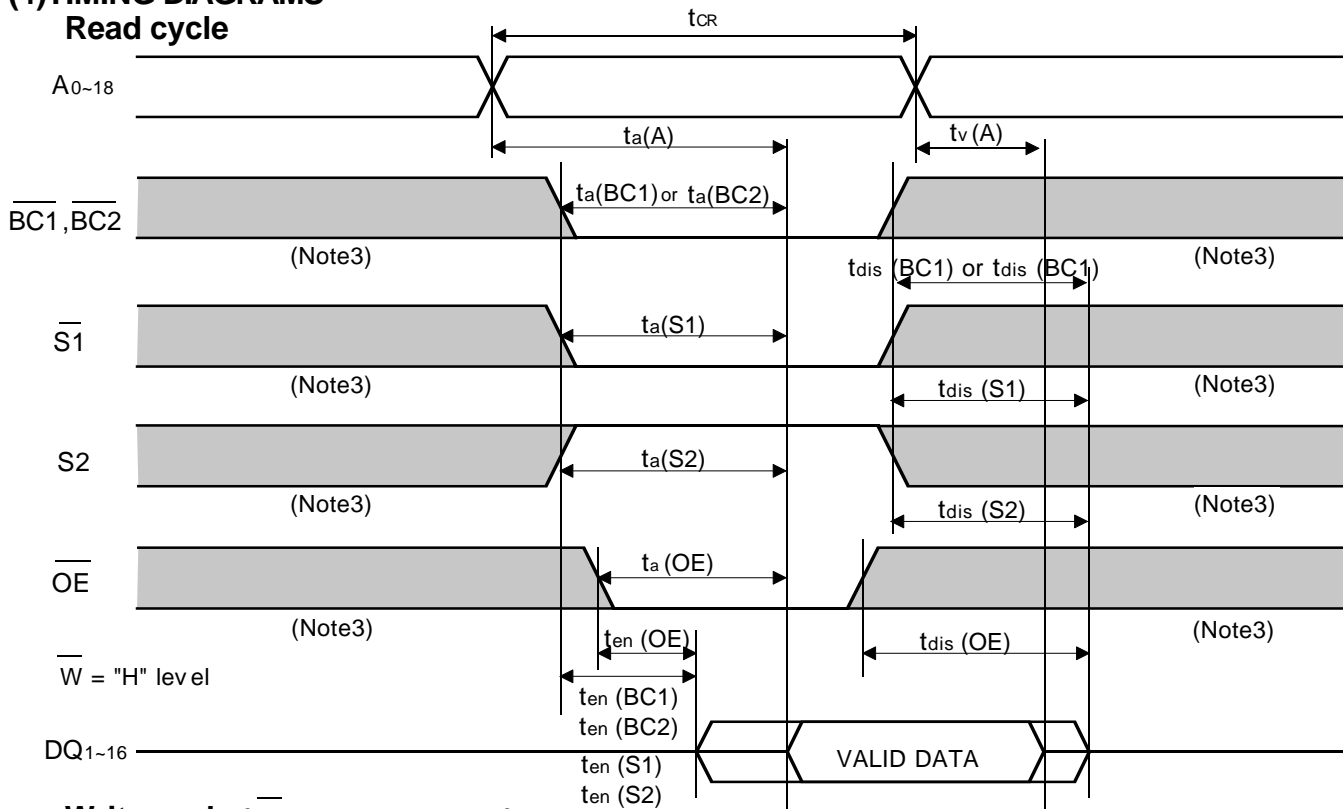
Symbol	Parameter	Limits		Units
		70HI		
		Min	Max	
t <sub>cw</sub>	Write cycle time	70		ns
t <sub>w(W)</sub>	Write pulse width	55		ns
t <sub>su(A)</sub>	Address setup time	0		ns
t <sub>su(A-WH)</sub>	Address setup time with respect to $\overline{W}$	60		ns
t <sub>su(BC1)</sub>	Byte control 1 setup time	60		ns
t <sub>su(BC2)</sub>	Byte control 2 setup time	60		ns
t <sub>su(S1)</sub>	Chip select 1 setup time	60		ns
t <sub>su(S2)</sub>	Chip select 2 setup time	60		ns
t <sub>su(D)</sub>	Data setup time	35		ns
t <sub>h(D)</sub>	Data hold time	0		ns
t <sub>rec(W)</sub>	Write recovery time	0		ns
t <sub>dis(W)</sub>	Output disable time f from $\overline{W}$ low		25	ns
t <sub>dis(OE)</sub>	Output disable time f from $\overline{OE}$ high		25	ns
t <sub>en(W)</sub>	Output enable time f from $\overline{W}$ high	5		ns
t <sub>en(OE)</sub>	Output enable time f from $\overline{OE}$ low	5		ns

# M5M5V416CWG -70HI

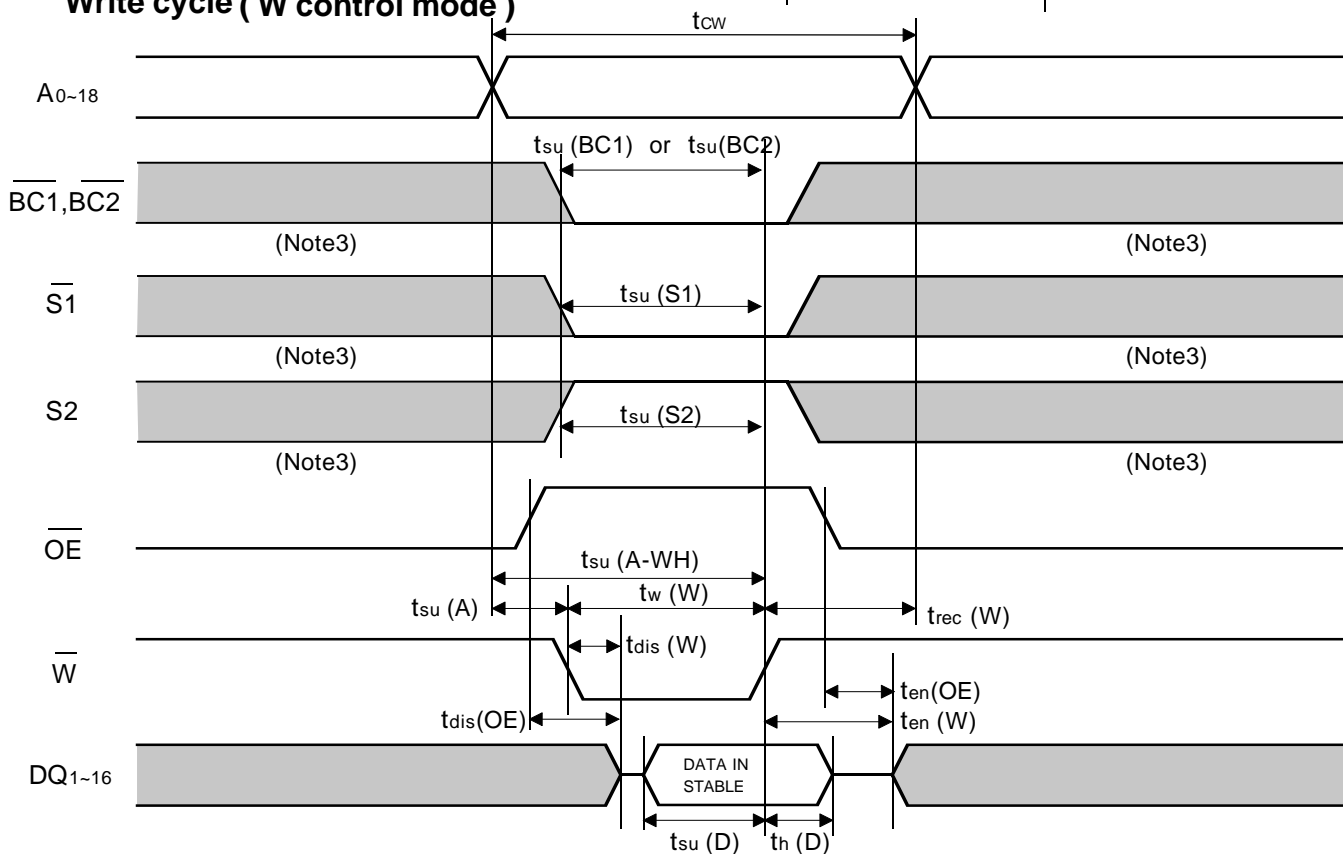
4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## (4)TIMING DIAGRAMS

### Read cycle

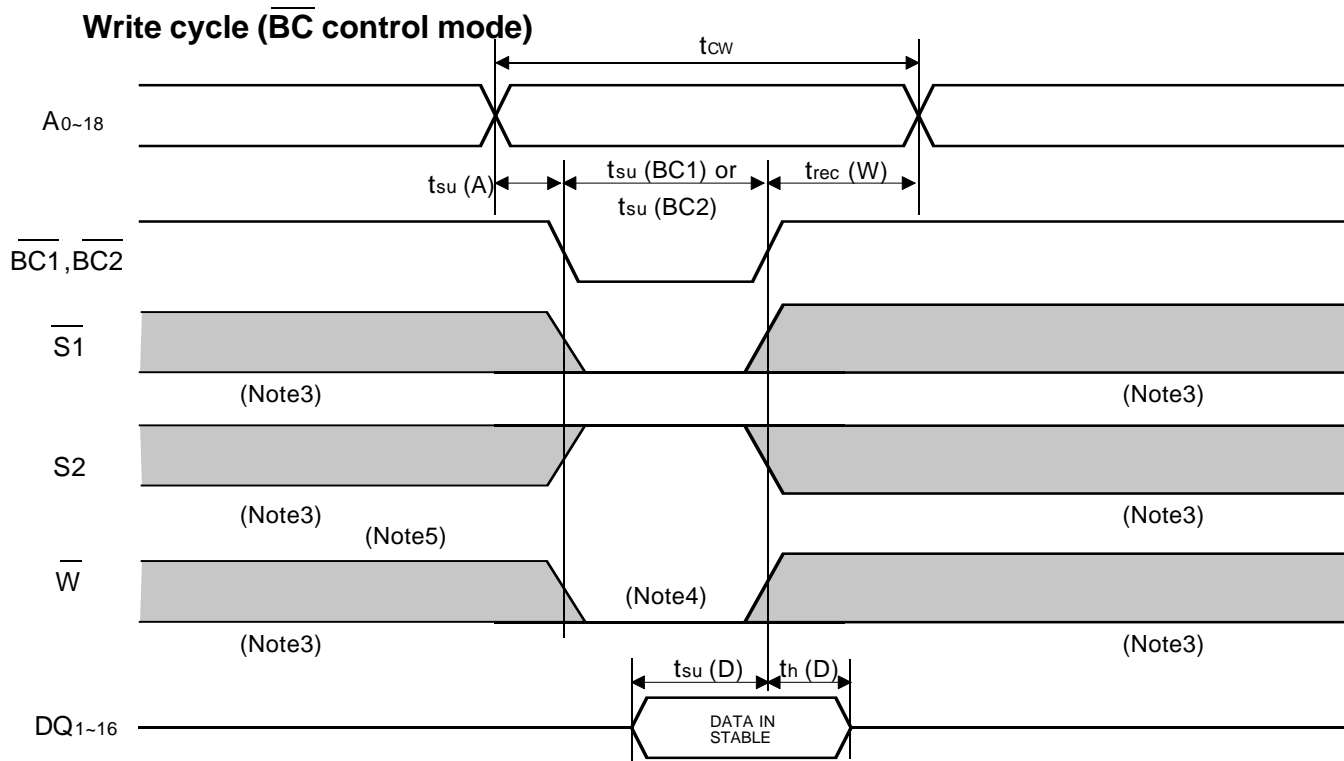


### Write cycle ( $\overline{W}$ control mode)



# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during S1 low, S2 high overlaps BC1 and/or BC2 low and W low.

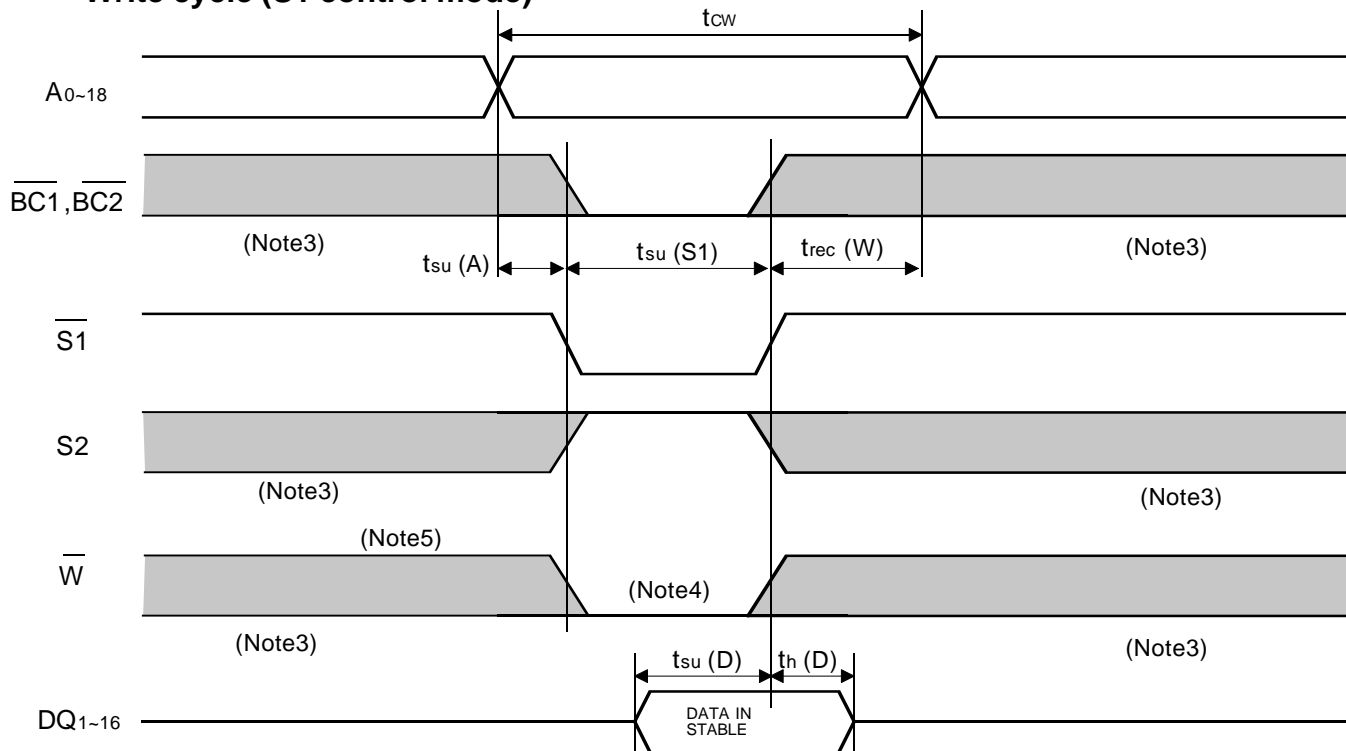
Note 5: When the falling edge of W is simultaneously or prior to the falling edge of BC1 and/or BC2 or the falling edge of S1 or rising edge of S2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

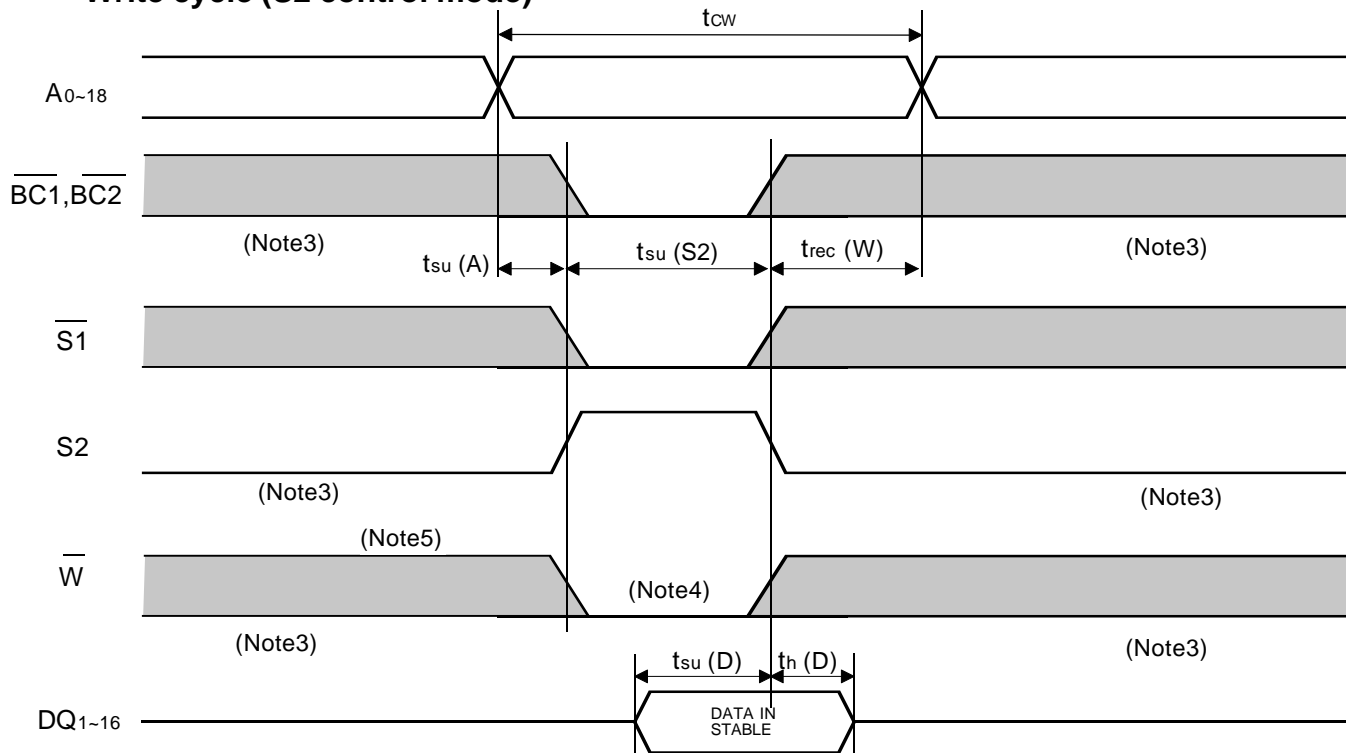
# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## Write cycle ( $\overline{S1}$ control mode)



## Write cycle ( $S2$ control mode)



# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## POWER DOWN CHARACTERISTICS

### (1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ	Max		
V <sub>CC</sub> (PD)	Power down supply voltage		2.0			V	
V <sub>I</sub> (BC)	Byte control input $\overline{BC1}$ & $\overline{BC2}$	$2.7V \leq V_{CC}(PD)$	2.2			V	
		$2.0V \leq V_{CC}(PD) \leq 2.7V$		V <sub>CC</sub> (PD)			
V <sub>I</sub> ( $\overline{S1}$ )	Chip select input $\overline{S1}$	$2.7V \leq V_{CC}(PD)$	2.2			V	
		$2.0V \leq V_{CC}(PD) \leq 2.7V$		V <sub>CC</sub> (PD)			
V <sub>I</sub> (S2)	Chip select input S2				0.2		
I <sub>CC</sub> (PD)	Power down supply current	V <sub>CC</sub> =2.0V (1) $\overline{S1} \geq V_{CC} - 0.2V$ , other inputs = 0 ~ V <sub>CC</sub> (2) $S2 \leq 0.2V$ , other inputs = 0 ~ V <sub>CC</sub> (3) $\overline{BC1}$ and $\overline{BC2} \geq V_{CC} - 0.2V$ $S1 \leq 0.2V$ , $S2 \geq V_{CC} - 0.2V$ other inputs = 0 ~ V <sub>CC</sub>	~ +25°C	-	0.1	0.8	μA
			~ +40°C	-	0.2	1.5	
			~ +85°C	-	-	15	

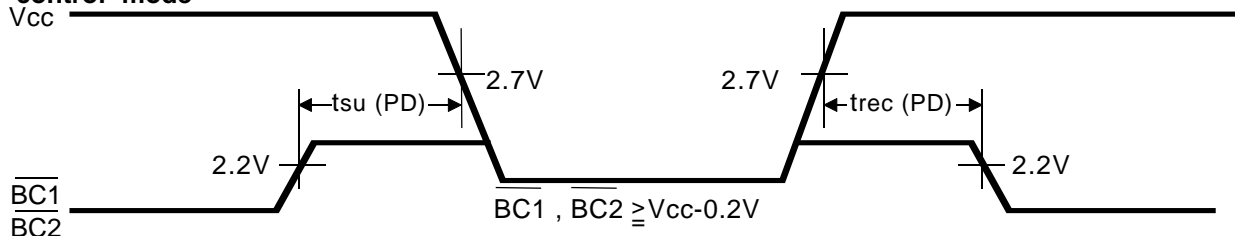
Note 2: Typical parameter of I<sub>CC</sub>(PD) indicates the value for the center of distribution at 2.0V, and not 100% tested.

### (2) TIMING REQUIREMENTS

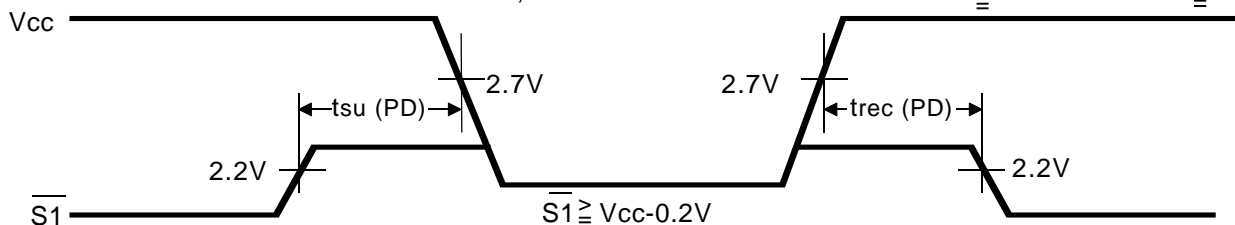
Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t <sub>su</sub> (PD)	Power down set up time		0			ns
t <sub>rec</sub> (PD)	Power down recovery time		5			ms

### (3) TIMING DIAGRAM

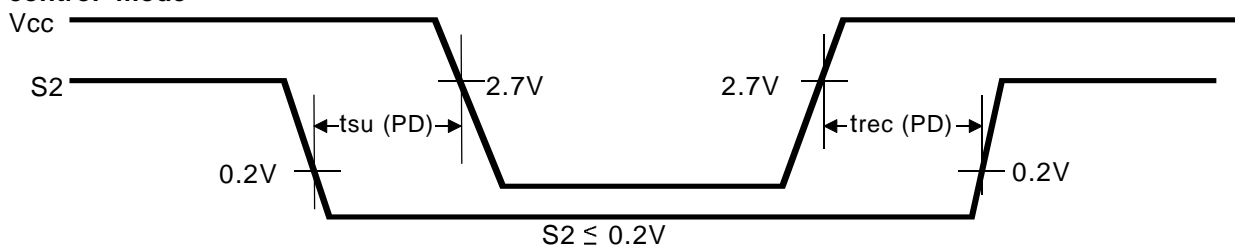
#### BC control mode



#### S1 control mode note7 : On the S1 mode, the level of $\overline{S2}$ must be fixed at $S2 \geq V_{CC} - 0.2V$ or $S2 \leq 0.2V$ .



#### S2 control mode





# M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

---

## Revision History

Ver. 0.0 / September.08.2000

Initial (-70HI)

## **Keep safety first in your circuit designs!**

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

## **Notes regarding these materials**

These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss arising from these inaccuracies or errors.

Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (<http://www.mitsubishichips.com>).

When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.